## **NTMS4107N**

## **Power MOSFET**

## 30 V, 18 A, Single N-Channel, SO-8

#### **Features**

- Ultra Low R<sub>DS(on)</sub> (at 4.5 V<sub>GS</sub>), Low Gate Resistance and Low Q<sub>G</sub>
- Optimized for Low Side Synchronous Applications
- High Speed Switching Capability

#### **Applications**

- Notebook Computer Vcore Applications
- Network Applications
- DC-DC Converters

#### **MAXIMUM RATINGS** (T<sub>.1</sub> = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	30	V
Gate-to-Source Voltage			$V_{GS}$	±20	V
Continuous Drain	Steady	T <sub>A</sub> = 25°C	I <sub>D</sub>	15	Α
Current (Note 1)	State	T <sub>A</sub> = 85°C		11	
	t ≤10 s	$T_A = 25^{\circ}C$		18	
Power Dissipation (Note 1)	Steady State T <sub>A</sub> = 25°C		P <sub>D</sub>	1.67	W
	t ≤10 s	,		2.5	
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	11	Α
Current (Note 2)	Steady	T <sub>A</sub> = 85°C		8.0	
Power Dissipation (Note 2)	State	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.93	W
Pulsed Drain Current	t <sub>p</sub> =	10 μs	I <sub>DM</sub>	56	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	–55 to 150	°C
Continuous Source Current (Body Diode)			I <sub>S</sub>	3.0	Α
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD}$ = 30 V, $V_{GS}$ = 10 V, $I_{PK}$ = 42 A, L = 1 mH, $R_G$ = 25 $\Omega$ )			E <sub>AS</sub>	880	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

## THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	75	°C/W
Junction-to-Ambient – $t \le 10 \text{ s (Note 1)}$	$R_{\theta JA}$	50	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	135	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

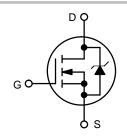
- Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412" sq.).



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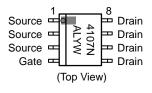
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX	
30 V	3.4 mΩ @ 10 V	18 A	
30 V	4.7 mΩ @ 4.5 V	1074	



#### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8 CASE 751 STYLE 12



4107N = Specific Device Code A = Assembly Location

L = Wafer Lot Y = Year W = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4107NR2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **NTMS4107N**

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

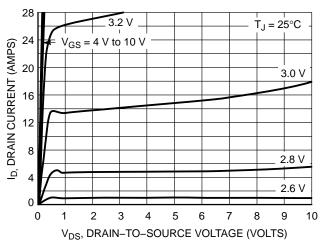
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Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				21		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		T <sub>J</sub> = 25°C			1.0	μΑ
	o Gate Voltage Drain Current $V_{GS} = 0 \text{ V, } V_{DS} = 24 \text{ V}$ $T_{J} = 25^{\circ}\text{C}$ $T_{J} = 125^{\circ}\text{C}$		T <sub>J</sub> = 125°C			10	]
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} =$				±100	nA
ON CHARACTERISTICS (Note 3)	•				•	-	
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 2$	250 μΑ	1.0		2.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				7.4		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> =	= 14 A		4.7	5.5	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> =	= 15 A		3.4	4.5	Ī
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V, I <sub>D</sub> =	= 18 A		25		S
CHARGES, CAPACITANCES AND GATE R	ESISTANCE				•		•
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 15 V			6000		pF
Output Capacitance	C <sub>OSS</sub>				1030		-
Reverse Transfer Capacitance	C <sub>RSS</sub>	1			550		
Total Gate Charge	Q <sub>G(TOT)</sub>				45		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 18 A			6.5		Ī
Gate-to-Source Charge	Q <sub>GS</sub>				16.3		Ī
Gate-to-Drain Charge	$Q_{GD}$	1			19.3		1
Gate Resistance	$R_{G}$				0.60		Ω
SWITCHING CHARACTERISTICS (Note 4)	•				•	•	
Turn-On Delay Time	t <sub>d(ON)</sub>	Voc = 10 V Vpc = 15 V			9.0		ns
Rise Time	t <sub>r</sub>				10		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 1.0 \text{ A}, R_{G} = 1.0 \text{ A}$	6.0 Ω		94		Ī
Fall Time	t <sub>f</sub>				38		Ī
DRAIN-SOURCE DIODE CHARACTERISTI	cs				•	•	
Forward Diode Voltage	$V_{SD}$ $T_{J} = 25^{\circ}C$		T <sub>J</sub> = 25°C		0.8	1.1	V
		V <sub>00</sub> = 0 V I <sub>0</sub> = 3 0 Δ <b></b>	T <sub>J</sub> = 125°C		0.6		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } d_{IS}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 3.0 \text{ A}$			41		ns
Charge Time	t <sub>a</sub>				20		1
Discharge Time	t <sub>b</sub>				21		1
Reverse Recovery Charge	Q <sub>RR</sub>				48		nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

## **TYPICAL PERFORMANCE CURVES**

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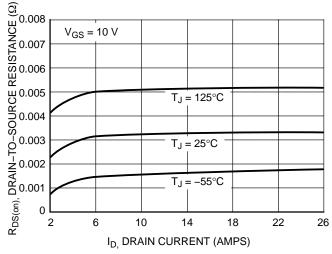


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VDS ≥ 10 V

VDS

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



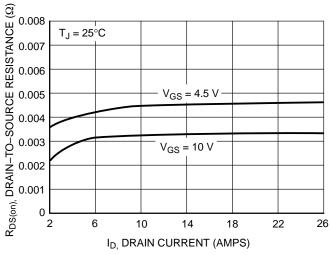
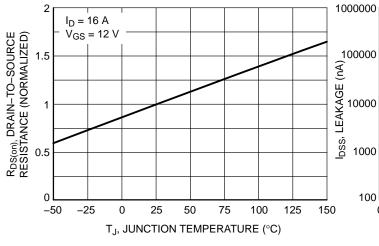


Figure 3. On–Resistance vs. Drain Current and Temperature

Figure 4. On–Resistance vs. Drain Current and Gate Voltage



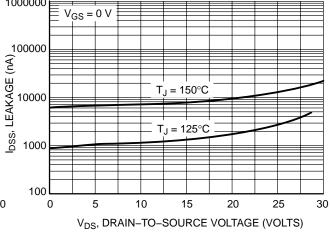
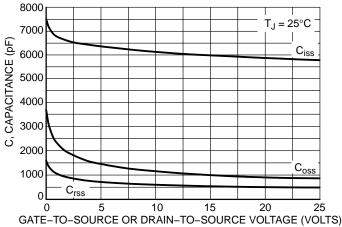


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

## **TYPICAL PERFORMANCE CURVES**

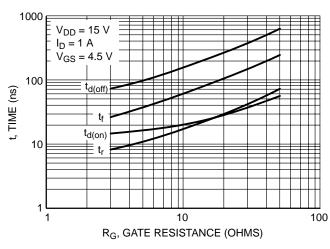
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Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge



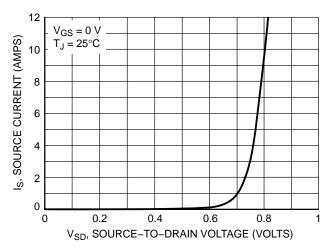


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

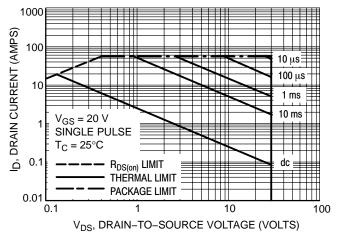
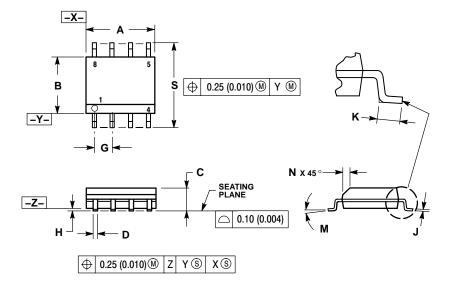


Figure 11. Maximum Rated Forward Biased Safe Operating Area

SO-8 CASE 751-07 **ISSUE AE** 



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
   DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
   751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD 18, 751, 07.
- STANDARD IS 751-07.

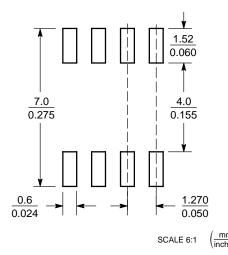
	MILLIMETERS		INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	4.80	5.00	0.189	0.197		
В	3.80	4.00	0.150	0.157		
ဂ	1.35	1.75	0.053	0.069		
D	0.33	0.51	0.013	0.020		
O	1.27 BSC		0.05	0 BSC		
H	0.10	0.25	0.004	0.010		
۲	0.19	0.25	0.007	0.010		
K	0.40	1.27	0.016	0.050		
М	0 °	8 °	0 °	8 °		
Z	0.25	0.50	0.010	0.020		
S	5.80	6.20	0.228	0 244		

## STYLE 12:

- PIN 1. SOURCE
  - SOURCE
     SOURCE
  - GATE

  - DRAIN DRAIN
  - 4. 5. 6. 7. DRAIN
  - DRAIN

### **SOLDERING FOOTPRINT**



#### **NTMS4107N**

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