

MOSFET - Power, Single N-Channel, DUAL COOL®, DFN8 5x6

80 V, 1.4 mΩ, 263 A

NTMFSCH1D4N08X

Features

- Advanced Dual-Sided Cooled Packaging with Lowest Junction-to-TOP Thermal Resistance
- Low Q_{RR}, Soft Recovery Body Diode
- Low R_{DS(on)} to Minimize Conduction Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- ORing FET Load Switching

MAXIMUM RATINGS (T_J = 25°C, Unless otherwise specified)

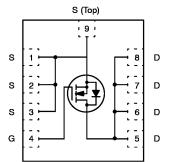
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25°C	I _D	263	Α
(Notes 1, 2)	T _C = 100°C		186	
Power Dissipation (Notes 1, 2)	tes 1, 2) T _C = 25°C		208	W
Pulsed Drain Current	T _C = 25°C,		1110	Α
Pulsed Source Current (Body Diode)	t _p = 100 μs	I _{SM}	1110	Α
Operating Junction and Storage Te	T _J , T _{stg}	-55 to +175	°C	
Source Current (Body Diode)	I _S	355	Α	
Single Pulse Avalanche Energy (I _{pk} = 84 A) (Note 3)		E _{AS}	352	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown.
 They are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal & electromechanical application board design.
- 3. EAS of 352 mJ is based on started T_J = 25 °C, I_{AS} = 84 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

V _{SSS}	R _{SS(ON)} MAX	I _D MAX	
80 V	1.4 mΩ @ 10 V	263 A	

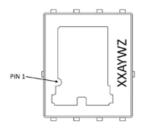
N-CHANNEL MOSFET





DFN8 5.1x6.15 CASE 506FF

MARKING DIAGRAM



3V = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	0.72	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	0.78	
Thermal Resistance, Junction-to-Ambient		39	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				1	.4
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_J}$	I _D = 1 mA. Referenced to 25 °C		33		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, T _J = 25 °C			1.0	μΑ
		V _{DS} = 80 V, T _J = 125 °C			250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 50 A, T _J = 25 °C		1.1	1.4	mΩ
		$V_{GS} = 6 \text{ V}, I_D = 34 \text{ A}, T_J = 25 ^{\circ}\text{C}$			2.4	1
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 348 \mu A, T_{J} = 25 ^{\circ}C$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	ΔV _{GS(TH)} / ΔT _J	$V_{GS} = V_{DS}$, $I_D = 348 \mu A$		-7		mV/°C
Forward Transconductance	9 _F s	V _{DS} = 5 V, I _D = 50 A		184		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE			•	-	
Input Capacitance	C _{ISS}			6303		pF
Output Capacitance	C _{OSS}	1		1825		
Reverse Transfer Capacitance	C _{RSS}	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}, f = 1 \text{ MHz}$		28		
Output Charge	Q _{OSS}			130		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 6 V, V _{DD} = 40 V; I _D = 50 A		55		
		V _{GS} = 10 V, V _{DD} = 40 V;		89		1
Threshold Gate Charge	Q _{G(TH)}	I _D = 50 A		19		1
Gate-to-Source Charge	Q _{GS}]		29		1
Gate-to-Drain Charge	Q_{GD}]		14		1
Gate Plateau Voltage	V_{GP}]		4.6		V
Gate Resistance	R _G	f = 1 MHz		0.5		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{d(ON)}	Resistive Load,		16		ns
Rise Time	t _r	$V_{GS} = 0/10 \text{ V}, V_{DD} = 20 \text{ V},$ $I_D = 50 \text{ A}, R_G = 2.5 \Omega$		60		1
Turn-Off Delay Time	t _{d(OFF)}]		28		1
Fall Time	t _f	1		80		1
SOURCE-TO-DRAIN DIODE CHARACTE	RISTICS			-	<u>-</u>	<u></u>
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 \text{ V}, I_{S} = 50 \text{ A}, T_{J} = 25 ^{\circ}\text{C}$		0.8	1.2	V
		V _{GS} = 0 V, I _S = 50 A, T _J = 125 °C		0.64		1

ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dl/dt = 1000 A/μs, I _S = 50 A, V _{DD} = 40 V, T _J = 25 °C		28		ns
Charge Time	t _a	I _S = 50 A, V _{DD} = 40 V, I _J = 25 °C		16		
Discharge Time	t _b			13		
Reverse Recovery Charge	Q_{RR}	1		249		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

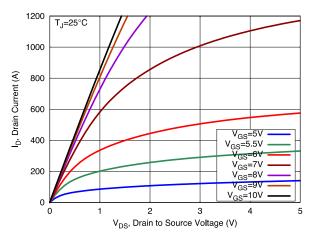


Figure 1. On-Region Characteristics

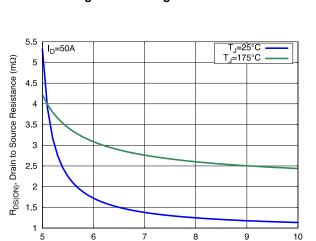


Figure 3. On-Resistance vs. Gate Voltage

V_{GS}, Gate to Source Voltage (V)

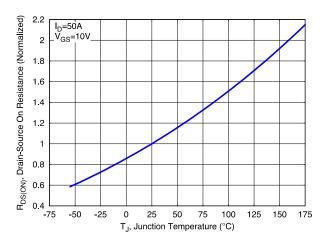


Figure 5. Normalized ON Resistance vs. Junction Temperature

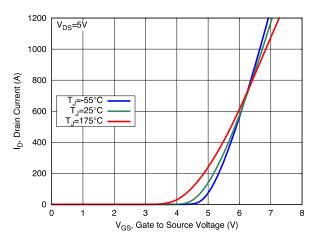


Figure 2. Transfer Characteristics

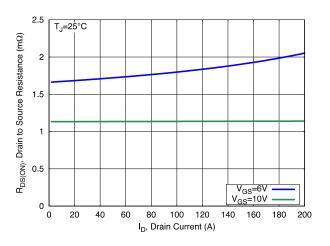


Figure 4. On-Resistance vs. Drain Current

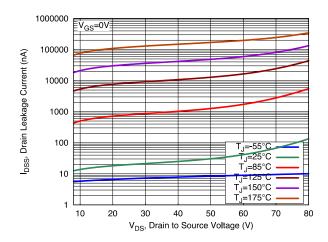


Figure 6. Drain Leakage Current vs Drain Voltage

TYPICAL CHARACTERISTICS

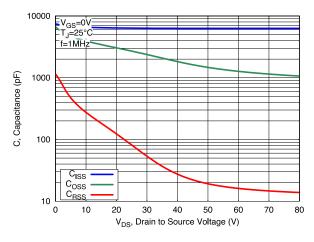


Figure 7. Capacitance Characteristics

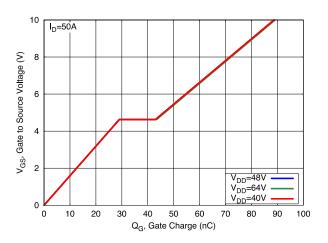


Figure 8. Gate Charge Characteristics

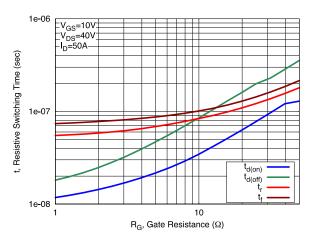


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

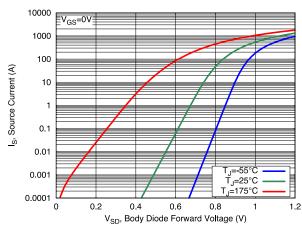


Figure 10. Diode Forward Characteristics

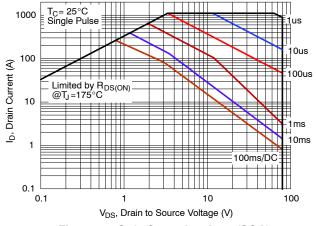


Figure 11. Safe Operating Area (SOA)

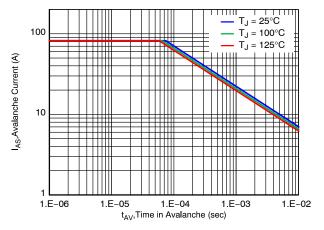
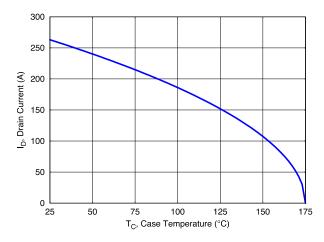


Figure 12. Avalanche Current vs Pulse Time (UIS)

TYPICAL CHARACTERISTICS



1000 (V) 1000 1.E-06 1.E-05 1.E-04 1.E-03 1.E-02 1.E-01 1.E+00 Pulse Width(s)

Figure 13. Maximum Current vs. Case Temperature

Figure 14. IDM vs. Pulse Width

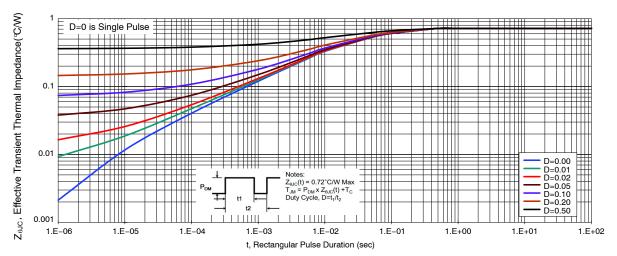


Figure 15. Transient Thermal Response

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSCH1D4N08XTWG	3V	DFN8 5.1x6.15 (Pb-Free/Halogen Free)	3000 / Tape & Reel

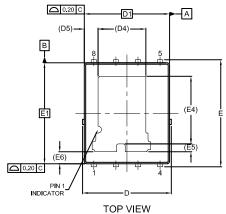
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

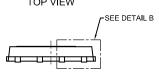
DUAL COOL is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

PACKAGE DIMENSIONS

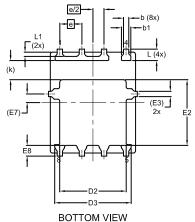
DFN8 4.90x5.80x0.90, 1.27P

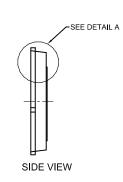
CASE 506FF ISSUE C

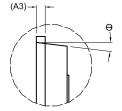




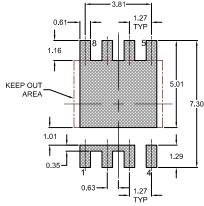
FRONT VIEW







DETAIL A



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRW/D.

SCA	ALE: 2:1	
// 0.10 C		
0.08 C	<u> </u>	
	DETAIL B SCALE: 2:1	SEATING PLANE

NOTES

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- SEATING PLANE IS DEFINED BY THE TERMINALS.
 "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS				
Dilvi	MIN.	NOM.	MAX.		
Α	0.85	0.90	0.95		
A1	-	-	0.05		
A3		0.25 REF			
b	0.21	0.31	0.41		
b1	0.44	0.54	0.64		
D	4.90	5.10	5.30		
D1	4	4.90 BSC	;		
D2	3.72	3.82	3.92		
D3	4.30	4.40	4.50		
D4	2.75 REF				
D5		0.79 REF	=		
Е	6.05	6.15	6.25		
E1	5.80 BSC				
E2	3.67	3.77	3.87		
E3	0.30 REF				
E4	;	3.89 REF	=		
E5	0.45 REF				
E6	0.69 REF				
E7	0.50 REF				
E8	0.52	0.62	0.72		
е	1.27 BSC				
e/2	0.635BSC				
k	1.10 REF				
L	0.56	0.66	0.76		
L1	0.15	0.25	0.35		
θ	0°		7°		

onsemi, ONSEMI, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at

www.onsemi.com/support/sales