MOSFET - Power, Single N-Channel, DUAL COOL®, DFN8 5x6
80 V, 1.4 mΩ, 263 A

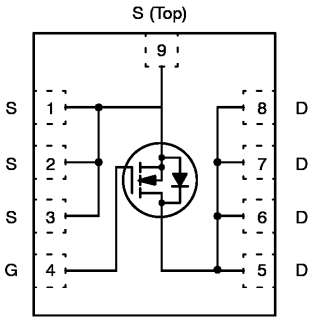
NTMFSCH1D4N08X

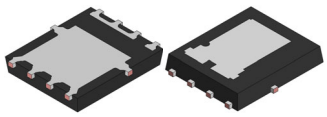
V_{SSS}	$R_{SS(ON)}$ MAX	I_D MAX
80 V	1.4 mΩ @ 10 V	263 A

Features
- Advanced Dual-Sided Cooled Packaging with Lowest Junction-to-TOP Thermal Resistance
- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- ORing FET Load Switching

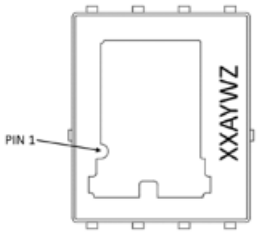
N−CHANNEL MOSFET





DFN8 5.1x6.15
CASE 506FF

MARKING DIAGRAM



3V = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION
See detailed ordering and shipping information on page 6 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C, Unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Notes 1, 2)	T_C = 25°C	I_D	263	A
	T_C = 100°C		186	
Power Dissipation (Notes 1, 2)	T_C = 25°C	P_D	208	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	1110	A
Pulsed Source Current (Body Diode)		I_{SM}	1110	A
Operating Junction and Storage Temperature		T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)		I_S	355	A
Single Pulse Avalanche Energy (I_{pk} = 84 A) (Note 3)		E_{AS}	352	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. EAS of 352 mJ is based on started T_J = 25 °C, I_{AS} = 84 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	0.72	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	0.78	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA. Referenced to 25 °C		33		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25 °C			1.0	μA
		V_{DS} = 80 V, T_J = 125 °C			250	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A, T_J = 25 °C		1.1	1.4	mΩ
		V_{GS} = 6 V, I_D = 34 A, T_J = 25 °C			2.4	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 348 μA, T_J = 25 °C	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 348 μA		−7		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 50 A		184		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		6303		pF
Output Capacitance	C_{OSS}			1825		
Reverse Transfer Capacitance	C_{RSS}			28		
Output Charge	Q_{OSS}			130		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DD} = 40 V; I_D = 50 A		55		
		V_{GS} = 10 V, V_{DD} = 40 V; I_D = 50 A		89		
Threshold Gate Charge	$Q_{G(TH)}$			19		
Gate-to-Source Charge	Q_{GS}			29		
Gate-to-Drain Charge	Q_{GD}			14		
Gate Plateau Voltage	V_{GP}			4.6		V
Gate Resistance	R_G	f = 1 MHz		0.5		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 20 V, I_D = 50 A, R_G = 2.5 Ω		16		ns
Rise Time	t_r			60		
Turn-Off Delay Time	$t_{d(OFF)}$			28		
Fall Time	t_f			80		
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A, T_J = 25 °C		0.8	1.2	V
		V_{GS} = 0 V, I_S = 50 A, T_J = 125 °C		0.64		

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 1000 A/μs, I_S = 50 A, V_{DD} = 40 V, T_J = 25 °C		28		ns
Charge Time	t_a			16		
Discharge Time	t_b			13		
Reverse Recovery Charge	Q_{RR}			249		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

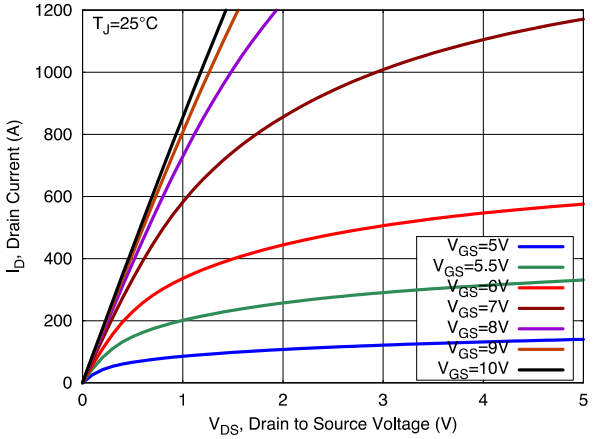


Figure 1. On-Region Characteristics

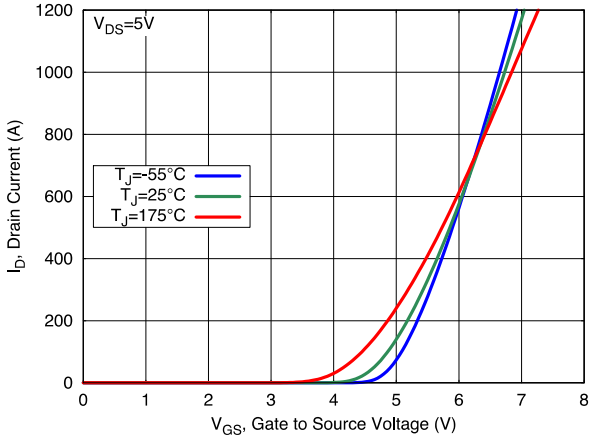


Figure 2. Transfer Characteristics

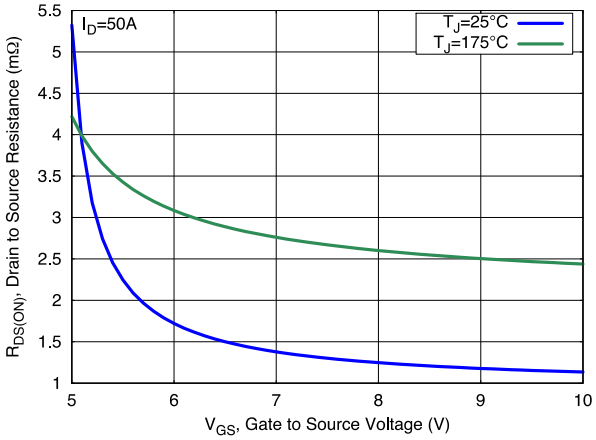


Figure 3. On-Resistance vs. Gate Voltage

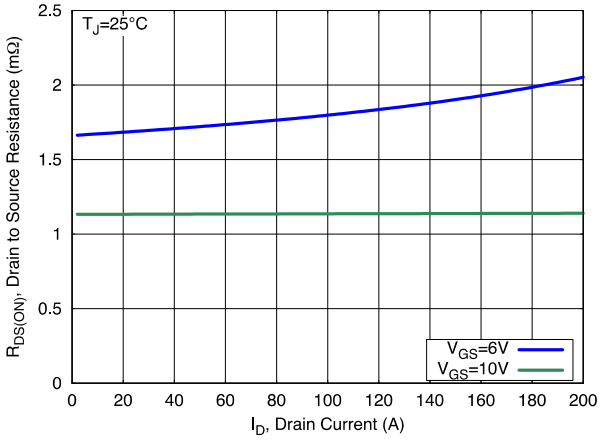


Figure 4. On-Resistance vs. Drain Current

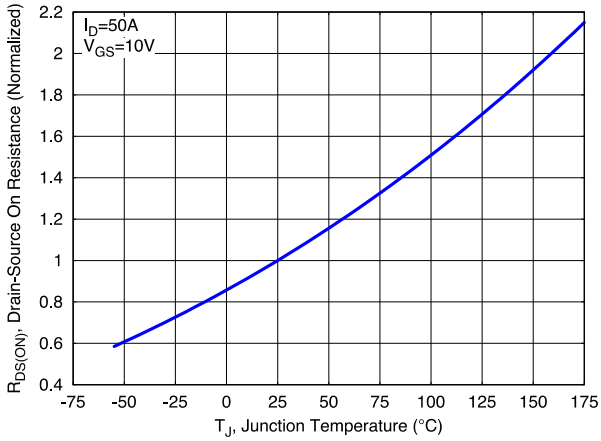


Figure 5. Normalized ON Resistance vs. Junction Temperature

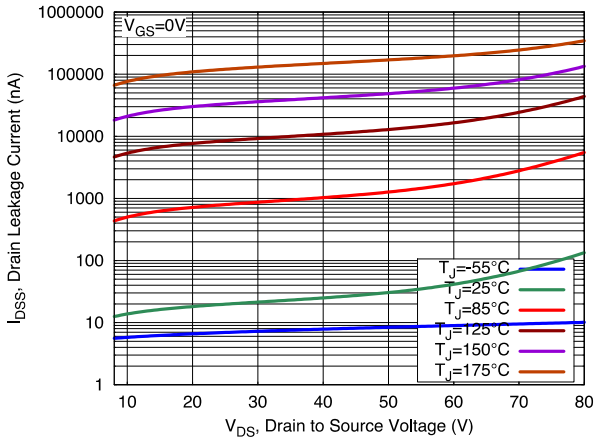


Figure 6. Drain Leakage Current vs Drain Voltage

TYPICAL CHARACTERISTICS

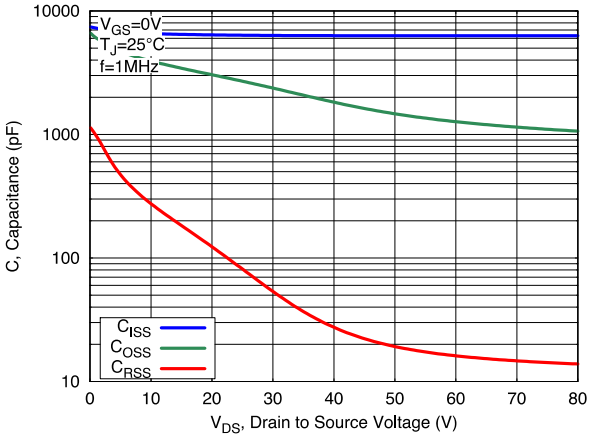


Figure 7. Capacitance Characteristics

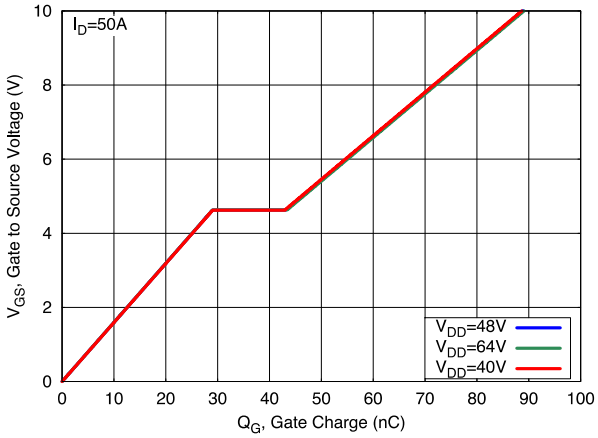


Figure 8. Gate Charge Characteristics

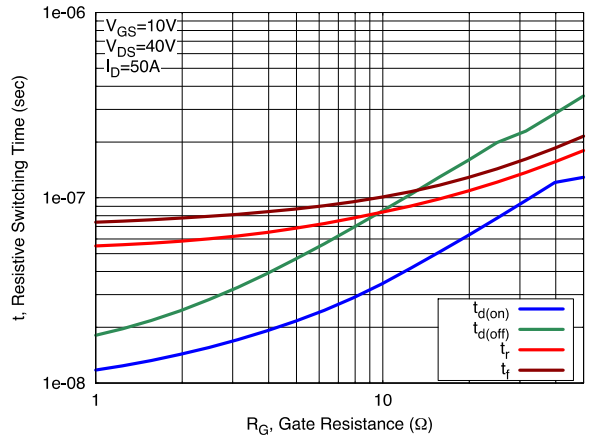


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

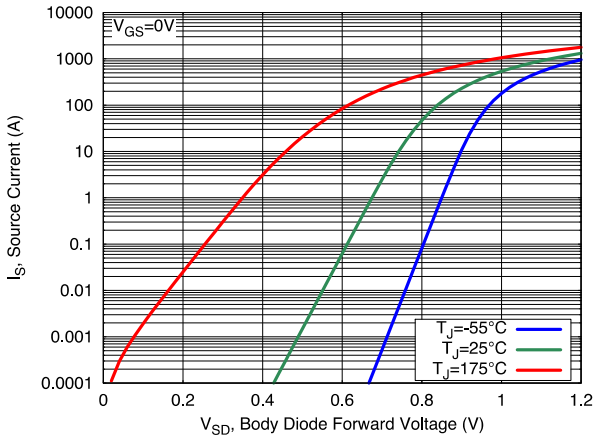


Figure 10. Diode Forward Characteristics

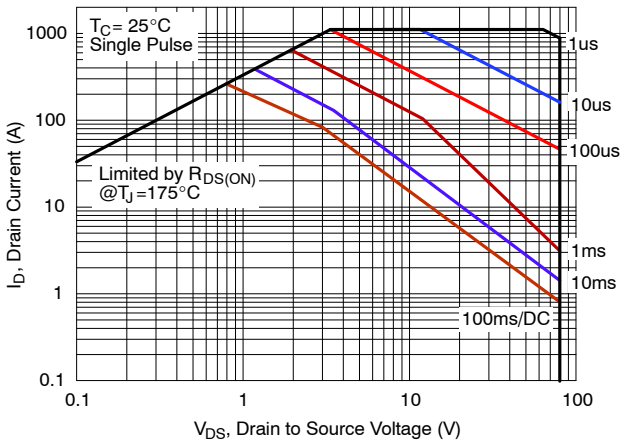


Figure 11. Safe Operating Area (SOA)

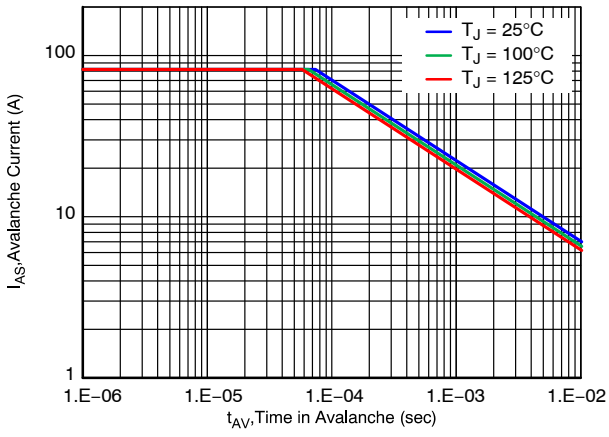


Figure 12. Avalanche Current vs Pulse Time (UIS)

TYPICAL CHARACTERISTICS

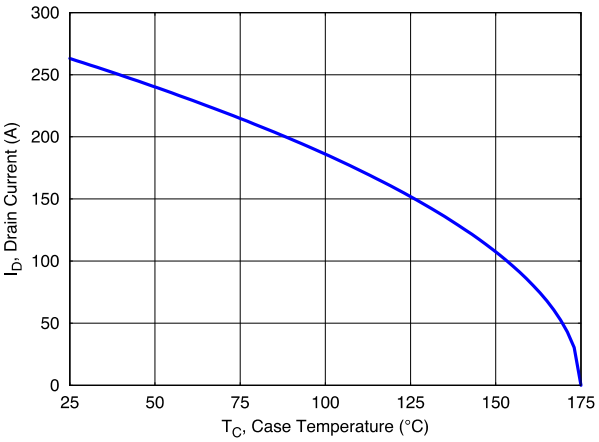


Figure 13. Maximum Current vs. Case Temperature

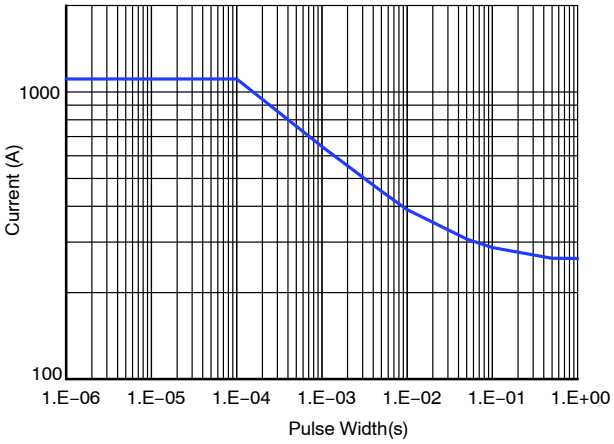


Figure 14. IDM vs. Pulse Width

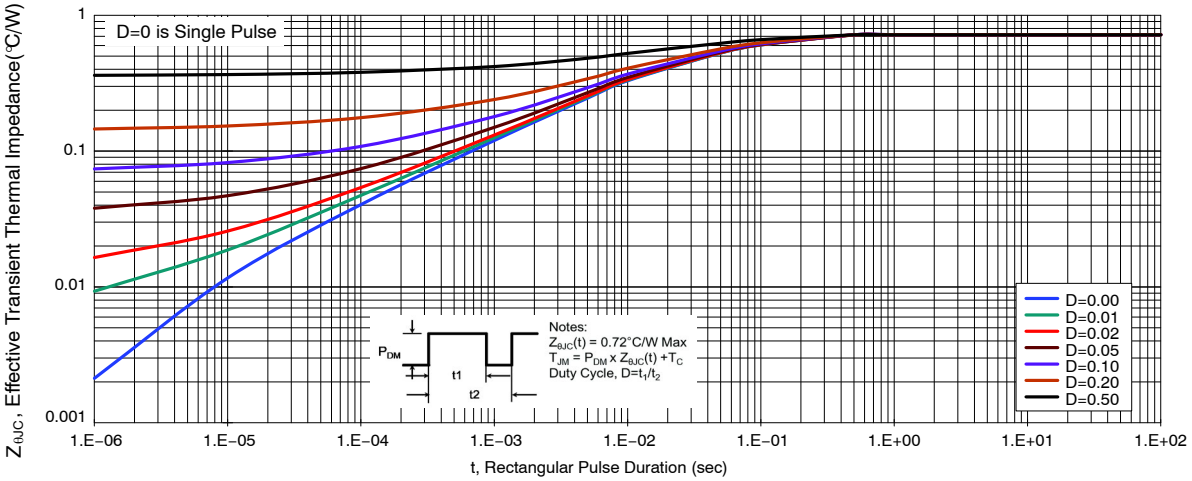


Figure 15. Transient Thermal Response

ORDERING INFORMATION

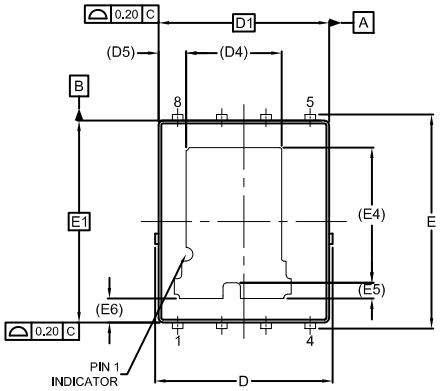
Device	Device Marking	Package	Shipping†
NTMFSCH1D4N08XTWG	3V	DFN8 5.1x6.15 (Pb-Free/Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

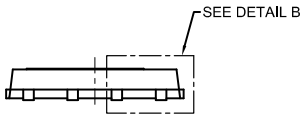
PACKAGE DIMENSIONS

DFN8 4.90x5.80x0.90, 1.27P

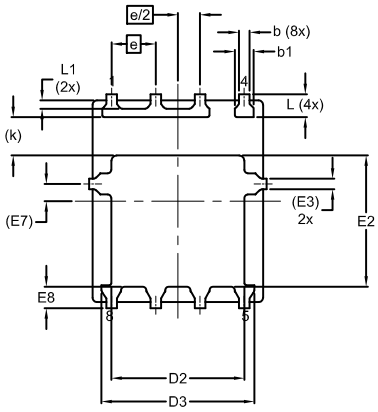
CASE 506FF
ISSUE C



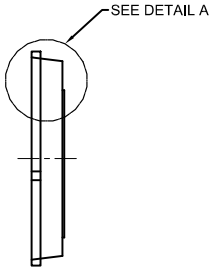
TOP VIEW



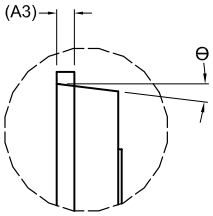
FRONT VIEW



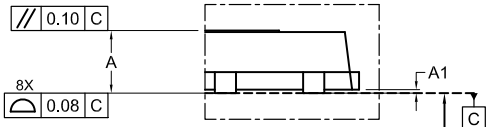
BOTTOM VIEW



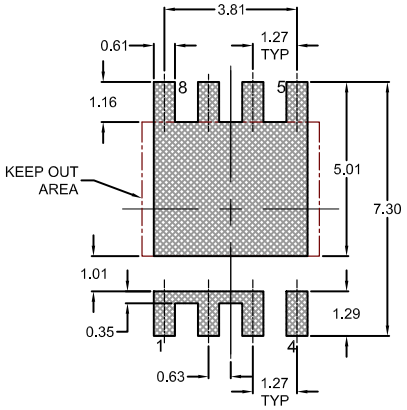
SIDE VIEW



DETAIL A
SCALE: 2:1



DETAIL B
SCALE: 2:1



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A3	0.25 REF		
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.10	5.30
D1	4.90 BSC		
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4	2.75 REF		
D5	0.79 REF		
E	6.05	6.15	6.25
E1	5.80 BSC		
E2	3.67	3.77	3.87
E3	0.30 REF		
E4	3.89 REF		
E5	0.45 REF		
E6	0.69 REF		
E7	0.50 REF		
E8	0.52	0.62	0.72
e	1.27 BSC		
e/2	0.635BSC		
k	1.10 REF		
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
Θ	0°	---	7°

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales