MOSFET - Power, Single N-Channel, SO8-FL
25 V, 0.68 mΩ, 365 A

NTMFS0D8N02P1E

Features
- Small Footprint (5x6mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
- DC−DC Converters
- Power Load Switch
- Notebook Battery Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	25	V
Gate−to−Source Voltage			V_{GS}	+16/ −12	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	365	A
		T_C =85°C		263	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	139	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	55	A
		T_A = 85°C		40	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	3.2	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25°C	I_D	30	A
		T_A = 85°C		21	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25°C	P_D	0.93	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	762	A
Single Pulse Drain−to−Source Avalanche Energy (I_L = 115.4 A_{pk}, L = 0.1 mH) (Note 4)			E_{AS}	666	mJ
Operating Junction and Storage Temperature Range			T_J, T_{STG}	−55 to +150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro−mechanical application board design. $R_{\theta JC}$ is determined by the user's board design.
4. 100% UIS tested at L = 1 mH, I_{AS} = 30.7 A.

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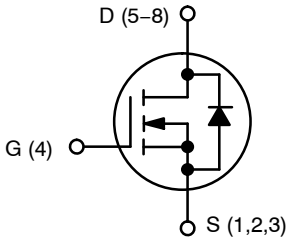
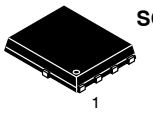
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
25 V	0.68 mΩ @ 10 V	365 A
	0.80 mΩ @ 4.5 V	

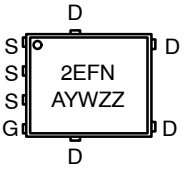


N−CHANNEL MOSFET

MARKING DIAGRAMS



SO−8 FLAT LEAD CASE 488AA STYLE 1



2EFN = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION
See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	0.9	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	39	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	135	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA. ref to 25°C			16		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C			1	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +16 V/−12 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 2 mA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 2 mA. ref to 25°C			−4.4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 46 A			0.44	0.68	mΩ
		V_{GS} = 4.5 V, I_D = 43 A			0.54	0.80	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 46 A			307		S
Gate Resistance	R_G	T_A = 25°C			0.48		Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 13 V, f = 1 MHz			8600		pF
Output Capacitance	C_{OSS}				2285		
Reverse Transfer Capacitance	C_{RSS}				129		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 13 V; I_D = 46 A			52		nC
Threshold Gate Charge	$Q_{G(TH)}$				10		
Gate−to−Source Charge	Q_{GS}				21		
Gate−to−Drain Charge	Q_{GD}				9		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 13 V; I_D = 46 A			116		nC
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 13 V, I_D = 46 A, R_G = 6.0 Ω			45		ns
Rise Time	t_r				24		
Turn−Off Delay Time	$t_{d(OFF)}$				68		
Fall Time	t_f				20		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 13 V, I_D = 46 A, R_G = 6.0 Ω			23		ns
Rise Time	t_r				6.8		
Turn−Off Delay Time	$t_{d(OFF)}$				123		
Fall Time	t_f				19		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 46 A	T_J = 25°C		0.77	1.2	V
			T_J = 125°C		0.62		

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 46 A		64		ns
Reverse Recovery Charge	Q_{RR}			87		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

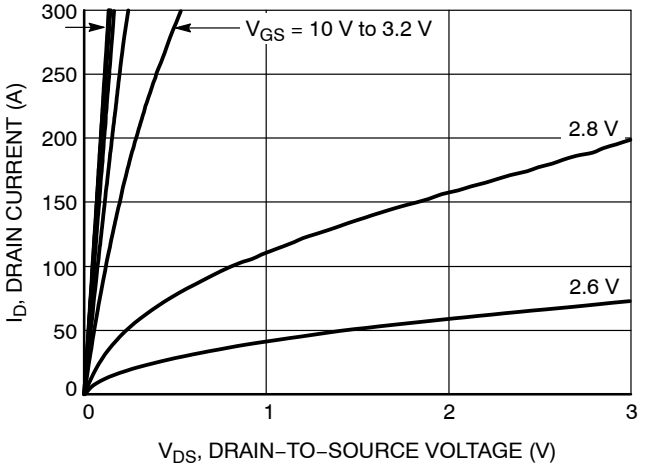


Figure 1. On−Region Characteristics

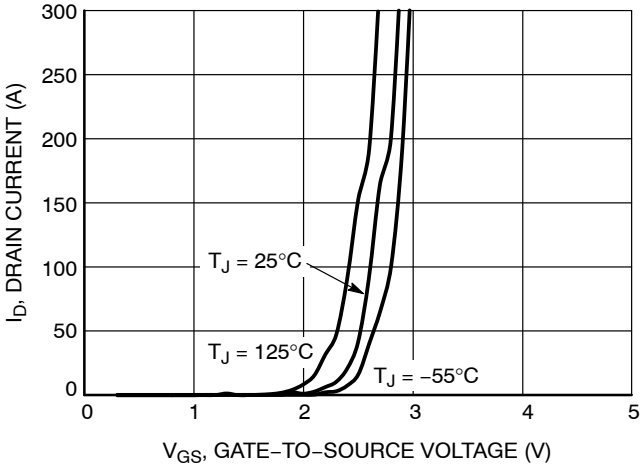


Figure 2. Transfer Characteristics

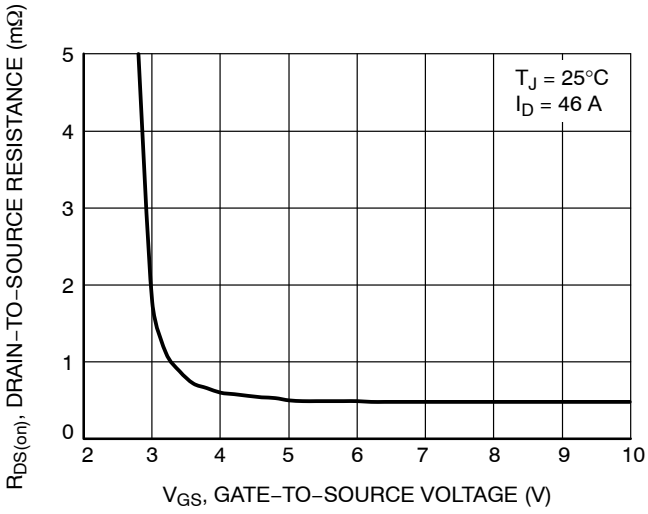


Figure 3. On−Resistance vs. Gate−to−Source Voltage

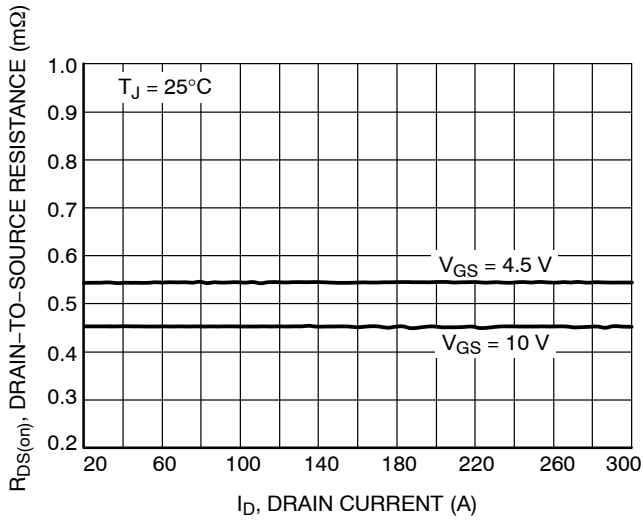


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

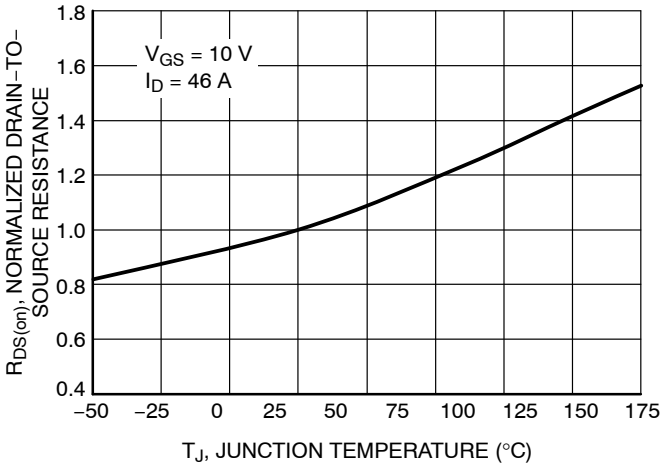


Figure 5. On−Resistance Variation with Temperature

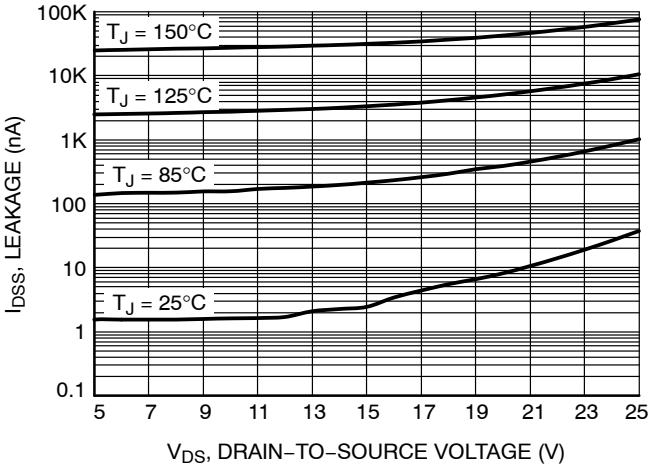


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

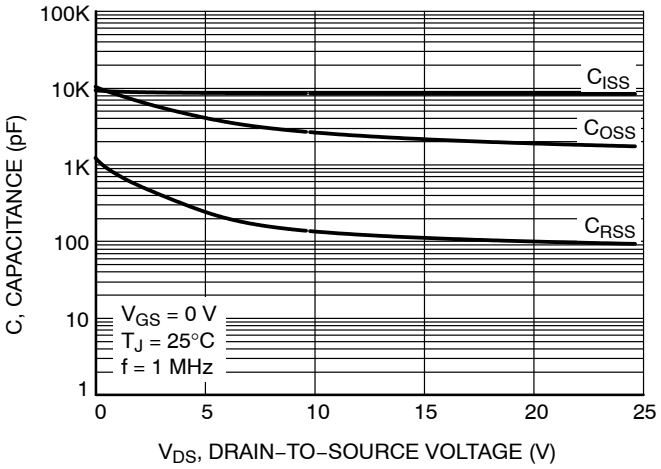


Figure 7. Capacitance Variation

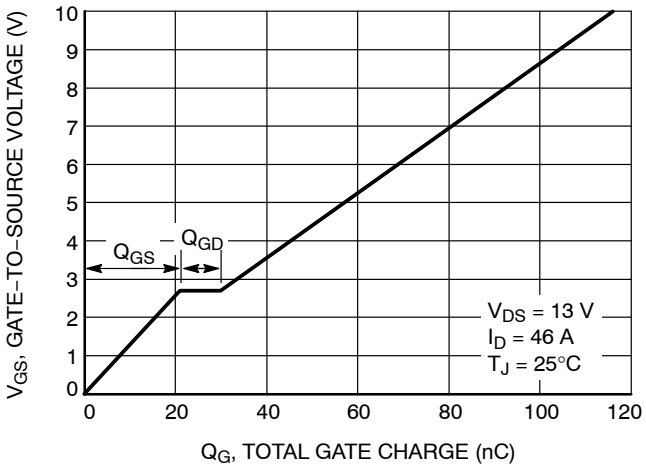


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

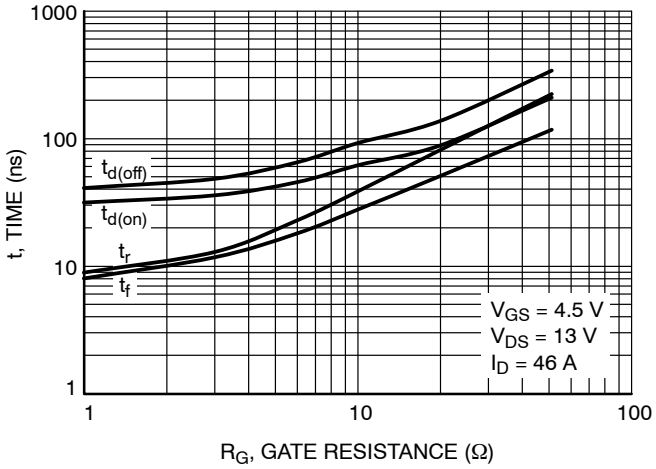


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

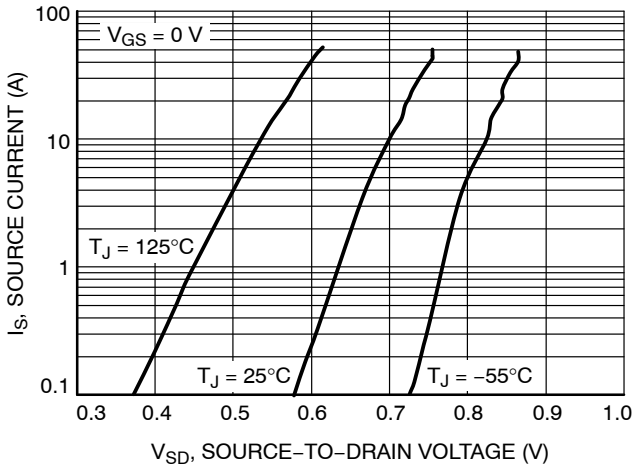


Figure 10. Diode Forward Voltage vs. Current

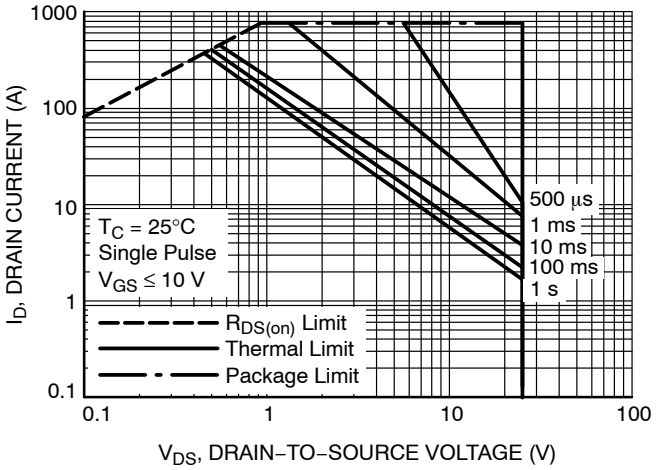


Figure 11. Safe Operating Area

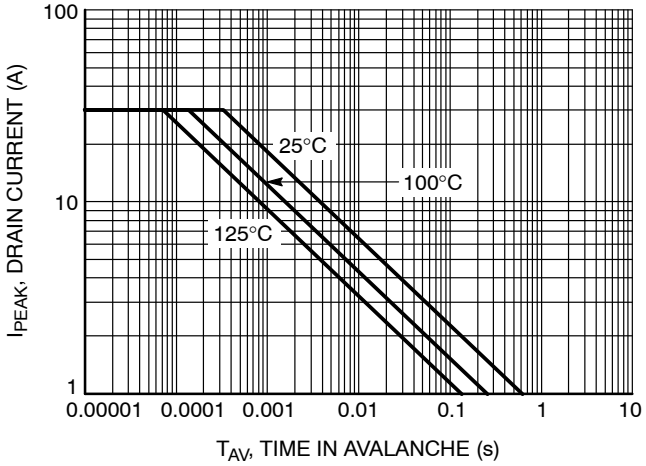


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

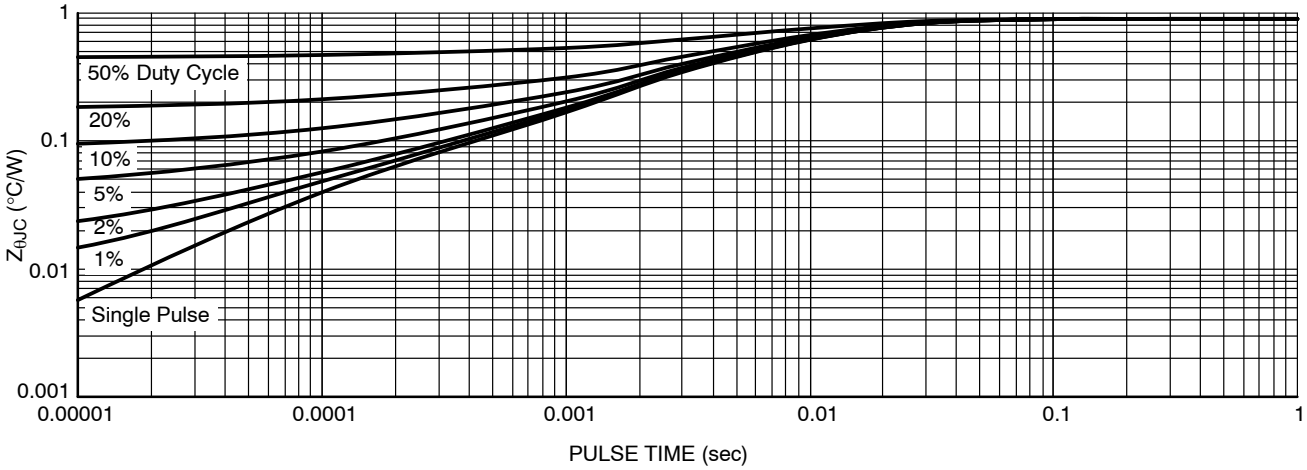
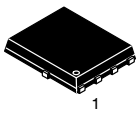


Figure 13. Thermal Impedance

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS0D8N02P1ET1G	2EFN	DFN5 (Pb−Free)	1500 / Tape & Reel

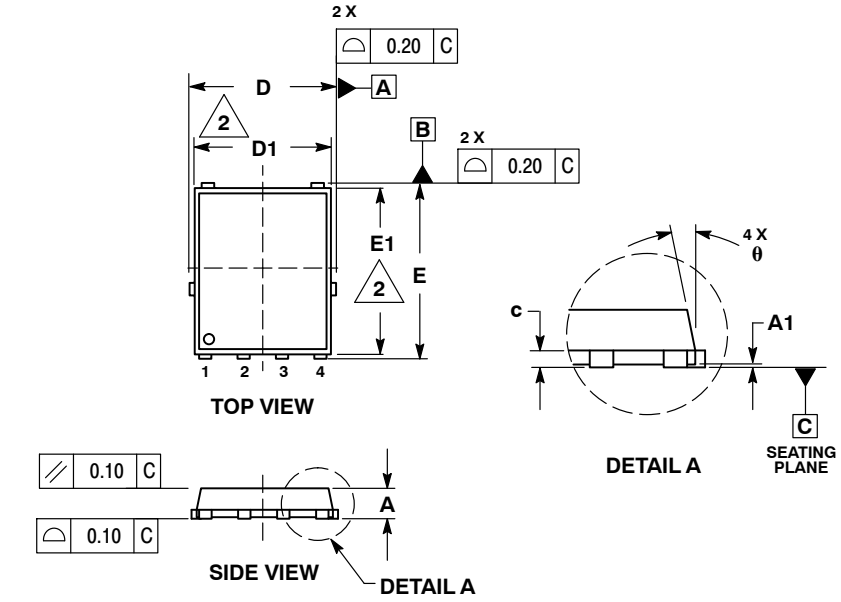
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

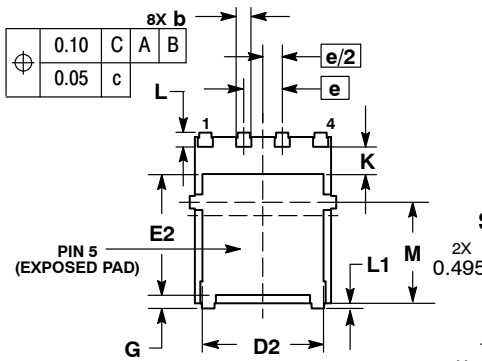
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

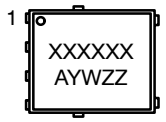


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °



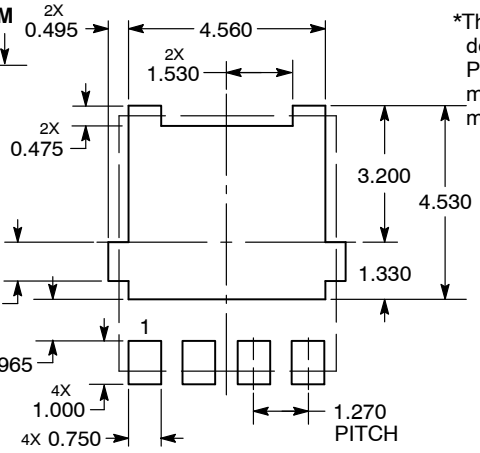
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON14036D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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