Power MOSFET

30 V, 4.6 A, µCool™ Dual N–Channel, 2x2 mm WDFN Package

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88
- Lowest R_{DS(on)} Solution in 2x2 mm Package
- 1.5 V R_{DS(on)} Rating for Operation at Low Voltage Gate Drive Logic Level
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- DC-DC Converters (Buck and Boost Circuits)
- Low Side Load Switch
- Optimized for Battery and Load Management Applications in Portable Equipment such as, Cell Phones, PDA's, Media Players, etc.
- Level Shift for High Side Load Switch

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage	Gate-to-Source Voltage			±8.0	V
Continuous Drain	Steady	$T_A = 25^{\circ}C$	I _D	3.7	Α
Current (Note 1)	State	T _A = 85°C		2.7	
	t ≤ 5 s	T _A = 25°C		4.6	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.5	W
	t ≤ 5 s			2.3	
Continuous Drain		$T_A = 25^{\circ}C$	I _D	2.5	Α
Current (Note 2)	Steady	T _A = 85°C		1.8	
Power Dissipation (Note 2)	State	T _A = 25°C	P _D	0.71	W
Pulsed Drain Current	t _p =	10 μs	I_{DM}	20	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	2.0	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz Cu.

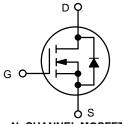


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V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX (Note 1)
	70 mΩ @ 4.5 V	
30 V	90 mΩ @ 2.5 V	4.6 A
	125 mΩ @ 1.8 V	
	250 mΩ @ 1.5 V	



N-CHANNEL MOSFET

MARKING DIAGRAM



WDFN6 CASE 506AN



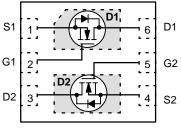
JF = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTLJD4116NT1G	WDFN6 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
SINGLE OPERATION (SELF-HEATED)			
Junction-to-Ambient - Steady State (Note 3)	$R_{ heta JA}$	83	
Junction-to-Ambient - Steady State Min Pad (Note 4)	$R_{ heta JA}$	177	°C/W
Junction-to-Ambient - t ≤ 5 s (Note 3)	$R_{ heta JA}$	54	ururur DataShao
DUAL OPERATION (EQUALLY HEATED)		·	
Junction-to-Ambient - Steady State (Note 3)	$R_{ hetaJA}$	58	
Junction-to-Ambient - Steady State Min Pad (Note 4)	$R_{ hetaJA}$	133	°C/W
Junction–to–Ambient – t ≤ 5 s (Note 3)	$R_{ hetaJA}$	40	

Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise noted)

Parameter	Symbol	Test Condition	าร	Min	Тур	Max	Unit
OFF CHARACTERISTICS					•		•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, Ref to	25°C		18.1		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V 04.V.V 0.V	$T_J = 25^{\circ}C$			√1,0 _W ,	Data A heet
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	T _J = 85°C			10	1
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm$	8.0 V			100	nA
ON CHARACTERISTICS (Note 5)							•
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 25$	50 μΑ	0.4	0.7	1.0	V
Negative Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J				2.8		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	$V_{GS} = 4.5, I_D = 2$.0 A		47	70	mΩ
		$V_{GS} = 2.5, I_D = 2$.0 A		56	90	1
		$V_{GS} = 1.8, I_D = 1$.8 A		88	125	1
		V _{GS} = 1.5, I _D = 1.5 A			133	250	
Forward Transconductance	9 _{FS}	$V_{DS} = 5.0 \text{ V}, I_{D} = 2.0 \text{ V}$	2.0 A		4.5		S
CHARGES, CAPACITANCES AND GA	TE RESISTAN	CE					
Input Capacitance	C _{ISS}				427		pF
Output Capacitance	C _{OSS}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ V}_{DS} = 15 \text{ V}$	MHz,		51		
Reverse Transfer Capacitance	C _{RSS}	103 - 10 V			32		
Total Gate Charge	$Q_{G(TOT)}$				5.4	6.5	nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$ $I_{D} = 2.0 \text{ A}$			0.5		7
Gate-to-Source Charge	Q_GS	$I_D = 2.0 \text{ A}$			0.8		
Gate-to-Drain Charge	Q_{GD}				1.24		
Gate Resistance	R_{G}				0.37		Ω
SWITCHING CHARACTERISTICS (No	ote 6)						
Turn-On Delay Time	t _{d(ON)}				4.8		ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{DD} =$	15 V,		11.8		1
Turn-Off Delay Time	t _{d(OFF)}	$V_{GS} = 4.5 \text{ V}, V_{DD} = 15 \text{ V},$ $I_{D} = 2.0 \text{ A}, R_{G} = 2.0 \Omega$			14.2		1
Fall Time	t _f				1.7		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Recovery Voltage	V_{SD}	V 0V 10 0 5 1	T _J = 25°C		0.78	1.2	.,
		$V_{GS} = 0 \text{ V, IS} = 2.0 \text{ A}$	T _J = 125°C		0.62		V
Reverse Recovery Time	t _{RR}		•		10.5		
Charge Time	t _a	$V_{GS} = 0 \text{ V, } d_{ISD}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 2.0 \text{ A}$			7.6		ns
Discharge Time	t _b				2.9		1
Reverse Recovery Time	Q_{RR}				5.0		nC

^{5.} Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

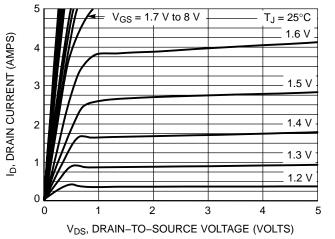


Figure 1. On–Region Characteristics

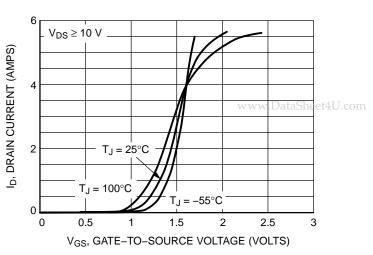


Figure 2. Transfer Characteristics

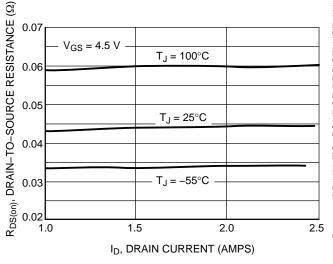


Figure 3. On-Resistance versus Drain Current

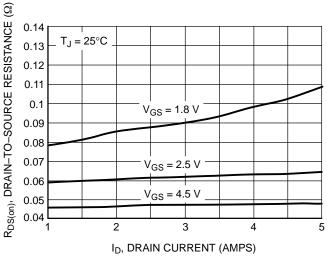


Figure 4. On–Resistance versus Drain Current and Gate Voltage

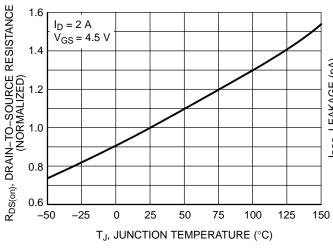


Figure 5. On–Resistance Variation with Temperature

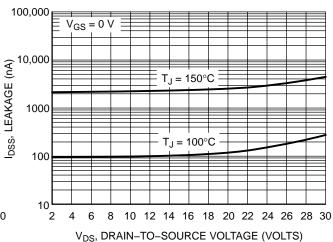
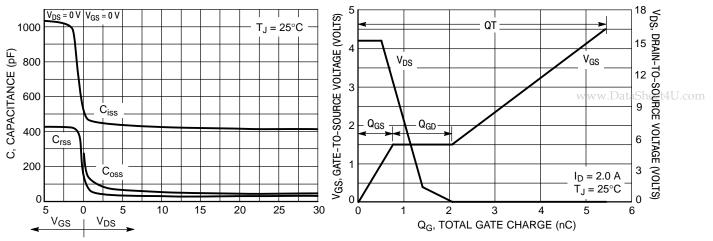


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

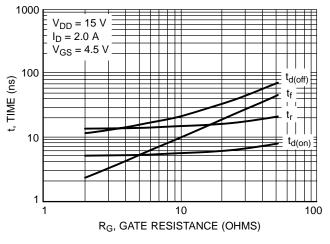


Figure 9. Resistive Switching Time Variation versus Gate Resistance

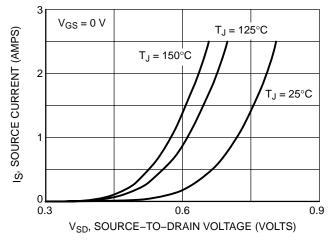


Figure 10. Diode Forward Voltage versus Current

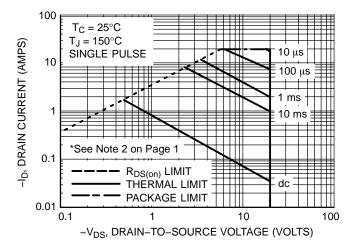


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

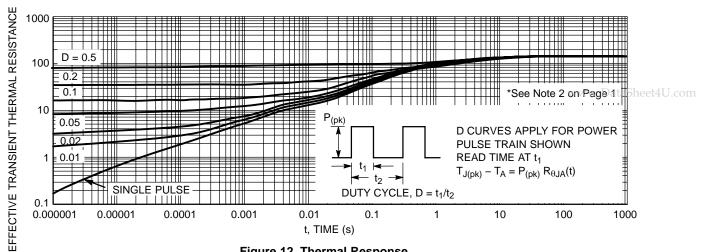
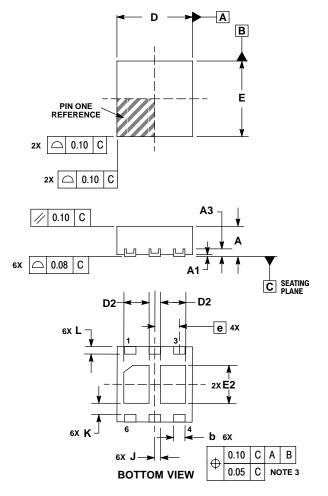


Figure 12. Thermal Response

PACKAGE DIMENSIONS

WDFN6, 2x2 CASE 506AN-01 **ISSUE B**



NOTES:

- OTES:

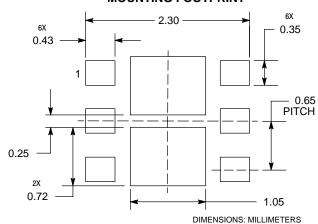
 1. DIMENSIONING AND TOLERANCING PER
 ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

 DIMENSION & ARRIVES TO PLATED.

 DIMENSION & ARRIVES TO PLATED.
- DIMENSION & APPLIES TO PLATED
 TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS			
DIM	MIN	MAX		
Α	0.70	0.80		
A1	0.00	0.05		
A3	0.20 REF			
b	0.25	0.35		
D	2.00 BSC			
D2	0.57	0.77		
E	2.00 BSC			
E2	0.90	1.10		
е	0.65 BSC			
K	0.25 REF			
L	0.20	0.30		
J	0.15 REF			

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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