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NTE74C221
Integrated Circuit
TTL– CMOS Dual Monostable Multivibrator
16–Lead DIP

Description:

The NTE74C221 dual monostable multivibrator is a monolithic complementary MOS (CMOS) integrated circuit in a 16–Lead DIP type package. Each multivibrator features a negative–transition–triggered input and a positive–transition–triggered input, either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature an V_{CC}.

Features:

- Wide Supply Range: 4.5V to 15V
- Guaranteed Noise Margin: 1.0V
- High Noise Immunity: 0.45 V_{CC} (typ)
- Low Power TTL Compatibility: Fan Out of 2 Driving 74L

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin . . . . –0.3V to V_{CC} +0.3V
Power Dissipation, P_D 700mW
Operating V_{CC} Range . . . . 4.5V to 15V
Maximum V_{CC} Voltage ($R_{EXT} \geq 80\ V_{CC}$ (Ω)) 18V
Operating Temperature Range, T_A . . . . –40° to +85°C
Storage Temperature Range, T_{stg} . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which th safety of the device cannot be guaranteed. Except for “Operating Temperature Range”, they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = −40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical "1" Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V	I_O = −10µA	4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical "0" Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V	I_O = 10µA	–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical "1" Input Current	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		–	0.005	1.0	µA
Logical "0" Input Current	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V		−1.0	−0.005	–	µA
Supply Current (Standby)	I_{CC}	V_{CC} = 15V, R_{EXT} = ∞, Q1, Q2 = Logic "0", Note 2		–	0.05	300	µA
Supply Current (During Output Pulse)	I_{CC}	V_{CC} = 15V, Q1 = Logic "1", Q2 = Logic "0"		–	15	–	mA
				–	2	–	mA
Leakage Current at R/C_{EXT}Pin		V_{CC} = 15V, V_{CEXT} = 5V		–	0.01	3.0	µA
CMOS/LPTTL Interface							
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}−1.5	–	–	V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical "1" Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360µA		2.4	–	–	V
Logical "0" Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = 360µA		–	–	0.4	V
Output Drive							
Output Source Current (P−Channel)	I_{SOURCE}	V_{CC} = 5V	V_{OUT} = 0, T_A = +25°C	−1.75	–	–	mA
		V_{CC} = 10V		−8	–	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{CC} = 5V	V_{OUT} = V_{CC}, T_A = +25°C	1.75	–	–	mA
		V_{CC} = 10V		8	–	–	mA

Note 2. In Standby (Q = Logic "0") the power dissipation equals the leakage current plus V_{CC}/R_{EXT}.

AC Electrical Characteristics: (T_A = +25°, C_L = 50pF, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay from Trigger Input (A, B) to Output Q, $\overline{Q}$	$t_{PD(A)}$, $t_{PD(B)}$	V_{CC} = 5V	–	250	500	ns
		V_{CC} = 10V	–	120	250	ns
Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$	$t_{PD(CL)}$	V_{CC} = 5V	–	250	500	ns
		V_{CC} = 10V	–	120	250	ns
Time Prior to Trigger Input (A, B) that Clear must be Set	t_S	V_{CC} = 5V	150	50	–	ns
		V_{CC} = 10V	60	20	–	ns
Trigger Input (A, B) Pulse Width	$t_{W(A,B)}$	V_{CC} = 5V	150	50	–	ns
		V_{CC} = 10V	70	30	–	ns
Clear Input (CL) Pulse Width	$t_{W(CL)}$	V_{CC} = 5V	150	50	–	ns
		V_{CC} = 10V	70	30	–	ns

Note 3. AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Cont'd): (T_A = +25°, C_L = 50pF, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Q or $\overline{Q}$ Output Pulse Width	$t_{W(OUT)}$	V_{CC} = 5V	R_{EXT} = 10kΩ, C_{EXT} = 0pF	–	900	–	ns
		V_{CC} = 10V		–	350	–	ns
		V_{CC} = 15V		–	320	–	ns
Q or $\overline{Q}$ Output Pulse Width	$t_{W(OUT)}$	V_{CC} = 5V	R_{EXT} = 10kΩ, C_{EXT} = 1000pF	9.0	10.6	12.2	μs
		V_{CC} = 10V		9.0	10.0	11.0	μs
		V_{CC} = 15V		5.9	9.8	10.8	μs
Q or $\overline{Q}$ Output Pulse Width	$t_{W(OUT)}$	V_{CC} = 5V	R_{EXT} = 10kΩ, C_{EXT} = 0.1pF	900	1020	1200	μs
		V_{CC} = 10V		900	1000	1100	μs
		V_{CC} = 15V		900	990	1100	μs
ON Resistance of Transistor between R/C_{EXT} to C_{EXT}	R_{ON}	V_{CC} = 5V		–	50	150	Ω
		V_{CC} = 10V		–	25	65	Ω
		V_{CC} = 15V		–	16.7	45	Ω
Output Duty Cycle		C = 1000pF	R = 10kΩ, Note 4	900	1020	1200	μs
		C = 0.1μF		900	1000	1100	μs
Input Capacitance	C_{IN}	R/C_{EXT} Input, Note 5		–	15	25	pF
		Any Other Input, Note 6		–	5	–	pF

Note 3. AC Parameters are guaranteed by DC correlated testing.
Note 4. Maximum output duty cycle = R_{EXT}/R_{EXT} + 1000.
Note 5. Capacitance is guaranteed by periodic testing.

Truth Table:

Inputs			Outputs	
Clear	**A**	**B**	**Q**	**$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔

H = High Level
L = Low Level
X = Irrelavent
↑ = Transition from LOW–to–HIGH
↓ = Transition from HIGH–to–LOW
⎍ = One HIGH Level Pulse
⊔ = One LOW Level Pulse

Pin Connection Diagram