

# NTD6414AN

## N-Channel Power MOSFET 100 V, 32 A, 37 mΩ

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	100	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$	$I_D$	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Power Dissipation $R_{\theta JC}$	$P_D$	100	W
Pulsed Drain Current	$I_{DM}$	117	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	$-55$ to $+175$	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	32	A
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 50$ Vdc, $V_{GS} = 10$ Vdc, $I_{L(pk)} = 32$ A, $L = 0.3$ mH, $R_G = 25$ $\Omega$ )	$E_{AS}$	154	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	$T_L$	260	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	1.5	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	37	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

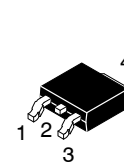
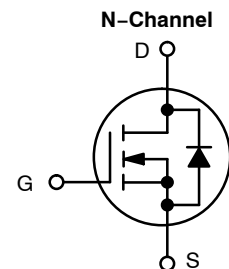
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).



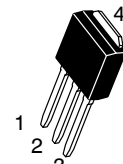
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX (Note 1)
100 V	37 mΩ @ 10 V	32 A

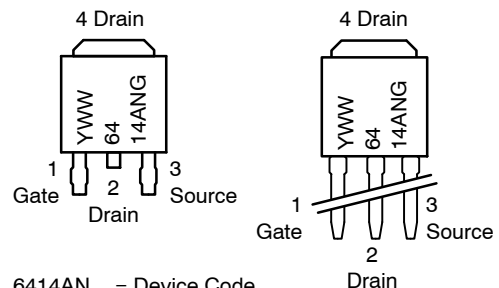


**DPAK  
CASE 369AA  
STYLE 2**



**IPAK  
CASE 369D  
STYLE 2**

### MARKING DIAGRAM & PIN ASSIGNMENTS



6414AN = Device Code  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			107		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

**ON CHARACTERISTICS** (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			8.3		mV/ $^\circ\text{C}$
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 32\text{ A}$		30	37	m $\Omega$
Forward Transconductance	gFS	$V_{GS} = 5.0\text{ V}, I_D = 10\text{ A}$		18		S

**CHARGES, CAPACITANCES AND GATE RESISTANCE**

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1450		pF
Output Capacitance	$C_{OSS}$			230		
Reverse Transfer Capacitance	$C_{RSS}$			95		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 80\text{ V}, I_D = 32\text{ A}$		40		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.7		
Gate-to-Source Charge	$Q_{GS}$			8.0		
Gate-to-Drain Charge	$Q_{GD}$			20		
Plateau Voltage	$V_{GP}$			5.9		
Gate Resistance	$R_G$			1.9		$\Omega$

**SWITCHING CHARACTERISTICS** (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 80\text{ V}, I_D = 32\text{ A}, R_G = 6.1\text{ }\Omega$		11		ns
Rise Time	$t_r$			52		
Turn-Off Delay Time	$t_{d(off)}$			38		
Fall Time	$t_f$			48		

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**DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 32\text{ A}$	$T_J = 25^\circ\text{C}$		0.87	1.2	V
			$T_J = 125^\circ\text{C}$		0.76		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 32\text{ A}$			68		ns
Charge Time	$T_a$				51		
Discharge Time	$T_b$				16		
Reverse Recovery Charge	$Q_{RR}$				195		nC

2. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

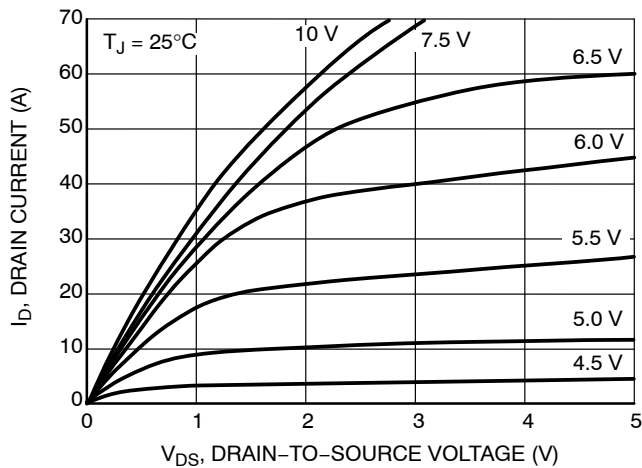


Figure 1. On-Region Characteristics

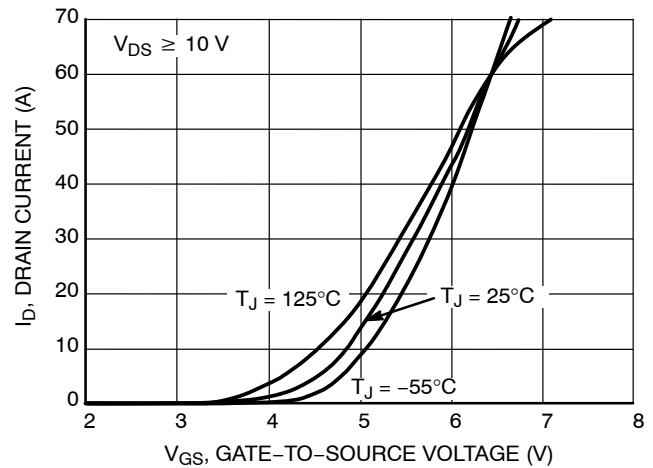


Figure 2. Transfer Characteristics

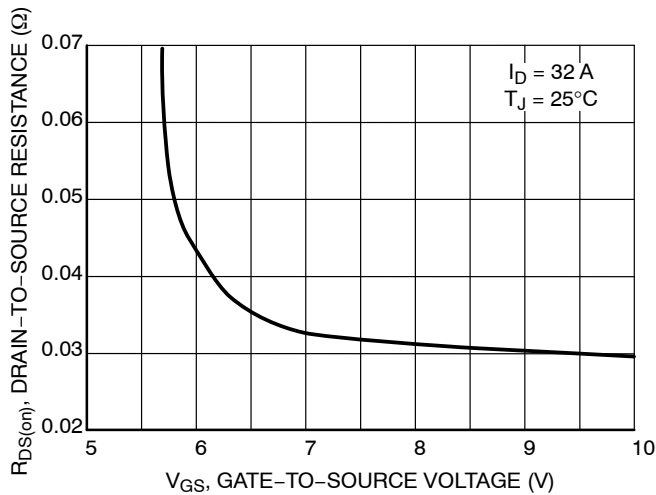


Figure 3. On-Region versus Gate Voltage

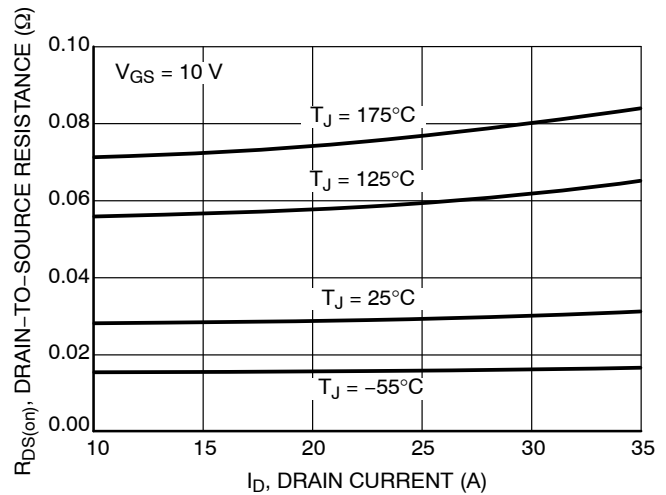


Figure 4. On-Resistance versus Drain Current and Gate Voltage

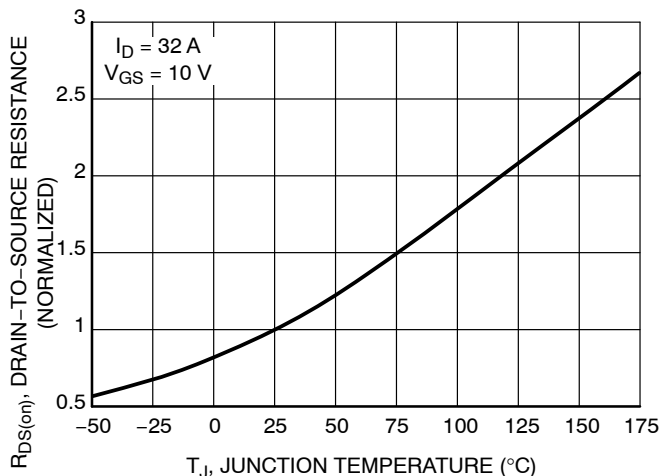


Figure 5. On-Resistance Variation with Temperature

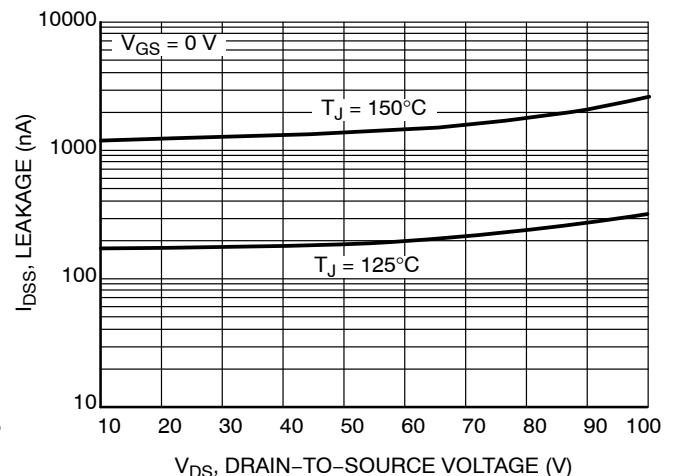


Figure 6. Drain-to-Source Leakage Current versus Voltage

## TYPICAL CHARACTERISTICS

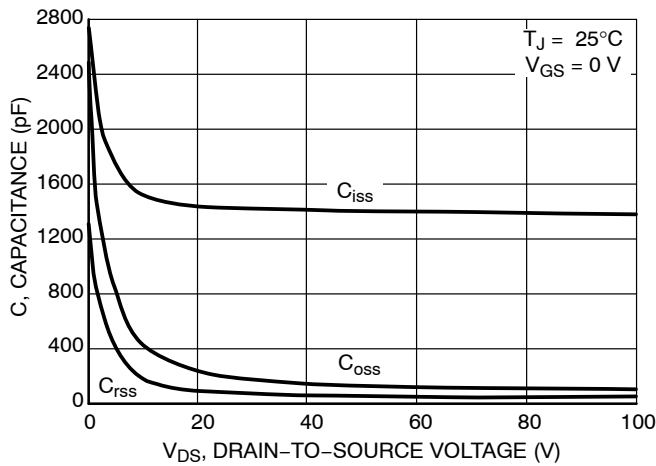


Figure 7. Capacitance Variation

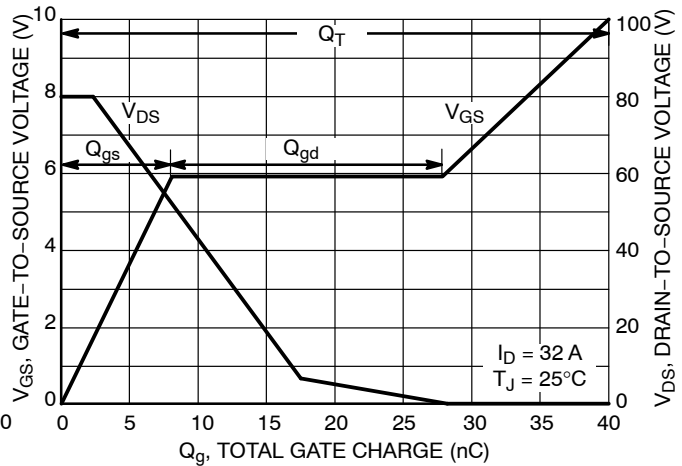


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

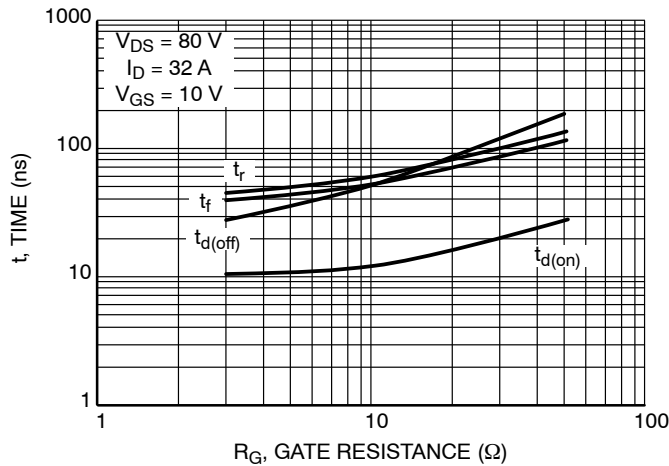


Figure 9. Resistive Switching Time Variation versus Gate Resistance

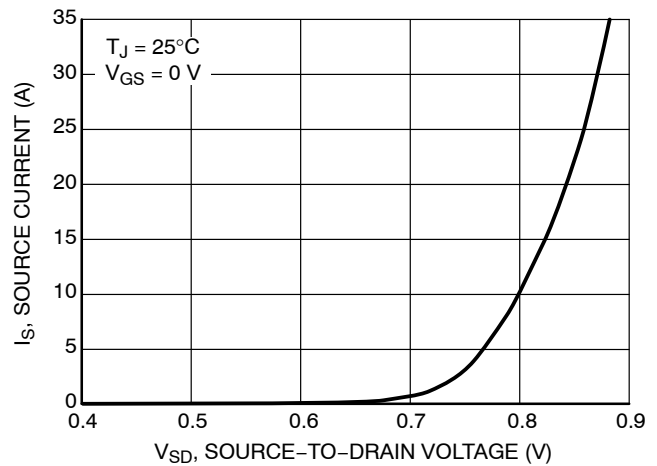


Figure 10. Diode Forward Voltage versus Current

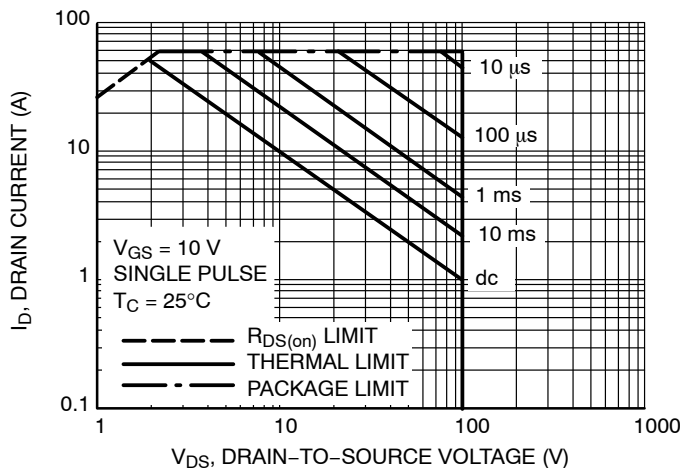


Figure 11. Maximum Rated Forward Biased Safe Operating Area

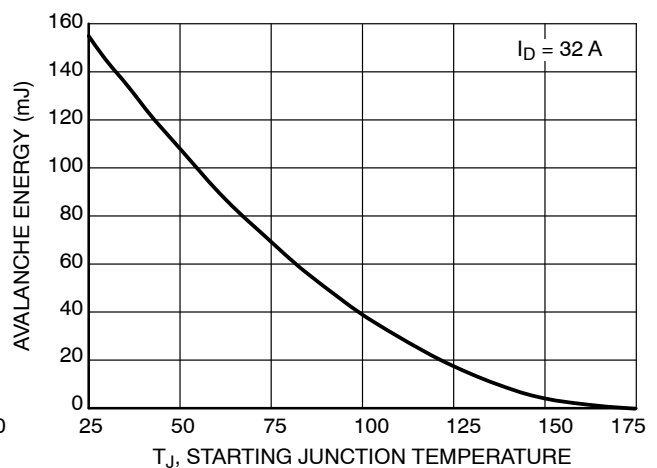


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL CHARACTERISTICS

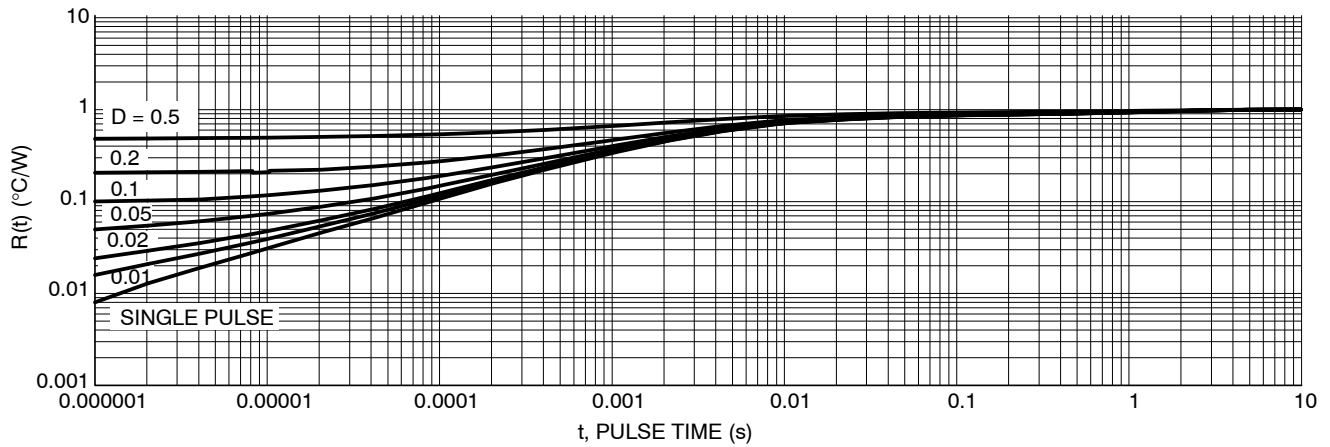


Figure 13. Thermal Response

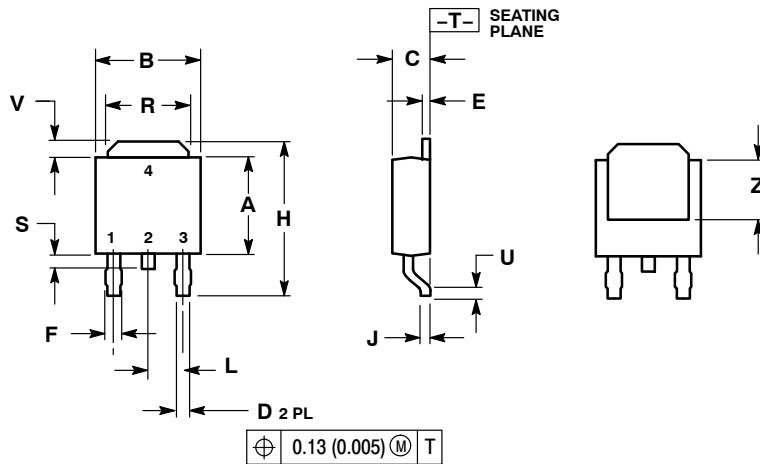
## ORDERING INFORMATION

Device	Package	Shipping†
NTD6414ANT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD6414AN-1G	IPAK (Pb-Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**DPAK**  
CASE 369AA-01  
ISSUE A



## NOTES:

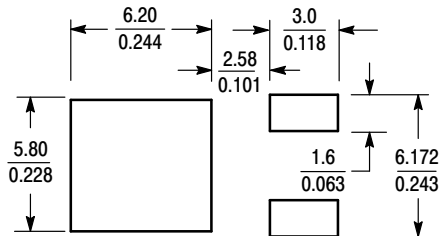
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

## STYLE 2:

- PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

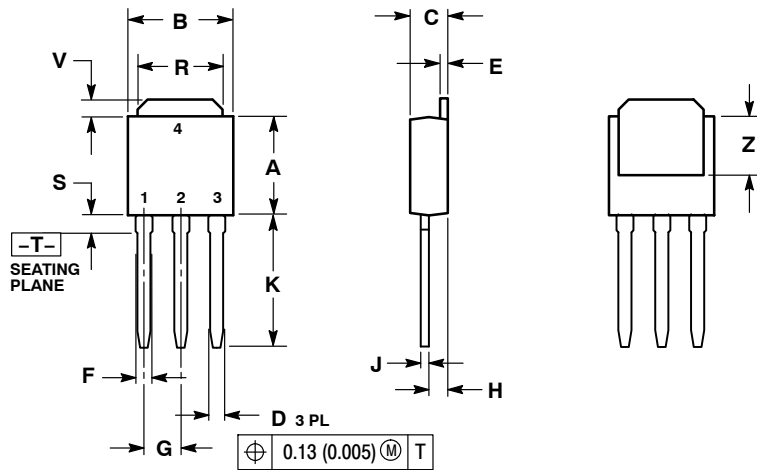
## SOLDERING FOOTPRINT\*



SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

DPAK  
CASE 369D-01  
ISSUE B


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

## STYLE 2:

- PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

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