



NOVATEK
聯詠科技

Data Sheet

NT7711

160 Output LCD Segment/Common Driver

V1.0

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Revision History

NT7711 Specification Revision History		
Version	Content	Date
1.0	Original	July. 2007

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Features

(Segment mode)

- Shift Clock frequency:
 - 20 MHz (Max.) (VDD = 5V±10%)
 - 12 MHz (Max.) (VDD = 2.5V~4.5V)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selected with a mode (MD) pin
- Automatic transfer function with an enable signal
- Automatic counting function which, in the chip select mode causes the internal clock to be stopped by automatically counting 160 bits of input data.

(Common mode)

- Shift clock frequency: 4.0MHz (Max.)
- Adjust AC signal generator (without any external component)
 - 2-line ~ 254 line inversion Single mode
 - 2-line ~ 126 line inversion Dual mode
 - Frame inversion Single and Dual mode
- Built-in 160-bit bi-directional shift register (divided into 80-bit x 2)
- Available in a single mode (160-bit shift register) or in a dual mode (80-bit shift register x 2)
 - Y1 → Y160 Single mode
 - Y160 → Y1 Single mode
 - Y1 → Y80, Y81 → Y160 Dual mode
 - Y160 → Y81, Y80 → Y1 Dual mode

The above 4 shift directions are pin-selectable

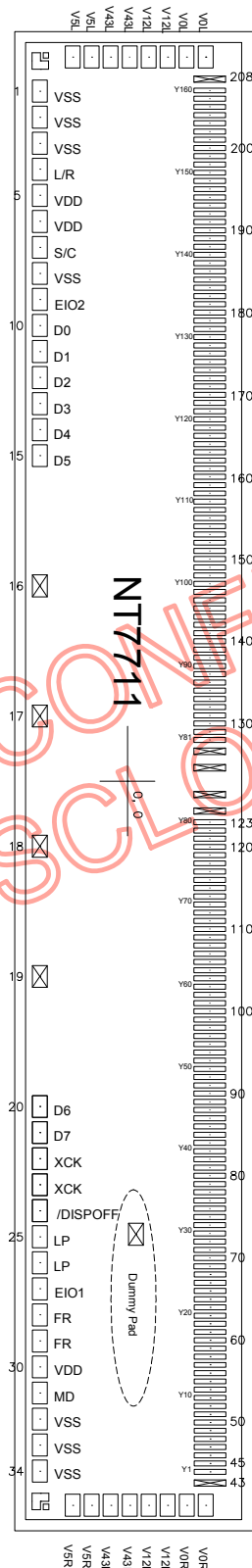
(Both segment mode and common mode)

- Supply voltage for LCD drive: 15.0 to 36.0V
- Number of LCD driver outputs: 160
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5V
- CMOS process
- Not designed or rated as radiation hardened

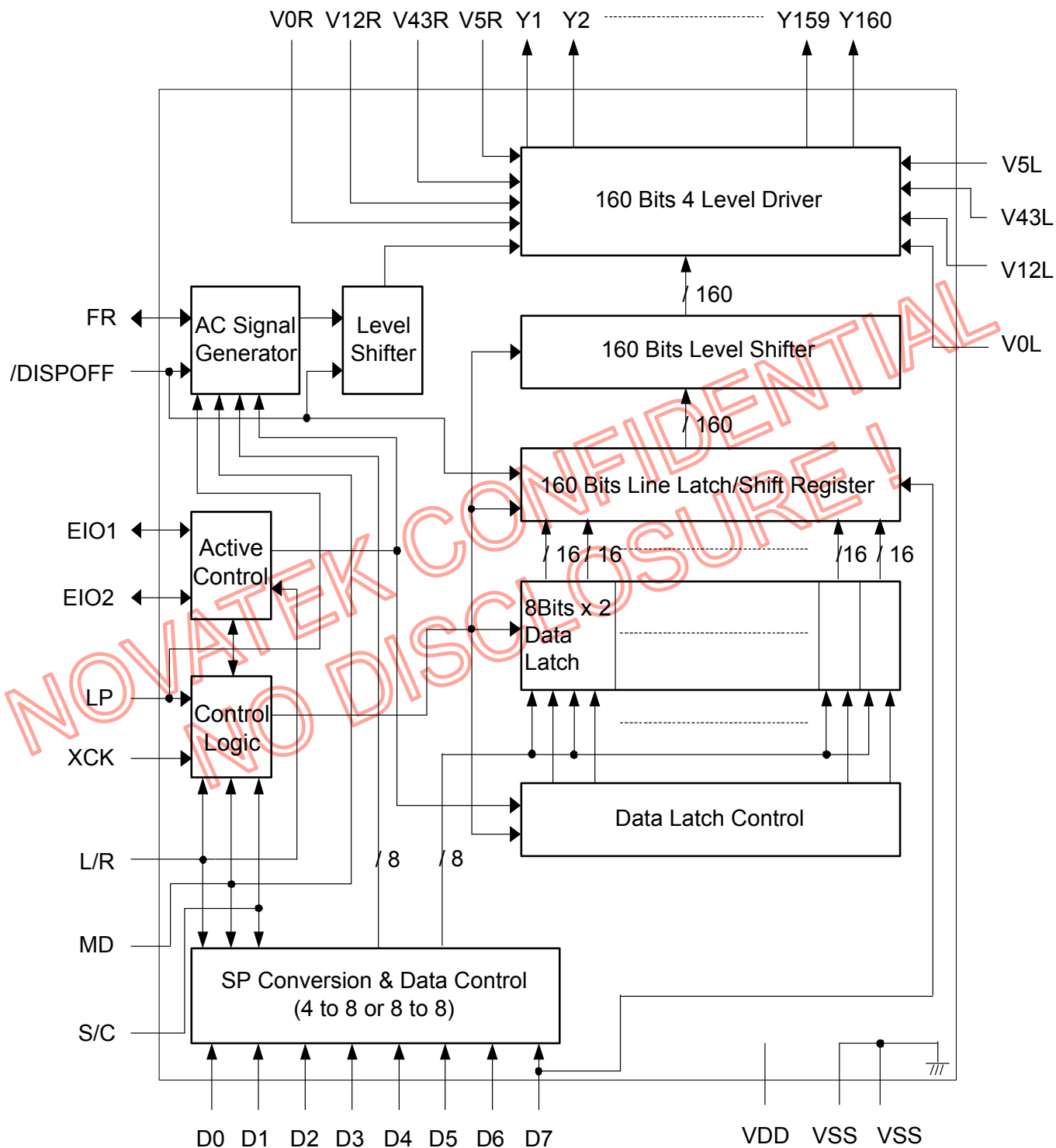
General Description

The NT7711 is a 160-bit output segment/common driver LSI suitable for driving the large-scale dot matrix LCD panels used by PDAs, personal computers and workstations. The NT7711 is good as both a segment driver and a common driver, and a low power consuming, high-precision LCD panel display can be assembled using the NT7711. In the segment mode, the data input is selected as a 4-bit parallel input mode or 8-bit parallel input mode by a mode (MD) pin. In common mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

Pad Configuration



Block Diagram



Pad Descriptions

Pad No.	Designation	I/O	Description
1~3	VSS	P	Ground (0V), these pads must be connected to each other.
4	L/R	I	Display data shift direction selection.
5~6	VDD	P	Power supply for the logic system (+2.5 to +5.5V).
7	S/C	I	Segment mode/common mode selection.
8	VSS	O	Ground output for pad option
9	EIO2	I/O	Input/output for chip selection or data of the shift register.
10~15,20	D0 ~ D6	I	Display data input for segment mode.
21	D7	I	Display data input for Segment mode/ Dual mode data input.
22~23	XCK	I	Display data shift clock input for segment mode.
24	/DISPOFF	I	Control input for deselect output level.
25~26	LP	I	Latch pulse input/shift clock input for the shift register.
27	EIO1	I/O	Input/output for chip select or data of the shift register.
28~29	FR	I/O	AC-converting signal input/output for LCD driver waveform.
30	VDD	O	Power supply output for pad option
31	MD	I	Mode selection input.
32~34	VSS	P	Ground (0V), these pads must be connected to each other.
35~36	V5R	I	Power supply for LCD driver.
37~38	V43R	P	Power supply for LCD driver.
39~40	V12R	P	Power supply for LCD driver.
41~42	V0R	P	Power supply for LCD driver.
44~123, 128~207	Y1 ~ Y160	O	LCD driver output.
209~210	V0L	P	Power supply for LCD driver.
211~212	V12L	P	Power supply for LCD driver.
213~214	V43L	P	Power supply for LCD driver.
215~216	V5L	P	Power supply for LCD driver.
16~19,43, 124~127,208	Dummy	x	Must be no connection.

Functional Descriptions

Block Description

Active Control

In the case of the segment mode, it controls the selection or deselection of the chip. Following an LP signal input, and after the select signal is input, a select signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.

In common mode, it controls the input/output data of bi-directional pins.

SP Conversion & Data Control

In segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

Data Latch Control

In the case of the segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

Data Latch

In the case of the segment mode, it latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch controlling 160 bits of data are read in 20 sets of 8 bits.

Line Latch / Shift Register

In the case of the segment mode, all 160 bits that have been read into the data latch are latched on to the falling edge of the LP signal and output to the level shift block simultaneously.

In the case of common mode, it shifts data from the data input pin on the falling edge of the LP signal.

Level Shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

4-Level Driver

It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V0, V12, V43, V5) based on the S/C, FR and /DISPOFF signals.

Control Logic

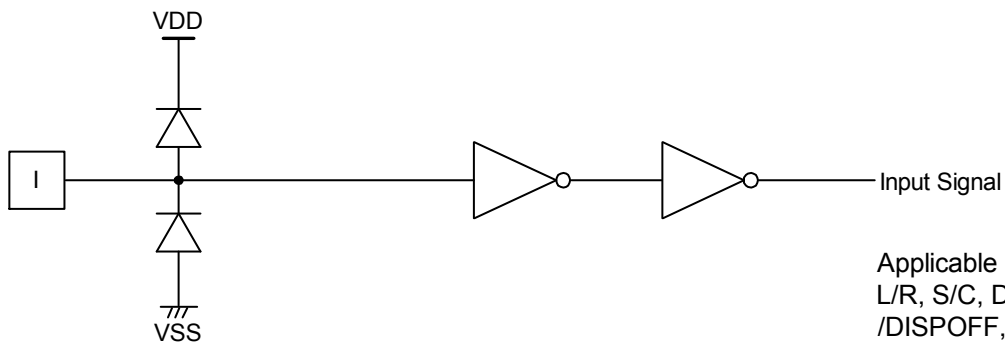
It controls the operation of each block. In the case of the segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected.

In common mode, it controls the direction of the data shift.

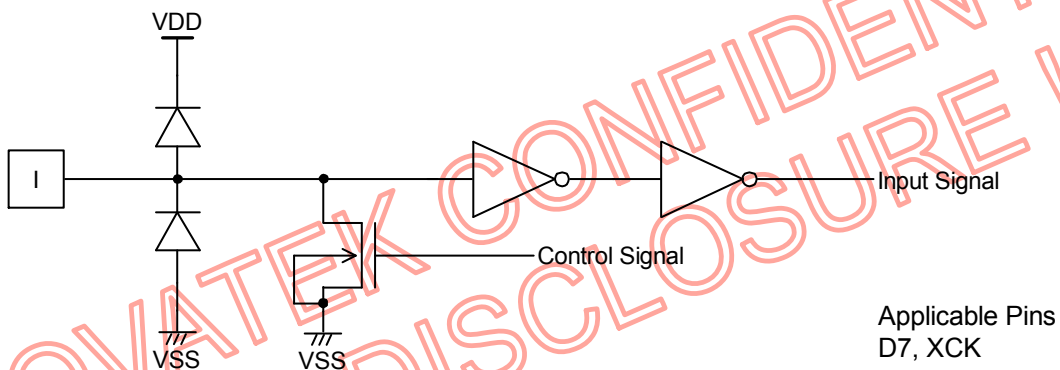
AC Signal Generator

In the case of the common mode, it consists of N-line inversions and frame inversion functions. The AC signal will be transferred to output at the rising edge or the falling edge base on XCK pin setting.

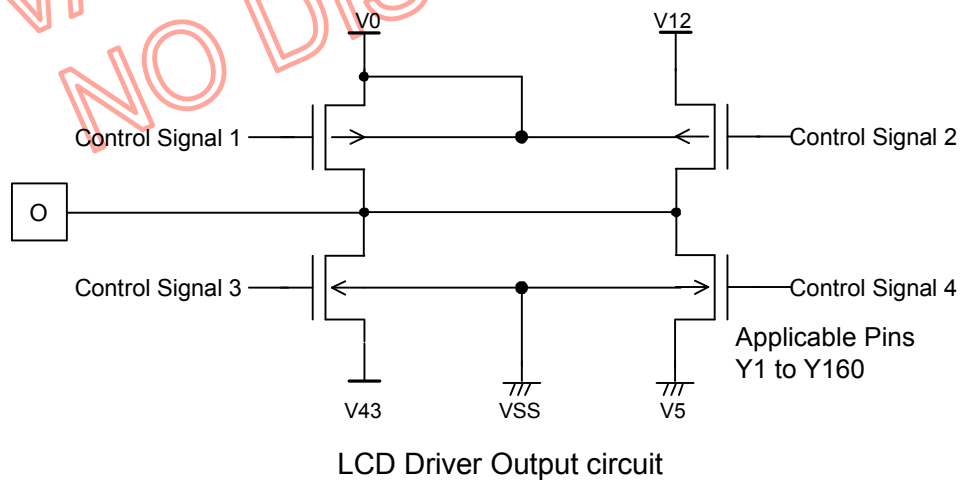
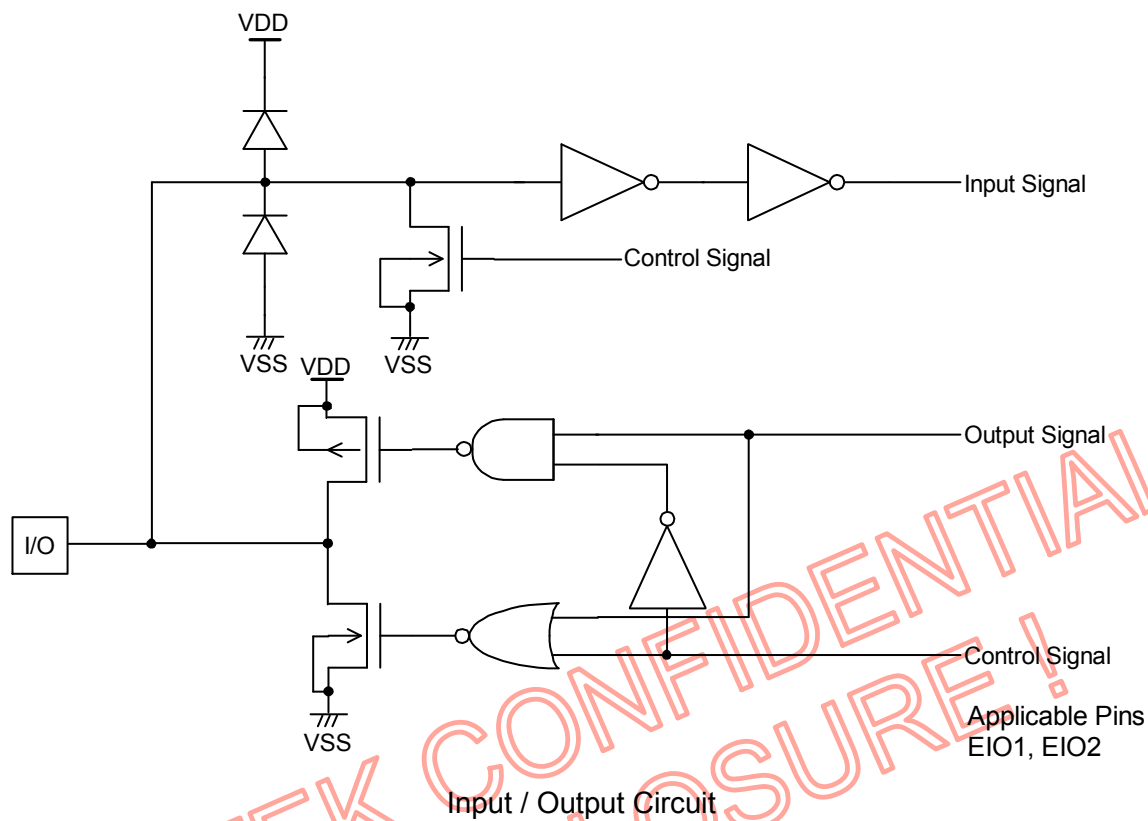
Input / Output Circuits



Input Circuit (1)



Input Circuit (2)



Pad Function
Segment mode

Symbol	Function
VDD	Logic system power supply pin connects to +2.5 to +5.5V.
VSS	Ground pin connects to 0V.
V0R, V0L V12R, V12L V43R, V43L V5R, V5L	Power supply pin for LCD driver voltage bias. <ul style="list-style-type: none"> • Normally, the bias voltage used is set by a resistor divider. • Ensure that the voltages are set such that $VSS \leq V5 < V43 < V12 < V0$. • To further reduce the differences between the output waveforms of the LCD driver output pins Y1 to Y160, externally connect ViR and ViL (i = 0, 12, 43, 5).
D0 ~ D7	Input pin for display data. <ul style="list-style-type: none"> • In 4-bit parallel input mode, input data into the 4 pins D0 ~ D3. Connect D4 ~ D7 to VSS or VDD. • In 8-bit parallel input mode, input data into the 8 pins D0 ~ D7.
XCK	Clock input pin for taking display data. <ul style="list-style-type: none"> • Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data. <ul style="list-style-type: none"> • Data is latched on the falling edge of the clock pulse.
L/R	Direction selection pin for reading display data. <ul style="list-style-type: none"> • When set to VSS level "L", data is read sequentially from Y160 to Y1. • When set to VDD level "H", data is read sequentially from Y1 to Y160.
/DISPOFF	Control input pin for output deselect level. <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD driver circuit. • When set to "L", the LCD driver output pins Y1 to Y160 are set to level V5. • While /DISPOFF is set to "L", the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs deselect level (V12 or V43), then outputs the contents of the data latch on to the next falling edge of the LP. At that time, if /DISPOFF removal time can not regulate what is shown AC characteristics, can not output the reading data correctly.
FR	AC signal input for LCD driving waveform. <ul style="list-style-type: none"> • The input signal is level-shifted from the logic voltage level to the driver voltage level, and controls the LCD driver circuit. • Normally inputs a frame inversion signal. <p>The LCD driver output pin's output voltage level can be set to the line latch output signal and the FR signal.</p>
MD	Mode selection pin. <ul style="list-style-type: none"> • When set to VSS level "L", 4-bit parallel input mode is set. • When set to VDD level "H", 8-bit parallel input mode is set.

Segment mode (continuous)

Symbol	Function
S/C	Segment mode / common mode selection pin. • When set to VDD level "H", segment mode is set. • When set to VSS level "L", common mode is set.
EIO1, EIO2	Input/output pin for chip selection. • When L/R input is at VSS level "L", EIO1 is set for output, and EIO2 is set for input. • When L/R input is at VDD level "H", EIO1 is set for input, and EIO2 is set for output. • During output, it is set to "H" while LP*(/XCK) is "H" and after 160-bits of data have been read, it is set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". • During input, after the LP signal is input, the chip is selected while EI is set to "L". After 160-bits of data have been read, the chip is deselected.
Y1 ~ Y160	LCD driver output pins • These correspond directly to each bit of the data latch, and one level (V0, V12, V43, or V5) is selected and the output.

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Common mode

Symbol	Function
VDD	Logic system power supply pin connects to +2.5 to +5.5V.
VSS	Ground pin connects to 0V.
V0R, V0L V12R, V12L V43R, V43L V5R, V5L	Power supply pin for LCD driver voltage bias. <ul style="list-style-type: none"> • Normally, the bias voltage used is set by a resistor divider. • Ensure that the voltages are set such that $VSS \leq V5 < V43 < V12 < V0$. • To further reduce the differences between the output waveforms of the LCD driver output pins Y1 to Y160, externally connect ViR and ViL (i = 0, 12, 43, 5).
EIO1	Bi-directional shift register shift data input/output pin. <ul style="list-style-type: none"> • Is an Output pin when L/R is at VSS level "L" and an input pin when L/R is at VDD level "H". • When EIO1 is used as an input pin, it will be pulled-down internally. • When EIO1 is used as an output pin, it won't be pulled-down internally.
EIO2	Bi-directional shift register shift data input/output pin. <ul style="list-style-type: none"> • Is an Input pin when L/R is at VSS level "L" and an output pin when L/R is at VDD level "H". • When EIO2 is used as an input pin, it will be pulled-down internally. • When EIO2 is used as an output pin, it won't be pulled-down internally.
LP	Bi-directional shift register shift clock pulse input pin. <ul style="list-style-type: none"> • Data is shifted on the falling edge of the clock pulse.
L/R	Bi-directional shift register shift direction selection pin. <ul style="list-style-type: none"> • Data is shifted from Y160 to Y1 when it is set to VSS level "L", and data is shifted from Y1 to Y160 when it is set to VDD level "H".
/DISPOFF	Control input pin for output deselect level. <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls the LCD driver circuit. • When set to "L", the LCD driver output pins Y1 to Y160 are set to level V5. • While /DISPOFF is set to "L", the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs deselect level (V12 or V43), then outputs the contents of the data latch onto the next falling edge of the LP. <p>At that time, if /DISPOFF removal time can not regulate what is shown AC characteristics, can not output the reading data correctly.</p>
FR	AC signal input for LCD driving waveform. <ul style="list-style-type: none"> • The input signal is level-shifted from the logic voltage level to the driver voltage level, and controls LCD driver circuit. • Normally inputs a frame inversion signal. <p>The LCD driver output pin's output voltage level can be set to the line latch output signal and the FR signal.</p> <ul style="list-style-type: none"> • When AC signal generator circuit is enabled, the AC signal will be output from this pin.
MD	Mode selection pin. <ul style="list-style-type: none"> • When set to VSS level "L", single mode operation is selected. When set to VDD level "H", dual mode operation is selected.

Common mode (continuous)

Symbol	Function
S/C	Segment mode / common mode selection pin. • When set to VSS level “L”, common mode is set.
D0 ~ D7	AC signal generator disable (Data bus D0~D7=00H or FFH) • When single mode is used, connect D0~D7 to VSS or VDD, to avoid floating. • When dual mode is used, D7 is dual mode data input pin, according to the data shift direction of the data shift register, data can be input starting from the 81 st bit. Connect D0~D6 to VSS or VDD, to avoid floating. AC signal generator enable (Data bus D0~D7=01H to FEH) • When single mode is used, use D0~D7 pins to set the N-Line inversion data. • When dual mode is used, use D0~D6 pins to set the N-Line inversion data.
XCK	AC signal generator disable (Data bus D0~D7=00H or FFH) • Connect XCK to VSS or VDD, to avoid floating. AC signal generator enable (Data bus D0~D7=01H to FEH) • XCK=“L”: AC signal output at LP rising edge. • XCK=“H”: AC signal output at LP falling edge.
Y1 ~ Y160	LCD driver output pins. • These correspond directly to each bit of the data latch, and one level (V0, V12, V43, or V5) is selected and the output.

LCD Driver Output Voltage Level

The relationship amongst the data bus signal, AC converted signal FR and LCD driver output voltage is shown in the table below:

Segment Mode

FR	Latch Data	/DISPOFF	Driver Output Voltage Level (Y1 ~ Y160)
L	L	H	V43
L	H	H	V5
H	L	H	V12
H	H	H	V0
X	X	L	V5

Here, $VSS \leq V5 < V43 < V12 < V0$, H: VDD (+2.5 to +5.5V), L: VSS (0V), X: Don't care

Common Mode

FR	Latch Data	/DISPOFF	Driver Output Voltage Level (Y1 ~ Y160)
L	L	H	V43
L	H	H	V0
H	L	H	V12
H	H	H	V5
X	X	L	V5

Here, $VSS \leq V5 < V43 < V12 < V0$, H: VDD (+2.5 to +5.5V), L: VSS (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage, which is assigned by specification for each power pin. At that time "Don't care" should be fixed to "H" or "L" to avoid floating.

Relationship between Display Data and Driver Output Pins

Segment Mode

(a) 4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					1 st	2 nd	3 rd	~	38 th	39 th	40 th
L	L	Output	Input	D0	Y157	Y153	Y149	~	Y9	Y5	Y1
				D1	Y158	Y154	Y150	~	Y10	Y6	Y2
				D2	Y159	Y155	Y151	~	Y11	Y7	Y3
				D3	Y160	Y156	Y152	~	Y12	Y8	Y4
L	H	Input	Output	D0	Y4	Y8	Y12	~	Y152	Y156	Y160
				D1	Y3	Y7	Y11	~	Y151	Y155	Y159
				D2	Y2	Y6	Y10	~	Y150	Y154	Y158
				D3	Y1	Y5	Y9	~	Y149	Y153	Y157

(b) 8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					1 st	2 nd	3 rd	~	18 th	19 th	20 th
H	L	Output	Input	D0	Y153	Y145	Y137	~	Y17	Y9	Y1
				D1	Y154	Y146	Y138	~	Y18	Y10	Y2
				D2	Y155	Y147	Y139	~	Y19	Y11	Y3
				D3	Y156	Y148	Y140	~	Y20	Y12	Y4
				D4	Y157	Y149	Y141	~	Y21	Y13	Y5
				D5	Y158	Y150	Y142	~	Y22	Y14	Y6
				D6	Y159	Y151	Y143	~	Y23	Y15	Y7
				D7	Y160	Y152	Y144	~	Y24	Y16	Y8
H	H	Input	Output	D0	Y8	Y16	Y24	~	Y144	Y152	Y160
				D1	Y7	Y15	Y23	~	Y143	Y151	Y159
				D2	Y6	Y14	Y22	~	Y142	Y150	Y158
				D3	Y5	Y13	Y21	~	Y141	Y149	Y157
				D4	Y4	Y12	Y20	~	Y140	Y148	Y156
				D5	Y3	Y11	Y19	~	Y139	Y147	Y155
				D6	Y2	Y10	Y18	~	Y138	Y146	Y154
				D7	Y1	Y9	Y17	~	Y137	Y145	Y153

Common Mode

MD	L/R	Data Transfer Direction	EIO1	EIO2	D7
L (Single)	L (shift to left)	Y160 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y160	Input	Output	X
H (Dual)	L (shift to left)	Y160 to Y81 Y80 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y80 Y81 to Y160	Input	Output	Input

Here, L: VSS (0V), H: VDD (+2.5V to +5.5V), X: Don't care

Note: "Don't care" should be fixed to "H" or "L" to avoid floating.

AC signal Generator Function

(a) Single Mode

FR	Data Input								LP ↑	LP ↓	Selected n-line inversion
	D7	D6	D5	D4	D3	D2	D1	D0	XCK	XCK	
Input	L	L	L	L	L	L	L	L	L	L	Disable
Output	L	L	L	L	L	L	L	H	L	H	Frame inversion
Output	L	L	L	L	L	L	H	L	L	H	2-line inversion
Output	L	L	L	L	L	L	H	H	L	H	3-line inversion
:	:	:	:	:	:	:	:	:	:	:	:
Output	H	H	H	H	H	H	L	H	L	H	253-line inversion
Output	H	H	H	H	H	H	H	L	L	H	254-line inversion
Input	H	H	H	H	H	H	H	H	L	L	Disable

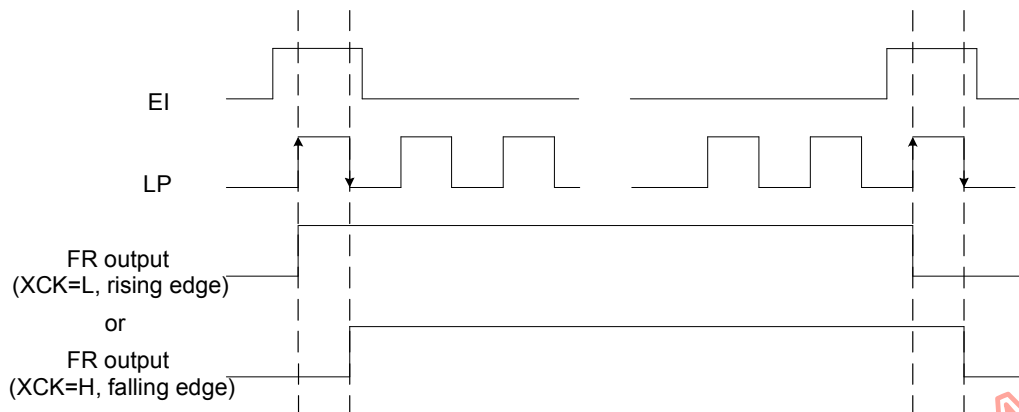
(b) Dual Mode

FR	Data Input								LP ↑	LP ↓	Selected n-line inversion
	D7	D6	D5	D4	D3	D2	D1	D0	XCK	XCK	
Input	*	L	L	L	L	L	L	L	L	L	Disable
Output	*	L	L	L	L	L	L	H	L	H	Frame inversion
Output	*	L	L	L	L	L	H	L	L	H	2-line inversion
Output	*	L	L	L	L	L	H	H	L	H	3-line inversion
:	:	:	:	:	:	:	:	:	:	:	:
Output	*	H	H	H	H	H	L	H	L	H	125-line inversion
Output	*	H	H	H	H	H	H	L	L	H	126-line inversion
Input	*	H	H	H	H	H	H	H	L	L	Disable

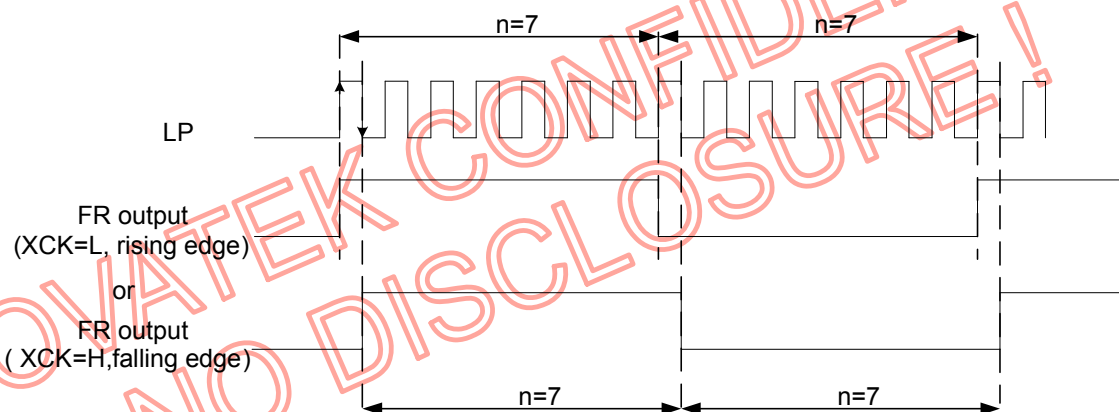
Note: "*" D7 is dual mode data input pin.

Timing waveform for AC signal generator

(a) Frame inversion (D0~D7=00000001b)

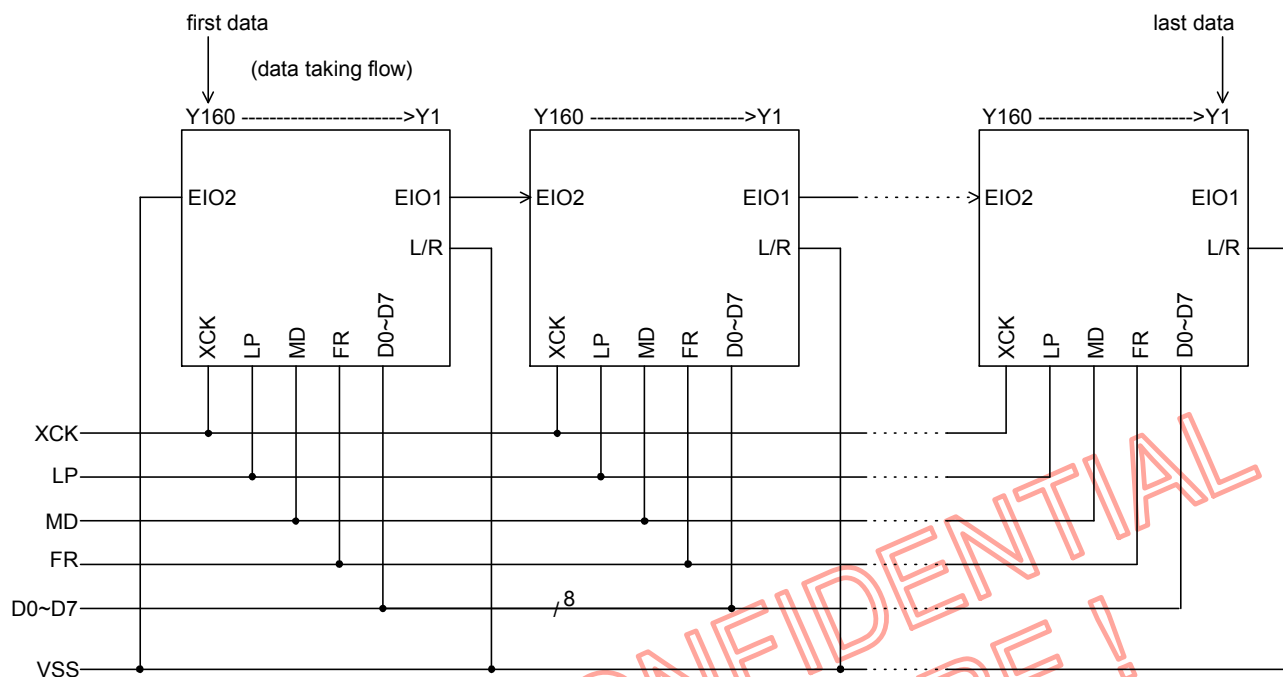


(b) n-line inversion (n=00000111b)

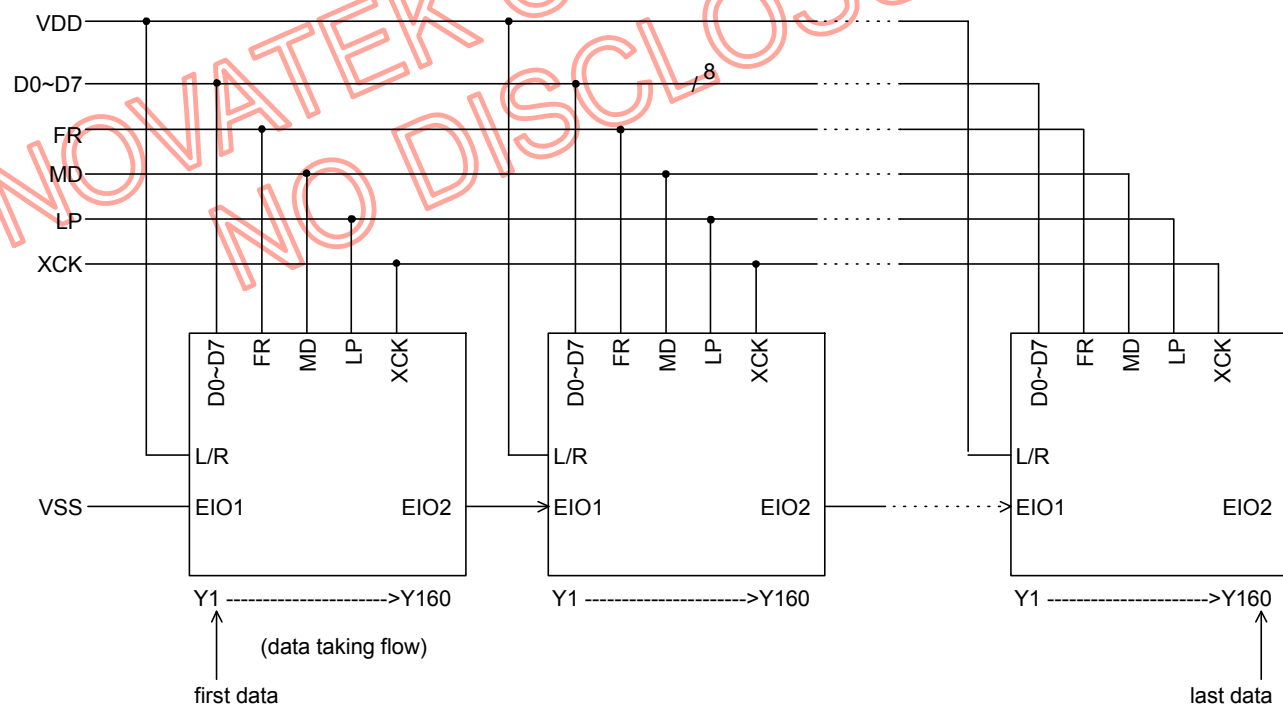


Connection Examples of Segment Drivers

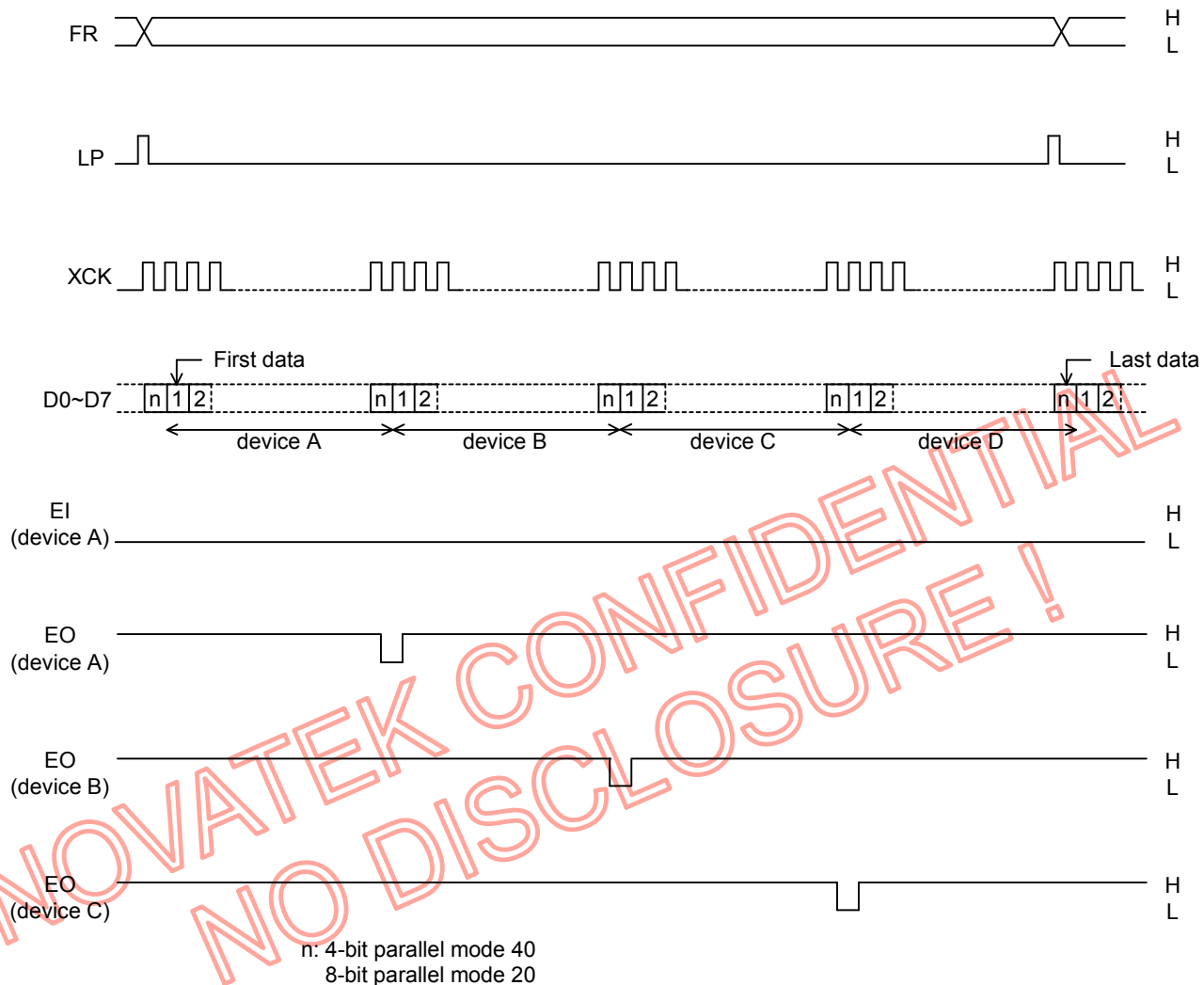
Case of L/R = "L"



Case of L/R = "H"

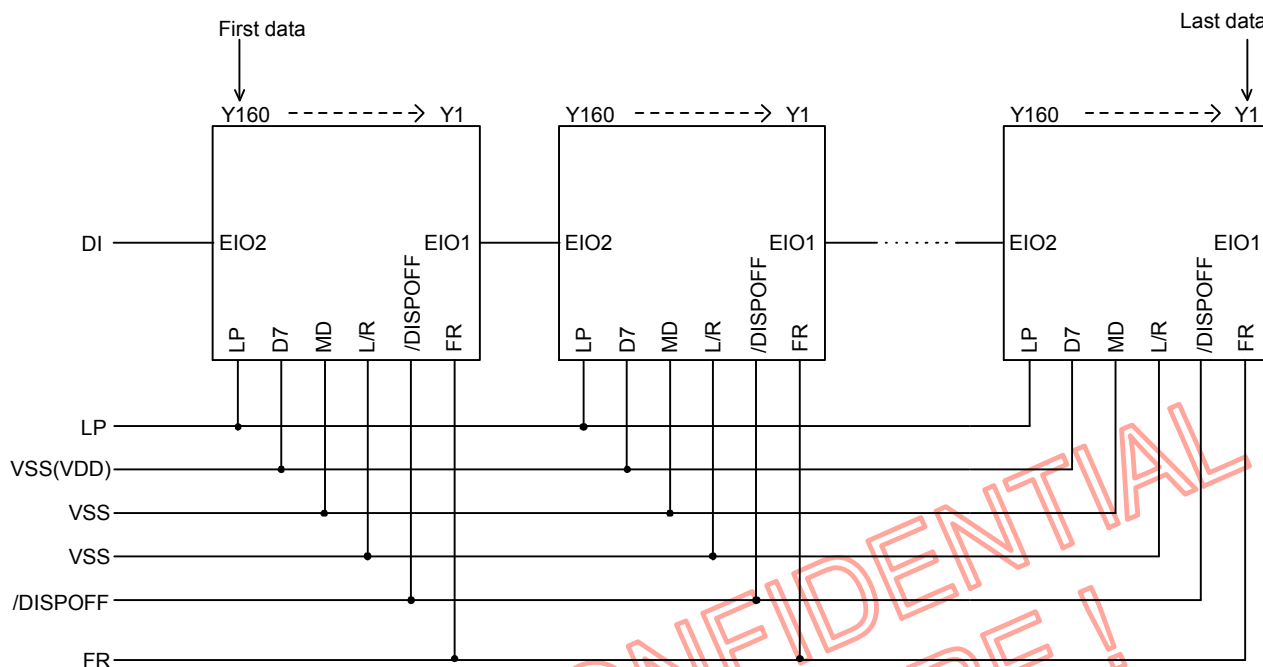


Timing Waveform of 4-Device Cascade Connection of Segment Drivers



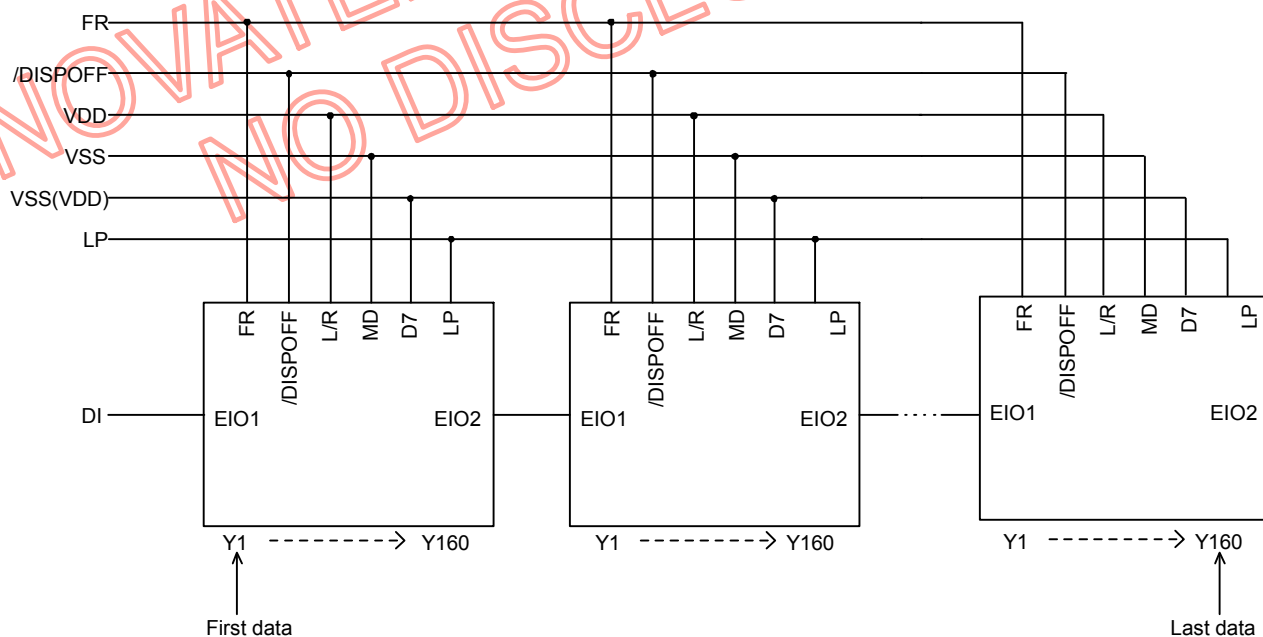
Connection Examples for Common Drivers

Case of L/R = "L"



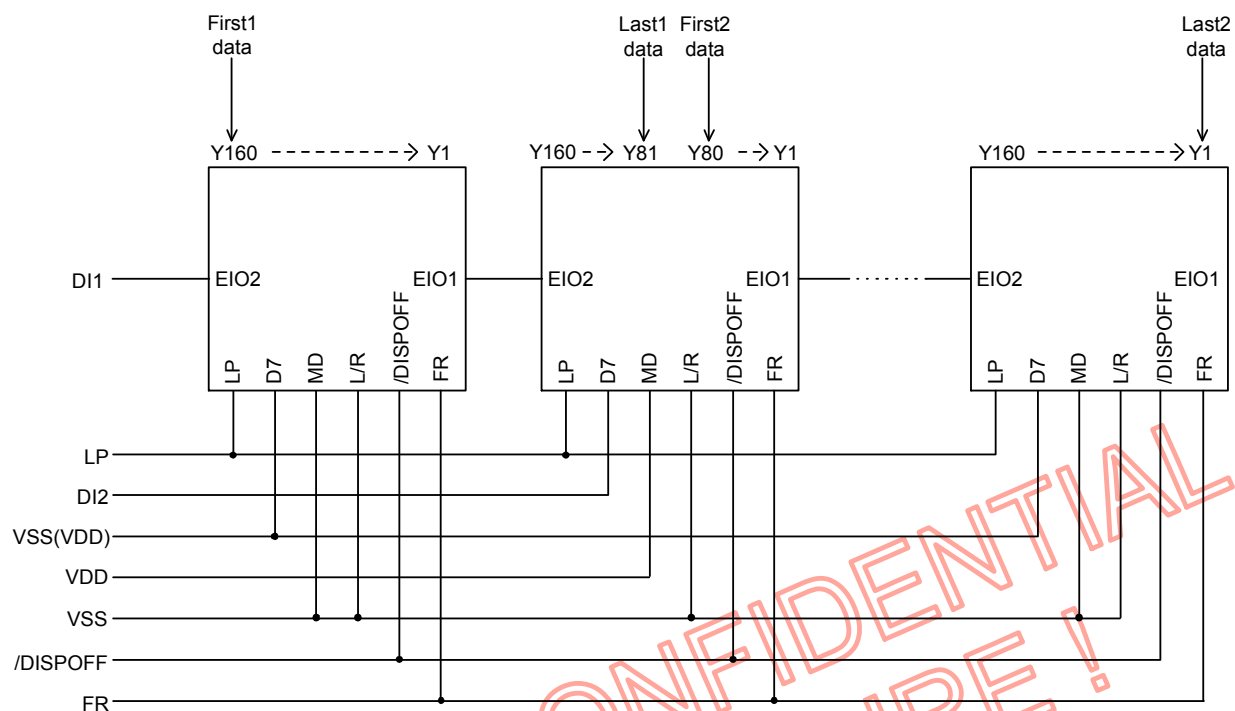
Single Mode (Shifting towards the left)

Case of L/R = "H"



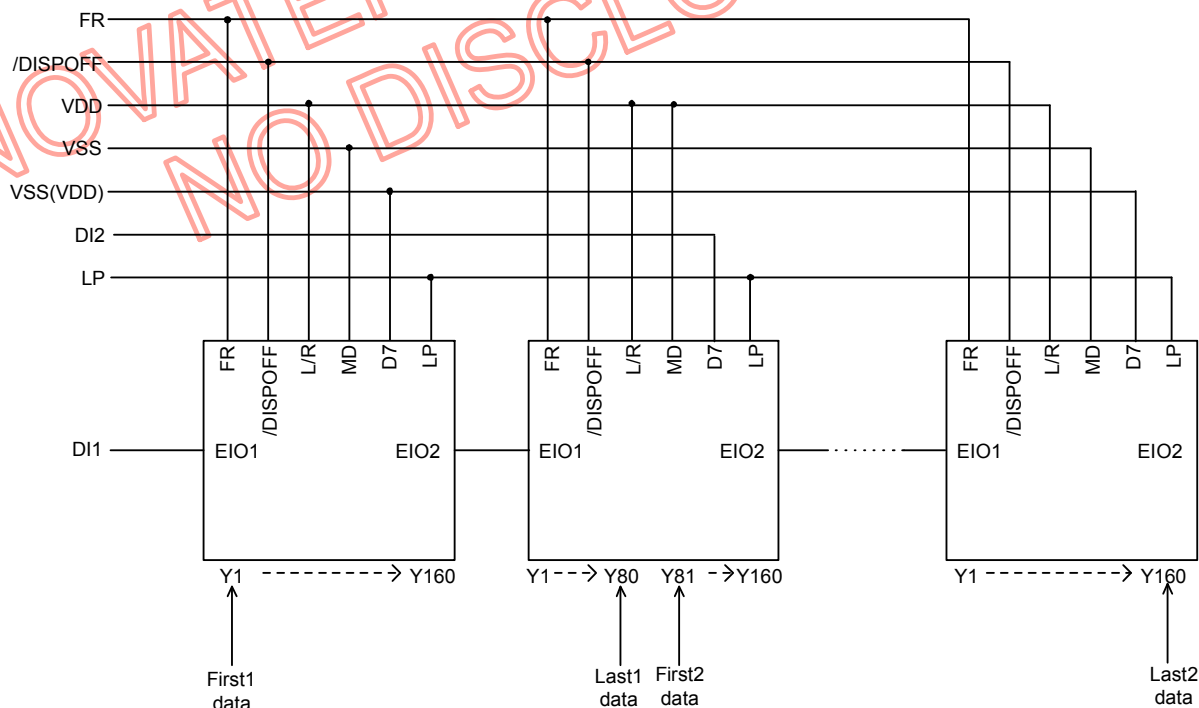
Single Mode (Shifting towards the right)

Case of L/R = "L"



Dual mode (Shifting towards the left)

Case of L/R = "H"



Dual mode (Shifting towards the right)

Precaution

Be careful when connecting or disconnecting the power.

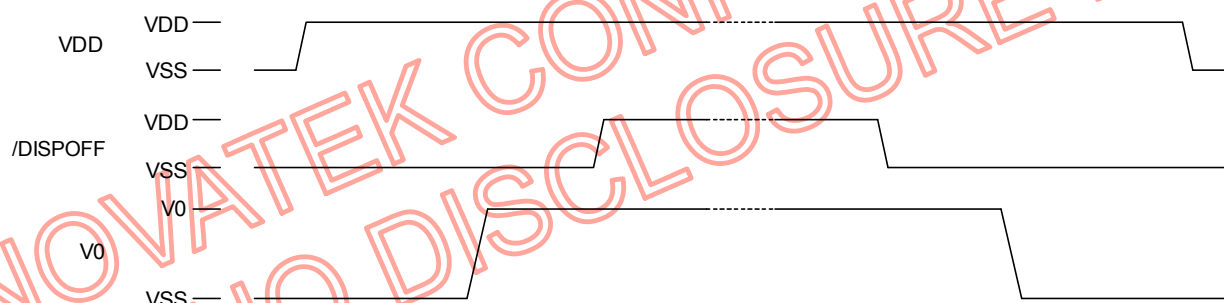
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur, if voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50 ~ 100 Ω) or fuse to the LCD driver power V0 of the system as a current limiting device. Also, set a suitable value for the resistor in consideration of the LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore connect the LCD driver power supply after resetting the logic condition of this LSI inside on DISPOFF function. After that, the /DISPOFF cancels the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level VSS on the /DISPOFF function. After that, disconnect the logic system power after disconnecting the LCD driver power.

When connecting the power supply, follow the recommended sequence shown here.



Absolute Maximum Rating

DC Supply Voltage VDD	-0.3V to 7.0V
DC Supply Voltage V0	-0.3V to +38.0V
Input Voltage (Vin)	-0.3V to VDD +0.3V
Operating Ambient Temperature	-30°C to +85°C
Storage Temperature	-45°C to +125°C

*Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics

Segment Mode (VSS=V5=0V, VDD=2.5~5.5V, V0=15~36V, Ta = -30 to +85°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.5	-	5.5	V	
V0	Operating Voltage	15	-	36	V	
VIH	Input high voltage	0.8 X VDD	-	-	V	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins
VIL	Input low voltage	-	-	0.2 X VDD	V	
VOH	Output high voltage	VDD - 0.4	-	-	V	EIO1, EIO2 pins, IOH = -0.4mA
VOL	Output low voltage	-	-	+0.4	V	EIO1, EIO2 pins, IOL = +0.4mA
I _{IH}	Input leakage current 1	-	-	+1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VDD
I _{IL}	Input leakage current 2	-	-	-1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VSS
RON	Output resistance	-	1.0	1.5	KΩ	V0 = +36V
		-	1.5	2.0	KΩ	V0 = +30V
ISB	Stand-by current	-	-	5.0	μA	VSS pin, Note 1
IDD1	Consumed current 1 (Non-selection)	-	-	0.5	mA	VDD pin, Note 2
IDD2	Consumed current 2 (Selection)	-	-	1.0	mA	VDD pin, Note 3
I0	Consumed current	-	-	0.5	mA	V0 pin, Note 4

Common Mode (VSS=V5=0V, VDD=2.5~5.5V, V0=15~36V, Ta = -30 to +85°C, unless otherwise noted)

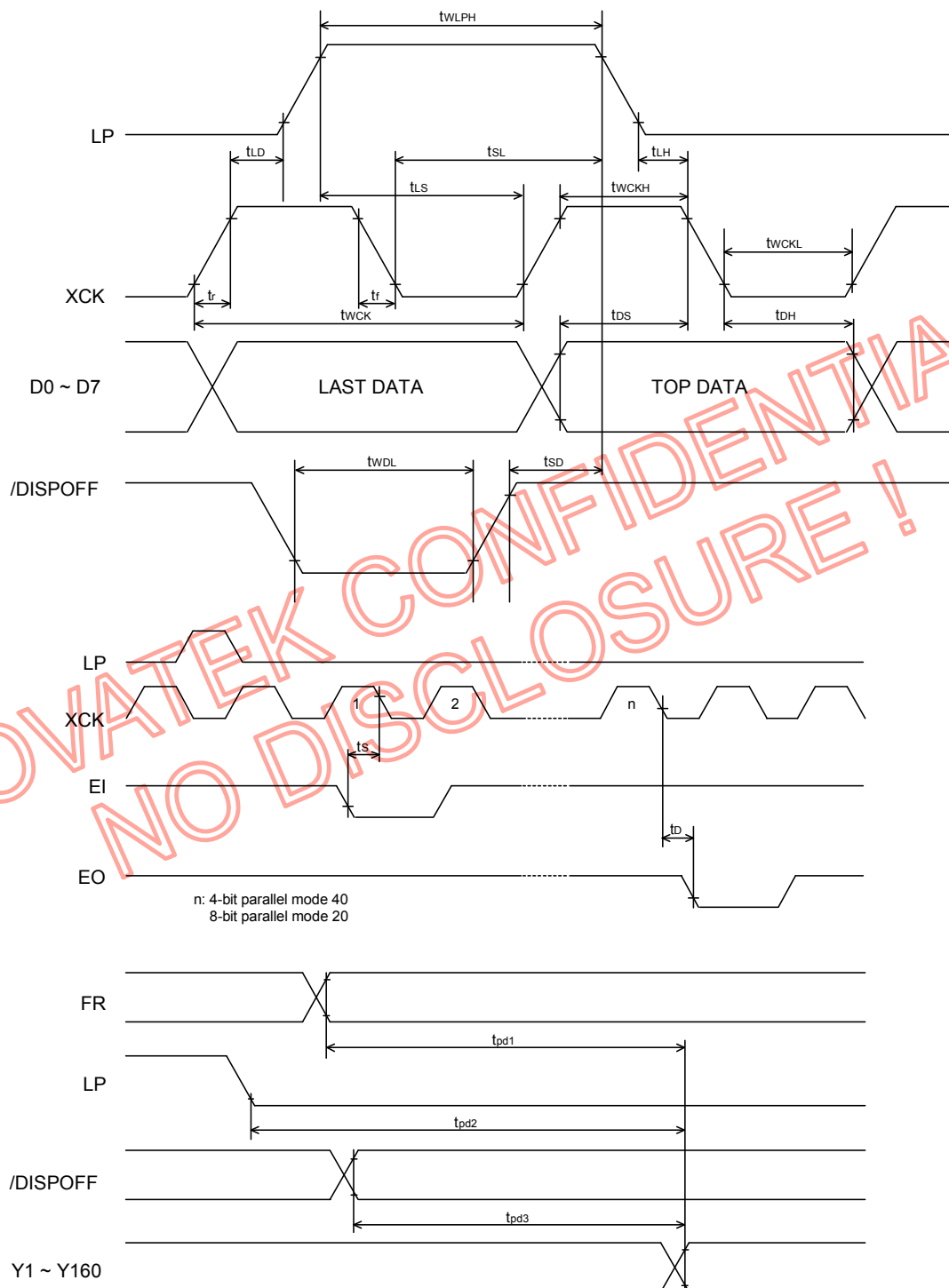
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.5	-	5.5	V	
V0	Operating Voltage	15	-	36	V	
VIH	Input high voltage	0.8 X VDD	-	-	V	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins
VIL	Input low voltage	-	-	0.2 X VDD	V	
VOH	Output high voltage	VDD - 0.4	-	-	V	EIO1, EIO2, FR pins, IOH = -0.4mA
VOL	Output low voltage	-	-	+0.4	V	EIO1, EIO2, FR pins, IOL = +0.4mA
IIH	Input leakage current 1	-	-	+1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VDD
IIL	Input leakage current 2	-	-	-1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VSS
IPD	Input pull down current	-	-	100	μA	EIO1, EIO2, D7 pins
RON	Output resistance	-	1.0	1.5	KΩ	V0 = +36V
		-	1.5	2.0	KΩ	V0 = +30V
ISB	Stand-by current	-	-	5	μA	VSS pin, Note 5
IDD	Consumed current 1	-	-	80	μA	VDD pin, Note 6
I0	Consumed current 2	-	-	160	μA	V0 pin, Note 6

Notes:

1. VDD = +5.0V, V0 = +36V, Vin = VSS
2. VDD = +5.0V, V0 = +36V, fXCK = 20MHz, No-load, EIO = VDD
The input data is turned over by data taking clock (4-bit parallel input mode)
3. VDD = +5.0V, V0 = +36V, fXCK = 20MHz, No-load. EIO = VSS
The input data is turned over by data taking clock (4-bit parallel input mode)
4. VDD = +5.0V, V0 = +36V, fXCK = 20MHz, fLP = 41.6kHz. fFR = 80Hz, No-load
The input data is turned over by data taking clock (4-bit parallel-input mode)
5. VDD = +5.0V, V0 = +36V, Vin = VSS
6. VDD = +5.0V, V0 = +36V, fLP = 41.6KHz, fFR = 80Hz, in case of 1/480 duty operation, no-load

AC Characteristics

1. Timing Characteristics of Segment Mode



Segment Mode 1 (VSS=V5=0V, VDD=4.5~5.5V, V0=15~36V, Ta = -30~+85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t _{wck}	50	-		ns	tr, tf ≤ 10ns, Note 1
Shift clock "H" pulse width	t _{wckH}	15	-		ns	
Shift clock "L" pulse width	t _{wckL}	15	-		ns	
Data setup time	t _{DS}	10	-		ns	
Data hold time	t _{DH}	12	-		ns	
Latch pulse "H" pulse width	t _{wLPH}	15	-		ns	
Shift clock rise to Latch pulse rise time	t _{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t _{SL}	30	-		ns	
Latch pulse rise to Shift clock rise time	t _{LS}	25	-		ns	
Latch pulse fall to Shift clock fall time	t _{LH}	25	-		ns	
Input signal rise time	t _r		-	50	ns	Note 2
Input signal fall time	t _f		-	50	ns	Note 2
Enable setup time	t _s	20	-		ns	
/DISPOFF Removal time	t _{SD}	100	-		ns	
/DISPOFF enable pulse width	t _{wDL}	1.2	-		μs	
Output delay time (1)	t _D		-	30	ns	CL=15pF
Output delay time (2)	t _{pd1} , t _{pd2}		-	1.2	μs	CL=15pF
Output delay time (3)	t _{pd3}		-	1.2	μs	CL=15pF

Note

1. Take the cascade connection into consideration.
2. (t_{wck} - t_{wckH} - t_{wckL})/2 is the maximum in the case of high speed operation.

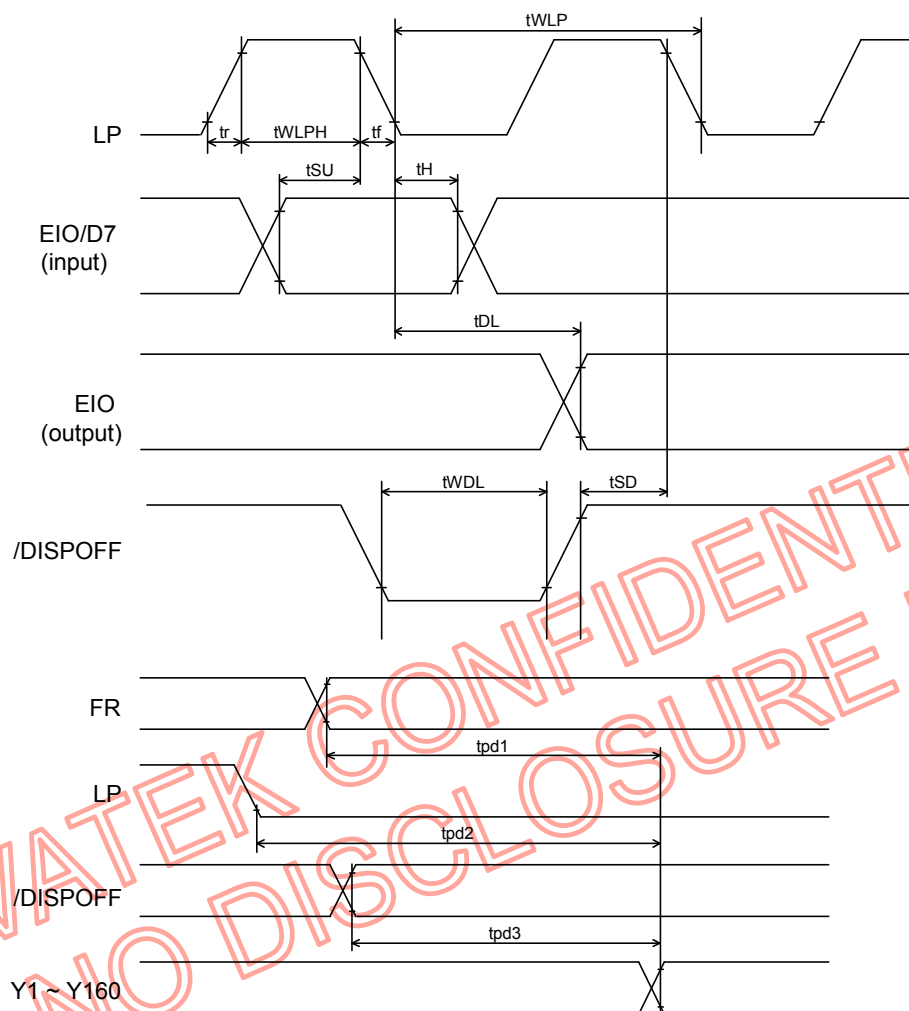
Segment Mode 2 (VSS=V5=0V, VDD=2.5~4.5V, V0=15~36V, Ta = -30~+85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{wck}	82	-		ns	$t_r, t_f \leq 10\text{ns}$, Note 1
Shift clock "H" pulse width	t_{wckH}	28	-		ns	
Shift clock "L" pulse width	t_{wckL}	28	-		ns	
Data setup time	t_{DS}	20	-		ns	
Data hold time	t_{DH}	23	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	30	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	65	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	30	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	35	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_s	30	-		ns	
/DISPOFF Removal time	t_{SD}	100	-		ns	
/DISPOFF enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	57	ns	CL=15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL=15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL=15pF

Note

1. Take the cascade connection into consideration.
2. $(t_{wck} - t_{wckH} - t_{wckL})/2$ is the maximum in the case of high speed operation.

2. Timing Characteristics of Common Mode



Common Mode (VSS=V5=0V, VDD=2.5~5.5V, V0=15~36V, Ta=-30~+85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t _{WLP}	250	-	-	ns	t _r , t _f ≤ 20ns
Shift clock "H" pulse width	t _{WLPH}	15	-	-	ns	VDD=5.0V±10%
		30	-	-	ns	VDD=2.5~4.5V
Data setup time	t _{su}	30	-	-	ns	
Data hold time	t _h	50	-	-	ns	
Input signal rise time	t _r		-	50	ns	
Input signal fall time	t _f		-	50	ns	
/DISPOFF Removal time	t _{SD}	100	-	-	ns	
/DISPOFF enable pulse width	t _{WDL}	1.2	-	-	μs	
Output delay time (1)	t _{DL}	-	-	200	ns	CL=15pF
Output delay time (2)	t _{pd1} , t _{pd2}	-	-	1.2	μs	CL=15pF
Output delay time (3)	t _{pd3}	-	-	1.2	μs	CL=15pF

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Application & ITO Layout Notice (for reference only)

Application Notices

1. To adjust the voltage of V1 and V4 you can amend the phenomena of “cross talk” (V1& V4 range of adjustment is less than 100mV, be sure V0-V1=V4-VSS after adjusting).
2. Add 0.1μf high frequency capacitors between VDD & V0 ~ V4 and VSS.
3. When OP (LP324) is used as following bias voltage, ensure OP power voltage must be 1.5V (or more) higher than output voltage.
4. XCK, D0~D7, LP are high frequency (Max. 20MHz) signals: pay attention to the distance between them and other signals nearby to avoid high frequency interference.
5. EIO1, EIO2 are enable signals for connecting chips: pay attention to the distance between them and other signals nearby to avoid interference. The distance of connection between two chips is the shorter the better.

ITO Layout Notice (It is for application of COG type)

1. We suggest that the LCD panel is made of glass whose ITO resistor is under 15Ω/square. ITO will be better if it is straight. Its resistor value is the smaller the better.
2. Among interface Pins, first ensure ITO resistor values of VDD, VSS and V0 ~ V4 are less than values we suggest as shown below:

- ITO resistance value of power pins.

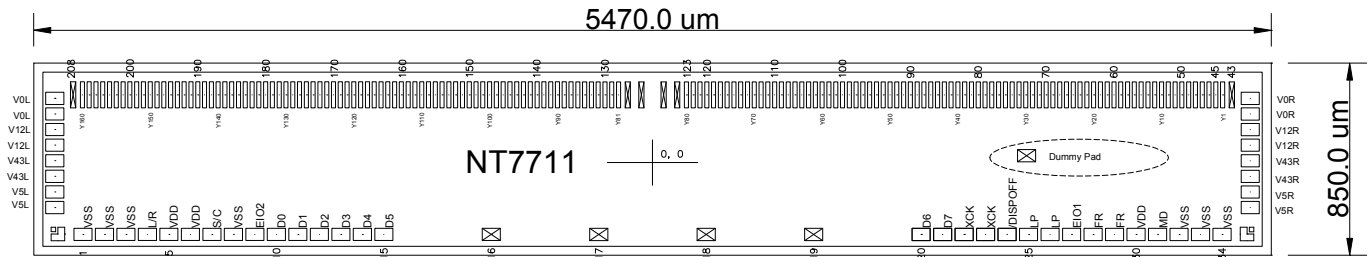
ITO path	Max. Resistance (Ω)	
	VDD < 2.7V	VDD ≥ 2.7V
VDD	75	130
VSS	75	130
V0L(R)	200	
V12L(R)		
V43L(R)		
V5L(R)		

- ITO resistance value of digital pins.

ITO path	Max. Resistance (Ω)
XCK, D0~D7, LP	500
EIO1, EIO2, FR, L/R, S/C, MD, /DISPOFF	1K

3. Single VSS and V0, V12, V43, V5 R/L are connected to FPC by ITO separately. At last shorten the distance of ITO by using metal on PCB.
4. VDD/VSS of IC and VDD/VSS of FPC are at the same vertical level as far as possible. ITO can be straight.
5. The distance of connection between IC to FPC is the shorter the better.

Bonding Diagram



Pad Location

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	VSS	-2517.5	-333.0	33	VSS	2422.5	-333.0
2	VSS	-2422.5	-333.0	34	VSS	2517.5	-333.0
3	VSS	-2327.5	-333.0	35	V5R	2642.0	-214.0
4	L/R	-2232.5	-333.0	36	V5R	2642.0	-145.0
5	VDD	-2137.5	-333.0	37	V43R	2642.0	-76.0
6	VDD	-2042.5	-333.0	38	V43R	2642.0	-7.0
7	S/C	-1947.5	-333.0	39	V12R	2642.0	62.0
8	VSS	-1852.5	-333.0	40	V12R	2642.0	131.0
9	EIO2	-1757.5	-333.0	41	V0R	2642.0	200.0
10	D0	-1662.5	-333.0	42	V0R	2642.0	269.0
11	D1	-1567.5	-333.0	43	DUMMY	2561.0	284.5
12	D2	-1472.5	-333.0	44	Y1	2520.0	284.5
13	D3	-1377.5	-333.0	45	Y2	2490.0	284.5
14	D4	-1282.5	-333.0	46	Y3	2460.0	284.5
15	D5	-1187.5	-333.0	47	Y4	2430.0	284.5
16	DUMMY	-712.5	-333.0	48	Y5	2400.0	284.5
17	DUMMY	-237.5	-333.0	49	Y6	2370.0	284.5
18	DUMMY	237.5	-333.0	50	Y7	2340.0	284.5
19	DUMMY	712.5	-333.0	51	Y8	2310.0	284.5
20	D6	1187.5	-333.0	52	Y9	2280.0	284.5
21	D7	1282.5	-333.0	53	Y10	2250.0	284.5
22	XCK	1377.5	-333.0	54	Y11	2220.0	284.5
23	XCK	1472.5	-333.0	55	Y12	2190.0	284.5
24	/DISPOFF	1567.5	-333.0	56	Y13	2160.0	284.5
25	LP	1662.5	-333.0	57	Y14	2130.0	284.5
26	LP	1757.5	-333.0	58	Y15	2100.0	284.5
27	EIO1	1852.5	-333.0	59	Y16	2070.0	284.5
28	FR	1947.5	-333.0	60	Y17	2040.0	284.5
29	FR	2042.5	-333.0	61	Y18	2010.0	284.5
30	VDD	2137.5	-333.0	62	Y19	1980.0	284.5
31	MD	2232.5	-333.0	63	Y20	1950.0	284.5
32	VSS	2327.5	-333.0	64	Y21	1920.0	284.5

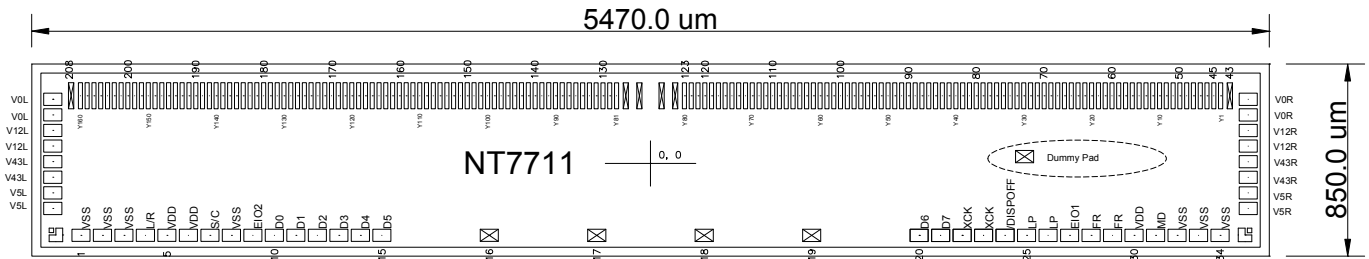
Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
65	Y22	1890.0	284.5	107	Y64	630.0	284.5
66	Y23	1860.0	284.5	108	Y65	600.0	284.5
67	Y24	1830.0	284.5	109	Y66	570.0	284.5
68	Y25	1800.0	284.5	110	Y67	540.0	284.5
69	Y26	1770.0	284.5	111	Y68	510.0	284.5
70	Y27	1740.0	284.5	112	Y69	480.0	284.5
71	Y28	1710.0	284.5	113	Y70	450.0	284.5
72	Y29	1680.0	284.5	114	Y71	420.0	284.5
73	Y30	1650.0	284.5	115	Y72	390.0	284.5
74	Y31	1620.0	284.5	116	Y73	360.0	284.5
75	Y32	1590.0	284.5	117	Y74	330.0	284.5
76	Y33	1560.0	284.5	118	Y75	300.0	284.5
77	Y34	1530.0	284.5	119	Y76	270.0	284.5
78	Y35	1500.0	284.5	120	Y77	240.0	284.5
79	Y36	1470.0	284.5	121	Y78	210.0	284.5
80	Y37	1440.0	284.5	122	Y79	180.0	284.5
81	Y38	1410.0	284.5	123	Y80	150.0	284.5
82	Y39	1380.0	284.5	124	DUMMY	109.0	284.5
83	Y40	1350.0	284.5	125	DUMMY	49.0	284.5
84	Y41	1320.0	284.5	126	DUMMY	-49.0	284.5
85	Y42	1290.0	284.5	127	DUMMY	-109.0	284.5
86	Y43	1260.0	284.5	128	Y81	-150.0	284.5
87	Y44	1230.0	284.5	129	Y82	-180.0	284.5
88	Y45	1200.0	284.5	130	Y83	-210.0	284.5
89	Y46	1170.0	284.5	131	Y84	-240.0	284.5
90	Y47	1140.0	284.5	132	Y85	-270.0	284.5
91	Y48	1110.0	284.5	133	Y86	-300.0	284.5
92	Y49	1080.0	284.5	134	Y87	-330.0	284.5
93	Y50	1050.0	284.5	135	Y88	-360.0	284.5
94	Y51	1020.0	284.5	136	Y89	-390.0	284.5
95	Y52	990.0	284.5	137	Y90	-420.0	284.5
96	Y53	960.0	284.5	138	Y91	-450.0	284.5
97	Y54	930.0	284.5	139	Y92	-480.0	284.5
98	Y55	900.0	284.5	140	Y93	-510.0	284.5
99	Y56	870.0	284.5	141	Y94	-540.0	284.5
100	Y57	840.0	284.5	142	Y95	-570.0	284.5
101	Y58	810.0	284.5	143	Y96	-600.0	284.5
102	Y59	780.0	284.5	144	Y97	-630.0	284.5
103	Y60	750.0	284.5	145	Y98	-660.0	284.5
104	Y61	720.0	284.5	146	Y99	-690.0	284.5
105	Y62	690.0	284.5	147	Y100	-720.0	284.5
106	Y63	660.0	284.5	148	Y101	-750.0	284.5

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
149	Y102	-780.0	284.5	184	Y137	-1830.0	284.5
150	Y103	-810.0	284.5	185	Y138	-1860.0	284.5
151	Y104	-840.0	284.5	186	Y139	-1890.0	284.5
152	Y105	-870.0	284.5	187	Y140	-1920.0	284.5
153	Y106	-900.0	284.5	188	Y141	-1950.0	284.5
154	Y107	-930.0	284.5	189	Y142	-1980.0	284.5
155	Y108	-960.0	284.5	190	Y143	-2010.0	284.5
156	Y109	-990.0	284.5	191	Y144	-2040.0	284.5
157	Y110	-1020.0	284.5	192	Y145	-2070.0	284.5
158	Y111	-1050.0	284.5	193	Y146	-2100.0	284.5
159	Y112	-1080.0	284.5	194	Y147	-2130.0	284.5
160	Y113	-1110.0	284.5	195	Y148	-2160.0	284.5
161	Y114	-1140.0	284.5	196	Y149	-2190.0	284.5
162	Y115	-1170.0	284.5	197	Y150	-2220.0	284.5
163	Y116	-1200.0	284.5	198	Y151	-2250.0	284.5
164	Y117	-1230.0	284.5	199	Y152	-2280.0	284.5
165	Y118	-1260.0	284.5	200	Y153	-2310.0	284.5
166	Y119	-1290.0	284.5	201	Y154	-2340.0	284.5
167	Y120	-1320.0	284.5	202	Y155	-2370.0	284.5
168	Y121	-1350.0	284.5	203	Y156	-2400.0	284.5
169	Y122	-1380.0	284.5	204	Y157	-2430.0	284.5
170	Y123	-1410.0	284.5	205	Y158	-2460.0	284.5
171	Y124	-1440.0	284.5	206	Y159	-2490.0	284.5
172	Y125	-1470.0	284.5	207	Y160	-2520.0	284.5
173	Y126	-1500.0	284.5	208	DUMMY	-2561.0	284.5
174	Y127	-1530.0	284.5	209	V0L	-2642.0	269.0
175	Y128	-1560.0	284.5	210	V0L	-2642.0	200.0
176	Y129	-1590.0	284.5	211	V12L	-2642.0	131.0
177	Y130	-1620.0	284.5	212	V12L	-2642.0	62.0
178	Y131	-1650.0	284.5	213	V43L	-2642.0	-7.0
179	Y132	-1680.0	284.5	214	V43L	-2642.0	-76.0
180	Y133	-1710.0	284.5	215	V5L	-2642.0	-145.0
181	Y134	-1740.0	284.5	216	V5L	-2642.0	-214.0
182	Y135	-1770.0	284.5		ALK_L	-2628.0	-331.0
183	Y136	-1800.0	284.5		ALK_R	2628.0	-331.0

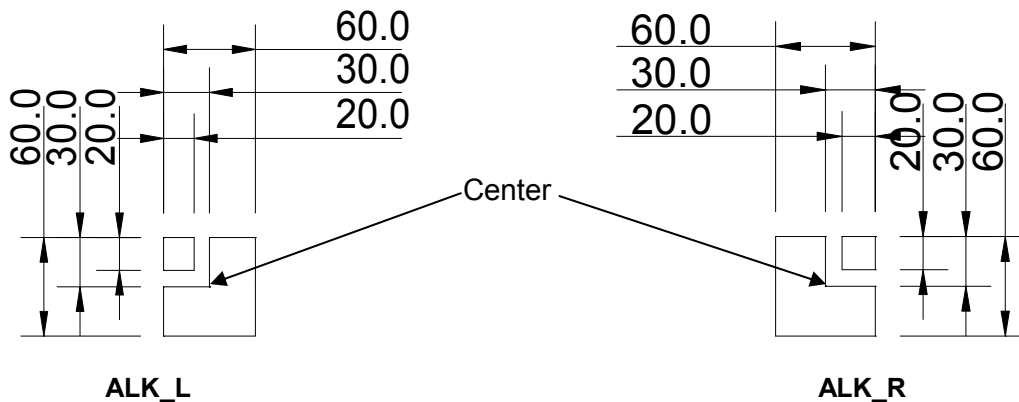
Package Information



Pad Dimensions

	Pad No.	Size		UNIT
		X	Y	
Chip size	-	5470	850	μm
Chip thickness	-	525		μm
Pad pitch	1~15, 20~34	95	-	μm
	15~20	475	-	
	35~42, 209~216	-	69	
	44~123, 128~207	30	-	
	43~44, 123~124, 127~128, 207~208	41	-	
	124~125, 126~127	60	-	
	125~126	98	-	
Bump size	1~42, 209~216	80	54	μm
	44~123, 128~207	18	115	
	43, 124~127, 208	23	115	
Bump height	All pads	15 ± 3		μm

Alignment Marks: (Unit: μm)



Ordering Information

Part No.	Package
NT7711H-D/3N	Gold bump on chip tray

Cautions

1. The contents of this document are subject to change without notice.
2. Precautions against light projection:
Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.
Observe the following instructions when using this product:
 - a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
 - b. Test and inspect the product under an environment free of light source penetration.
 - c. Confirm that all surfaces around the IC will not be exposed to a light source.

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