NT56V1680A0T
NT56V1640A0T

Data Sheet

8012-90010

Changes may be made without notice

DESCRIPTION

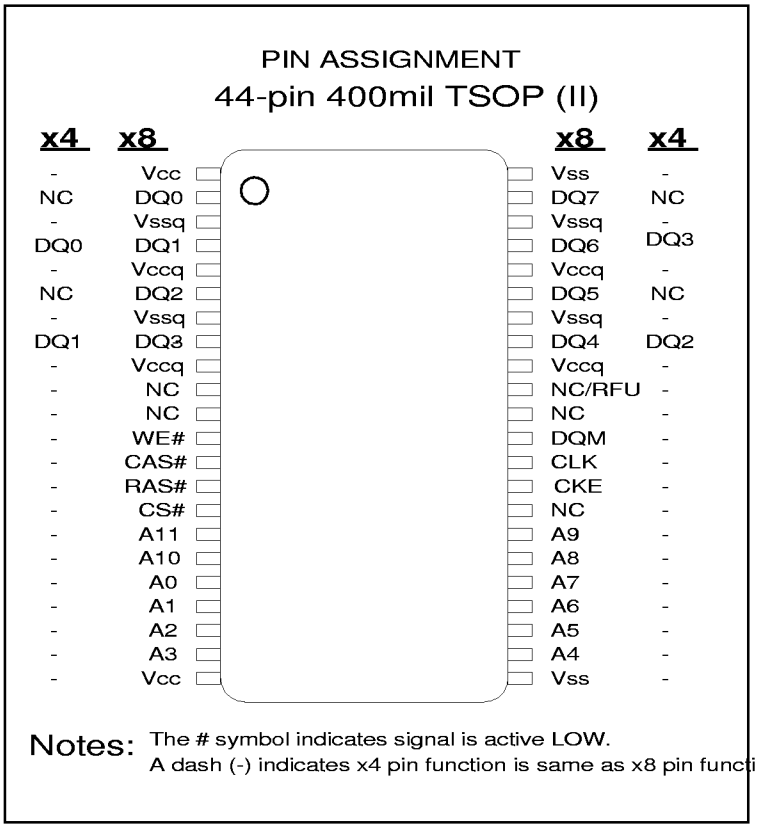
The NT56V1680A0T is a 2-bank×1,048,576-word×8-bit synchronous dynamic RAM and the NT56V1640A0T is a 2-bank×2,097,152-word×4-bit synchronous dynamic RAM fabricated in Nanya CMOS silicon-gate process technology. The device operates at 3.3V. The input and output are LVTTL compatible.

FEATURE

- JEDEC standard 3.3 V (+/- 10%) power supply.
- LVTTL compatible input and output.
- All inputs are sampled on positive edge of system clock.
- Dual Banks for hidden row access/precharge.
- Internal pipeline operation, column addresses can be changed every cycle.
- MRS cycle with address key programmability for:
  - CAS latency (2 , 3)
  - Burst Length (1 , 2 , 4 , 8)
  - Burst Type (Sequential & Interleave)
- DQM for masking.
- Auto Precharge and Auto Refresh modes.
- Self Refresh Mode.
- 64ms , 4096 cycle refresh (15.6 us/row)
- 44 –pin 400 mil plastic TSOP (type II) package.

PRODUCT FAMILY

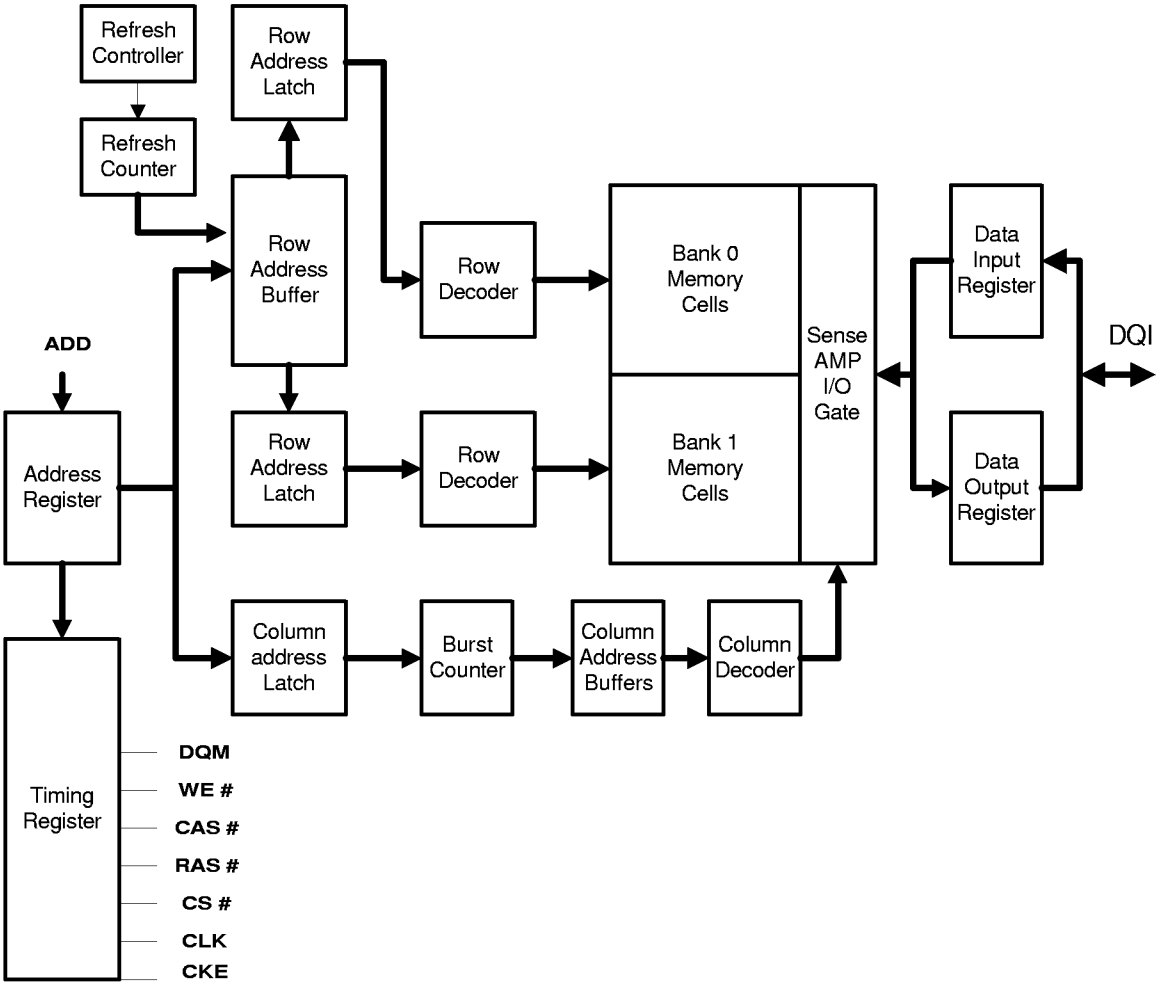
X8 Part NO.	Max Freq	Tac
NT56V1680A0T - 8	125 Mhz	6ns
NT56V1680A0T -10	100 Mhz	6ns
X4 Part NO.	**Max Freq**	**Tac**
NT56V1640A0T - 8	125Mhz	6ns
NT56V1640A0T-10	100 Mhz	6ns



Pin Functional Description

Symbol	Function	Description
A0 –A10 A11	Address	Row address:RA0 – RA10. Column address: CA0 –CA8. Bank selection: A11
CLK	System Clock	Fetches all input at the "H" edge.
CKE	Clock Enable	Master system clock to deactivate the subsequent CLK operation.
RAS#	Row address Strobe	
CAS#	Column Address Strobe	
WE#	Write Enable	
CS#	Chip Select	Disables or enables device operation by masking or enabling all controls except CLK, CKE and DQM.
DQM	Data input/output Mask	Active high. Controls the data output buffers in read mode. In write mode it masks the data from being written to the memory array.
DQi	Data Input/Output	Data I/O are multiplexed on the same table.
NC/RFU	No connect/ Reserved for Future Use	This pin should be left No Connect on the device so that the normal functionality of the device is not effected by the external connection to this pin.
Vcc, Vss	Power supply , Ground	Supply pins for the core.
VccQ, VssQ	Data output power supply , Ground.	Supply pins for the output buffers.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to V_{cc} +0.5	V
Voltage on V_{cc} Supply Relative to Vss	V_{cc}, $V_{cc}Q$	-0.5 to 4.5	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Ambient Temperature	T_a	0 to 65	
Storage Temperature	T_{stg}	-55 to 125	

- Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect reliability.

Recommended Operating Conditions

(Ta=0 to 65)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{cc}, $V_{cc}Q$	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	-	V_{cc} +0.2	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

Capacitance

(Vcc= 3.3V±10%,Ta=25 ,f=1 MHZ)

Parameter	Symbol	Min.	Max.	Unit
Input Pin Capacitance	C_{IN}	2.5	5.0	pF
I/O Pin Capacitance	$C_{I/O}$	4.0	6.5	pF
Clock Pin Capacitance	C_{Clk}	2.5-	4.0	pF

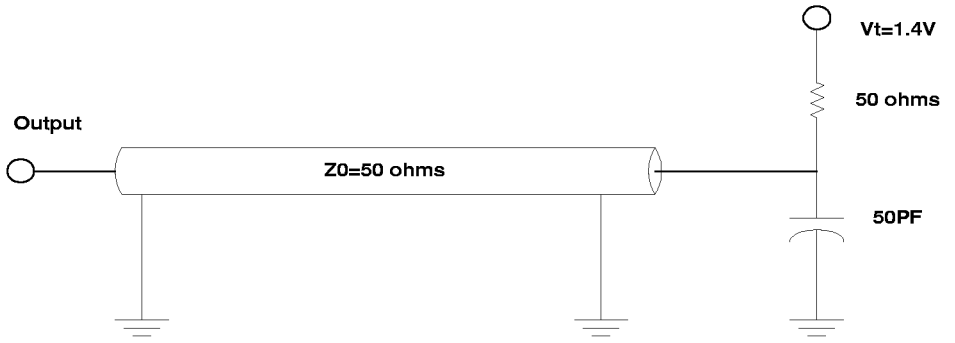
DC Characteristics

(Vcc=3.3V±10%
,Ta=0 to 65)

Parameter	Symbol	Condition	NT56V1680A0T-10/8		NT56V1640A0T-10/8		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH}=-4.0 mA	2.4	Vcc	2.4	Vcc	V	
Output Low Voltage	V_{OL}	I_{OL}=4.0 mA	0	0.4	0	0.4	V	
Input Leakage Current	I_{L1}	$0<V_{In}< V_{cc}$	-10	10	-10	10	µA	1
ICC Active	I_{CC-AC}	All banks open ping-pong read, BL=4		140		140	mA	2
ICC Low Power	I_{CCLP}	CKE Low, all banks closed		2		2	mA	
ICC Self Refresh Current	I_{CCSLFR}			1		1	mA	

Note:
1. Input leakage current includes hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. No Active or Precharge current.

AC Output Load Circuit.



AC TIMING PARAMETERS

Parameter	Symbol	Speed Grade 125MHz		Speed Grade 100MHz		Unit	Notes Ta=0-65C, Vcc=3v-3.6v
		Min	Max	Min	Max		
Clock Period	Tclk	8.0		10.0		nS	
Clock High Time	Tch	3.0		3.0		nS	Measure @ 1.5V
Clock Low Time	Tcl	3.0		3.0		nS	
Input Setup Time	Tsi	2.0		2.0		nS	
Input Hold Time	Thi	1.0		1.0		nS	
Output Valid from Clock	Tac					nS	LVTTL Levels, Rated @ 50pf with outputs switching
Cas Latency = 2			-		6.0	nS	
Cas Latency = 3			6.0		6.0	nS	
Output Hold from Clock	Toh	3.0		3.0			3ns @ 50pf
CAS to CAS Delay	Tccd	1		1		Tclk	
CAS Bank Delay	Tcbd	1		1		Tclk	
CKE to Clock Disable	Tcke	1		1		Tclk	
RAS Precharge Time	Trp	2		2		Tclk	
RAS Active Time	Tras	5		5		Tclk	
Active to Command Delay (RAS to CAS Delay)	Trcd	2		2		Tclk	
RAS to RAS Bank Active Delay	Trrd	2		2		Tclk	
RAS Cycle Time	Trc	8		7		Tclk	7 for Trp=2
DQM to Input Data Delay	Tdqd	0		0		Tclk	
Write Command to Input Data Delay	Tdwd	0		0		Tclk	
Mode Register Set to Active Delay	Tmrd	3		3		Tclk	
Precharge to O/P in High-Z	Troh	CL		CL		Tclk	CL=Cas Latency
DQM to Data in HiZ for Read	Tdqz	2		2		Tclk	
DQM to Data Mask for Write	Tdqm	0		0		Tclk	Data masked on the same clock
Data-in to PRE command Period	Tdpl	2		2		Tclk	
Data-in to ACT (PRE) cmd period (Auto-precharge)	Tdal	5		5		Tclk	
Power Down Mode Entry	Tsb		1		1	Tclk	
Self Refresh Exit Time	Tsrx	10		10		Tclk	Unit = ns
Power Down Exit Setup Time	Tpde	1		1		Tclk	CKE is latched on next clock cycle
Clock Stop During Self Refresh or Power Down	Tclkstp	200		200		nS	If CLK stop during Self Refresh

Mode Register Definition

Mode Register Set: (Programming mode)

BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address bus
11	10	9	8	7	6	5	4	3	2	1	0	Mode Register (Mx)
Reserved		0	0	0	CAS Latency			BT	Burst Length			

Bit (654)	Cas Latency
010	2
011	3
All Other	Reserved

Bit (3)	Type
0	Sequential
1	Interleave

Bit (210)	Burst Length
000	1
001	2
010	4
011	8
All Other	Reserved

Burst Length	Starting Bit	Interleave	Sequential
2	0	0,1	0,1
2	1	1,0	1,0
4	00	0,1,2,3	0,1,2,3
4	01	1,0,3,2	1,2,3,0
4	10	2,3,0,1	2,3,0,1
4	11	3,2,1,0	3,0,1,2
8	000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
8	001	1,0,3,2,5,4,7,6	1,2,3,4,5,6,7,0
8	010	2,3,0,1,6,7,4,5	2,3,4,5,6,7,0,1
8	011	3,2,1,0,7,6,5,4	3,4,5,6,7,0,1,2
8	100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
8	101	5,4,7,6,1,0,3,2	5,6,7,0,1,2,3,4
8	110	6,7,4,5,2,3,0,1	6,7,0,1,2,3,4,5
8	111	7,6,5,4,3,2,1,0	7,0,1,2,3,4,5,6

FUNCTION TRUTH TABLE (TABLE 1)

Current State	CS#	RAS#	CAS#	WE#	Address	Bank Address	Action	Notes
Idle	H	X	X	X	X	X	No Operation command	
	L	H	H	H	X	X	No Operation command	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	X	CA,A10	BA	ILLEGAL	2
	L	L	H	H	RA	BA	Row Active	
	L	L	H	L	A10	BA	No Operation command	4
	L	L	L	H	X	X	Auto Refresh or Self refresh	5
	L	L	L	L	Op Code	L	Mode Register Access	5
Row Active	H	X	X	X	X	X	No Operation command	
	L	H	H	X	X	X	No Operation command	
	L	H	L	H	CA,A10	BA	Read	
	L	H	L	L	CA,A10	BA	Write	
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	Precharge	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
Read	H	X	X	X	X	X	Continue burst to end, row active	
	L	H	H	H	X	X	Continue burst to end, row active	
	L	H	L	H	CA,A10	BA	Term burst, start new burst read	
	L	H	L	L	CA,A10	BA	Term burst, start new burst write	
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	Term burst, precharge	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
Write	H	X	X	X	X	X	Continue burst to end, row active	
	L	H	H	H	X	X	Continue burst to end, row active	
	L	H	L	H	CA,A10	BA	Term burst start read	
	L	H	L	L	CA,A10	BA	Term burst, new write	
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	Term burst precharge	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	Continue burst to end and enter Row precharge	
	L	H	H	H	X	X	Continue burst to end and enter Row precharge	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	H	CA,A10	BA	ILLEGAL	2
	L	H	L	L	X	X	ILLEGAL	
	L	L	H	X	RA,A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	Continue burst to end and enter Row precharge	
	L	H	H	H	X	X	Continue burst to end and enter Row precharge	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	H	CA,A10	BA	ILLEGAL	2
	L	H	L	L	X	X	ILLEGAL	
	L	L	H	X	RA,A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	

FUNCTION TRUTH TABLE (TABLE 1)

Current State	CS #	RAS#	CAS#	WE#	Address	Bank Address	Action	Notes
Precharge	H	X	X	X	X	X	NOP-enter idle after tRP	
	L	H	H	H	X		NOP-enter idle after tRP	
	L	H	L	H	X	BA	ILLEGAL	2
	L	H	L	X	CA	BA	ILLEGAL	2
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	NOP-enter idle after tRP	4
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	X	ILLEGAL	
Row Active	H	X	X	X	X	X	NOP-enter idle after tRCD	
	L	H	H	H	X	X	NOP-enter idle after tRCD	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	X	CA	BA	ILLEGAL	2
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	X	ILLEGAL	
Write Recovery	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	X	CA	BA	ILLEGAL	2
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	X	ILLEGAL	
Refresh	H	X	X	X	X	X	NOP – enter idle after tRC	
	L	H	H	H	X	X	NOP – enter idle after tRC	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Set	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Note:

1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. Satisfy the timing of Tccd and Twr(Write Recovery Time)to prevent bus contention.
4. NOP to bank precharge or in idle state. Precharge activated bank by BA or A10.
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State(n)	CKE n-1	CKE n	CS #	RAS#	CAS#	WE#	Address	Action	Notes
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh-Idle after tRFC(ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh-Idle after tRFC(ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP	
Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down - ABI	
	L	H	L	H	H	H	X	Exit Power Down - ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP	
All Banks Idle (ABI)	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	H	H	X	X	Enter Power Down	
	H	L	L	H	H	X	X	Enter Power Down	8
	H	L	L	H	L	L	X	ILLEGAL	8
	H	L	L	L	H	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (&bank) Active	
	H	L	L	L	L	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	8
	H	L	L	L	X	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State Other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Note:

6. CKE low to high transition is asynchronous.
7. CKE low to high transition is asynchronous if restart internal clock.
   A minimum setup time 1CLK + tsi must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the both banks idle state.
9. Must be a legal command.

1. When cs# is set ‘ High ’ at a clock transition from ‘Low’ to ‘high’, all inputs except CKE and DQM are invalid.
2. When issuing an active, read or write command, the bank is selected by A11

A11	Active, read or write
0	Bank A
1	Bank B

3. The auto precharge function is enable or disable by the A10 input when the read and write command is issued.

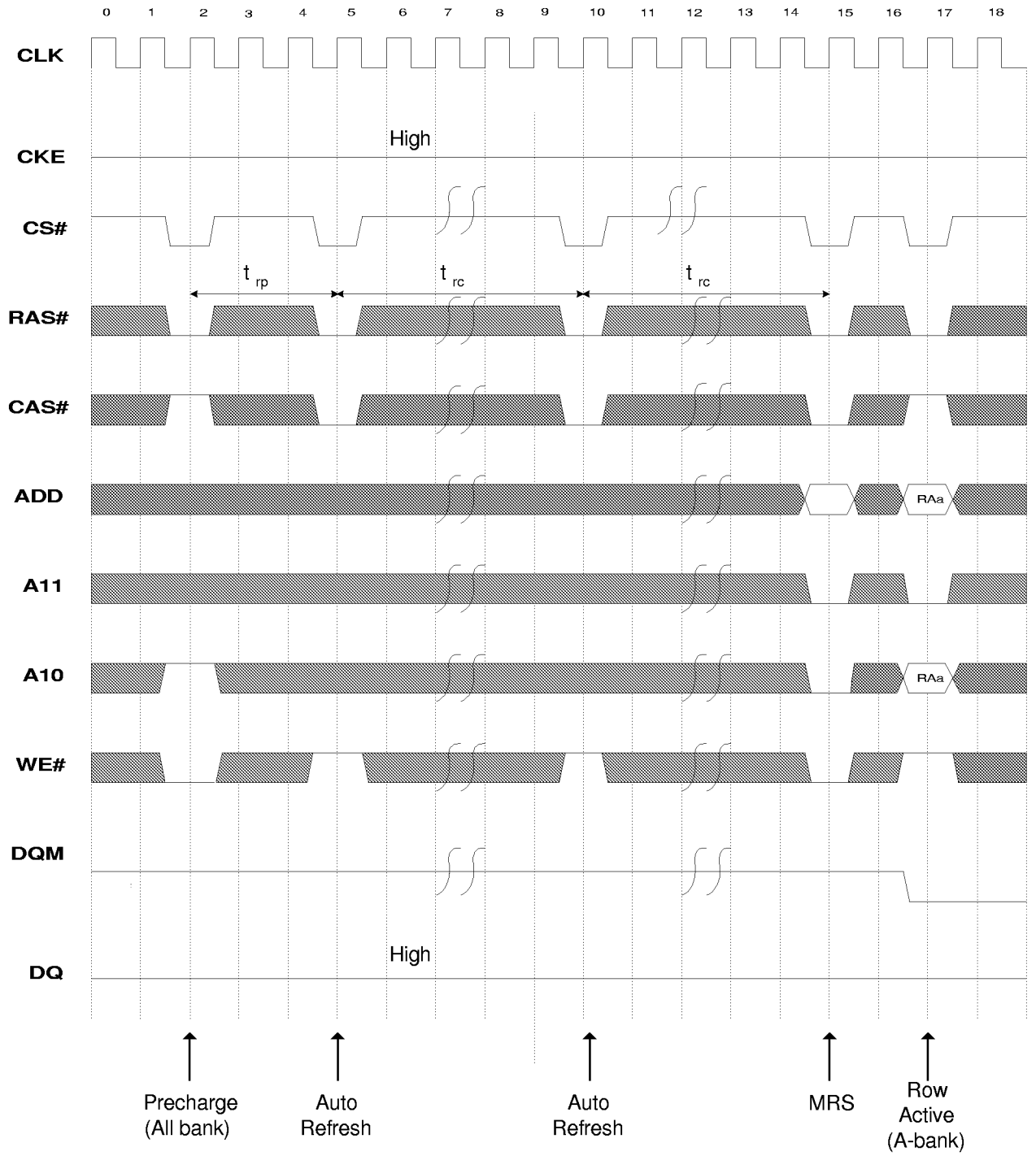
A10	A11	Operation
0	0	After the end of burst, bank A holds the idle status.
1	0	After the end of burst, bank A is precharged automatically.
0	1	After the end of burst, bank B holds the idle status.
1	1	After the end of burst, bank B is precharged automatically.

4. when issuing a precharge command, the bank to be precharged is selected by the A10 and A11 input.

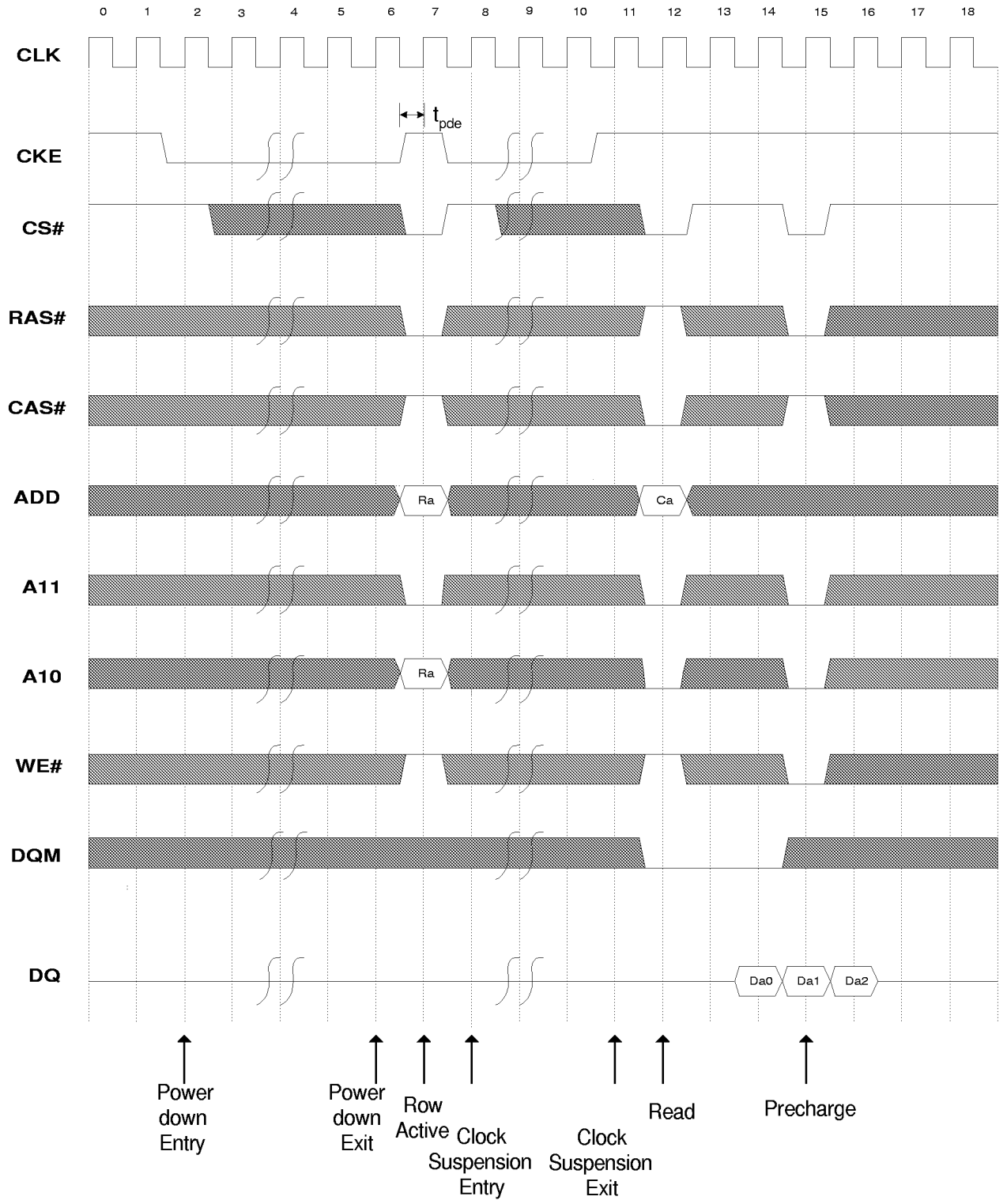
A10	A11	Operation
0	0	Bank A is precharge.
0	1	Bank B is Precharge.
1	x	Both banks A & B are precharged.

TIMING WAVEFORM

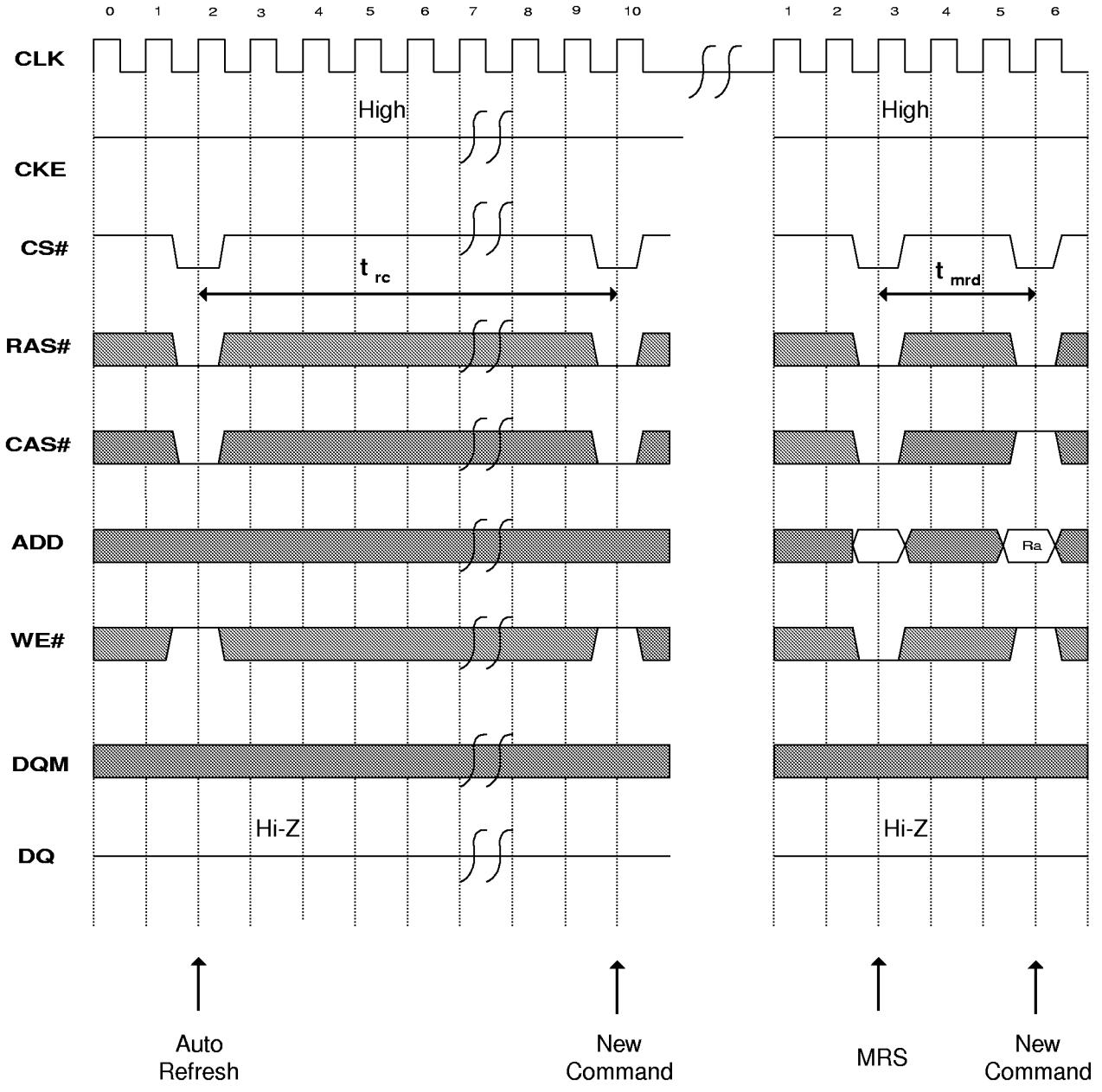
Power up sequence



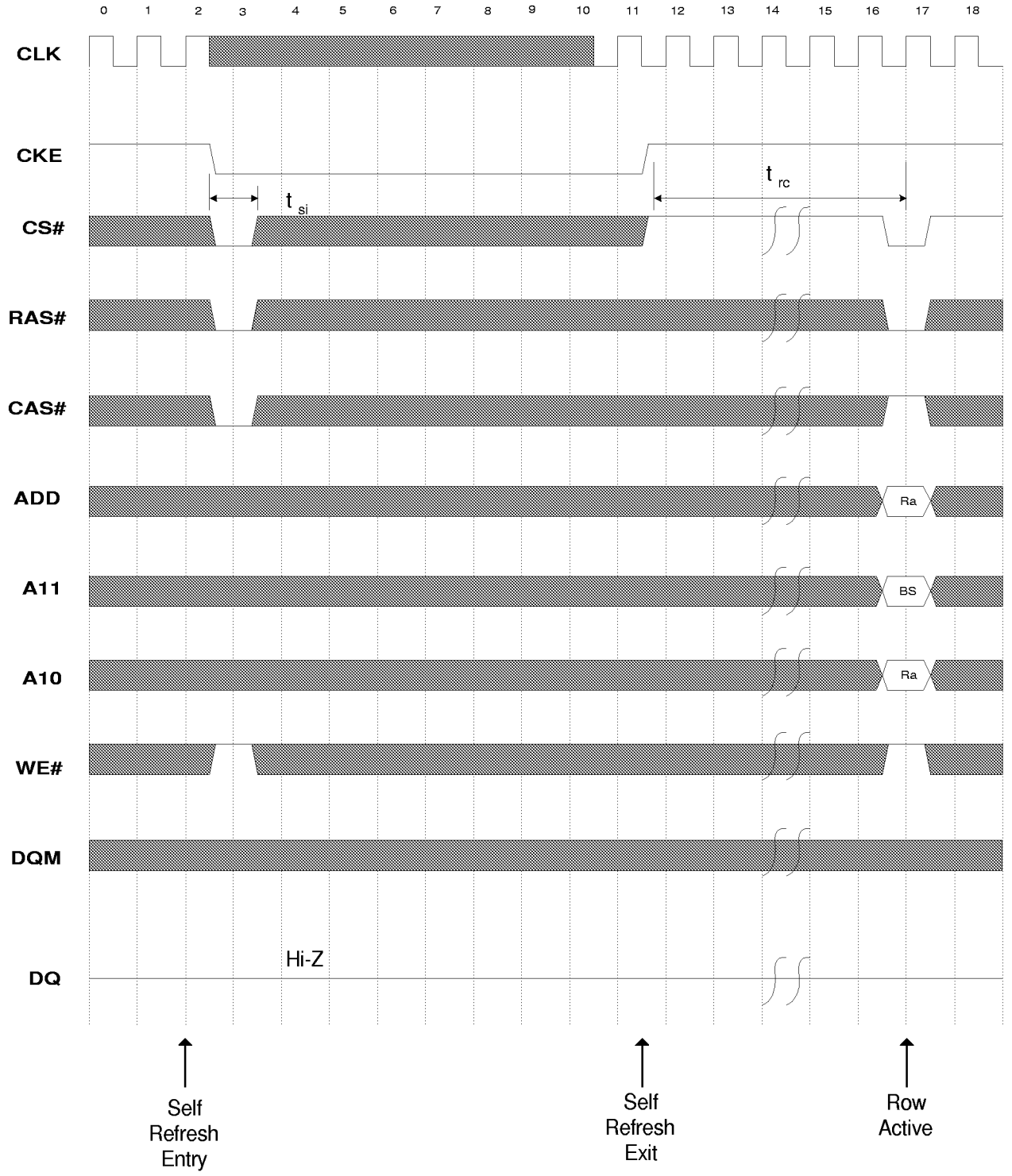
Power down Mode (CL =2 , BL =4)



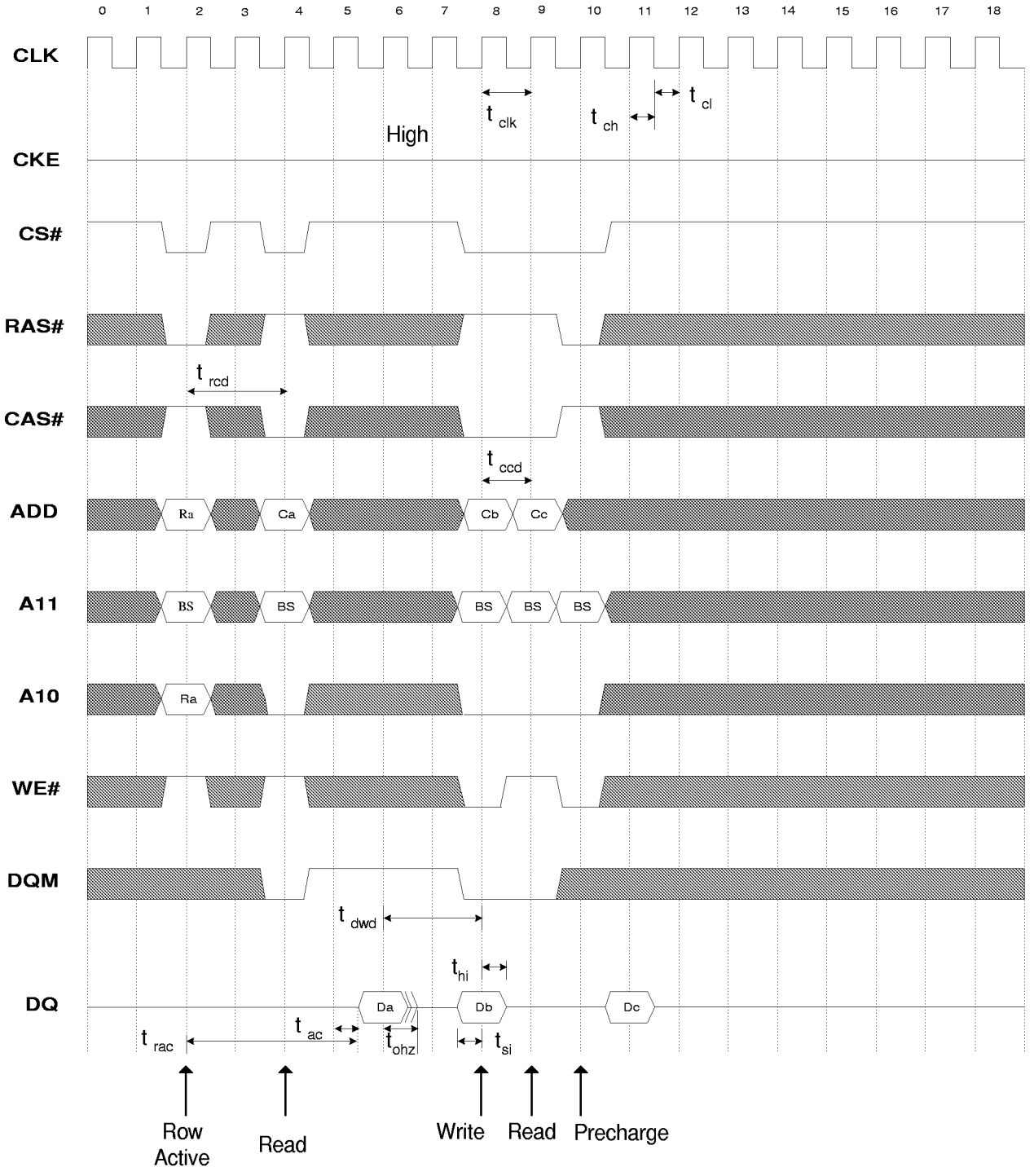
Auto Refresh Cycle & Mode Register Set Cycle



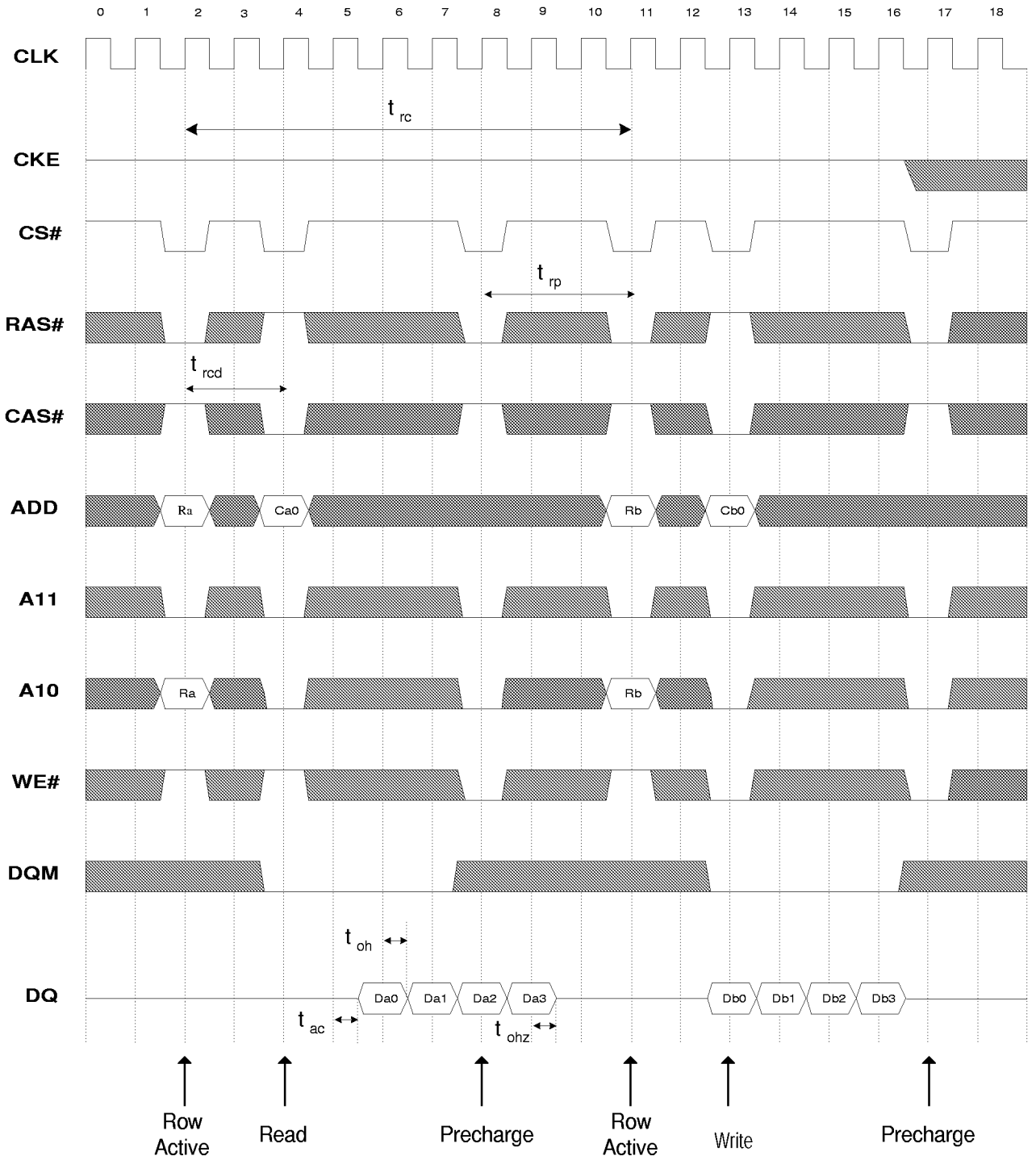
Self Refresh Cycle



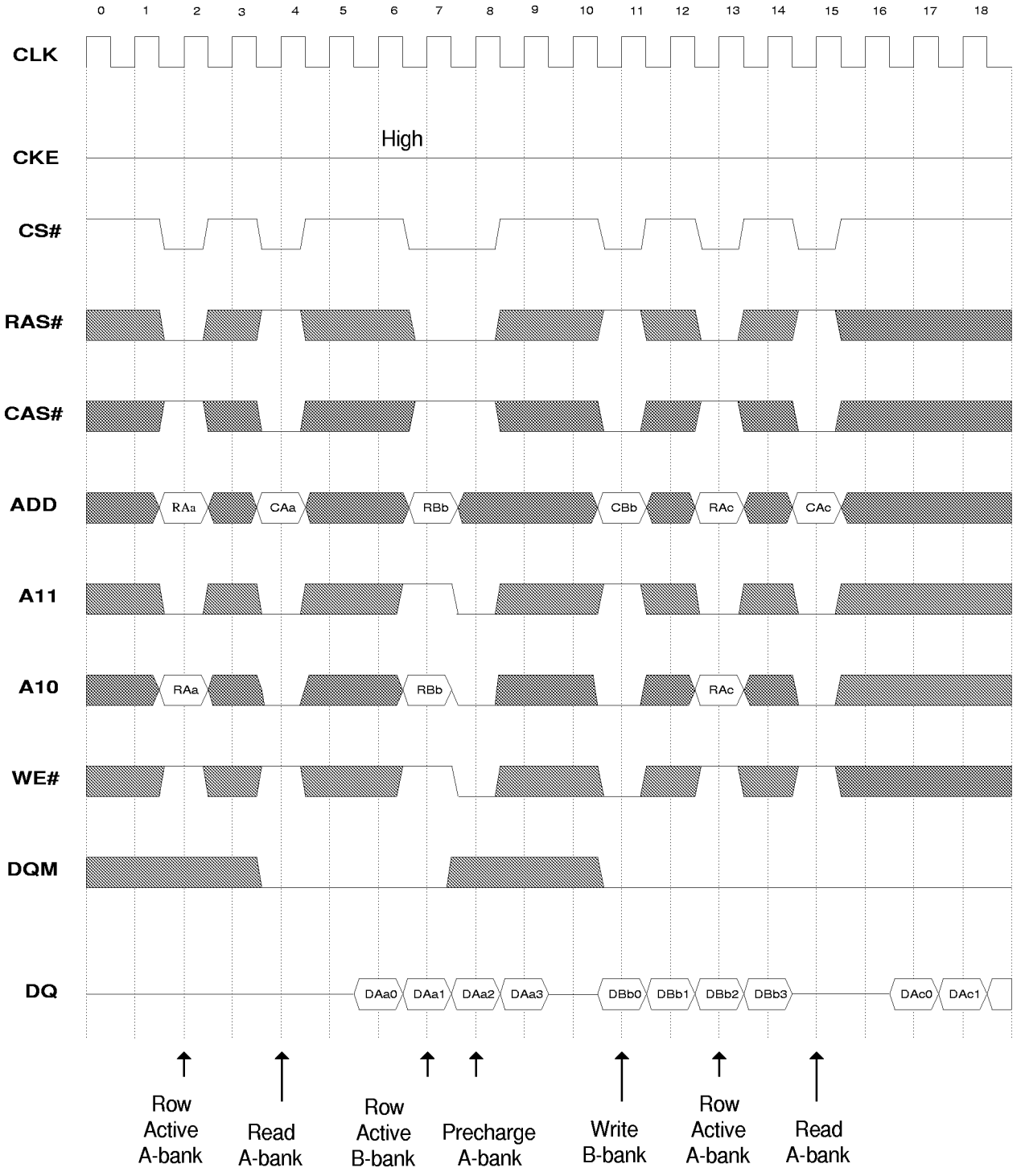
Single Bit Read-Write-Read Cycle at same page (CL =2 , BL = 1)



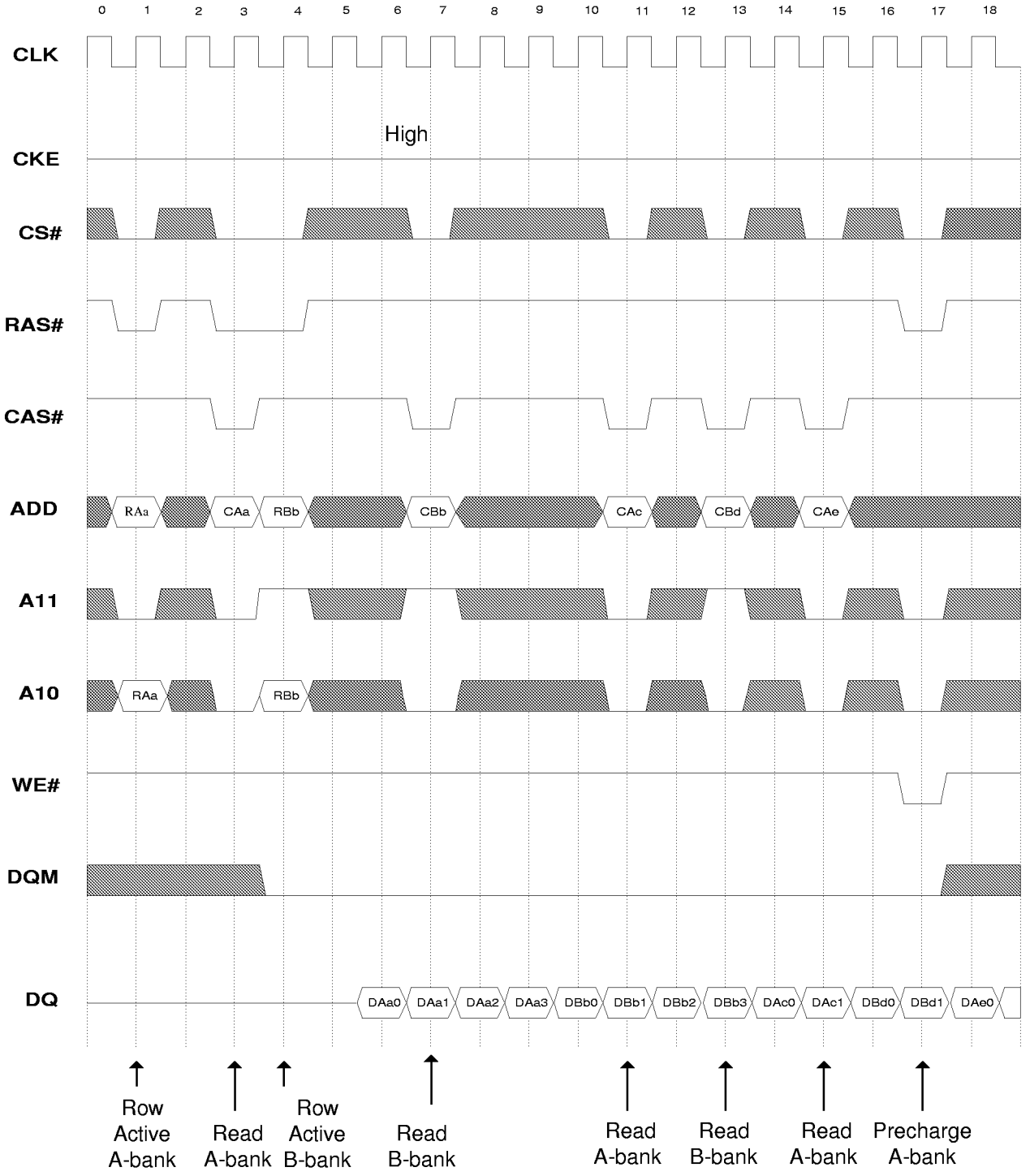
Read & Write Cycle at Same Bank (CL = 2 , BL = 4)



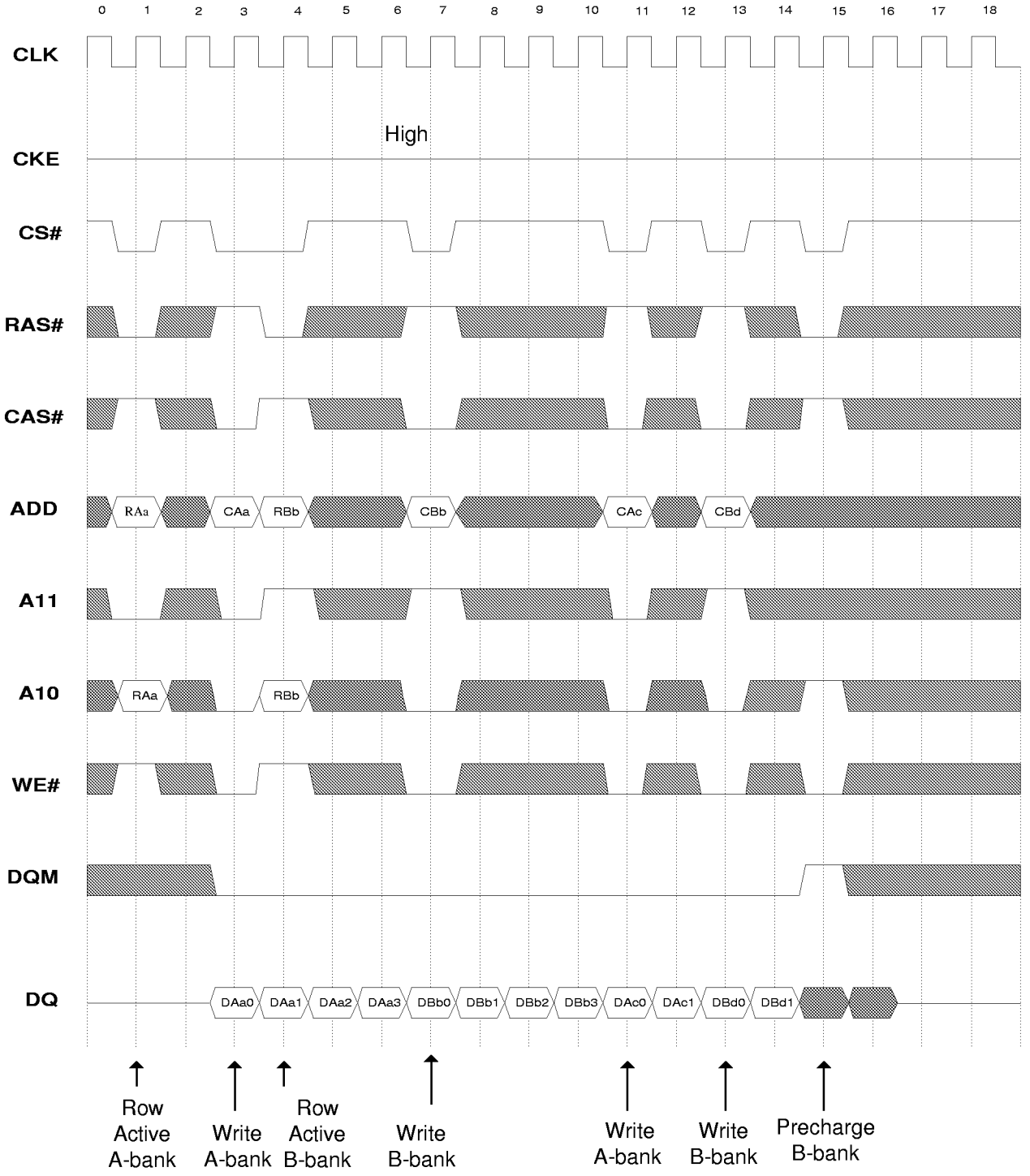
Read & Write Cycle with Random Row at Different Bank (CL = 2 , BL = 4)



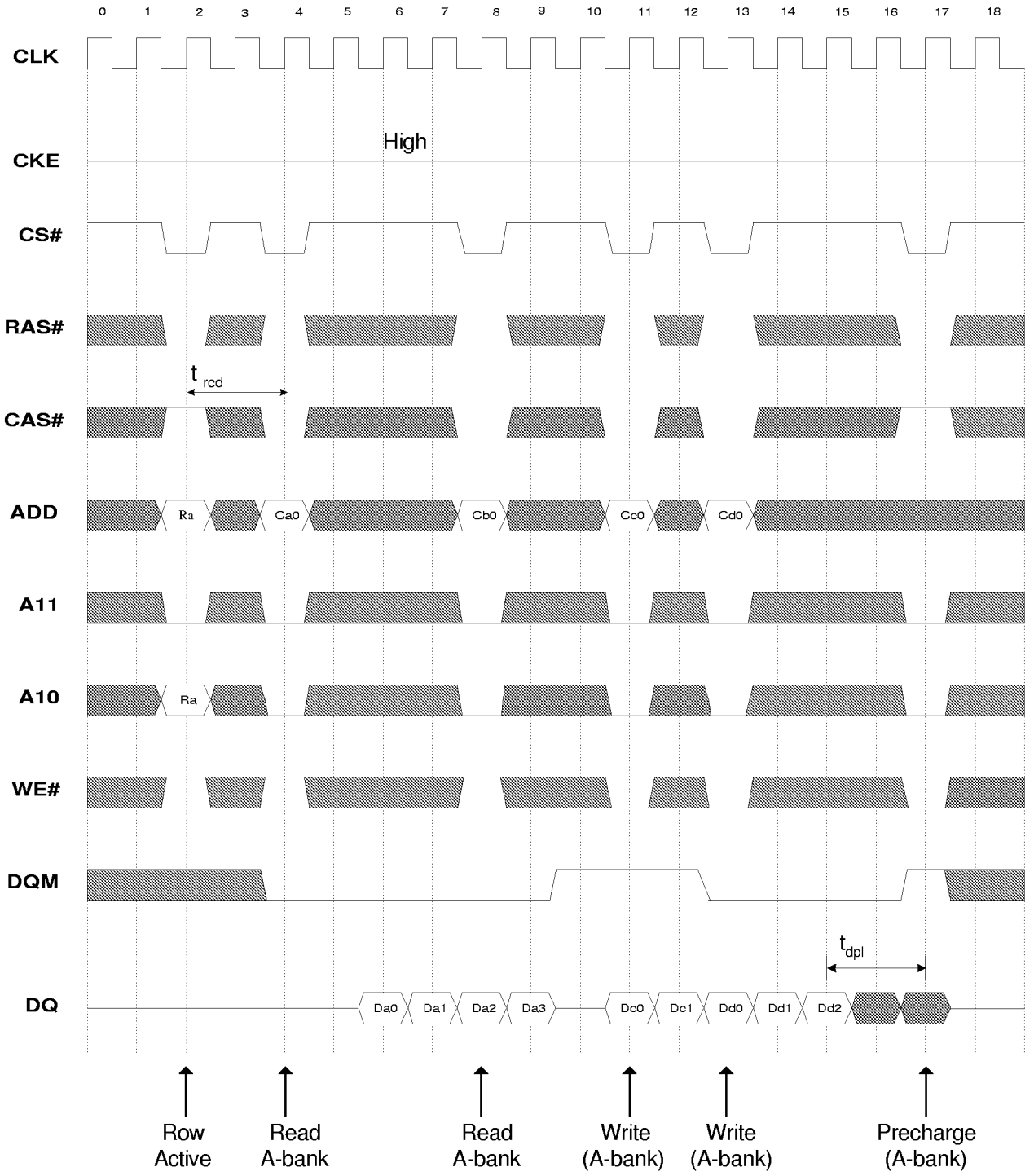
Page Read Cycle at Different Bank (CL = 3 , BL = 4)



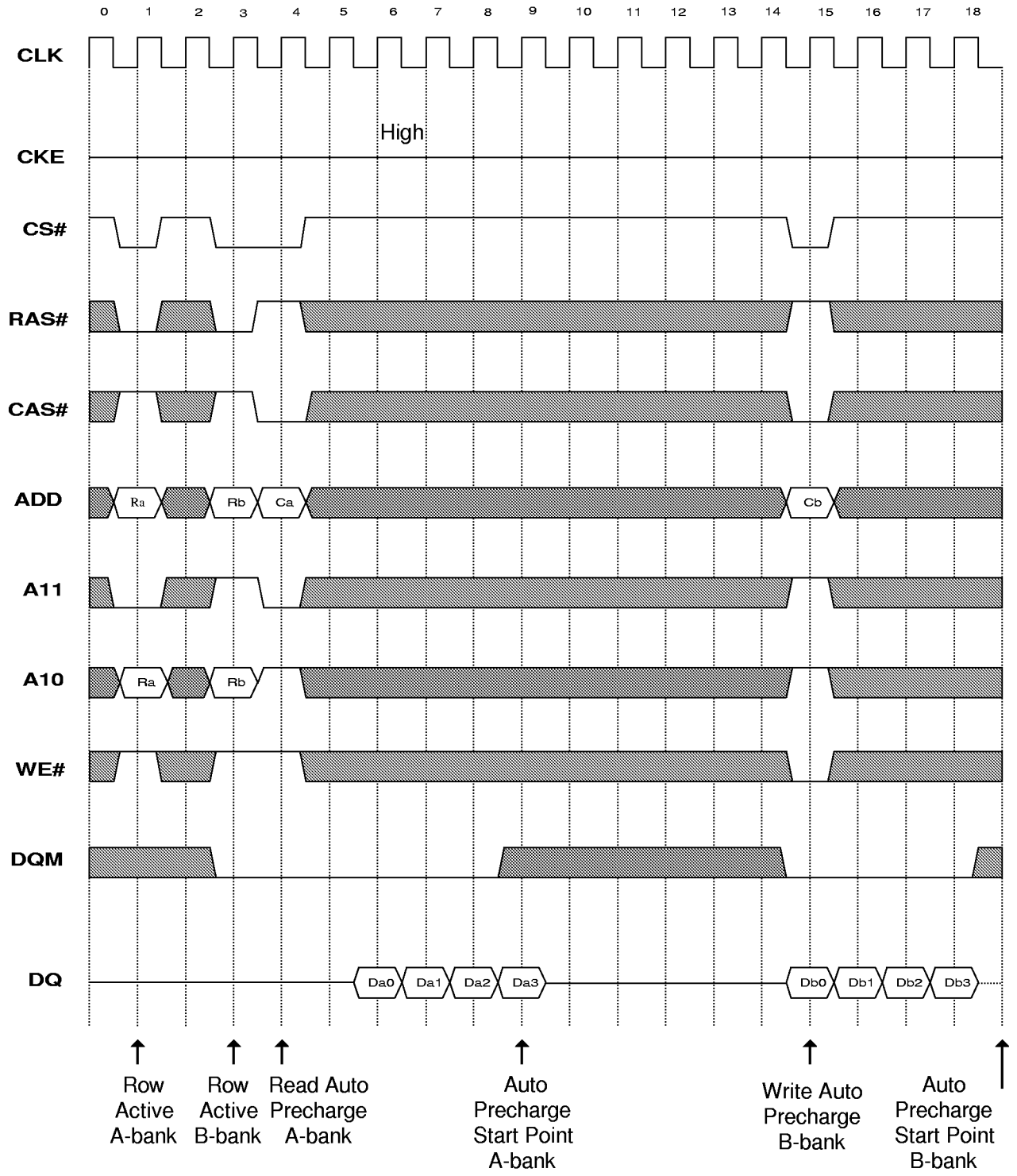
Page Write Cycle at Different Bank (BL = 4)



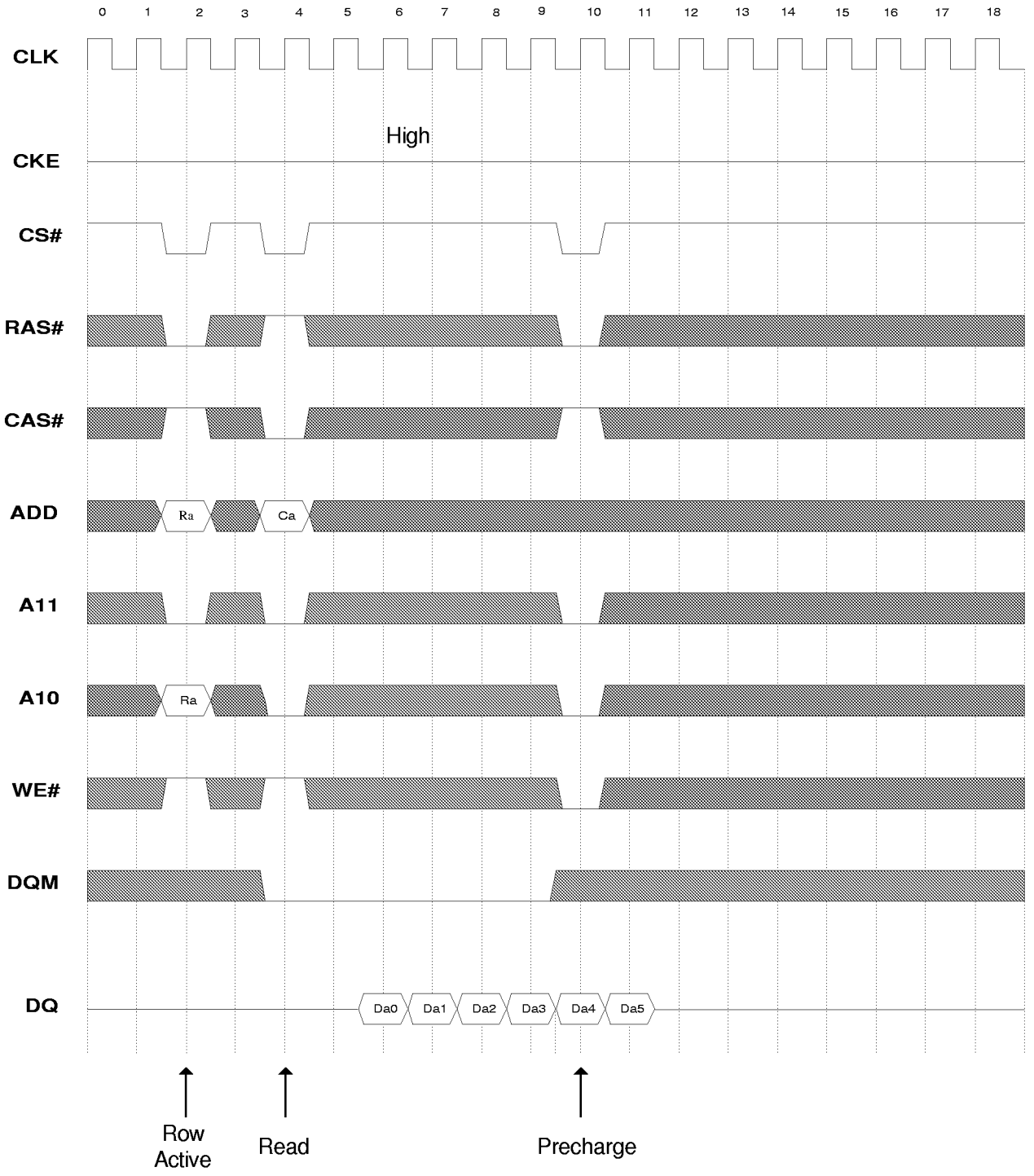
Page Read & Write Cycle at Same Bank (CL = 2 , BL = 4)



Read & Write Cycle with Auto Precharge (CL = 2 , BL = 4)



Read Interruption by Precharge (CL = 2 , BL = 8)



Clock Suspension & DQM Operation Cycle (CL = 2 , BL = 4)