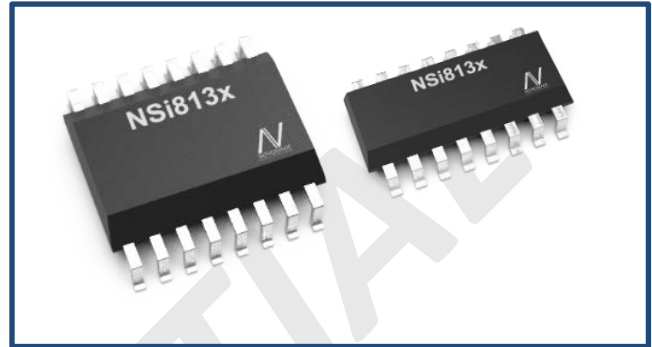


Product Overview

The NSi813x devices are high reliability triple-channel digital isolators. The NSi813x device is safety certified by UL1577 support several insulation withstand voltages ($3.75kV_{rms}$, $5kV_{rms}$), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi813x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi813x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi813x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to $5000V_{rms}$ Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- All devices are AEC-Q100 qualified
- High CMTI: 150kV/us
- Chip level ESD: HBM: $\pm 6kV$
- High system level EMC performance:
Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low-level option
- Isolation barrier life: >60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: $-40^{\circ}C \sim 125^{\circ}C$
- RoHS-compliant packages:
SOIC-16 narrow body
SOIC-16 wide body



Safety Regulatory Approvals

- UL recognition: up to $5000V_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11(DIN VDE V 0884-11):2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Functional Block Diagrams

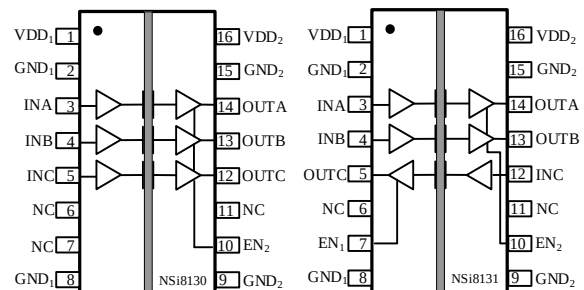


Figure 1. NSi813x Block Diagrams

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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC	-0.4		VDD+0.4	V	
Maximum Output Voltage	VOUA, VOUTB, VOUTC	-0.4		VDD+0.4	V	
Maximum Input/output Pulse Voltage	VINA, VINB, VINC, VOUA, VOUTB, VOUTC	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Common-Mode Transients	CMTI			±150	kV/us	
Output current	I _o	-15		15	mA	
Maximum Surge Isolation Voltage	V _{IOSM}			5.3	kV	
Operating Temperature	Topr	-40		125	°C	
Storage Temperature	Tstg	-40		150	°C	
Electrostatic discharge	HBM			± 6000	V	
	CDM			± 2000	V	

2.0 SPECIFICATIONS

2.1. ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR}		2.2		V	POR threshold as during power-up
	VDD _{HYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V _{IT}		1.6		V	Input Threshold at rising edge
	V _{IT_HYS}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V _{IH}	2			V	
Low Level Input Voltage	V _{IL}			0.8	V	
High Level Output Voltage	V _{OH}	VDD-0.3			V	I _{OH} ≤ 4mA

Low Level Output Voltage	V_{OL}			0.3	V	$I_{OL} \leq 4mA$
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	trbs		40		usec	
Common Mode Transient Immunity	CMTI	100		150	kV/us	

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSi8130					
	I _{DD1} (Q0)		0.75	1.125	mA	All Input 0V for NSi8130x0 Or All Input at supply for NSi8130x1
	I _{DD2} (Q0)		1.76	2.64	mA	
	I _{DD1} (Q1)		4.21	6.315	mA	All Input at supply for NSi8130x0 Or All Input 0V for NSi8130x1
	I _{DD2} (Q1)		1.84	2.76	mA	
	I _{DD1} (1M)		2.53	3.795	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.07	3.105	mA	
	I _{DD1} (10M)		2.64	3.96	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.36	6.54	mA	
	I _{DD1} (100M)		3.54	5.31	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		26.4	39.6	mA	
	NSi8131					
	I _{DD1} (Q0)		1.16	1.74	mA	All Input 0V for NSi8131x0 Or All Input at supply for NSi8131x1
	I _{DD2} (Q0)		1.57	2.355	mA	
	I _{DD1} (Q1)		3.35	5.025	mA	All Input at supply for NSi8131x0 Or All Input 0V for NSi8131x1
	I _{DD2} (Q1)		2.65	3.975	mA	
	I _{DD1} (1M)		2.37	3.555	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.3	3.45	mA	
	I _{DD1} (10M)		3.18	4.77	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		3.88	5.82	mA	
	I _{DD1} (100M)		11.4	17.1	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		19.5	29.25	mA	
Data Rate	DR	0		150	Mbps	

Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	5	8.20	15	ns	See Figure 2.7 , $C_L = 15pF$
	t_{PHL}	5	10.56	15	ns	See Figure 2.7 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 2.7 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 2.7 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 2.7 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{jit}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{sk}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{sk}(p2p)$			5.0	ns	
Disable high to Tri-State	t_{PHZ}		14.88		ns	See Figure 2.8 , $C_L = 15pF$, $R_L = 1k$
Enable to Data high Valid	t_{PZH}		10.00		ns	See Figure 2.8 , $C_L = 15pF$, $R_L = 1k$
Disable low to Tri-State	t_{PLZ}		17.25		ns	See Figure 2.8 , $C_L = 15pF$, $R_L = 1k$
Enable to Data high Valid	t_{PZL}		10.85		ns	See Figure 2.8 , $C_L = 15pF$, $R_L = 1k$

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSi8130					
	I _{DD1} (Q0)		0.69	1.035	mA	All Input 0V for NSi8130x0 Or All Input at supply for NSi8130x1
	I _{DD2} (Q0)		1.67	2.505	mA	
	I _{DD1} (Q1)		4.13	6.195	mA	All Input at supply for NSi8130x0 Or All Input 0V for NSi8130x1
	I _{DD2} (Q1)		1.75	2.625	mA	
	I _{DD1} (1M)		2.45	3.675	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.88	2.82	mA	
	I _{DD1} (10M)		2.52	3.78	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		3.34	5.01	mA	
	I _{DD1} (100M)		3.07	4.605	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		17.6	26.4	mA	
	NSi8131					
	I _{DD1} (Q0)		1.09	1.635	mA	All Input 0V for NSi8131x0 Or All Input at supply for NSi8131x1
	I _{DD2} (Q0)		1.5	2.25	mA	

	$I_{DD1}(Q1)$		3.28	4.92	mA	All Input at supply for NSi8131x0 Or All Input 0V for NSi8131x1
	$I_{DD2}(Q1)$		2.57	3.855	mA	
	$I_{DD1}(1M)$		2.27	3.405	mA	All Input with 1Mbps, $C_L=15pF$
	$I_{DD2}(1M)$		2.16	3.24	mA	
	$I_{DD1}(10M)$		2.8	4.2	mA	All Input with 10Mbps, $C_L=15pF$
	$I_{DD2}(10M)$		3.19	4.785	mA	
	$I_{DD1}(100M)$		7.83	11.745	mA	All Input with 100Mbps, $C_L=15pF$
	$I_{DD2}(100M)$		13.7	20.55	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	5	9.20	15	ns	See Figure 2.7 , $C_L = 15pF$
	t_{PHL}	5	10.40	15	ns	See Figure 2.7 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 2.7 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 2.7 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 2.7 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	
Disable high to Tri-State	t_{PHZ}		17.85		ns	See Figure 2.8 , $C_L = 15pF$, $R_L=1k$
Enable to Data high Valid	t_{PZH}		13.37		ns	See Figure 2.8 , $C_L = 15pF$, $R_L=1k$
Disable low to Tri-State	t_{PLZ}		20.6		ns	See Figure 2.8 , $C_L = 15pF$, $R_L=1k$
Enable to Data high Valid	t_{PZL}		13.67		ns	See Figure 2.8 , $C_L = 15pF$, $R_L=1k$

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSi8130					
	$I_{DD1}(Q0)$		0.66	0.99	mA	All Input 0V for NSi8130x0 Or All Input at supply for NSi8130x1
	$I_{DD2}(Q0)$		1.63	2.445	mA	
	$I_{DD1}(Q1)$		4.08	6.12	mA	All Input at supply for NSi8130x0 Or All Input 0V for NSi8130x1
	$I_{DD2}(Q1)$		1.7	2.55	mA	

	I _{DD1} (1M)		2.41	3.615	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.79	2.685	mA	
	I _{DD1} (10M)		2.44	3.66	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.89	4.335	mA	
	I _{DD1} (100M)		2.73	4.095	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		14.03	21.045	mA	
	NSi8131					
	I _{DD1} (Q0)		1.06	1.59	mA	All Input 0V for NSi8131x0 Or All Input at supply for NSi8131x1
	I _{DD2} (Q0)		1.46	2.19	mA	
	I _{DD1} (Q1)		3.24	4.86	mA	All Input at supply for NSi8131x0 Or All Input 0V for NSi8131x1
	I _{DD2} (Q1)		2.53	3.795	mA	
	I _{DD1} (1M)		2.22	3.33	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.09	3.135	mA	
	I _{DD1} (10M)		2.62	3.93	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.87	4.305	mA	
	I _{DD1} (100M)		6.58	9.87	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		10.46	15.69	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}	5	10.0	15	ns	See Figure 2.7 , C _L = 15pF
	t _{PHL}	5	10.0	15	ns	See Figure 2.7 , C _L = 15pF
Pulse Width Distortion	PWD			5.0	ns	See Figure 2.7 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 2.7 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 2.7 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT} (PK)		350		ps	
Channel-to-Channel Delay Skew	t _{SK} (c2c)			2.5	ns	
Part-to-Part Delay Skew	t _{SK} (p2p)			5.0	ns	
Disable high to Tri-State	t _{PHZ}		20.6		ns	See Figure 2.8 , C _L = 15pF, R _L =1k
Enable to Data high Valid	t _{PZH}		18.12		ns	See Figure 2.8 , C _L = 15pF, R _L =1k
Disable low to Tri-State	t _{PLZ}		21.85		ns	See Figure 2.8 , C _L = 15pF, R _L =1k
Enable to Data high Valid	t _{PZL}		20.02		ns	See Figure 2.8 , C _L = 15pF, R _L =1k

2.2. TYPICAL PERFORMANCE CHARACTERISTICS

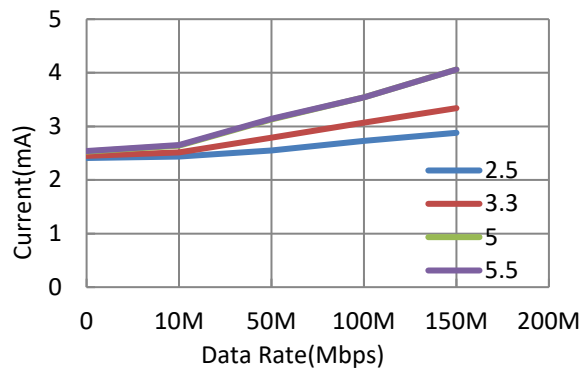


Figure 2.1 NSi8130 VDD1 Supply Current vs Data Rate

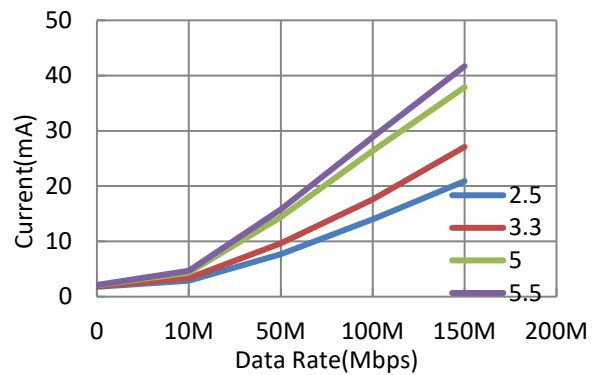


Figure 2.2 NSi8130 VDD2 Supply Current vs Data Rate

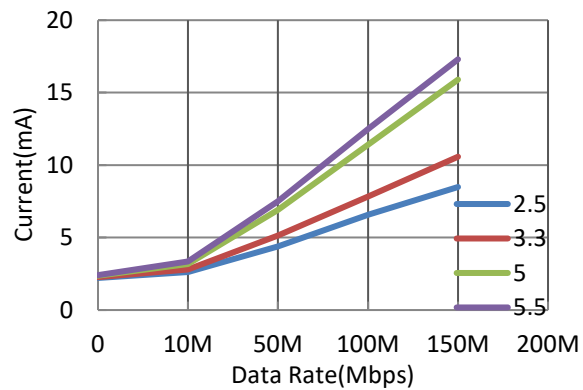


Figure 2.3 NSi8131 VDD1 Supply Current vs Data Rate

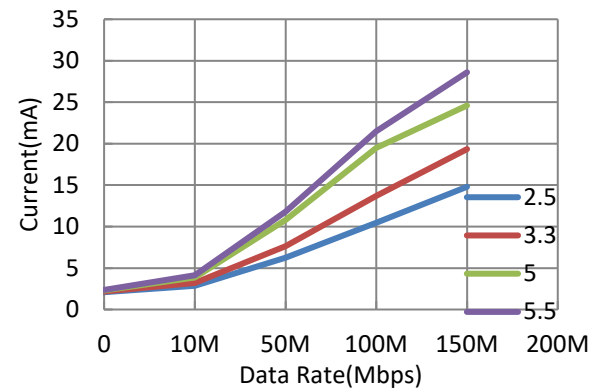


Figure 2.4 NSi8131 VDD2 Supply Current vs Data Rate

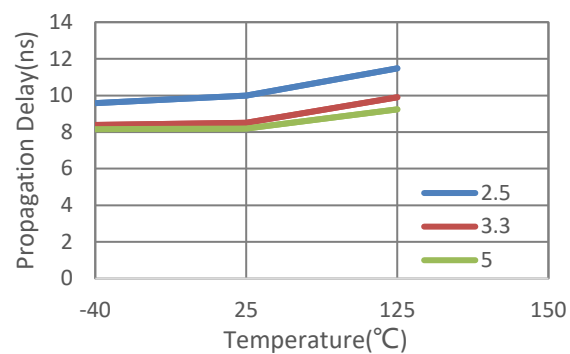


Figure 2.5 Rising Edge Propagation Delay Vs Temp

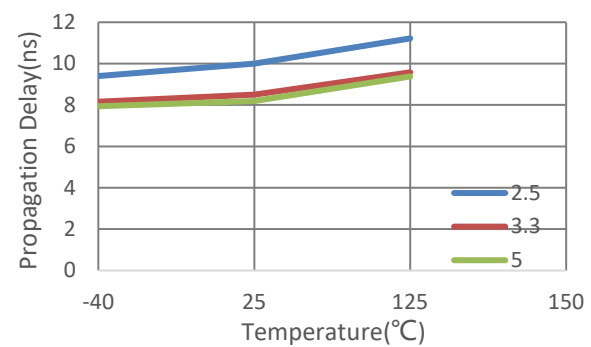


Figure 2.6 Falling Edge Propagation Delay Vs Temp

2.3. PARAMETER MEASUREMENT INFORMATION

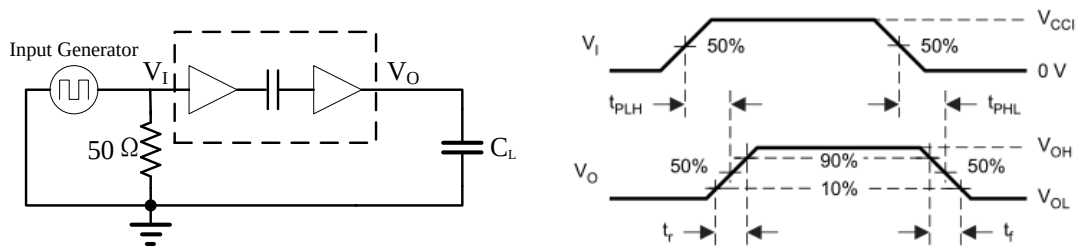


Figure 2.7 Switching Characteristics Test Circuit and Waveform

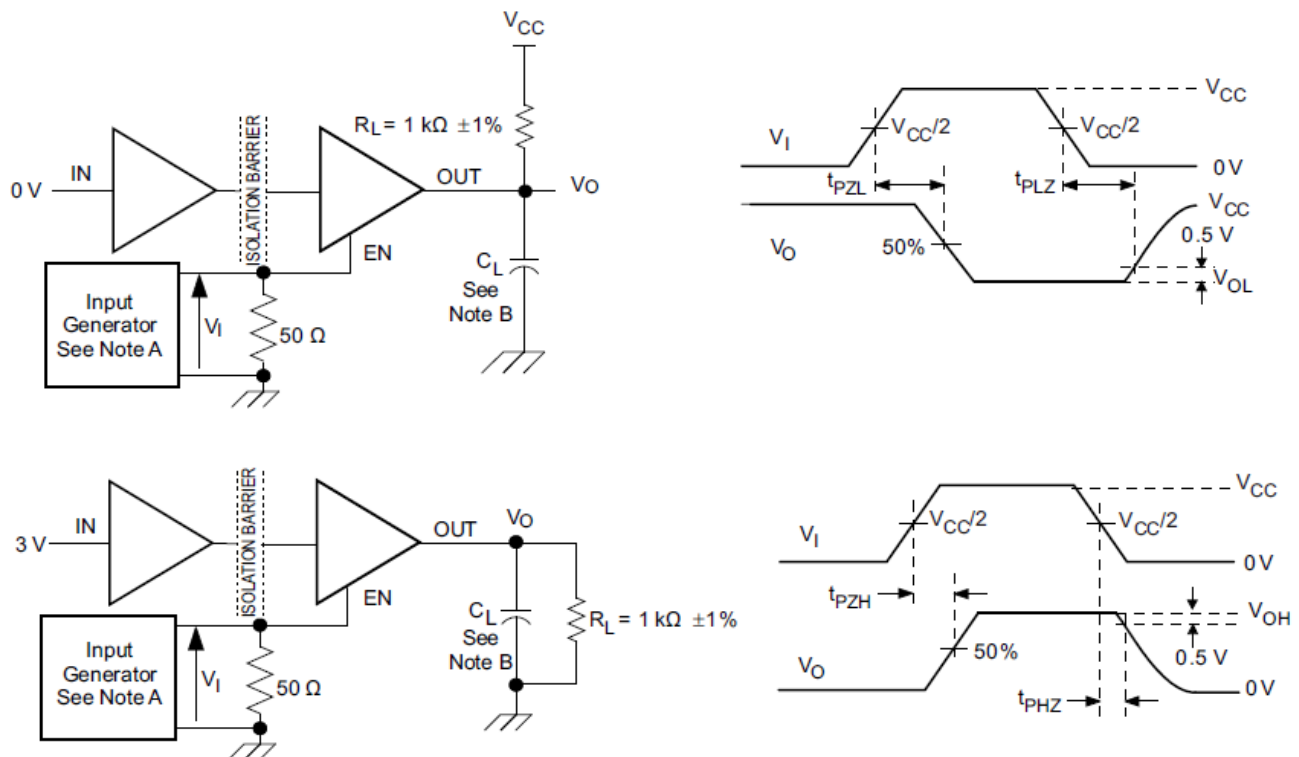


Figure 2.8 Enable/Disable Propagation Delay Time Test Circuit and Waveform

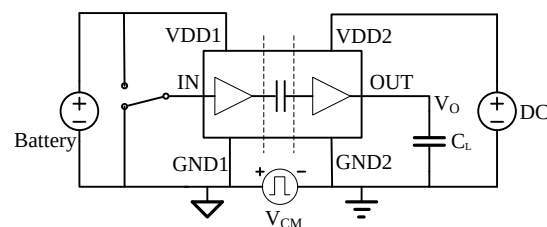


Figure 2.9 Common-Mode Transient Immunity Test Circuit

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	Symbol	Value		Unit	Comments
		NB-SOIC-16	WB-SOIC-16		
Minimum External Air Gap (Clearance)	L(I01)	4.0	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		II			

3.2. DIN VDE V 0884-11 (VDE V 0884-11) :2017-01 INSULATION CHARACTERISTICS

Description	Test Condition	Symbol	Value		Unit
			NB-SOIC-16	WB-SOIC-16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage $\leq 150V_{rms}$			I to IV	I to IV	
For Rated Mains Voltage $\leq 300V_{rms}$			I to III	I to IV	
For Rated Mains Voltage $\leq 400V_{rms}$			I to III	I to IV	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		VIORM	565	849	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	847	1273	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial	$V_{pd(m)}$	678	1019	Vpeak

	discharge < 5 pC				
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1019	Vpeak
Maximum transient isolation voltage	$t = 60$ sec	VIOTM	5300	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50us waveform, $V_{TEST} = V_{IOSM} \times 1.3$	VIOSM	5384	5384	Vpeak
Isolation resistance	$V_{IO} = 500V$	RIO	$>10^9$	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	CIO	0.6	0.6	pF
Input capacitance		CI	2	2	pF
Total Power Dissipation at 25°C		Ps		1499	mW
Safety input, output, or supply current	$\theta_{JA} = 140$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C	Is	160		mA
	$\theta_{JA} = 84$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C			237	mA
Case Temperature		Ts	150	150	°C

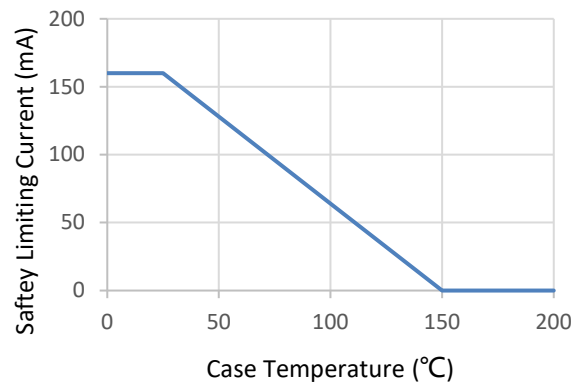


Figure 3.1 NSi8130N/NSi8131N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

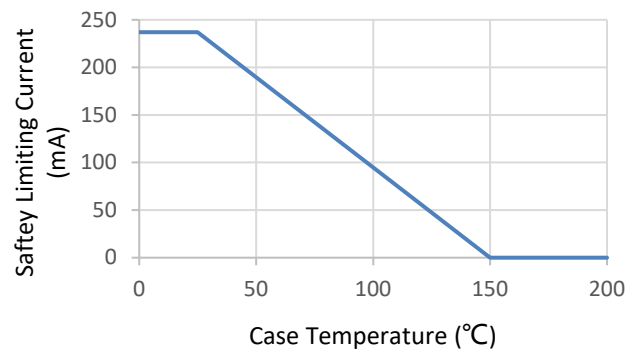


Figure 3.2 NSi8130W/NSi8131W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

3.3. REGULATORY INFORMATION

The NSi8130N/NSi8131N are approved by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01 ²	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V _{rms} Isolation voltage	Single Protection, 3750V _{rms} Isolation voltage	Basic Insulation 565V _{peak} , V _{IOSM} =5384V _{peak}	Basic insulation at 400V _{rms} (565V _{peak})
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

¹ In accordance with UL 1577, each NSi8130N/NSi8131N is proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 sec.

² In accordance with DIN VDE V 0884-11, each NSi8130N/NSi8131N is proof tested by applying an insulation test voltage ≥ 847 V_{peak} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

The NSi8130W/NSi8131W are approved by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01 ²	Certified by CQC11-471543-2012 GB4943.1-2011
Double Protection, 5000V _{rms} Isolation voltage	Double Protection, 5000V _{rms} Isolation voltage	Basic Insulation 849V _{peak} , V _{IOSM} =5384V _{peak}	Basic insulation at 800V _{rms} (1131V _{peak}) Reinforced insulation at 400V _{rms} (565V _{peak})
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

¹ In accordance with UL 1577, each NSi8130W/NSi8131W is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 sec.

² In accordance with DIN VDE V 0884-11, each NSi8130W/NSi8131W is proof tested by applying an insulation test voltage ≥ 1273 V_{peak} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

4.0 FUNCTION DESCRIPTION

The NSi813x is a Triple-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi813x devices are high reliability triple-channel digital isolator with AEC-Q100 qualified. The NSi813x device is safety certified by UL1577 support several insulations withstand voltages (3.75kV_{rms}, 5kV_{rms}), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi813x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi813x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi813x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi813x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 1us after powering up.

Table 4.1 Output status vs. power status

<i>Input</i>	<i>EN_x</i>	<i>VDD1 status</i>	<i>VDD2 status</i>	<i>Output</i>	<i>Comment</i>
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output Disabled, the output is high impedance
X	H or NC	Unready	Ready	L H	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	L	Unready	Ready	Z	Output Disabled, the output is high impedance
X	X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

5.0 APPLICATION NOTE

5.1. PCB LAYOUT

The NSi813x requires a 0.1 μ F bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 to Figure 5.2 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

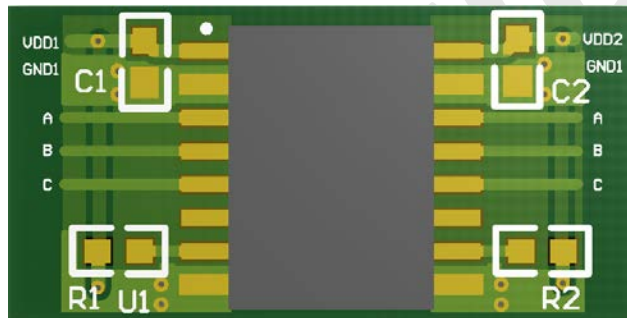


Figure 5.1 Recommended PCB Layout — Top Layer



Figure 5.2 Recommended PCB Layout — Bottom Layer

5.2. HIGH SPEED PERFORMANCE

Figure 5.5 shows the eye diagram of NSi813x at 200Mbps data rate output. The result shows a typical measurement on the NSi813x with 350ps p-p jitter.

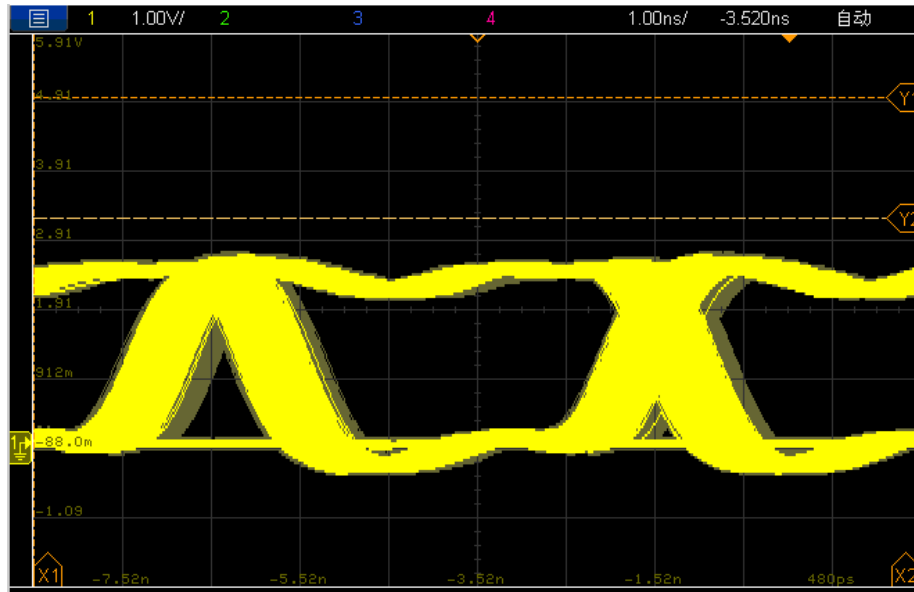


Figure 5.3 NSi813x Eye Diagram

5.3. TYPICAL SUPPLY CURRENT EQUATIONS

The typical supply current of NSi813x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSi8130:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD1 * f * C_L * c1 * 10^{-9}$$

When $a1$ is the channel number of low input at side 1, $b1$ is the channel number of high input at side 1, $c1$ is the channel number of switch signal input at side 1.

NSi8131:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When $b1$ is the channel number of high inputs at side 1, $c1$ is the channel number of switch signal input at side 1, $b2$ is the channel number of high input at side 2, $c2$ is the channel number of switch signal input at side 2.

6.0 PACKAGE INFORMATION

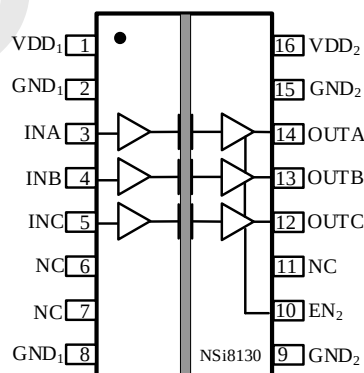


Figure 6.1 NSi8130N Package

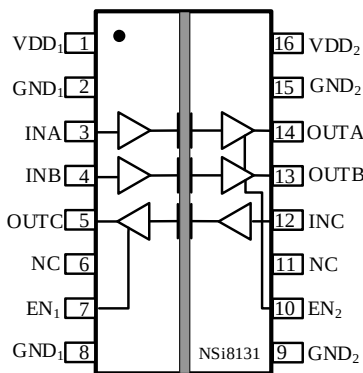


Figure 6.2 NSi8131N Package

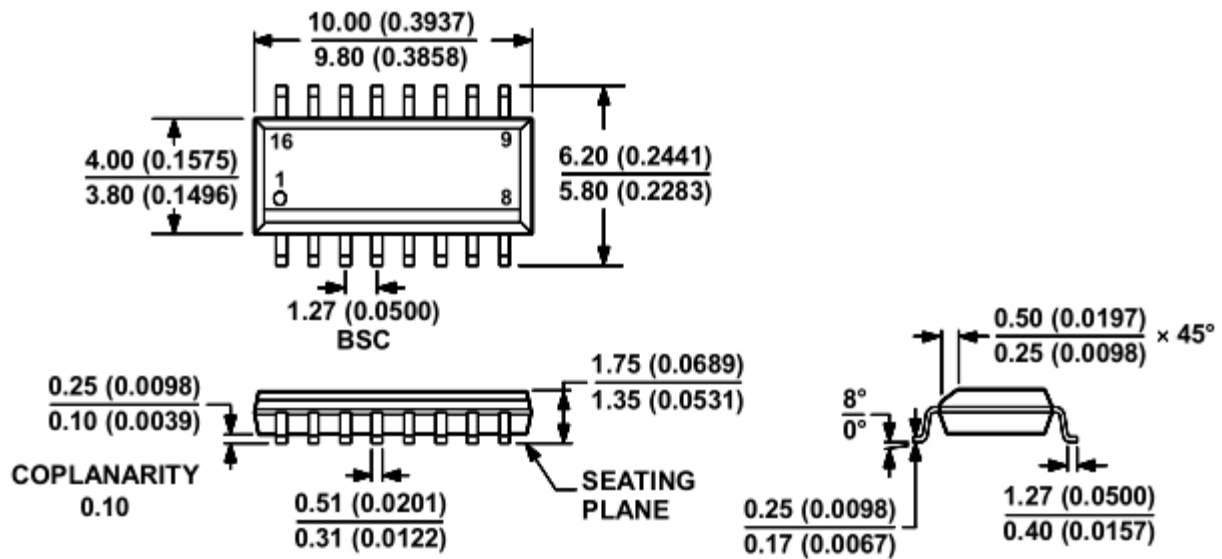


Figure 6.4 NB SOIC16 Package Shape and Dimension in millimeters (inches)

Table6.1 NSi8130N/ NSi8131N Pin Configuration and Description

NSi8130N PIN NO.	NSi8131N PIN NO.	SYMBOL	FUNCTION
1	1	VDD ₁	Power Supply for Isolator Side 1
2	2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	3	INA	Logic Input A
4	4	INB	Logic Input B
5	12	INC	Logic Input C
6	6	NC	No Connection.
7	7	NC/ EN ₁	No Connection. or Output Enable 1. Active high logic input. When EN ₁ is high or NC, the output of Side 1 are enabled. When EN ₁ is low, the output of Side 1 are disabled to high impedance state.
8	8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	10	EN ₂	Output Enable 2. Active high logic input. When EN ₂ is high or NC, the output of Side 2 are enabled. When EN ₂ is low, the output of Side 2 are disabled to high impedance state.
11	11	NC	No Connection.
12	5	OUTC	Logic Output C
13	13	OUTB	Logic Output B
14	14	OUTA	Logic Output A

15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	VDD2	Power Supply for Isolator Side 2

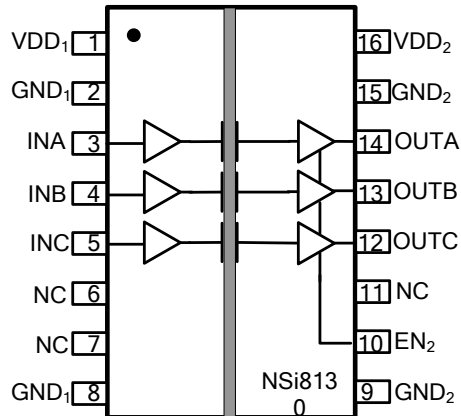


Figure 6.5 NSi8130W Package

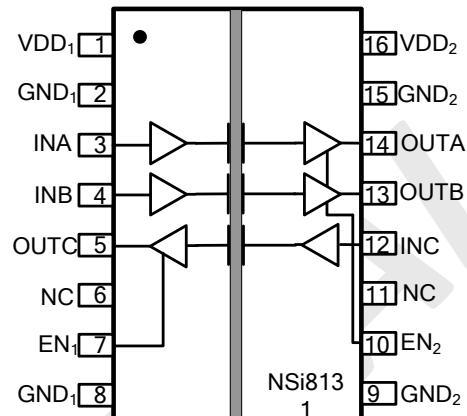


Figure 6.6 NSi8131W Package

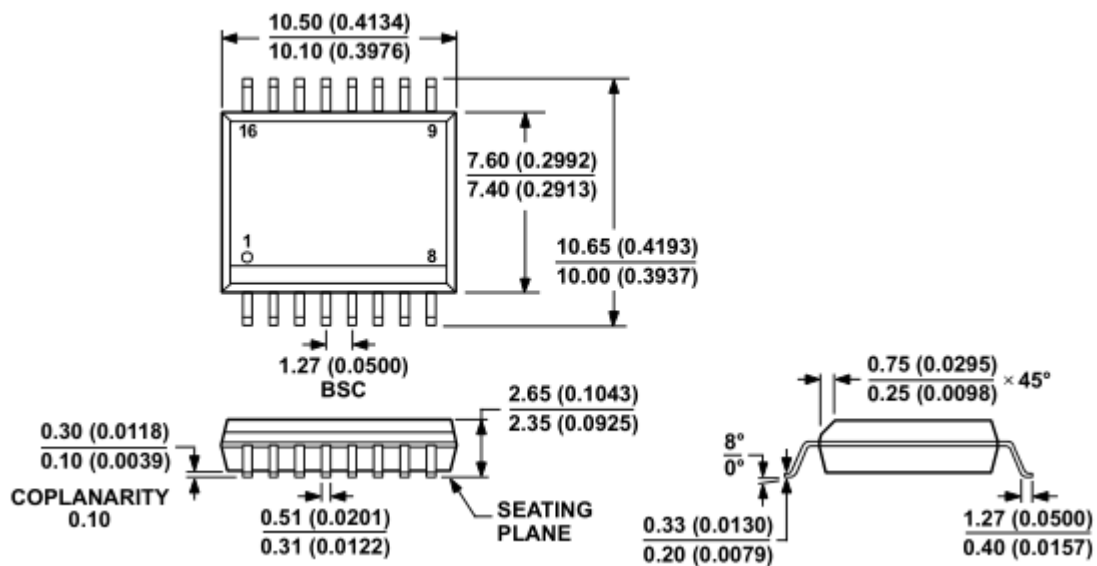


Figure 6.8 WB SOIC16 Package Shape and Dimension in millimeters and (inches)

Table 6.2 NSi8130W/ NSi8131W Pin Configuration and Description

NSi8130W PIN NO.	NSi8131W PIN NO.	SYMBOL	FUNCTION
1	1	VDD ₁	Power Supply for Isolator Side 1
2	2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	3	INA	Logic Input A
4	4	INB	Logic Input B
5	12	INC	Logic Input C

6	6	NC	No Connection.
7	7	NC/ EN ₁	No Connection. or Output Enable 1. Active high logic input. When EN ₁ is high or NC, the output of Side 1 are enabled. When EN ₁ is low, the output of Side 1 are disabled to high impedance state.
8	8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	10	EN ₂	Output Enable 2. Active high logic input. When EN ₂ is high or NC, the output of Side 2 are enabled. When EN ₂ is low, the output of Side 2 are disabled to high impedance state.
11	11	NC	No Connection.
12	5	OUTC	Logic Output C
13	13	OUTB	Logic Output B
14	14	OUTA	Logic Output A
15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	VDD2	Power Supply for Isolator Side 2

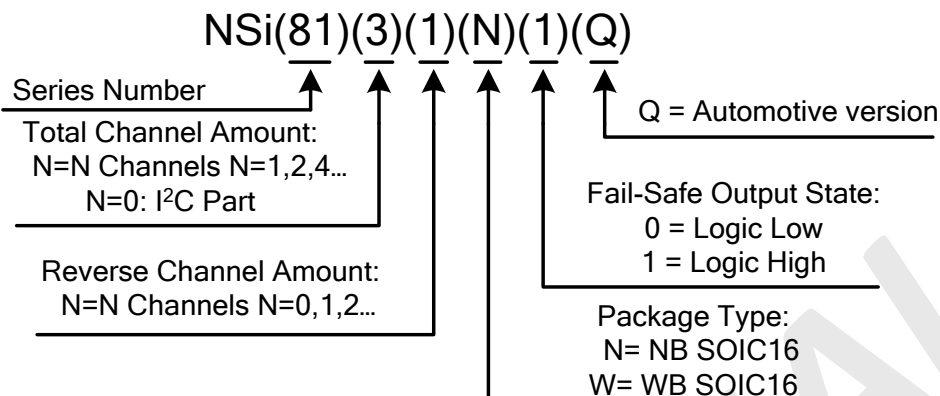
7.0 ORDER INFORMATION

Part No.	Isolation Rating(kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	Automotive	Package
NSi8130N0	3.75	3	0	150	Low	-40 to 125°C	NO	NB SOIC16
NSi8130N1	3.75	3	0	150	High	-40 to 125°C	NO	NB SOIC16
NSi8131N0	3.75	2	1	150	Low	-40 to 125°C	NO	NB SOIC16
NSi8131N1	3.75	2	1	150	High	-40 to 125°C	NO	NB SOIC16
NSi8130W0	5	3	0	150	Low	-40 to 125°C	NO	WB SOIC16
NSi8130W1	5	3	0	150	High	-40 to 125°C	NO	WB SOIC16
NSi8131W0	5	2	1	150	Low	-40 to 125°C	NO	WB SOIC16
NSi8131W1	5	2	1	150	High	-40 to 125°C	NO	WB SOIC16
NSi8130W0 Q	5	3	0	150	Low	-40 to 125°C	YES	WB SOIC16
NSi8130W1 Q	5	3	0	150	High	-40 to 125°C	YES	WB SOIC16
NSi8131W0 Q	5	2	1	150	Low	-40 to 125°C	YES	WB SOIC16
NSi8131W1 Q	5	2	1	150	High	-40 to 125°C	YES	WB SOIC16

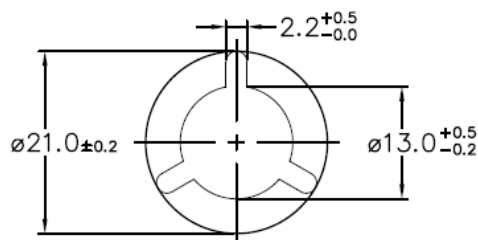
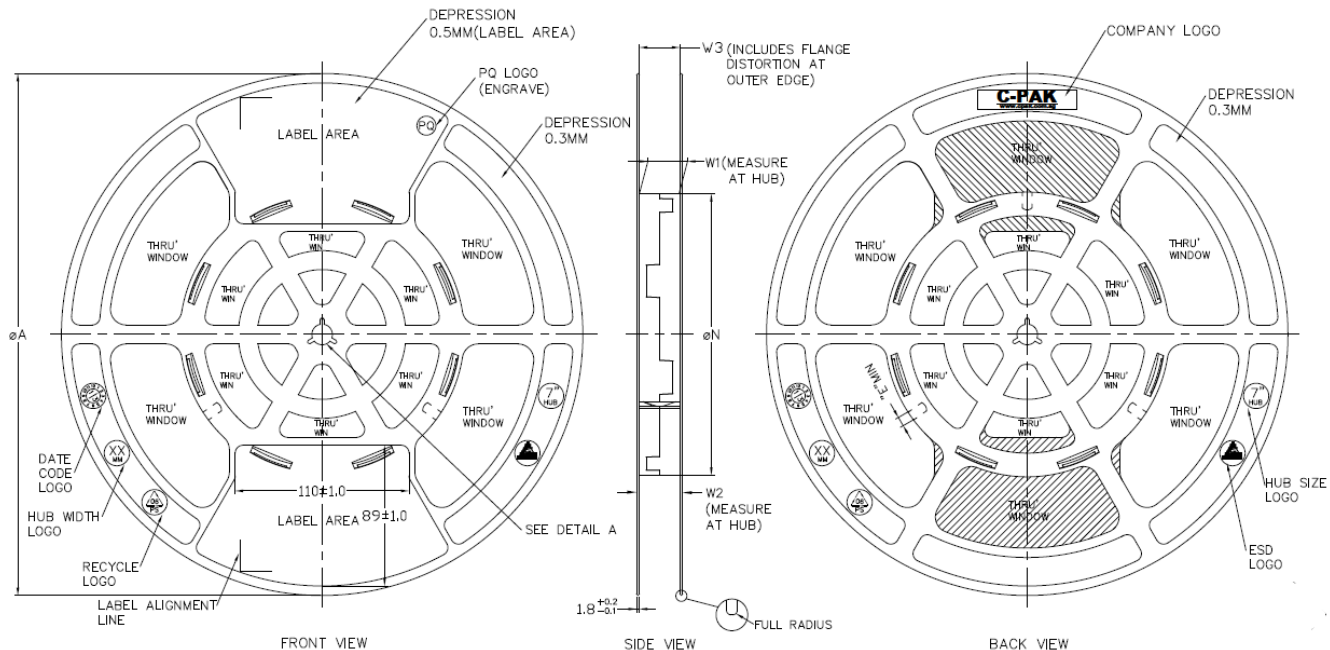
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

All devices are AEC-Q100 qualified.

Part Number Rule:



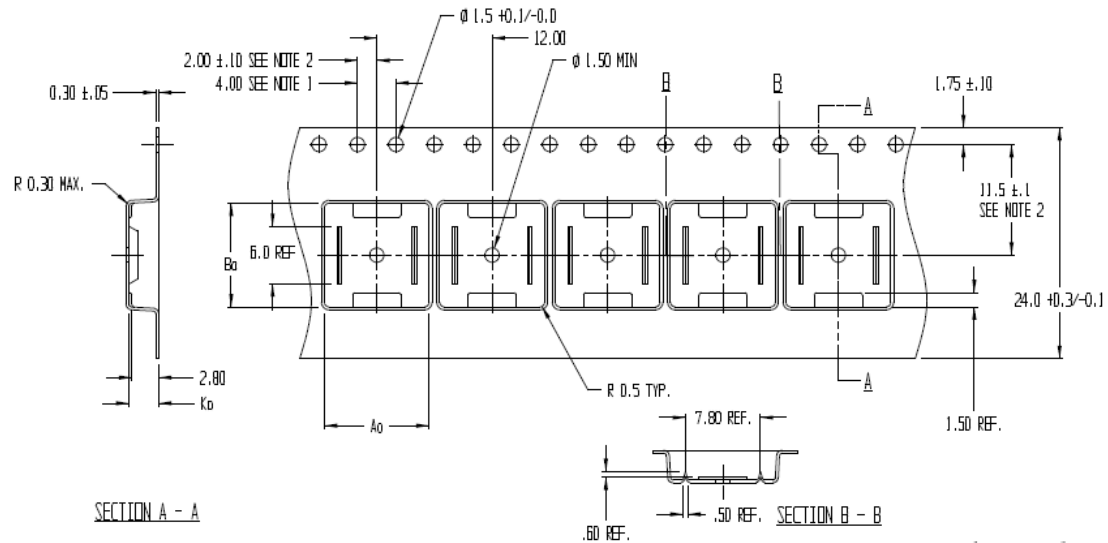
8.0 TAPE AND REEL INFORMATION



ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 ^{+1.5} _{-0.8}	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ^{+2.0} _{-0.8}	18.4		5.5
16MM	330	178	16.4 ^{+2.0} _{-0.8}	22.4		5.5
24MM	330	178	24.4 ^{+2.0} _{-0.8}	30.4		5.5
32MM	330	178	32.4 ^{+2.0} _{-0.8}	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ¹²	ANTISTATIC	ALL TYPES
B	10 ⁸ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁵ & BELOW 10 ⁵	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 ⁹ TO 10 ¹¹	ANTISTATIC (COATED)	ALL TYPES

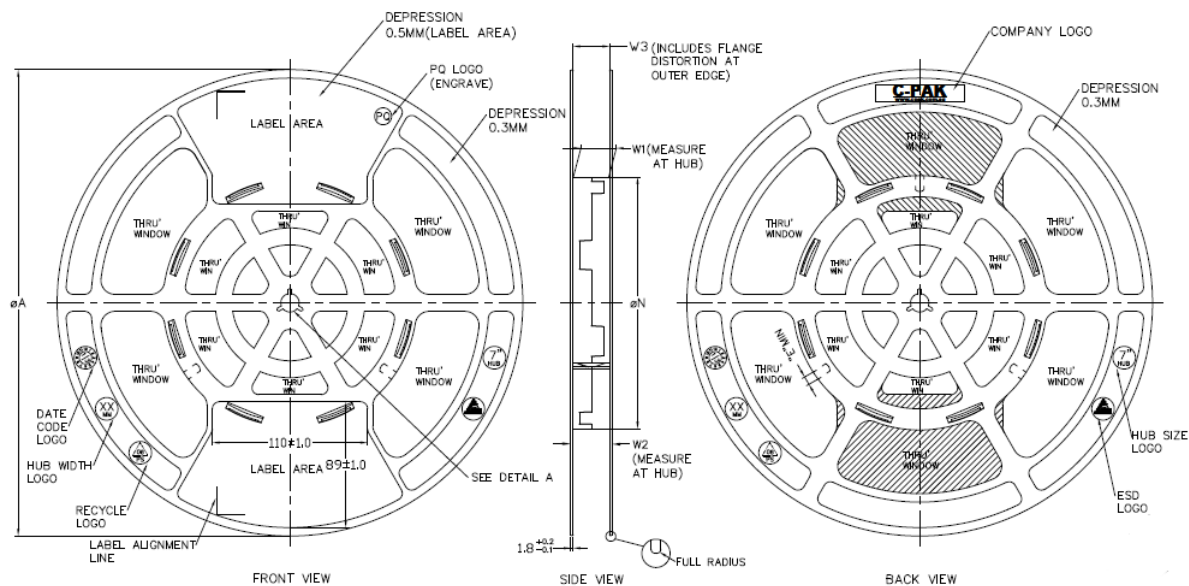


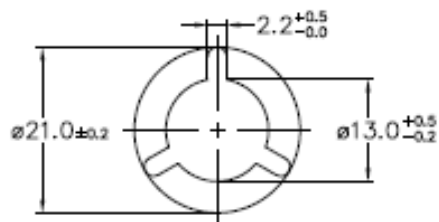
NOTES:

1. TO SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. A_0 AND B_0 ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

$A_0 = 10.90$
 $B_0 = 10.80$
 $K_0 = 3.1$

Figure8.1 Tape and Reel Information of WB SOIC16





ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 ±0.3	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ±0.3	18.4		5.5
16MM	330	178	16.4 ±0.3	22.4		5.5
24MM	330	178	24.4 ±0.3	30.4		5.5
32MM	330	178	32.4 ±0.3	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ⁹	ANTISTATIC	ALL TYPES
B	10 ⁹ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁸ & BELOW 10 ⁹	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 ⁸ TO 10 ¹¹	ANTISTATIC (COATED)	ALL TYPES

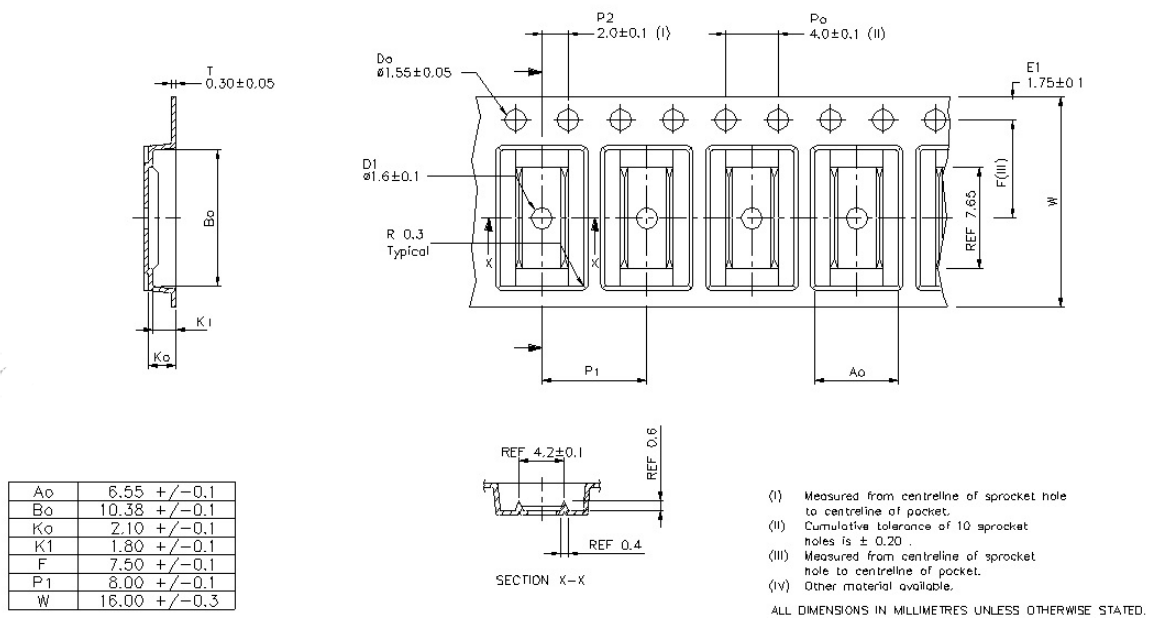


Figure8.2 Tape and Reel Information of NB SOIC16

9.0 REVISION HISTORY

Revision	Description	Date
1.0		2017/11/15
1.1	Change to Ordering information	2017/12/20
1.2	Change Certification Information	2019/06/17