NSi8120D0

Ultra Small Package Dual-Channel Digital Isolators

Datasheet (EN) 1.1

Product Overview

The NSi8120D0 devices are high reliability ultra small package dual-channel digital isolator. The NSi8120D0 device can support 2kVrms insulation withstand voltage while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi8120D0 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi8120D0 device provides the default output low level when the input power is lost. Wide supply voltage of the NSi8120D0 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 2000V_{RMS} Insulation voltage
- Creepage: 2mm
- Date rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 200kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
- Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Low power consumption: 1mA/ch (1 Mbps)
- Low propagation delay: <10ns

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	*Package*	*Body Size*
NSi8120D0	DFN8	3.00mm*2.00mm
NSi8120D0-DDNR	DFN8	3.00mm*2.00mm

Functional Block Diagrams

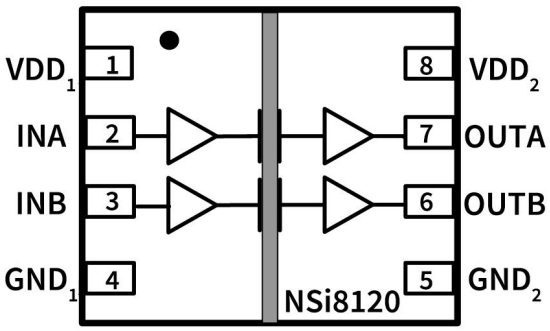

Figure 1. NSi8120D Block Diagram

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1. Pin Configuration and Functions

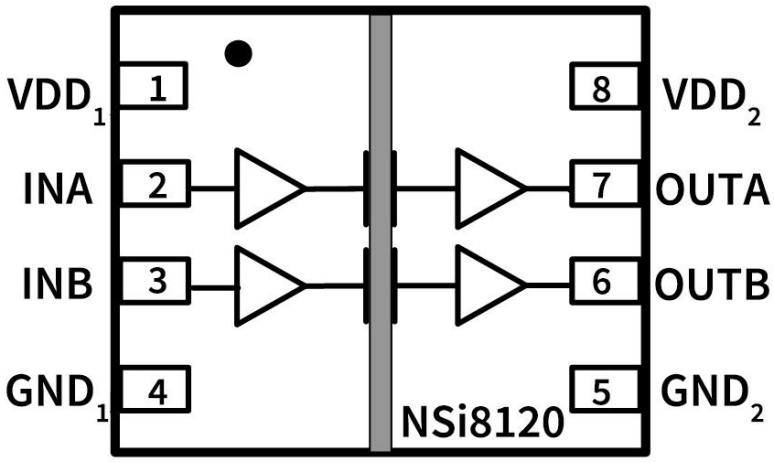


Figure 1.1 NSi8120D0 Package

Table1.1 NSi8120N/ NSi8121N/ NSi8122N Pin Configuration and Description

NSi8120D0 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power Supply for Isolator Side 1
2	INA	Logic Input A
3	INB	Logic Input B
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUTB	Logic Output B
7	OUTA	Logic Output A
8	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters		Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage		VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage		VINA, VINB	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage		V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage		VINA, VINB, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Common-Mode Transients		CMTI			±200	kV/us	
Output current		Io	-15		15	mA	
Maximum Surge Isolation Voltage		V_{IOSM}			5.3	kV	
Operating Temperature		Topr	-40		125	℃	
Junction temperature		Tj			150	℃	
Storage Temperature		Tstg	-65		150	℃	
Electrostatic discharge		HBM			±6000	V	
		CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	Topr	-40		125	℃
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			150	Mbps

4. Thermal Characteristics

Parameters	Symbol	WB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	60.3	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	24.0	°C/W

Junction-to-board thermal resistance	θ_{JB}	29.3	°C/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V_{IT}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	$I_{OH} \le 4mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} \le 4mA$
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	trbs		10		usec	
Common Mode Transient Immunity	CMTI	±150		±200	kV/us	

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.63	0.96	mA	All Input 0V
	I_{DD2}(Q0)		1.30	2.23	mA	
	I_{DD1}(Q1)		2.79	3.93	mA	All Input at supply
	I_{DD2}(Q1)		1.33	2.14	mA	
	I_{DD1}(1M)		1.72	2.42	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.40	2.23	mA	
	I_{DD1}(10M)		1.78	2.49	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.16	3.13	mA	

	I_{DD1}(100M)		2.16	3.52	mA	All Input with 100Mbps, C_L=15pF
	I_{DD2}(100M)		9.60	12.45	mA	

5.3. Supply Current Characteristics –3.3v Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.58	0.89	mA	All Input 0V
	I_{DD2}(Q0)		1.25	2.12	mA	
	I_{DD1}(Q1)		2.74	3.87	mA	All Input at supply
	I_{DD2}(Q1)		1.28	2.08	mA	
	I_{DD1}(1M)		1.67	2.36	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.32	2.12	mA	
	I_{DD1}(10M)		1.72	2.42	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.82	2.71	mA	
	I_{DD1}(100M)		2.08	3.20	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		6.72	9.14	mA	

5.4. Supply Current Characteristics–2.5v Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSi8120**					
	I_{DD1}(Q0)		0.56	0.86	mA	All Input 0V
	I_{DD2}(Q0)		1.23	2.00	mA	
	I_{DD1}(Q1)		2.71	3.84	mA	All Input at supply
	I_{DD2}(Q1)		1.25	2.04	mA	
	I_{DD1}(1M)		1.64	2.33	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.28	2.07	mA	
	I_{DD1}(10M)		1.69	2.38	mA	All Input with 10Mbps, C_L = 15pF
	I_{DD2}(10M)		1.67	2.53	mA	
	I_{DD1}(100M)		2.02	2.93	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.43	7.52	mA	

5.5. Switching Characteristics - 5v Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	6.54	15	ns	See Figure 5.5 , C_L = 15pF
	t_{PHL}	2.5	8.30	15	ns	See Figure 5.5 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.5 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.5 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.6. Switching Characteristics - 3.3v Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	8.0	15	ns	See Figure 5.5 , C_L = 15pF
	t_{PHL}	2.5	8.7	15	ns	See Figure 5.5 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.5 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.5 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.7. Switching Characteristics - 2.5v Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.5 , C_L = 15pF
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.5 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.5 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.5 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.8. Typical Performance Characteristics

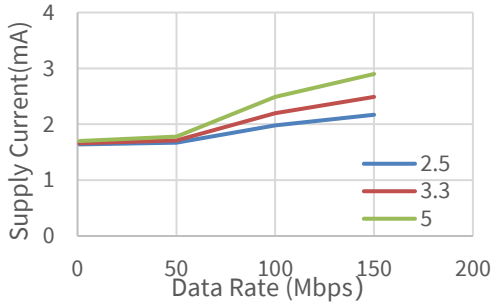


Figure 5.1 NSi8120 VDD1 Supply Current vs Data Rate

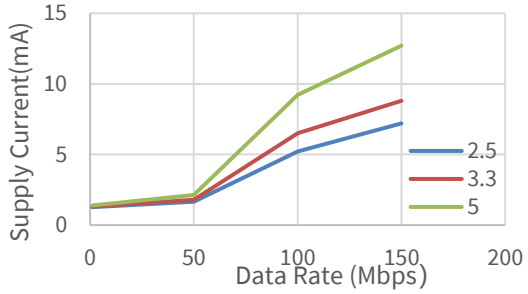


Figure 5.2 NSi8120 VDD2 Supply Current vs Data Rate

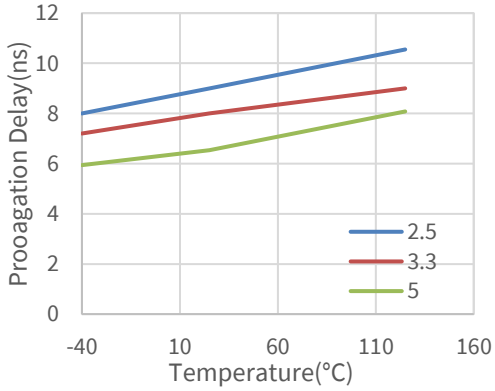


Figure 5.3 Rising Edge Propagation Delay Vs Temp

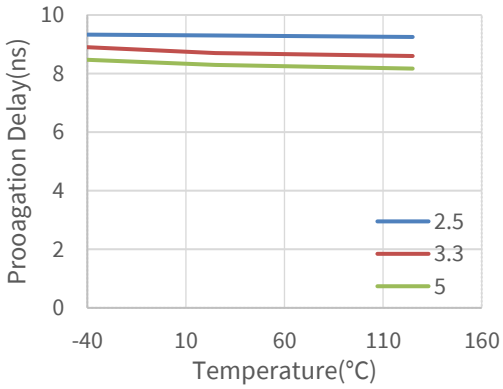


Figure 5.4 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

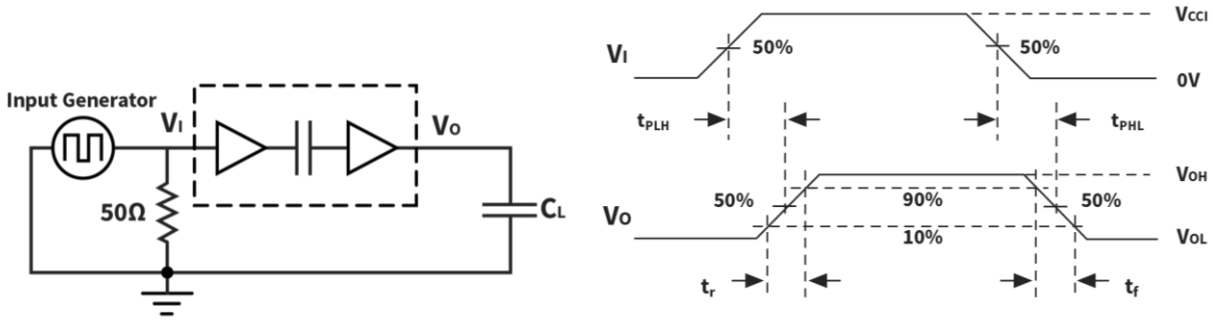


Figure 5.5 Switching Characteristics Test Circuit and Waveform

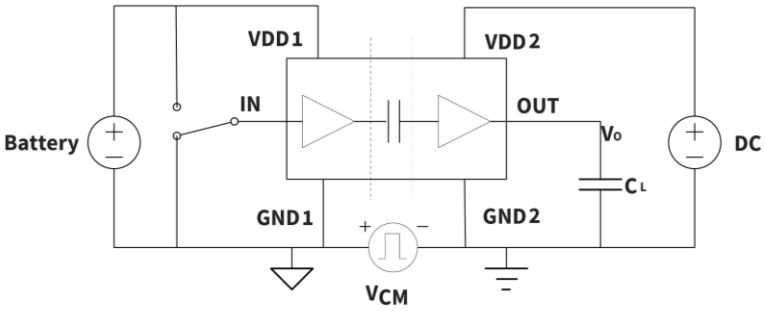


Figure 5.6 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	L(I01)	2.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	2.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	**V**	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		
Isolation Voltage	VISO	2000	Vrms	t = 60 sec

7. Function Description

7.1. Overview

The NSi8120D0 is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi8120 devices are high reliability dual-channel digital isolator with AEC-Q100 qualified. The NSi8120 device can support 2000Vrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi8120 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi8120 device provides the default output high level configuration when the input power is lost. Wide supply voltage of the NSi8120 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi8120 has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 20us after powering up.

Table 7.1 Output status vs. power status

Input	*VDD1 status*	*VDD2 status*	*Output*	*Comment*
H[1]	Ready	Ready	H	Normal operation.
L[2]	Ready	Ready	L	
X[3]	Unready	Ready	L H	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 20us after output side VDD2 is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high				

8. Application Note

8.1. PCB Layout

The NSi822x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be

placed as close as possible to the package. Figure 8.1 to Figure 8.2 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

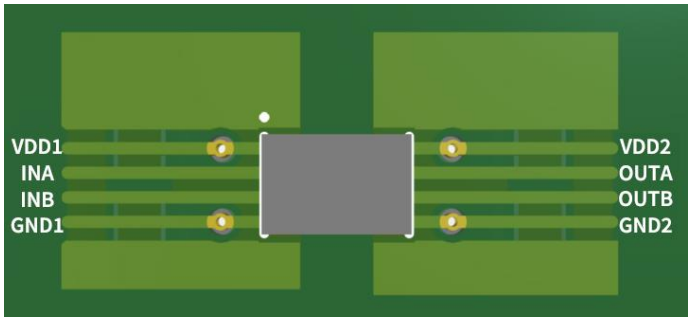


Figure8.1 Recommended PCB Layout — Top Layer

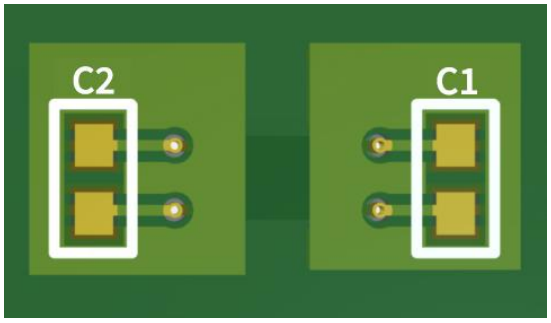


Figure8.2 Recommended PCB Layout — Bottom Layer

8.2. High Speed Performance

Figure 8.3 shows the eye diagram of NSi822x at 200Mbps data rate output. The result shows a typical measurement on the NSi822x with 350ps p-p jitter.

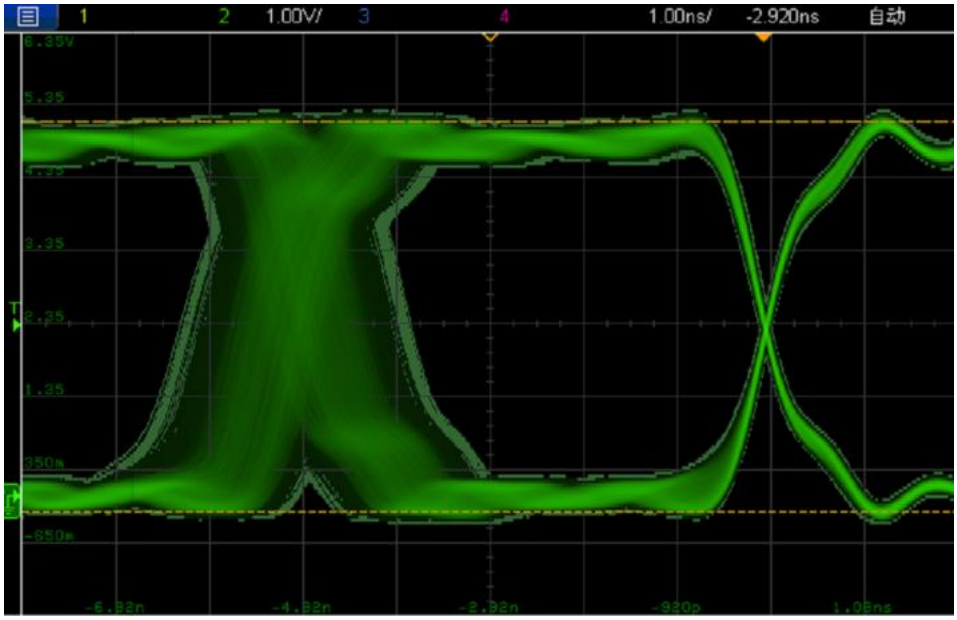


Figure8.3 NSi822x Eye Diagram

8.3. Typical Supply Current Equations

The typical supply current of NSi822x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSi8220:

I_{DD1} = 0.19 *a1+1.45*b1+0.82*c1.

I_{DD2} = 1.36+ VDD1*f* C_L *c1*10^{-9}

When a1 is the channel number of low input at side 1, b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1.

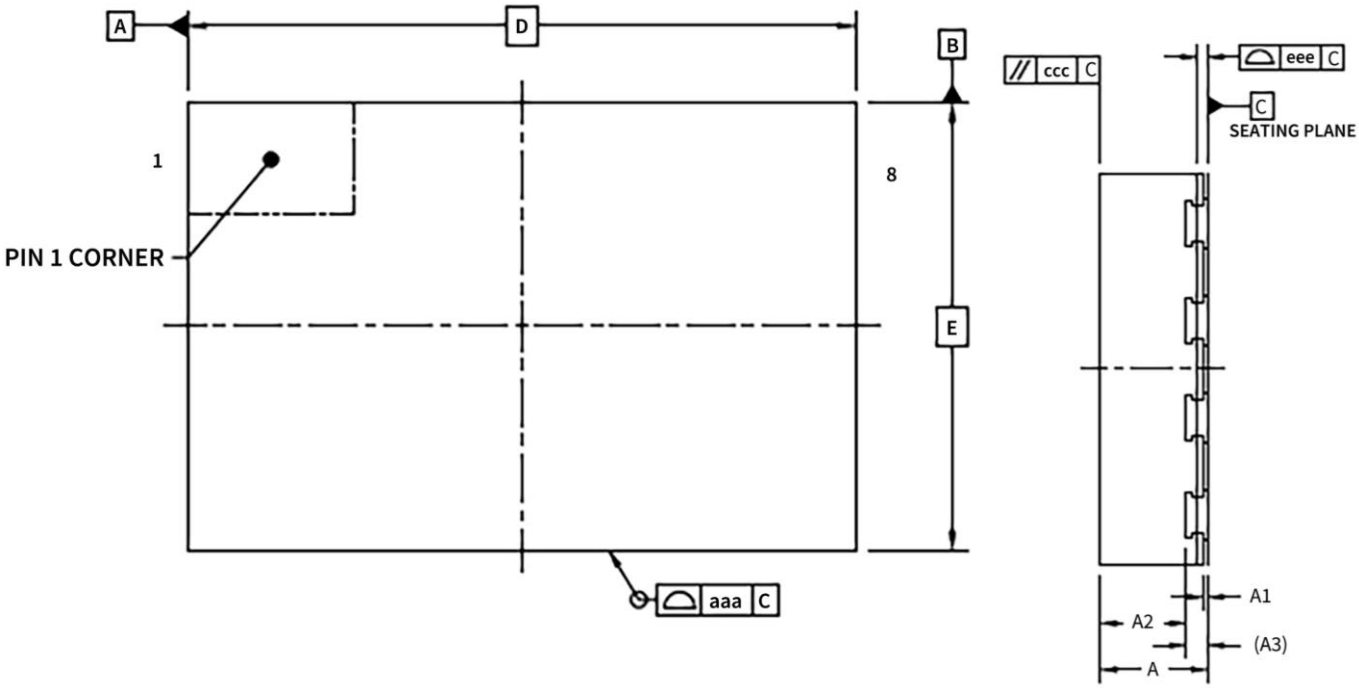
NSi8221/ NSi8222:

I_{DD1} = 0.87 +1.26*b1+0.63*c1+ VDD1*f* C_L *c2*10^{-9}

I_{DD2} = 0.87 +1.26*b2+0.63*c2+ VDD1*f* C_L *c1*10^{-9}

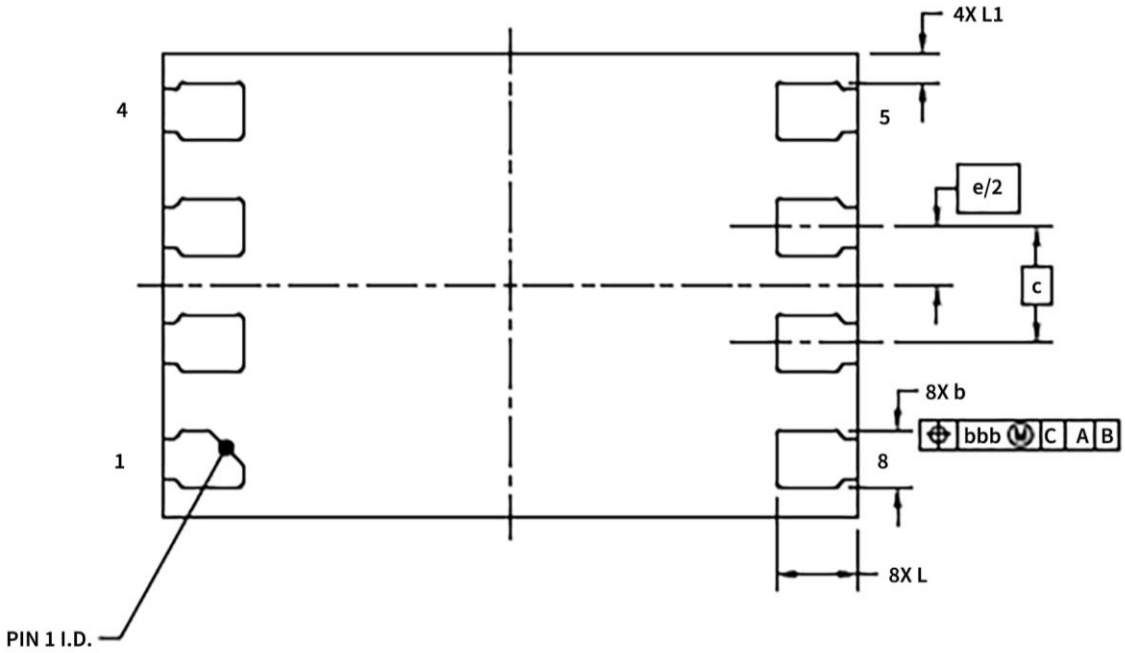
When b1 is the channel number of high input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of high input at side 2, c2 is the channel number of switch signal input at side 2.

9. Package Information



TOP VIEW

SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	-0.004	---	0.046
MOLD THICKNESS		A2	---	0.44	---
L/F THICKNESS		A3		0.11 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		2 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.3	0.35	0.4
LEAD EDGE TO PACKAGE LINE		L1		0.125 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	

Figure 9.1 DFN8 Package Shape and Dimension in millimeters

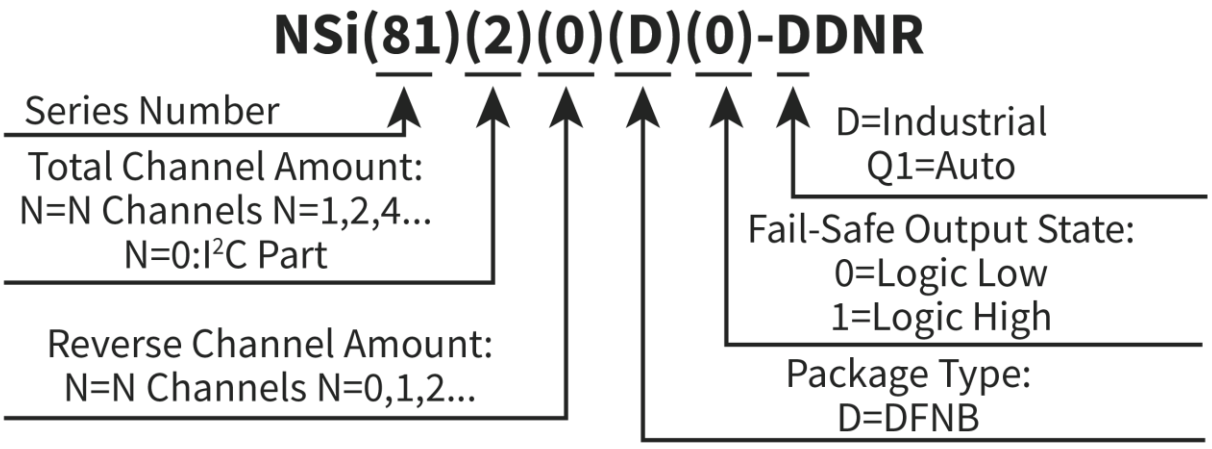
10. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSi8120D0	tbd	tbd	tbd	tbd

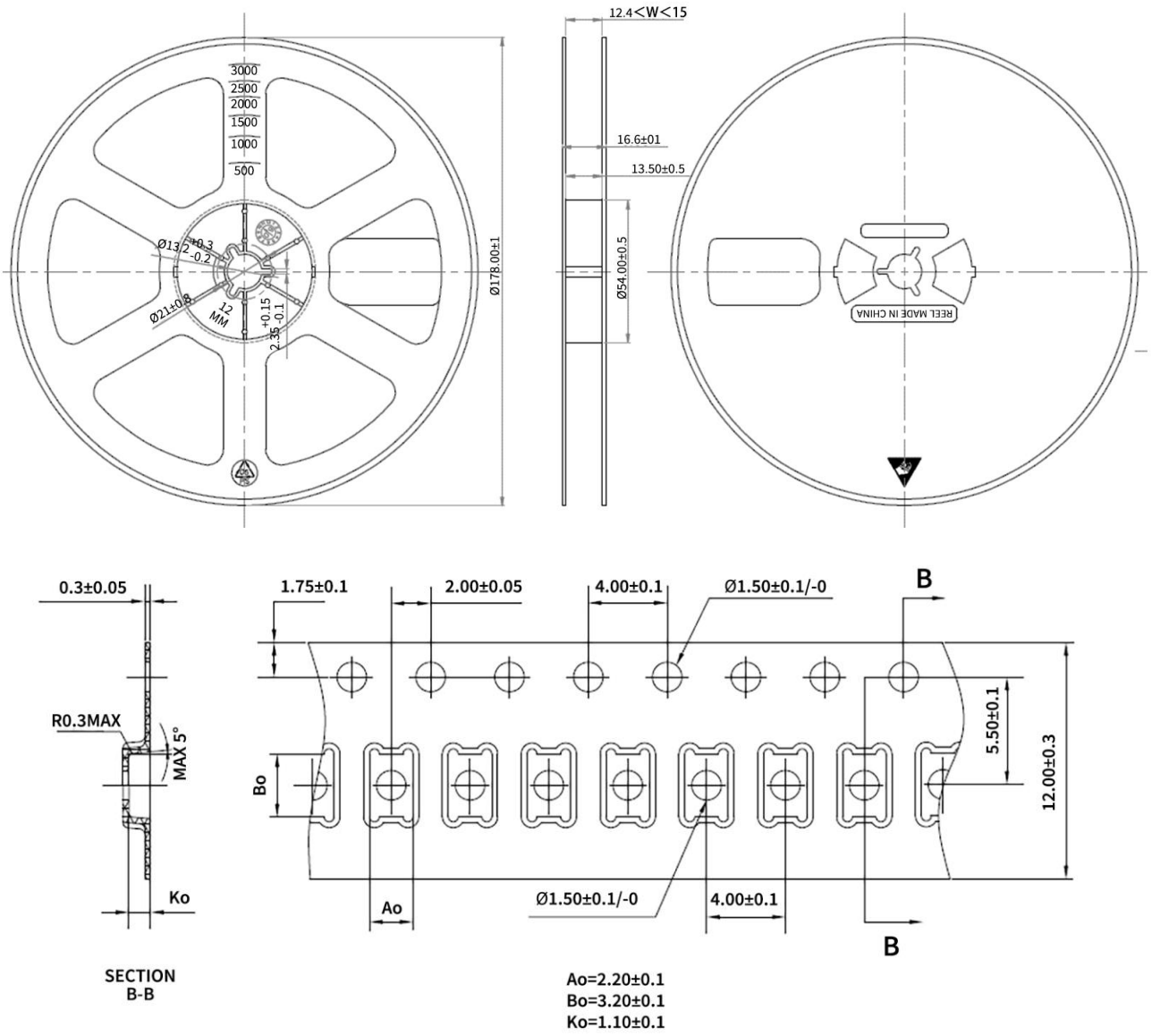
11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSi8120D0-DDNR	2	2	0	150	Low	-40 to 125℃	1	DFN8(2*3)	DFN8	3000
NSi8120D0	2	2	0	150	Low	-40 to 125℃	1	DFN8(2*3)	DFN8	3000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.										

Part Number Rule:



12. Tape and Reel Information



NOTES
1 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE±0.2
2 CAMBER IN COMPLANCE WITH EIA 481
3 POCKET POSITION RELATIVE TOSPROCKET HOLE MEASURED
AS TRUE POSITION OF POOKET,NOT POCKET HOLE

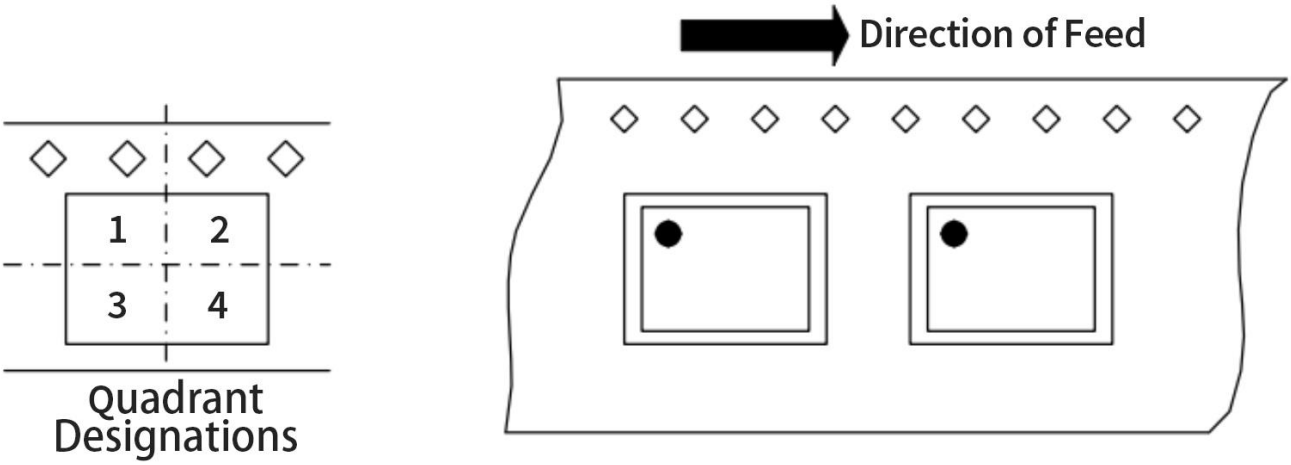


Figure 12.1 Tape and Reel Information of DFN8

13. Revision History

Revision	Description	Date
1.0	Initial version	2020/6/18
1.1	Change Storage Temperature	2021/12/2

IMPORTANT NOTICE

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