NOVOSENSE

NSI72xx
High Reliability Single-Channel and Dual-Channel Opto-Emulator
Datasheet (EN) 1.1

Product Overview

The NSI72xx devices are high speed single-channel and dual channel opto-emulator, it's certified by UL1577 and support 3750/7500V_{rms} insulation withstand voltage. The NSI72xx series operates from both 3.3V and 5V supply voltages with two logic-output options: CMOS output and Open-drain output. The data rate of NSI72xx is up to 15Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/μs. These devices are pin-compatible and replace many traditional optocouplers, allowing enhancement of industrial standard packages without PCB redesign.

Key Features

- Up to 3750V_{rms} Insulation voltage: SOP5, SOP8
- Up to 7500V_{rms} Insulation voltage: SOP8(600mil)
- Data rate: DC to 15Mbps
- Power supply voltage: 2.7V to 5.5V
- High CMTI: 100kV/μs
- Chip level ESD: HBM: ±8kV
- Single or dual diode-emulator input
- Output options:
  NSI7210: CMOS
  NSI7221/ NSI7211: Open-drain
- Low propagation delay: <70ns
- Operation temperature: -40°C ~125°C
- RoHS-compliant packages: SOP5, SOP8, SOP8 (600mil)

Safety Regulatory Approvals

- UL recognition:
  - SOP5: 3750V_{rms} for 1 minute per UL1577
  - SOP8: 3750V_{rms} for 1 minute per UL1577
  - SOP8(600mil): 7500V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A approval IEC60950-1 standard
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Motor Control
- Power supplies
- Isolated line receiver

Device Information

Part Number	Package	Body Size
NSI7210-DSPAR	SOP5	3.60mm × 4.40mm
NSI7210-DSWWAR	SOP8(600mil)	6.25mm × 13.60mm
NSI7211-DSPAR	SOP5	3.60mm × 4.40mm
NSI7211-DSWWAR	SOP8(600mil)	6.25mm × 13.60mm
NSI7211-DSPR	SOP8	4.90mm × 3.90mm
NSI7221-DSPR	SOP8	4.90mm × 3.90mm

Functional Block Diagrams

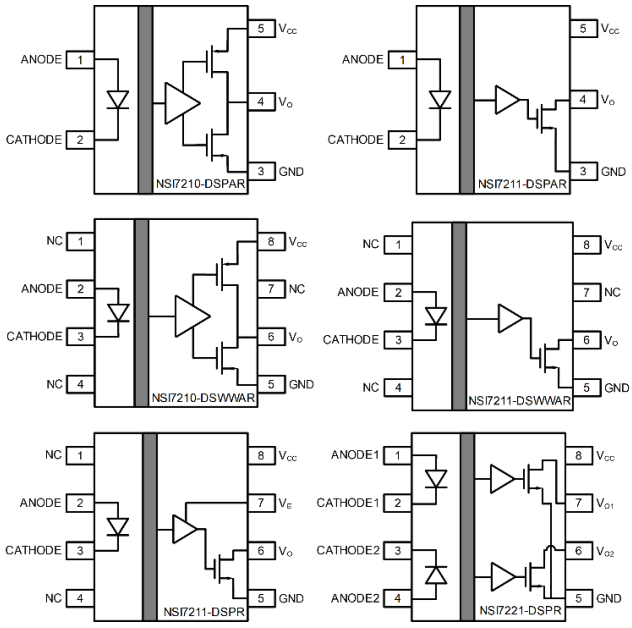

Figure 1. NSI72xx Block Diagram

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1. Pin Configuration and Functions

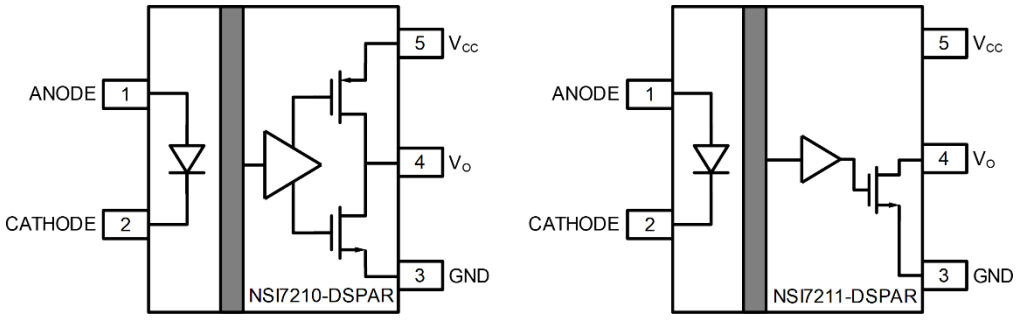


Figure 1.1 NSI721x SOP5 Package

Table 1.1 NSI721x SOP5 Package Pin Configuration and Description

NSI721x SOP5 PIN NO.	SYMBOL	FUNCTION
1	ANODE	Anode connection of diode emulator
2	CATHODE	Cathode connection of diode emulator
3	GND	Ground reference for V_O and V_{CC}
4	V_O	Logic output
5	V_{CC}	Power Supply for output

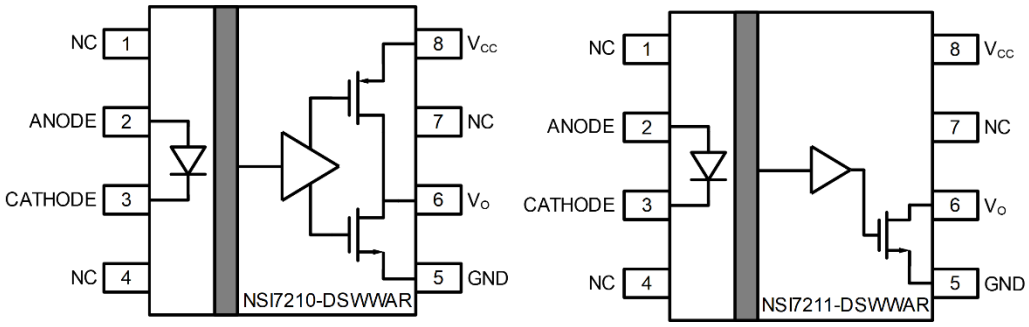


Figure 1.2 NSI721x SOP8(600mil) Package

Table 1.2 NSI721x SOP8(600mil) Package Pin Configuration and Description

NSI721x SOP8(600mil) PIN NO.	SYMBOL	FUNCTION
1	NC	Not connect pin; it has no internal connection
2	ANODE	Anode connection of diode emulator
3	CATHODE	Cathode connection of diode emulator
4	NC	Not connect pin; it has no internal connection
5	GND	Ground reference for V_O and V_{CC}
6	V_O	Logic output

NSI721x SOP8(600mil) PIN NO.	SYMBOL	FUNCTION
7	NC	Not connect pin; it has no internal connection
8	V_{CC}	Power Supply for output

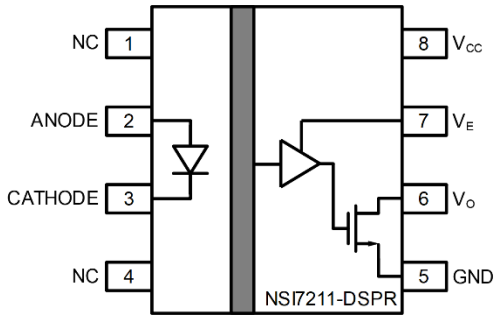


Figure 1.3 NSI7211 SOP8 Package

Table 1.3 NSI7211 SOP8 Package Pin Configuration and Description

NSI7211 SOP8 PIN NO.	SYMBOL	FUNCTION
1	NC	Not connect pin; it has no internal connection
2	ANODE	Anode connection of diode emulator
3	CATHODE	Cathode connection of diode emulator
4	NC	Not connect pin; it has no internal connection
5	GND	Ground reference for V_O and V_{CC}
6	V_O	Logic output
7	V_E	Output Enable. Active high logic input. When EN is high or NC, the output side is enabled. When EN is low, the output side is disabled to high impedance state
8	V_{CC}	Power Supply for output

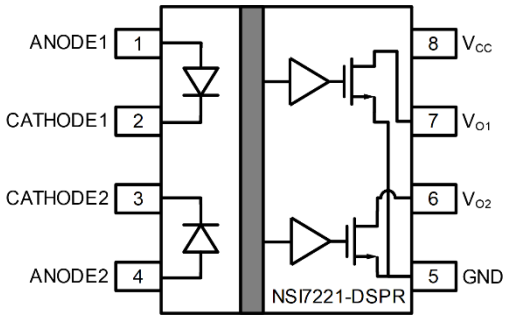


Figure 1.4 NSI7221 SOP8 Package

Table 1.4 NSI7221 SOP8 Pin Configuration and Description

NSI7221 SOP8 PIN NO.	SYMBOL	FUNCTION
1	ANODE1	Anode connection of diode emulator 1
2	CATHODE1	Cathode connection of diode emulator 1
3	CATHODE2	Cathode connection of diode emulator 2
4	ANODE2	Anode connection of diode emulator 2
5	GND	Ground reference for V_{O1}, V_{O2} and V_{CC}
6	V_{O2}	Logic output 2
7	V_{O1}	Logic output 1
8	V_{CC}	Power Supply for output

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	V_{CC}	-0.3		6.5	V	
Output Collector Voltage	V_{OC}	-0.3		VCC+0.5	V	NSI72x1 only
Reverse Input Voltage	V_{R_MAX}	5			V	I_R=10μA
Enable Voltage	V_E	-0.3		VCC+0.5	V	NSI7211-DSPR only
Input forward Current	I_F			25	mA	
Peak Transient Input Current	I_{F_PEAK}			1	A	
Output Collector Current	I_{OC}			50	mA	NSI72x1 only
Output Current	I_O	-15		15	mA	NSI7210 only
Operating Temperature	T_{opr}	-40		125	°C	
Junction Temperature	T_J			150	°C	
Storage Temperature	T_{stg}	-65		125	°C	

3. ESD Ratings (1)

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±2000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	V_{CC}	2.7		5.5	V	
Input ON Forward Current	$I_{F\ (ON)}$	2		20	mA	
Input OFF Forward Current	$I_{F\ (OFF)}$	0		250	μA	
Output Current	I_O	-4		4	mA	NSI7210 only
Logic Low Output Open-Drain Sinking Current	I_{OL} (sinking)			13	mA	NSI7211, NSI7221 only
Enable High Level Input Voltage	V_{EH}	2		V_{CC}	V	NSI7211-DSPR only
Enable Low Level Input Voltage	V_{EL}	0		0.8	V	NSI7211-DSPR only
Data Rate	DR			15	Mbps	I_F ≥6 mA
				10	Mbps	3 mA ≤ I_F ≤ 6 mA
				5	Mbps	2 mA ≤ I_F ≤ 3 mA
Ambient Temperature	T_A	-40		125	°C	

5. Thermal Information

Parameters	Symbol	SOP5	SOP8	SOP8(600mil)	Unit
Junction-to-Air thermal resistance	$R_{\theta JA}$	215.9	137.7	78.9	°C /W
Junction-to-Case(top) thermal resistance	$R_{\theta JC\ (top)}$	125.7	54.9	41.6	°C /W
Junction-to-Board thermal resistance	$R_{\theta JB}$	153.9	71.7	43.6	°C /W

6. Specifications

6.1. Electrical Characteristics

V_{CC}=2.7V to 5.5V, T_A=-40°C to 125°C. Unless otherwise noted, typical values are at **V_{CC} = 3.3V,** T_A = 25°C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Forward Voltage	V_F	1.3	1.7	2	V	I_F=6mA
Input Reverse Current	I_R			10	μA	
Input Threshold Current	I_{TH}	0.6	1	1.4	mA	
Input Current Hysteresis	I_{HYS}		0.1		mA	
Logic High Supply Current	I_{CCH}		0.73	1.2	mA	NSI721x only
			1.38	2	mA	NSI7221 only
Logic Low Supply Current	I_{CCL}		0.74	1.2	mA	NSI721x only
			1.39	2	mA	NSI7221 only
Enable High-level Input Current	I_{EH}		-5.4		μA	NSI7211-DSPR only; V_{CC}=5V, V_E=2V
Enable Low-level Input Current	I_{EL}		-5.8		μA	NSI7211-DSPR only; V_{CC}=5V, V_E=0.5V
Enable Threshold Voltage, rising	V_{EH}			2	V	NSI7211-DSPR only
Enable Threshold Voltage, falling	V_{EL}	0.8			V	NSI7211-DSPR only
Logic High Output Voltage	V_{OH}	V_{CC}-0.3	V_{CC}-0.2		V	NSI7210 only, I_O = -4 mA See Figure 6.20 , C_L = 15pF
Logic Low Output Voltage	V_{OL}		0.19	0.4	V	NSI7210 only, I_F = 6 mA, I_O = 4 mA See Figure 6.20 , C_L = 15pF
			0.46	0.6	V	NSI7211 only, I_F = 6 mA, I_{OL} (sinking)= 13 mA
			0.55	0.7	V	NSI7221 only, I_F = 6 mA, I_{OL} (sinking)= 13 mA See Figure 6.21 , C_L = 15pF
			0.22	0.4	V	NSI7221 only, I_F = 6 mA, I_{OL} (sinking)= 5 mA See Figure 6.21 , C_L = 15pF
Logic High Output Current	I_{OH}			10	μA	NSI72x1 only, V_{OUT} = V_{CC}
Terminal Capacitance	C_I		30		pF	Anode to Cathode capacitance; 1MHz, V_F = 0 V

6.2. Switching Characteristics, NSI7210

V_{CC}=2.7V to 5.5V, T_A=-40°C to 125°C. Unless otherwise noted, I_F=6mA, typical values are at **V_{CC} = 3.3V,** T_A = 25°C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Propagation Delay Time to High Output Level	t_{PLH}		56	70	ns	See Figure 6.18 , C_L = 15pF
Propagation Delay Time to Low Output Level	t_{PHL}		53	70	ns	See Figure 6.18 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	t_{PWD}		3	25	ns	See Figure 6.18 , C_L = 15pF
Rising Time	t_r		2		ns	See Figure 6.18 , C_L = 15pF
Falling Time	t_f		2		ns	See Figure 6.18 , C_L = 15pF
Propagation Delay Difference Between Any Two Parts (t_{pHL}-t_{pLH}) (1)	PDD	-15		15	ns	
Common Mode Transient Immunity	$\lvert CMTI_L \rvert$	100			kV/μs	See Figure 6.23 , I_F=6mA, output=LOW
	$\lvert CMTI_H \rvert$	100			kV/μs	See Figure 6.23 , I_F=0mA, output=HIGH

6.3. Switching Characteristics, NSI7211

V_{CC}=2.7V to 5.5V, T_A=-40°C to 125°C. Unless otherwise noted, pull-up resistor is 390 Ω, I_F=6mA, typical values are at VCC = 3.3V, T_A = 25°C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Propagation Delay Time to High Output Level	t_{PLH}		57	70	ns	See Figure 6.19 , C_L = 15pF
Propagation Delay Time to Low Output Level	t_{PHL}		56	70	ns	See Figure 6.19 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	t_{PWD}		1	25	ns	See Figure 6.19 , C_L = 15pF
Rising Time (10%-90%)	t_r		20		ns	See Figure 6.19 , C_L = 15pF
Falling Time (90%-10%)	t_f		3		ns	See Figure 6.19 , C_L = 15pF
Propagation Delay Difference Between Any Two Parts (t_{pHL}-t_{pLH}) (1)	PDD	-15		15	ns	
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{ELH}		13		ns	V_{EH}=2.5V, NSI7211-DSPR only See Figure 6.22
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{EHL}		13		ns	V_{EH}=2.5V, NSI7211-DSPR only See Figure 6.22
Common Mode Transient Immunity	$\lvert CMTI_L \rvert$	100			kV/μs	See Figure 6.24 , I_F=6mA, output=LOW
	$\lvert CMTI_H \rvert$	100			kV/μs	See Figure 6.24 , I_F=0mA, output=HIGH

6.4. Switching Characteristics, NSI7221

VCC=2.7V to 5.5V, T_A=-40°C to 125°C. Unless otherwise noted, pull-up resistor is 390 Ω, typical values are at I_F=6mA, VCC = 3.3V, T_A = 25°C

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Propagation Delay Time to High Output Level	t_{PLH}		60	70	ns	See Figure 6.19 , C_L = 15pF
Propagation Delay Time to Low Output Level	t_{PHL}		56	70	ns	See Figure 6.19 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	t_{PWD}		4	25	ns	See Figure 6.19 , C_L = 15pF
Rising Time (10%-90%)	t_r		20		ns	See Figure 6.19 , C_L = 15pF
Falling Time (90%-10%)	t_f		3		ns	See Figure 6.19 , C_L = 15pF
Propagation Delay Difference Between Any Two Parts (t_{pHL}-t_{pLH}) (1)	PDD	-15		15	ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			10	ns	
Common Mode Transient Immunity	$\lvert CMTI_L \rvert$	100			kV/μs	See Figure 6.24 , I_F=6mA, output=LOW
	$\lvert CMTI_H \rvert$	100			kV/μs	See Figure 6.24 , I_F=0mA, output=HIGH

6.5. Typical Characteristics

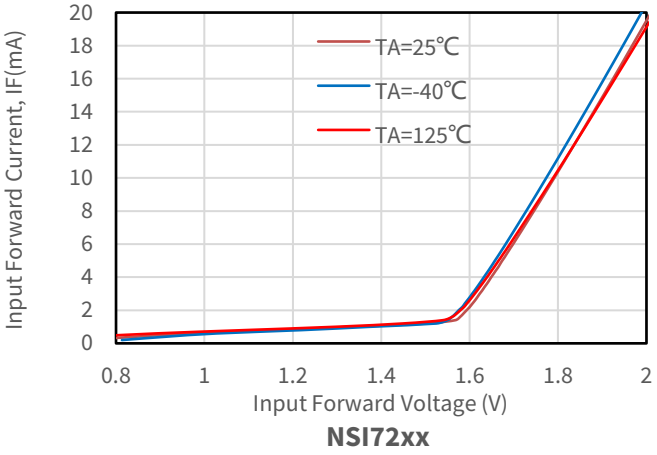


Figure 6.1 Input Forward Current vs Input Forward Voltage

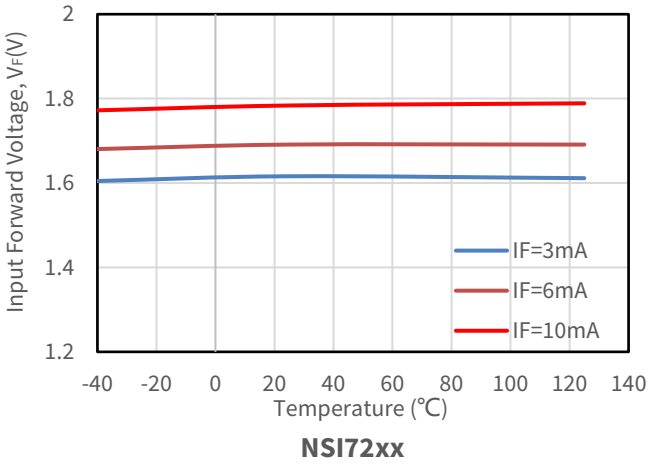


Figure 6.2 Input Forward Voltage vs Ambient Temperature

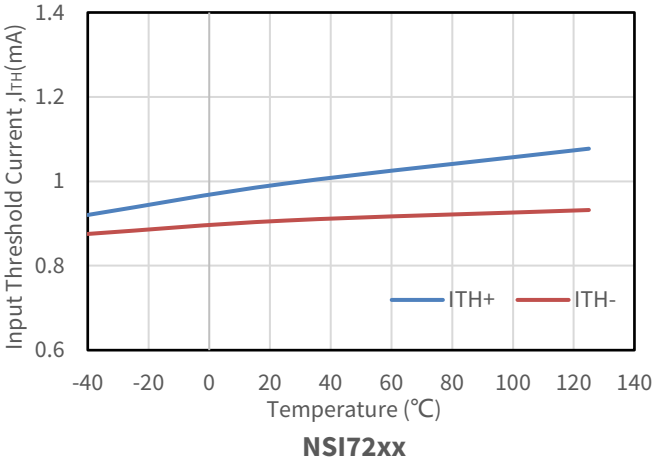


Figure 6.3 Input Threshold Current vs Ambient Temperature [1]

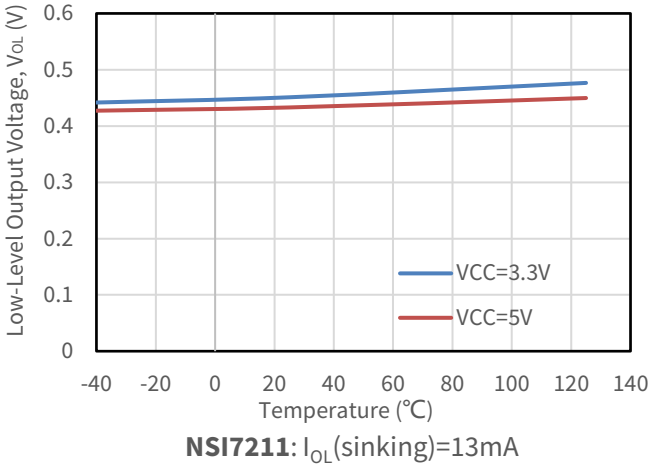


Figure 6.4 Low-Level Output Voltage vs Ambient Temperature

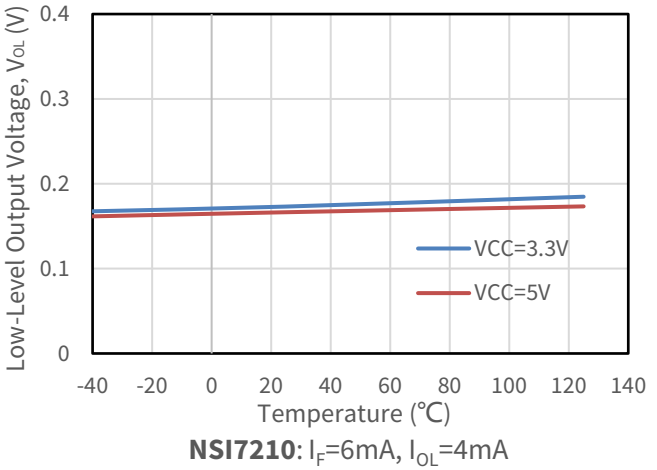


Figure 6.5 Low-Level Output Voltage vs Ambient Temperature

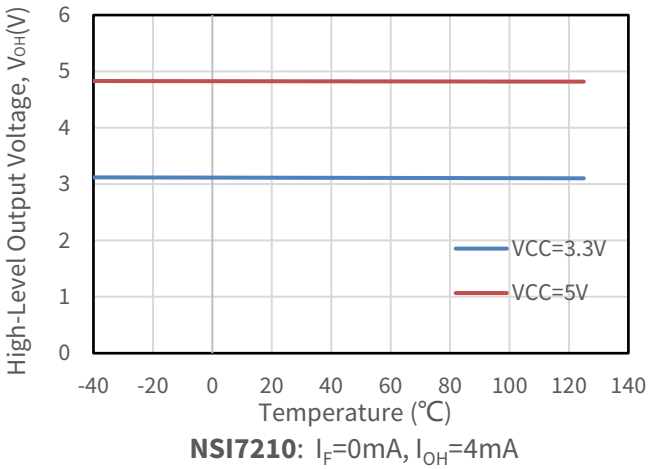
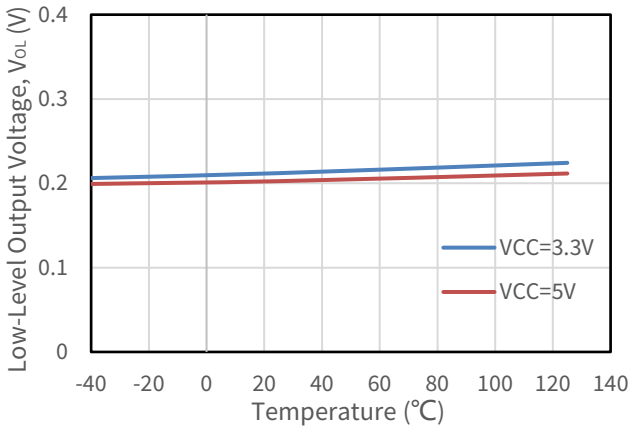
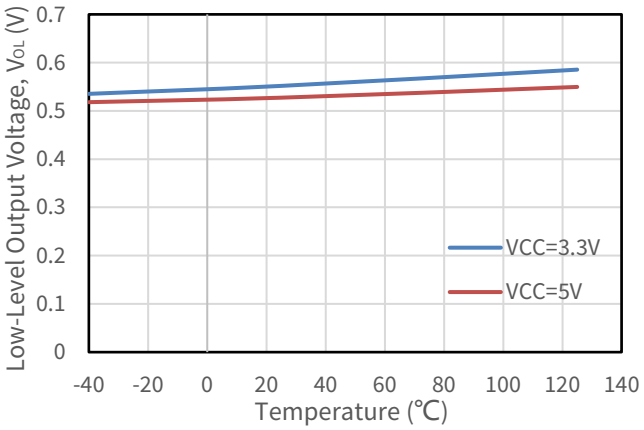


Figure 6.6 High-Level Output Voltage vs Ambient Temperature



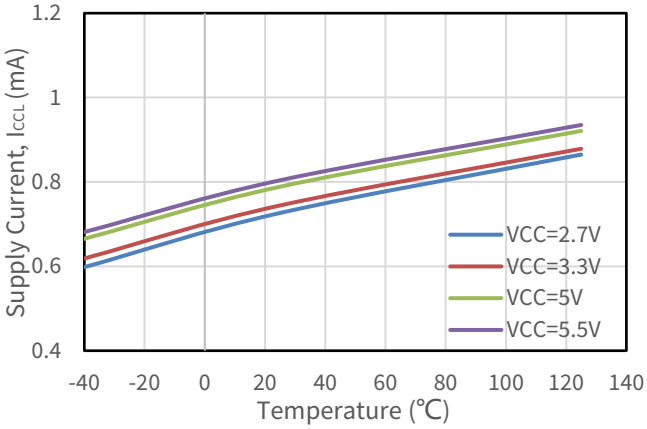
NSI7221: I_F=6mA, I_{OL}=5mA

Figure 6.7 Low-Level Output Voltage vs Ambient Temperature



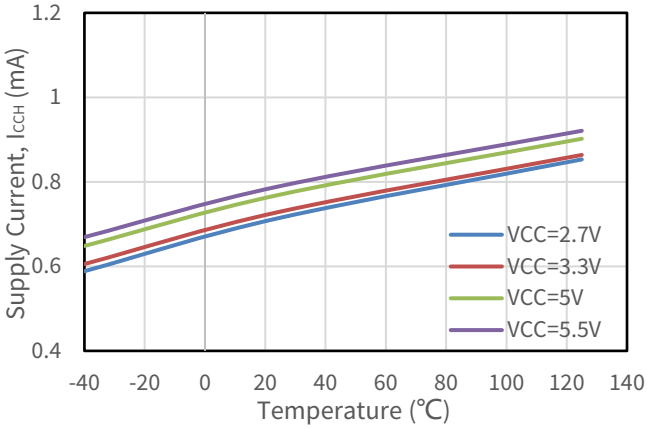
NSI7221: I_F=6mA, I_{OL}=13mA

Figure 6.8 Low-Level Output Voltage vs Ambient Temperature



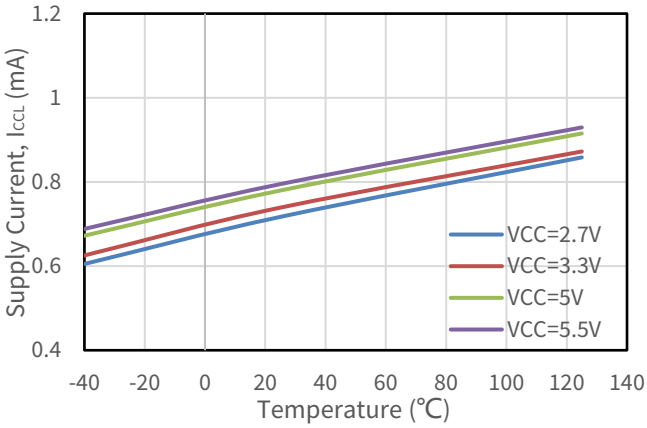
NSI7210: I_F=6mA

Figure 6.9 Logic Low Output Supply Current vs Ambient Temperature



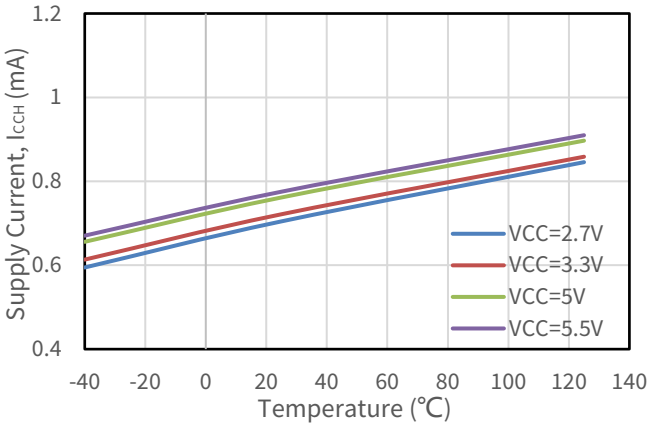
NSI7210: I_F=0mA

Figure 6.10 Logic High Output Supply Current vs Ambient Temperature



NSI7211: I_F=6mA

Figure 6.11 Logic Low Output Supply Current vs Ambient Temperature



NSI7211: I_F=0mA

Figure 6.12 Logic High Output Supply Current vs Ambient Temperature

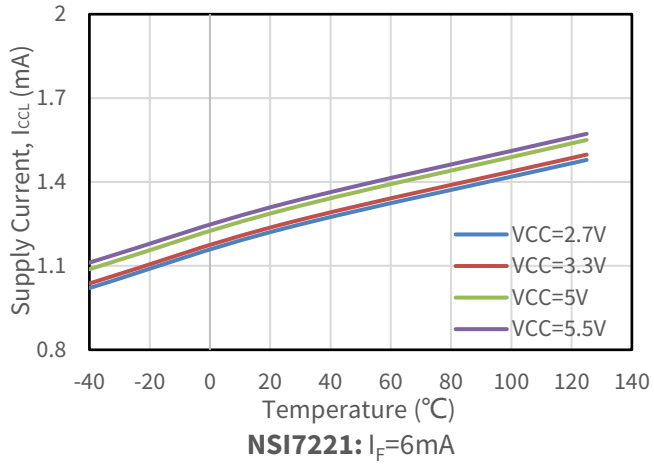


Figure 6.13 Logic Low Output Supply Current vs Ambient Temperature

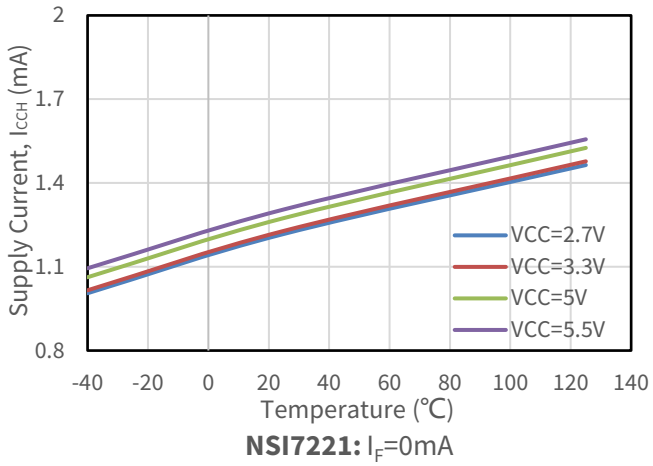


Figure 6.14 Logic Low Output Supply Current vs Ambient Temperature

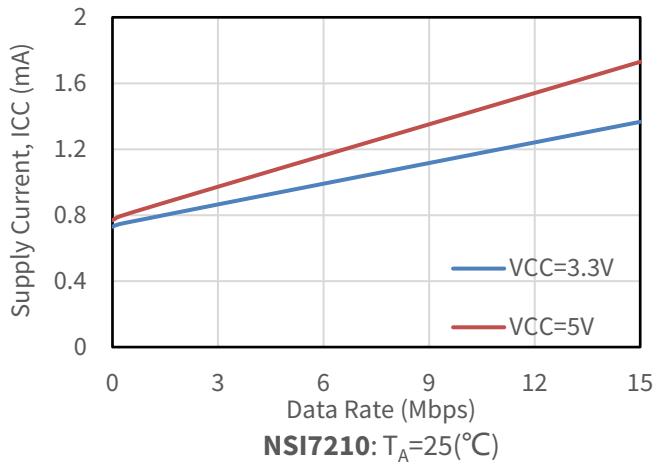


Figure 6.15 Output Supply Current vs Data Rate

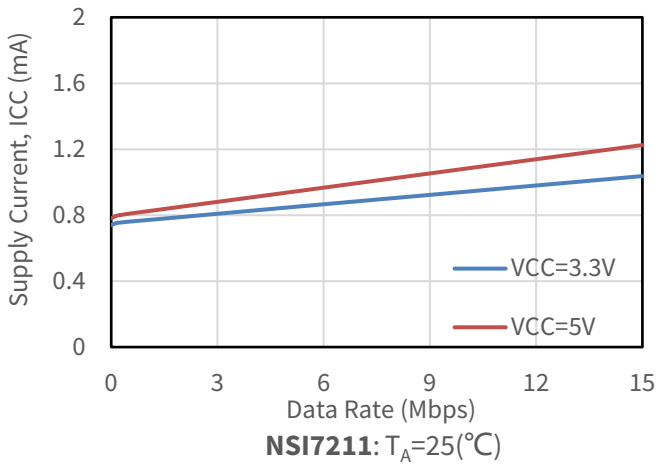


Figure 6.16 Output Supply Current vs Data Rate

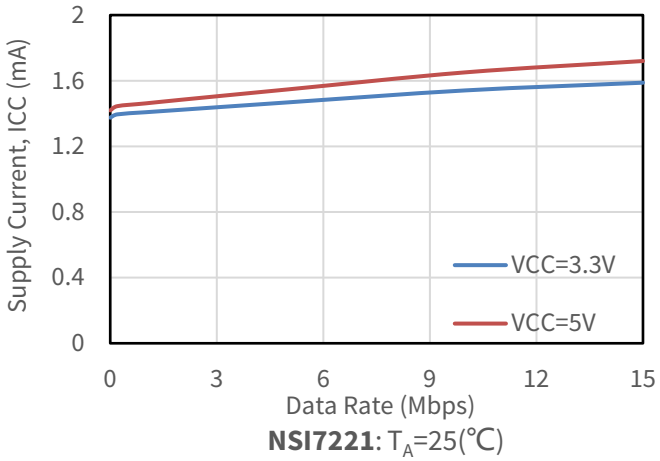
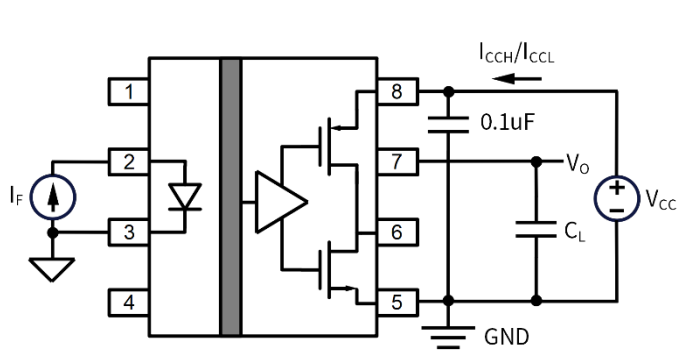


Figure 6.17 Output Supply Current vs Data Rate

[1] ITH+ represents the threshold current when the diode simulator is turned on, and ITH- represents the threshold current when it is turned off.

6.6. Parameter Measurement Information



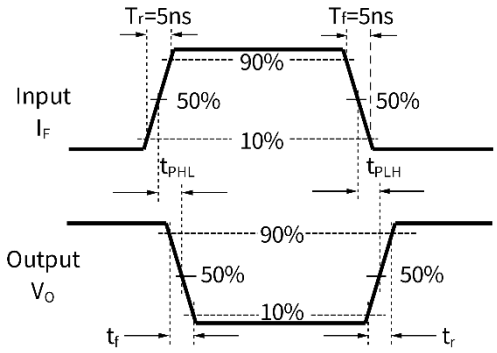
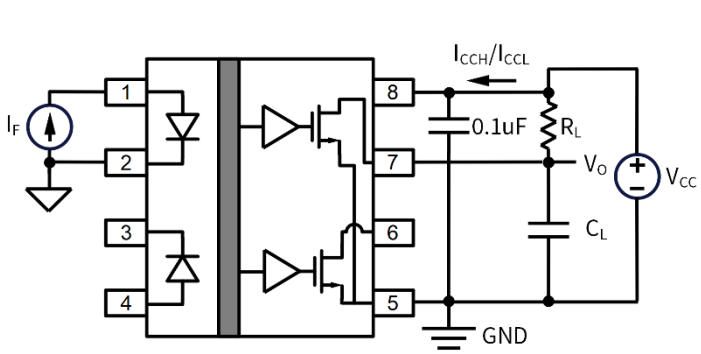


Figure 6.18 Electrical and Switching Characteristics Test Circuit for NSI7210



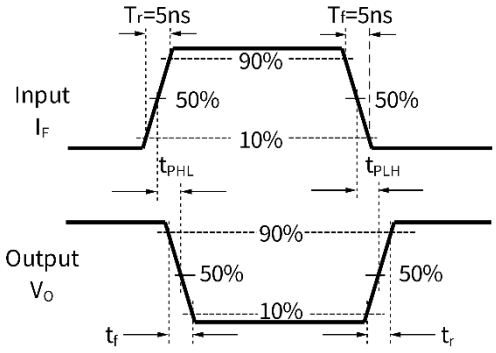


Figure 6.19 Electrical and Switching Characteristics Test Circuit for NSI7221

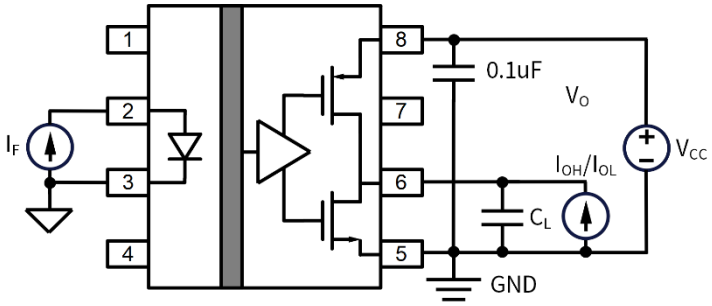


Figure 6.20 V_{OL} and V_{OH} Test Circuit for NSI7210

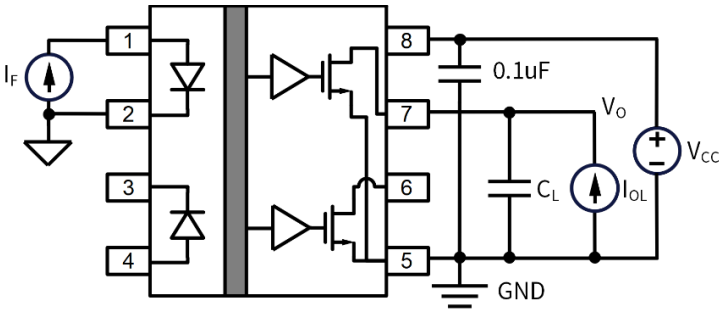


Figure 6.21 V_{OL} Test Circuit for NSI7221

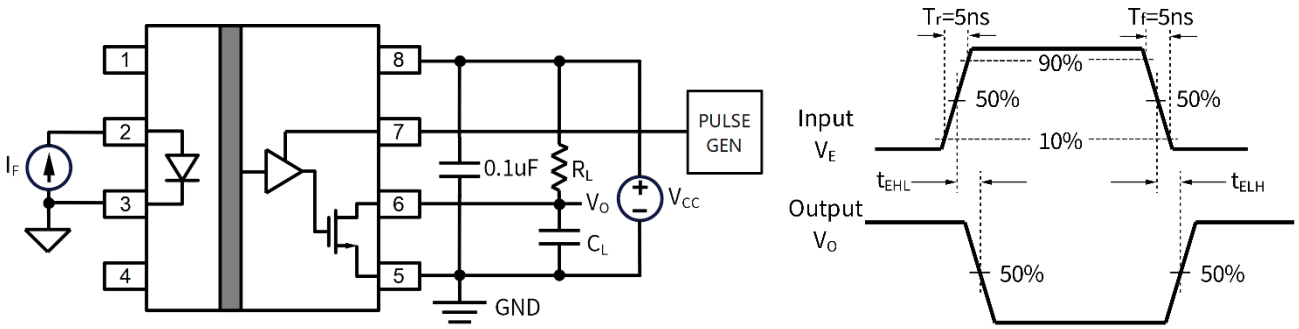


Figure 6.22 Enable Propagation Delay Test Circuit and Waveforms for NSI7211-DSPR

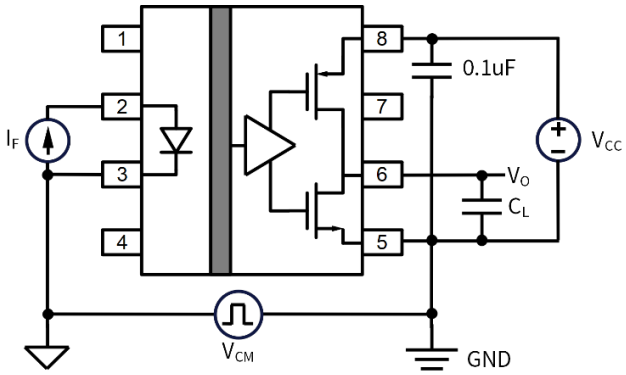


Figure 6.23 Common-Mode Transient Immunity Test Circuit for NSI7210

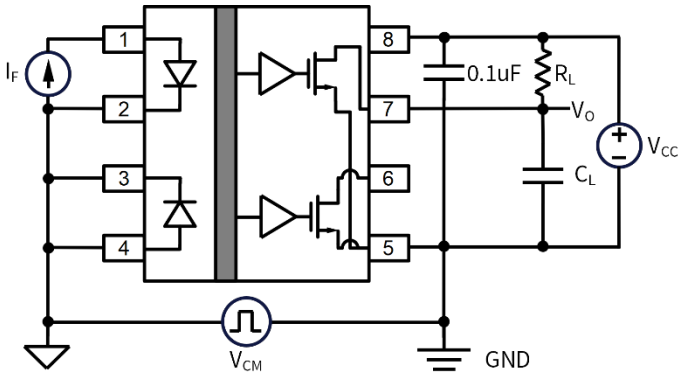


Figure 6.24 Common-Mode Transient Immunity Test Circuit for NSI7221

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value			Unit	Comments
		SOP5	SOP8	SOP8(600mil)		
Minimum External Clearance	CLR	4	4	15	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4	4	15	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	24			μm	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅰ	Ⅰ	Ⅰ		IEC 60664-1

Description	Test Condition	Value		
		SOP5	SOP8	SOP8(600mil)
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150V_{rms}	Ⅰ to IV	Ⅰ to IV	Ⅰ to IV
	For Rated Mains Voltage ≤ 300V_{rms}	Ⅰ to Ⅲ	Ⅰ to Ⅲ	Ⅰ to IV
	For Rated Mains Voltage ≤ 600V_{rms}	/	/	Ⅰ to IV
	For Rated Mains Voltage ≤ 1000V_{rms}	/	/	Ⅰ to Ⅲ
Climatic Classification		40/125/21		
Pollution Degree per DIN VDE 0110,		2		

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value			Unit
			SOP5	SOP8	SOP8(600mil)	
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	400	1500	V_{RMS}
	DC voltage		565	565	2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	565	565	2121	V_{PEAK}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	/	/	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s, $V_{pd(m)}=1.6*V_{IORM}$, t_m=10s					pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, t_{ini}=1s $V_{pd\ (m)}=1.875*V_{IORM}$, t_m=1s （method b1） or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)					pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}=1.2*V_{IORM}$, t_m=10s.	q_{pd}	<5	<5	/	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, t_{ini}=60s, $V_{pd(m)}=1.3*V_{IORM}$, t_m=10s					pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, t_{ini}=1s $V_{pd\ (m)}=1.5*V_{IORM}$, t_m=1s （method b1） or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)					pC
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	5300	5300	12000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	3000	3000	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	6000	6000	10000	V_{PEAK}

Description	Test Condition	Symbol	Value			Unit
Isolation Resistance	V_{IO} =500V, T_A=25°C	R_{IO}	>10^{12}			Ω
	V_{IO} = 500 V, 100 °C ≤ T_A ≤ 125 °C		>10^{11}			Ω
	V_{IO} = 500 V, T_A = T_S		>10^{9}			Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1.2			pF
UL1577						
Withstand Isolation Voltage	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 sec, 100% production test	V_{ISO}	3750	3750	7500	V_{RMS}

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI7210-DSPAR and NSI7211-DSPAR.

Description	Test Condition	Value	Unit
Safety input, output, or total Power	$R_{\theta JA}$ = 215.9 °C/W[1)], T_J = 150 °C, T_A = 25 °C	579	mW
Safety input, output, or supply Current	$R_{\theta JA}$ = 215.9 °C/W[1)], V_I = 5.5V, T_J = 150 °C, T_A = 25 °C	105	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP5 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

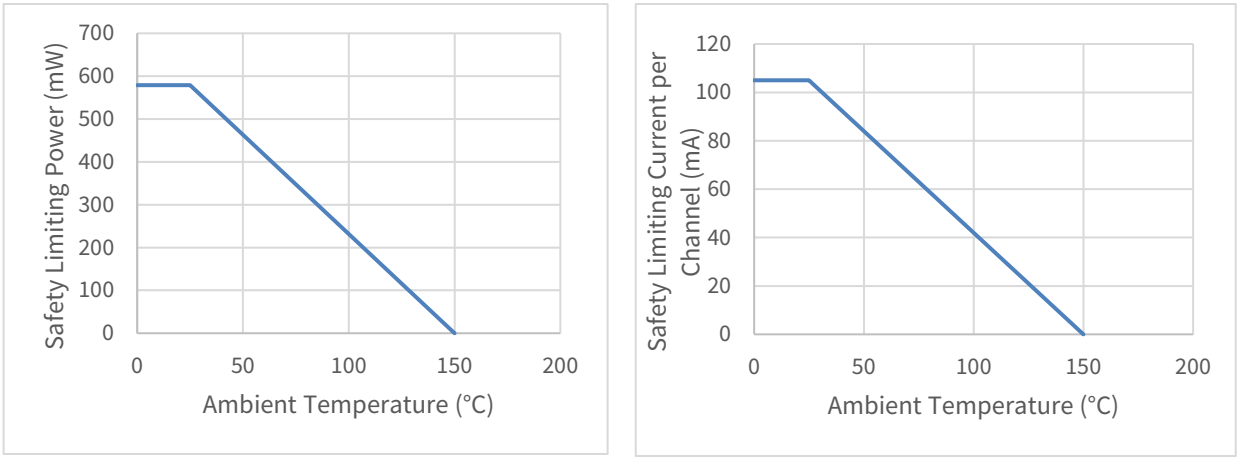


Figure 7.1 NSI7210-DSPAR and NSI7211-DSPAR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI7211-DSPR and NSI7221-DSPR.

Description	Test Condition	Value	Unit
Safety input, output, or total Power	$R_{\theta JA}$ = 137.7 °C/W[1)], T_J = 150 °C, T_A = 25 °C	908	mW
Safety input, output, or supply Current	$R_{\theta JA}$ = 137.7 °C/W[1)], V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	165	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

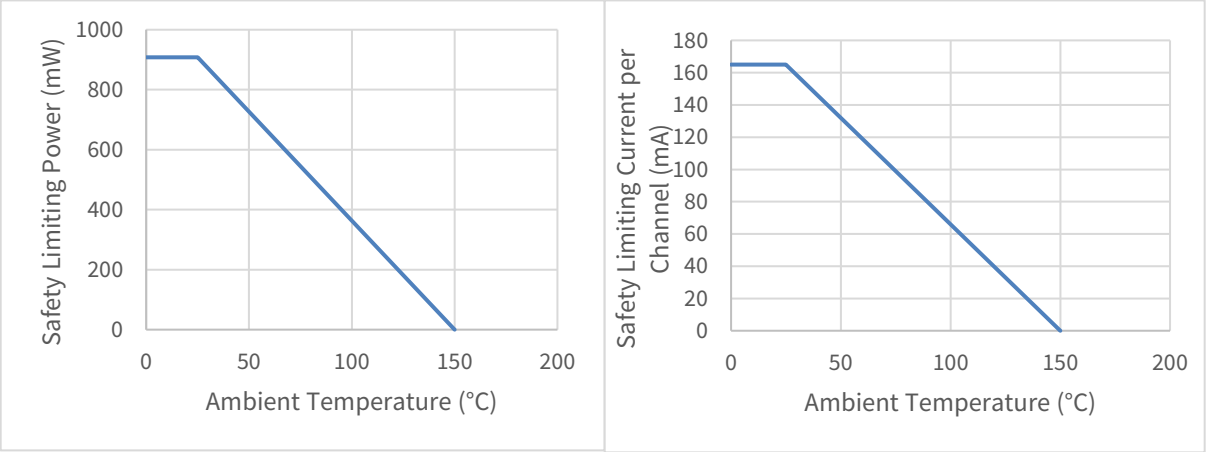


Figure 7.2 NSI7211-DSPR and NSI7221-DSPR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI7210-DSWWAR and NSI7211-DSWWAR.

Description	*Test Condition*	*Value*	*Unit*
Safety input, output, or total Power	$R_{\theta JA}$ = 78.9 °C/W[1)], T_J = 150 °C, T_A = 25 °C	1584	mW
Safety input, output, or supply Current	$R_{\theta JA}$ = 78.9 °C/W[1)], V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	288	mA
Safety Temperature[2)]		150	°C

3) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(600mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

4) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

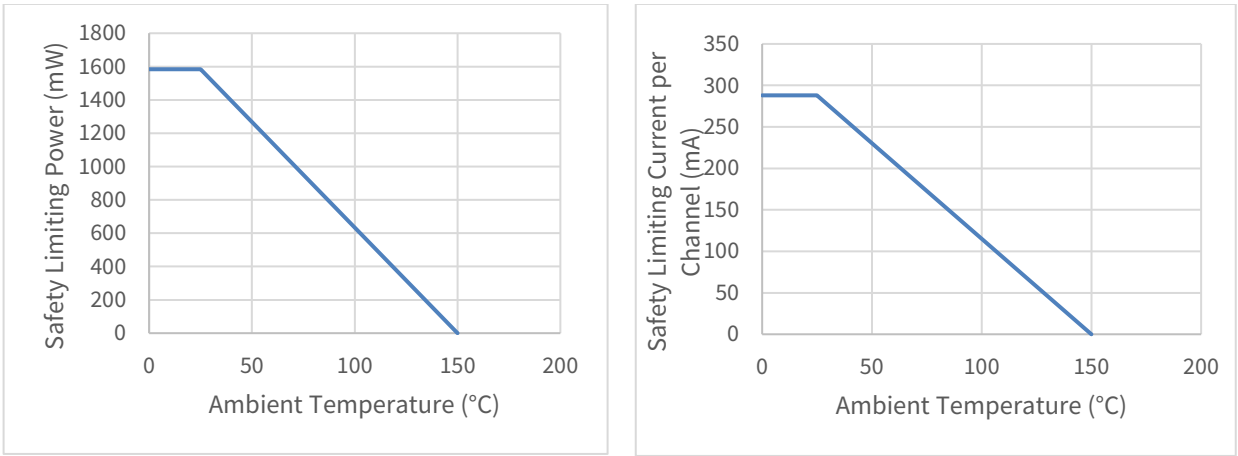


Figure 7.3 NSI7210-DSWWAR and NSI7211-DSWWAR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

7.4. Regulatory Information

The NSI7210-DSPAR and NSI7211-DSPAR are approved or pending approval by the organizations listed in table.

UL		*CQC*	*TUV*	
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to GB4943.1	DIN EN IEC 60747-17 (VDE 0884-17)	Certified According to EN IEC 62368-1
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750Vrms Isolation voltage	Basic insulation	Basic Insulation V_{IORM}=565V_{PEAK} V_{IOTM}=5300V_{PEAK}	Basic Insulation
E500602	E500602	CQC24001426622	R50632636	R50574061

The NSI7211-DSPR and NSI7221-DSPR are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*	*TUV*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation V_{IORM}=565V_{PEAK} V_{IOTM}=5300V_{PEAK} V_{IOSM}=6000V_{PEAK}	Basic insulation	Basic Insulation
E500602	E500602	File (pending)	CQC20001264940	R50574061

The NSI7210-DSWWAR and NSI7211-DSWWAR are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*	*TUV*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 7500V_{rms} Isolation voltage	Single Protection, 7500V_{rms} Isolation voltage	Reinforced Insulation V_{IORM}=2121V_{PEAK} V_{IOTM}=12000V_{PEAK} V_{IOSM}=10000V_{PEAK}	Reinforced insulation	Reinforced Insulation
E500602	E500602	File (pending)	CQC24001426054	R50574061

8. Function Description

8.1. Overview

The NSI72xx devices are high speed and high reliability Single-Channel and Dual-Channel Opto-Emulator. NSI72xx is safety certified by UL1577 support 3.75kVrms and 7.5kVrms insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate is up to 15Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/μs. Wide supply voltage of NSI72xx support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Table 8.1 Output status vs. Power status

V_{CC} status	V_E status	Input Current I_F	Output	Comment
Ready	/	>I_{TH}	L	Only for NSI7210. The output assumes the inverse logic state of the input single.
	/	<I_{TH}	H	
	/	>I_{TH}	L	Only for NSI72x1 with no output enable. The output assumes the inverse logic state of the input single.
	/	<I_{TH}	Z	
	H or NC	>I_{TH}	L	Only for NSI7211-DSPR. The output assumes the inverse logic state of the input single.
	L	>I_{TH}	Z	
	H or NC	<I_{TH}	Z	
	L	<I_{TH}	Z	
Unready		X	Undetermined	When VCC is unready (2), the output is in an undetermined state.
	Note: 1）H=Logic high; L=Logic low; Z= High Impedance, X= Logic low or logic high; 2）The outputs are in an undetermined state when 2 V < VCC < 2.7 V.			

8.2. OOK Modulation

The NSI72xx devices are based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Fig.8.1 & Fig.8.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

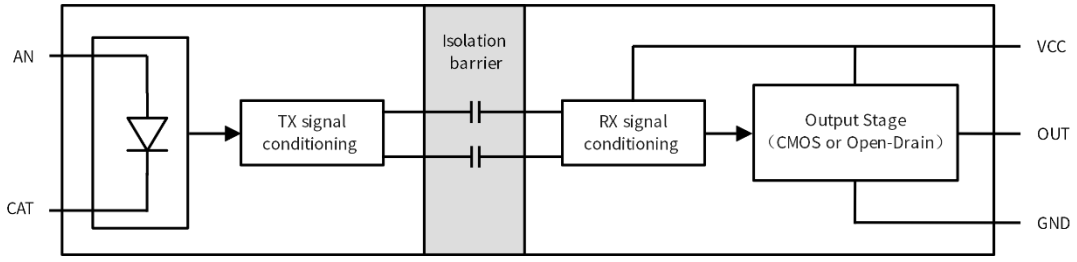


Figure 8.1 Single Channel Function Block Diagram

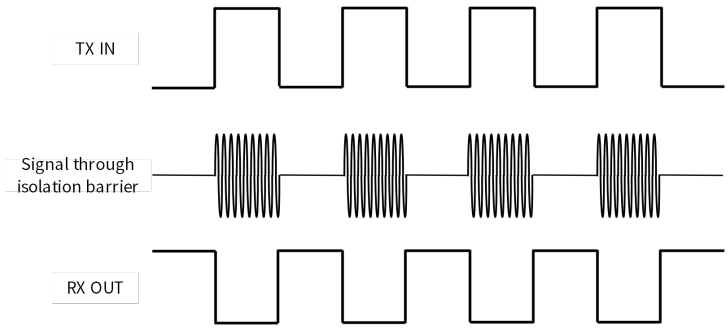


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

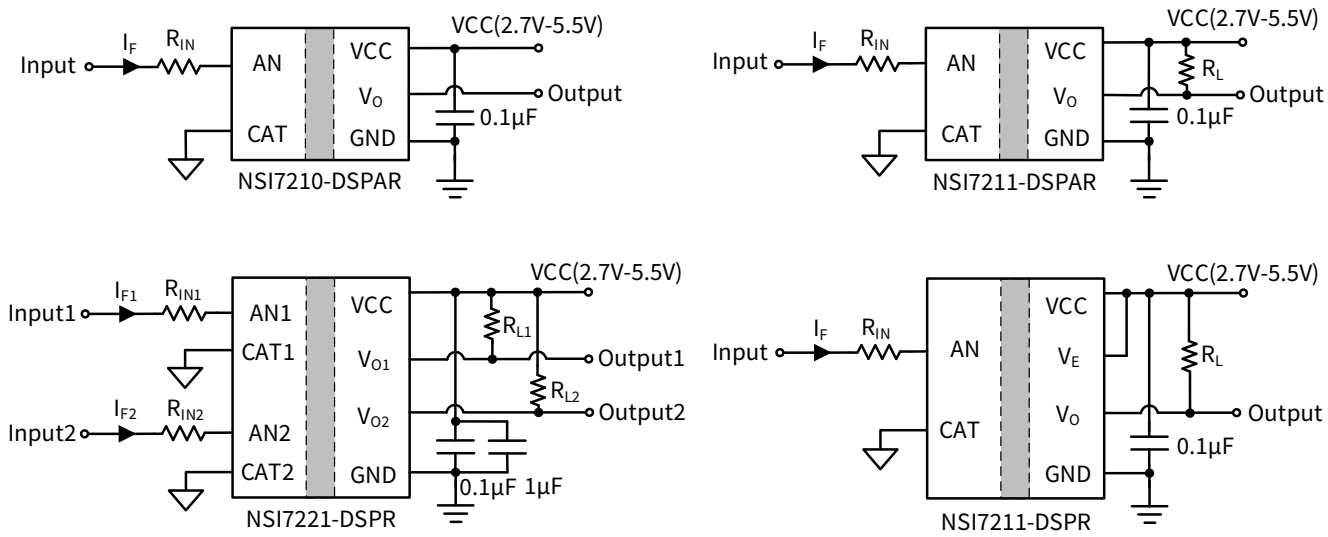


Figure9.1 Simplified Application Circuit

Note: For NSI7221, when Vo and VCC are connected to different power rails, ensure that the power rail voltage amplitude corresponding to Vo is smaller than the power rail voltage amplitude corresponding to VCC. Since there is a clamping diode between V_{O1}/V_{O2} and VCC to enhance the ESD capability of the V_{O1}/V_{O2}. If the voltage difference between Vo and VCC is too large, resulting in the diode conduction, there will be too much reverse current between VCC and V_{O1}/V_{O2}, which will quickly overload the clamping diode and damage it.

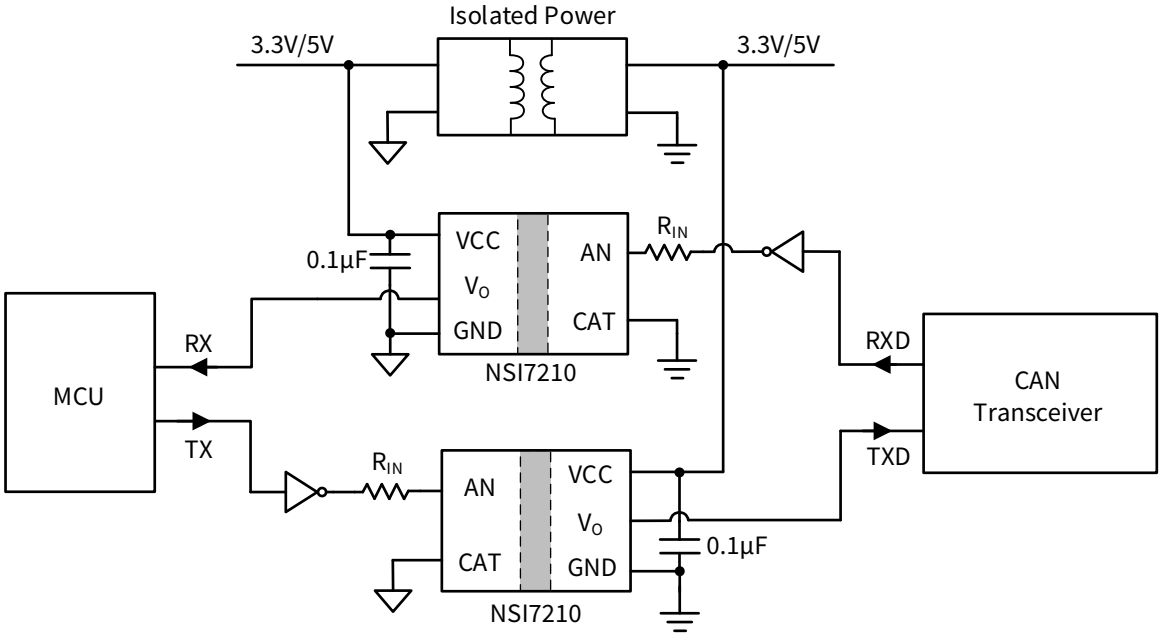


Figure9.2 Typical Isolated CAN Application

9.2. PCB Layout

NSI72xx requires a 0.1 μF bypass capacitor between VCC and GND. The capacitor should be placed as close as possible to the package. Figure 9.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via.

When the device operates in environments with high-frequency noise interference, it is recommended to use two parallel-connected low-ESR bypass capacitors (e.g., 0.1μF+1μF) on the VCC supply pin for high-frequency noise suppression across different bands. Ceramic capacitors with X5R or X7R dielectric grades are preferred for optimal performance.

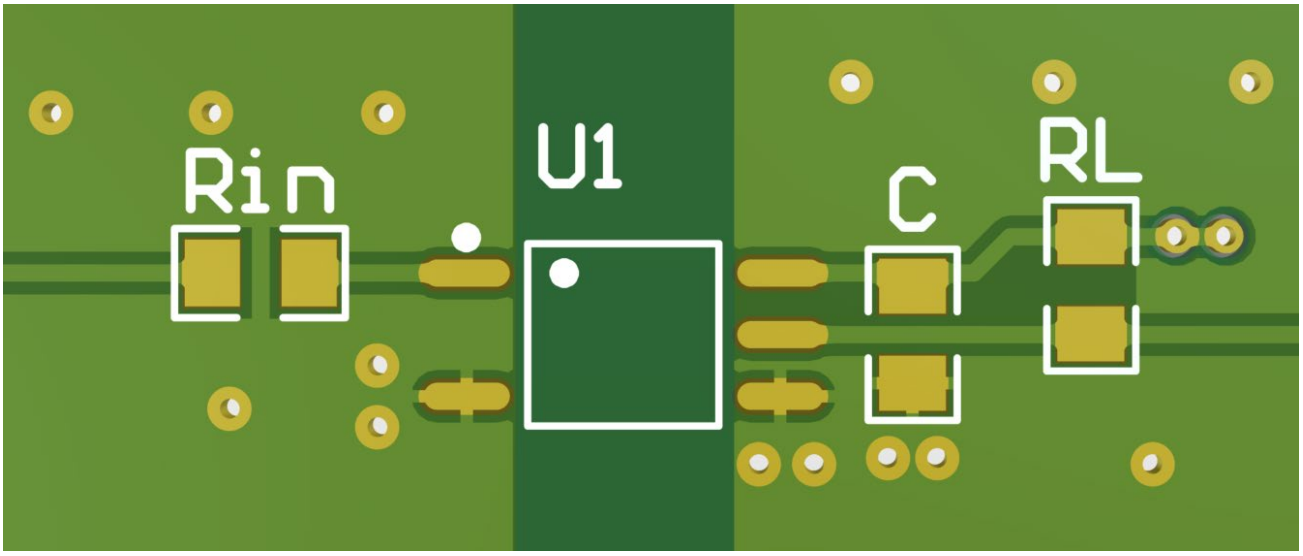
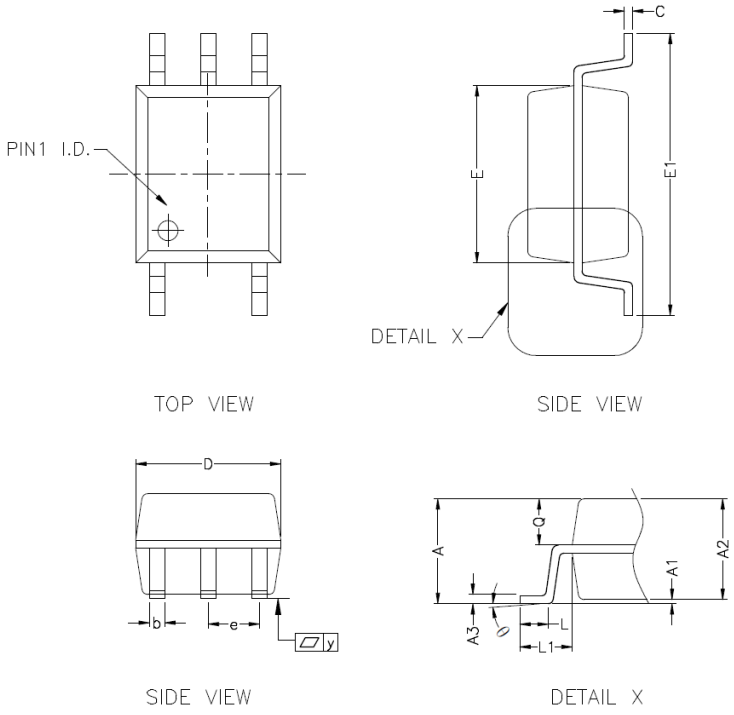


Figure 9.3 Recommended PCB Layout

10. Package Information

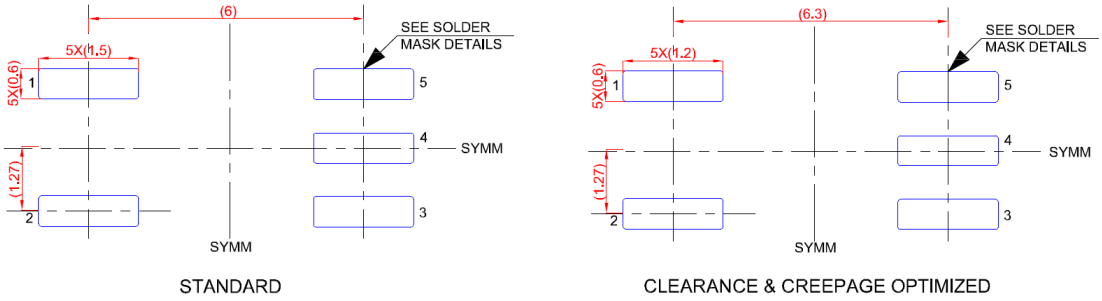


* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.602
A1	0.10	0.102	0.30
A2	2.40	2.50	2.60
A3	--	0.20	--
Q	1.10	1.15	1.20
b	0.265	0.38	0.495
c	--	0.20	--
D	3.50	3.60	3.70
E	4.30	4.40	4.50
E1	6.80	7.00	7.20
e	1.27 bsc		
L1	1.30 bsc		
L	0.71	--	--
y	--	0.10	--
θ	0°	--	7°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP5 Package Shape and Dimension in millimeters



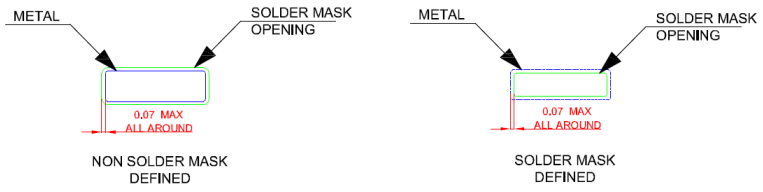
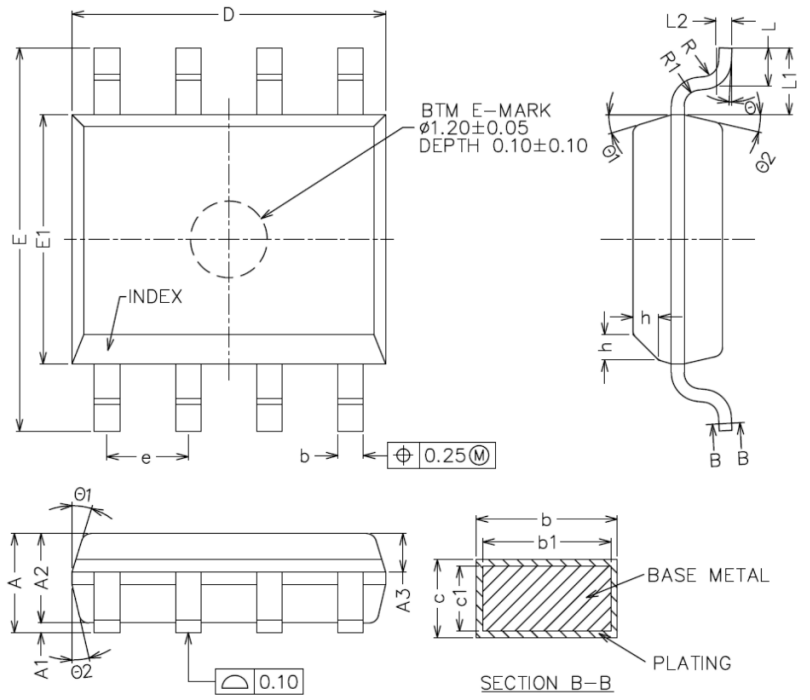


Figure 10.2 SOP5 Package Board Layout Example



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.3 SOP8 Package Shape and Dimension in millimeters

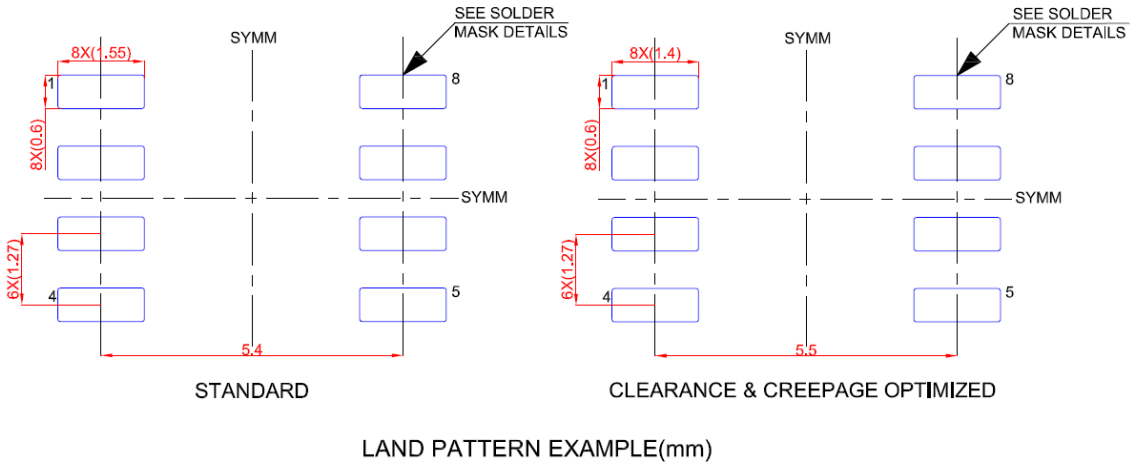
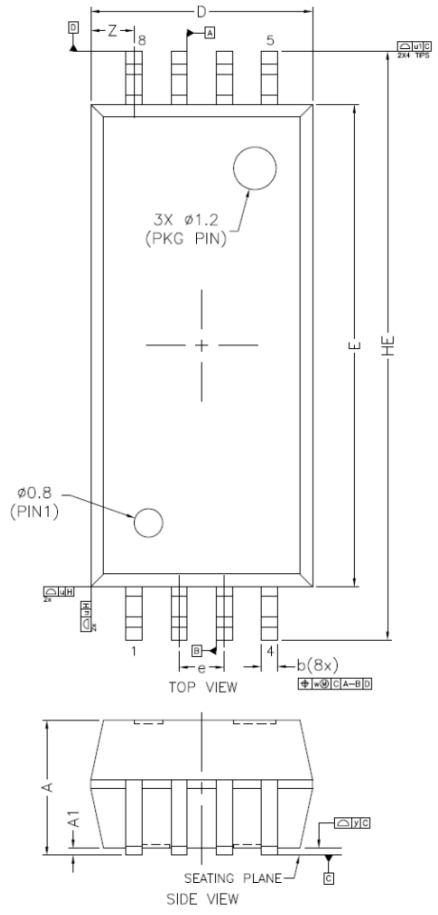
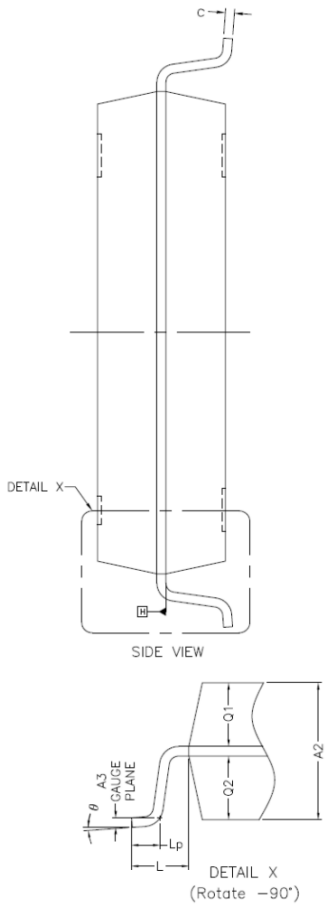


Figure 10.4 SOP8 Package Board Layout Example





* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	3.580	3.807	4.034
A1	0.100	0.200	0.300
A2	3.480	3.607	3.734
b	0.357	0.457	0.557
c	0.254 REF		
D	6.121	6.248	6.375
E	13.473	13.600	13.727
HE	16.36	16.61	16.86
Q1	1.6515	1.6765	1.7015
Q2	1.6515	1.6765	1.7015
e	1.27 BSC		
A3	0.25 REF		
L	1.505 REF		
Lp	0.635	--	--
w	0.25		
y	0.10		
u	0.10		
u1	0.20		
Z	1.219		
θ	0°	--	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.5 SOP8(600mil) Package Shape and Dimension in millimeters

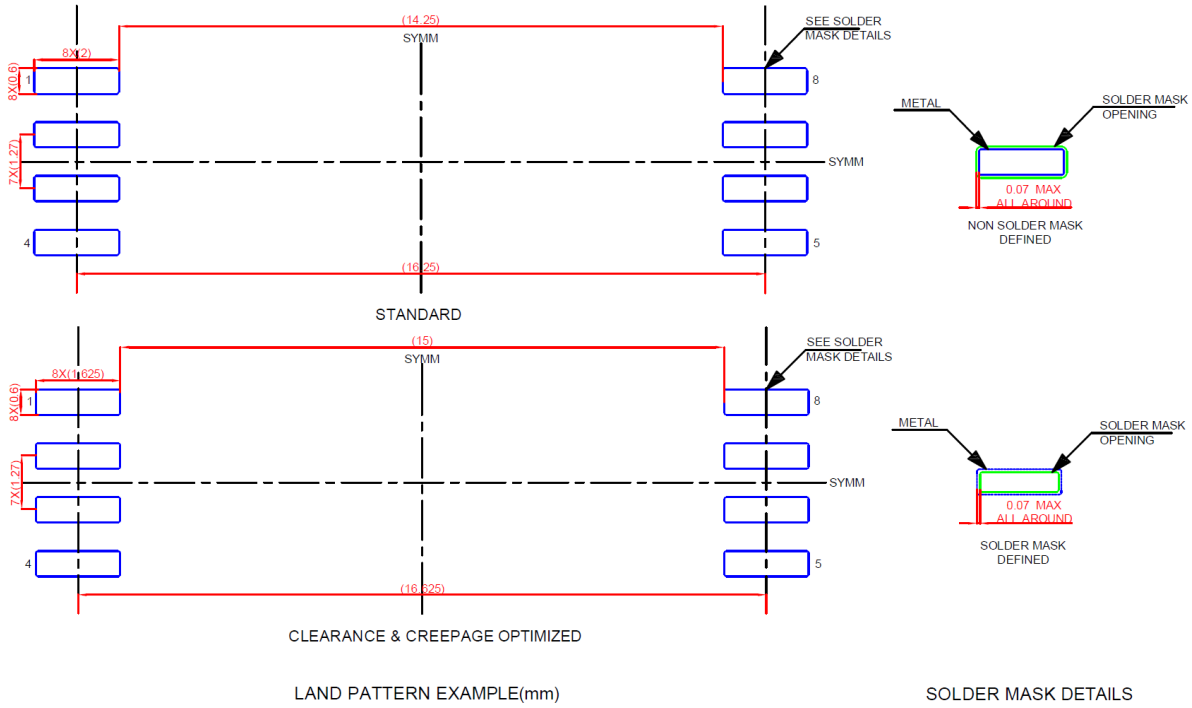


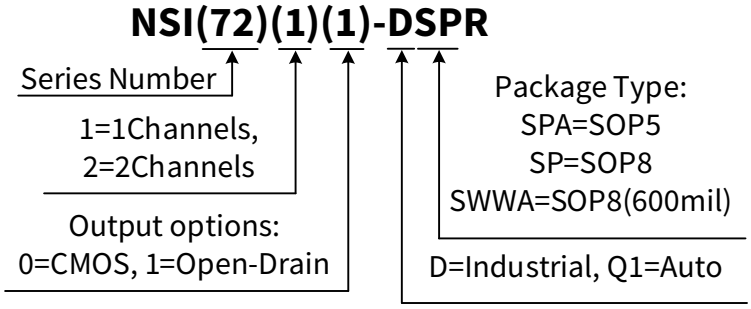
Figure 10.6 SOP8(600mil) Package Board Layout Example

11. Ordering Information

Part Number	Output Enable	Isolation Rating (kV)	Number of inputs	Output Option	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI7210-DSPAR	No	3.75	1	CMOS	15	H	-40 to 125°C	3	SOP5	SOP5	2500
NSI7211-DSPAR	No	3.75	1	Open-Drain	15	Z	-40 to 125°C	3	SOP5	SOP5	2500
NSI7211-DSPR	Yes	3.75	1	Open-Drain	15	Z	-40 to 125°C	3	SOP8	SOP8	2500
NSI7221-DSPR	No	3.75	2	Open-Drain	15	Z	-40 to 125°C	3	SOP8	SOP8	2500
NSI7211-DSWWAR	No	7.5	1	Open-Drain	15	Z	-40 to 125°C	3	SOP8(600mil)	SOWW8	1000
NSI7210-DSWWAR	No	7.5	1	CMOS	15	H	-40 to 125°C	3	SOP8(600mil)	SOWW8	1000

[1] H= Logic High, Z= High Impedance.

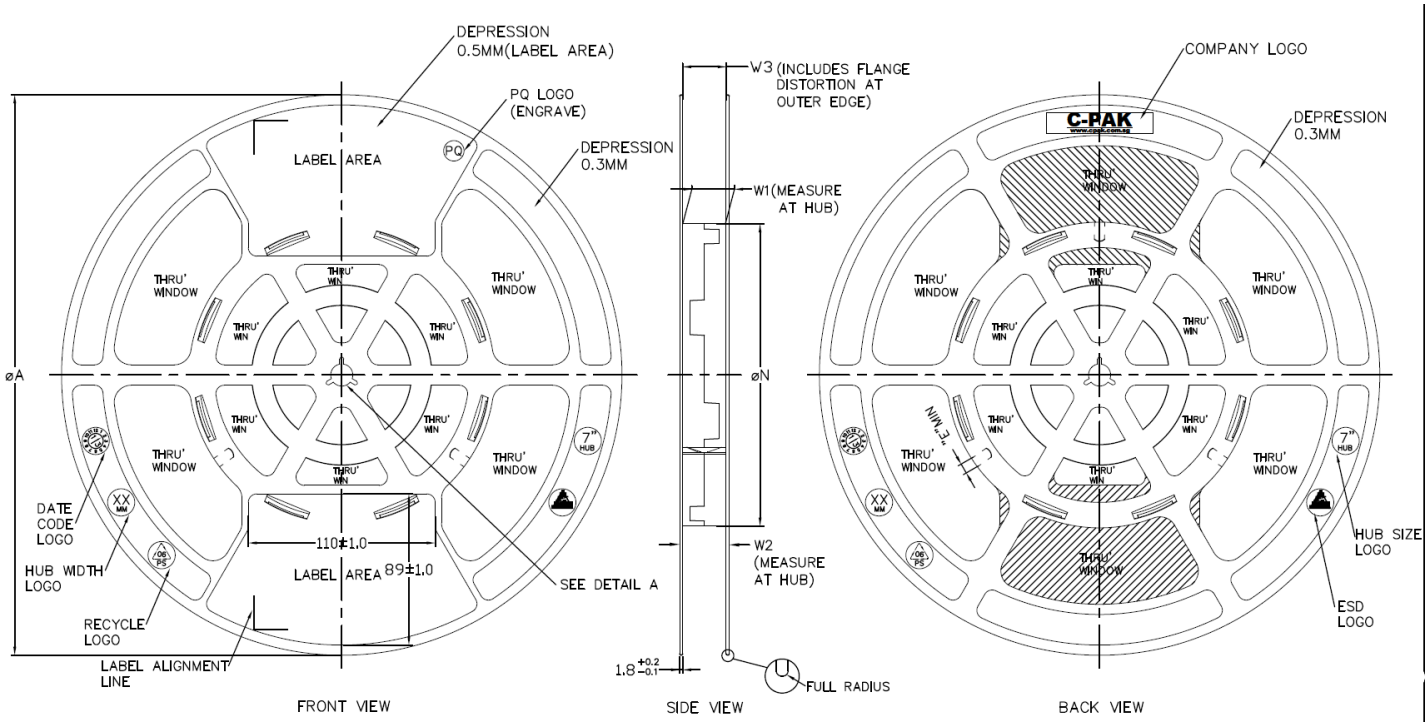
Part Number Rule:

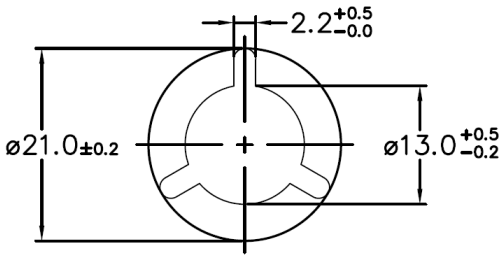


12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI72xx	Click here	Click here	Click here	Click here

13. Tape and Reel Information



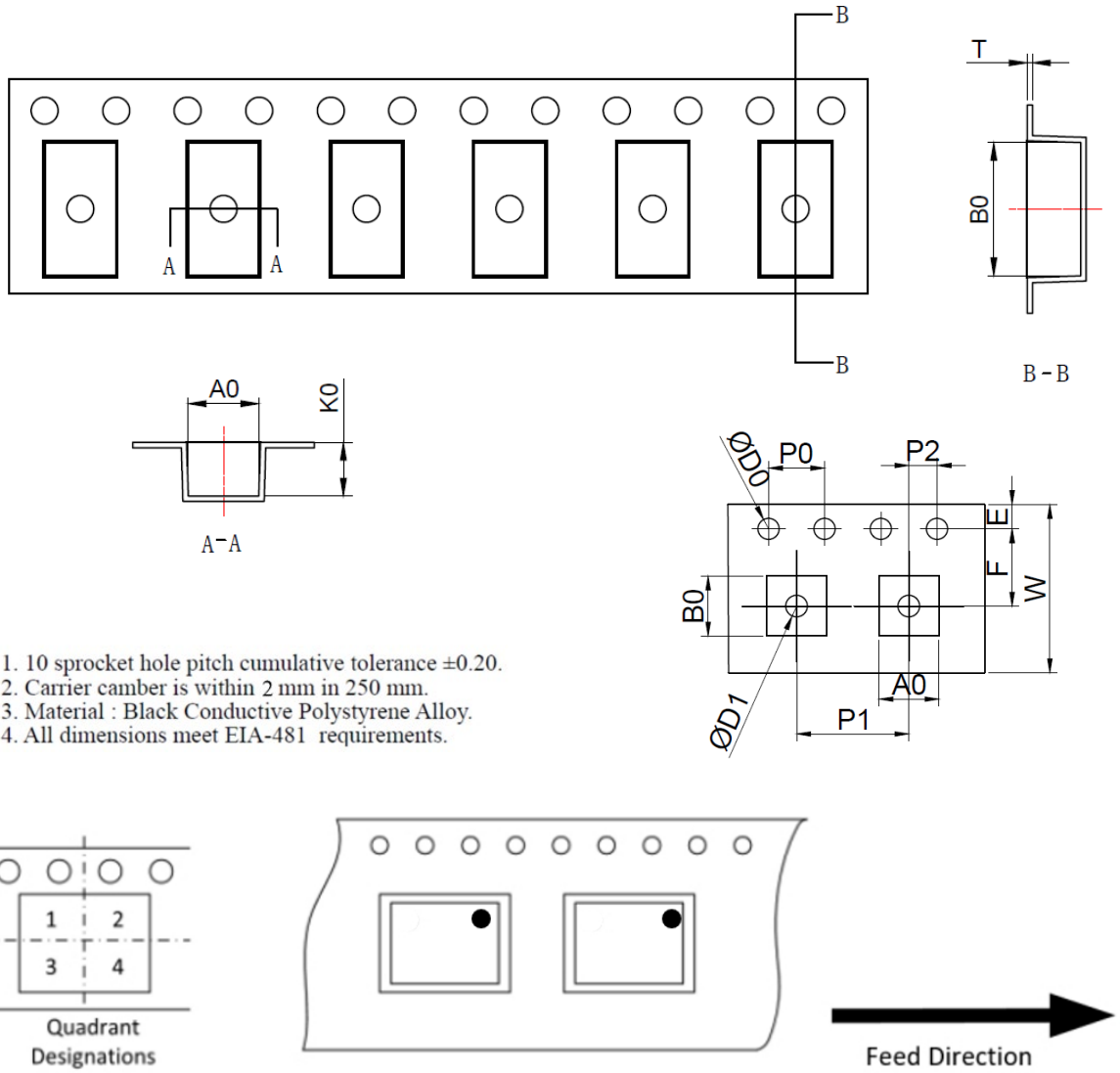


ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

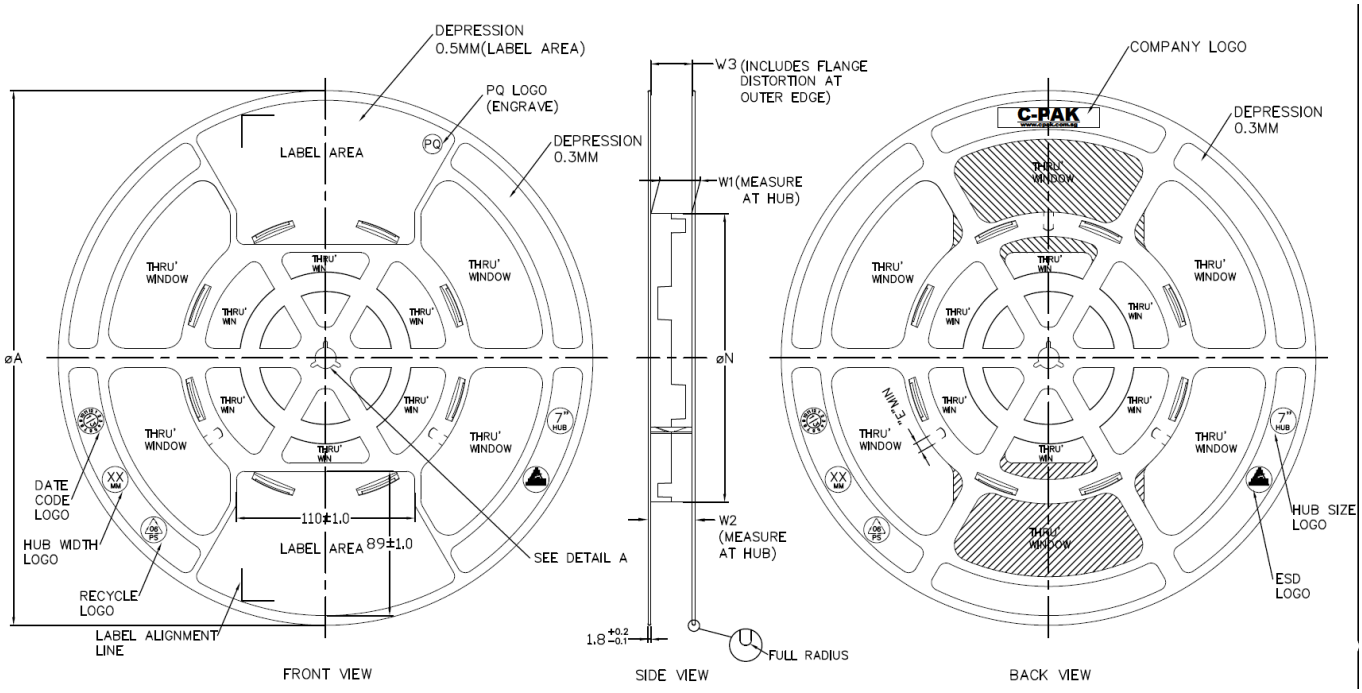
SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

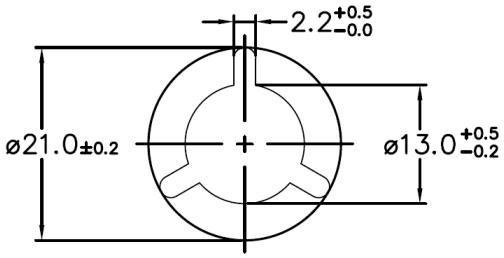
规 格	W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	T
尺 寸	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	1.50 +0.10/-0	1.50 +0.10/-0	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	8.00 ±0.10	3.95 ±0.10		7.45 ±0.10		3.00 ±0.10		0.30 ±0.05



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 2 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.

Figure 13.1 Tape and Reel Information of SOP5

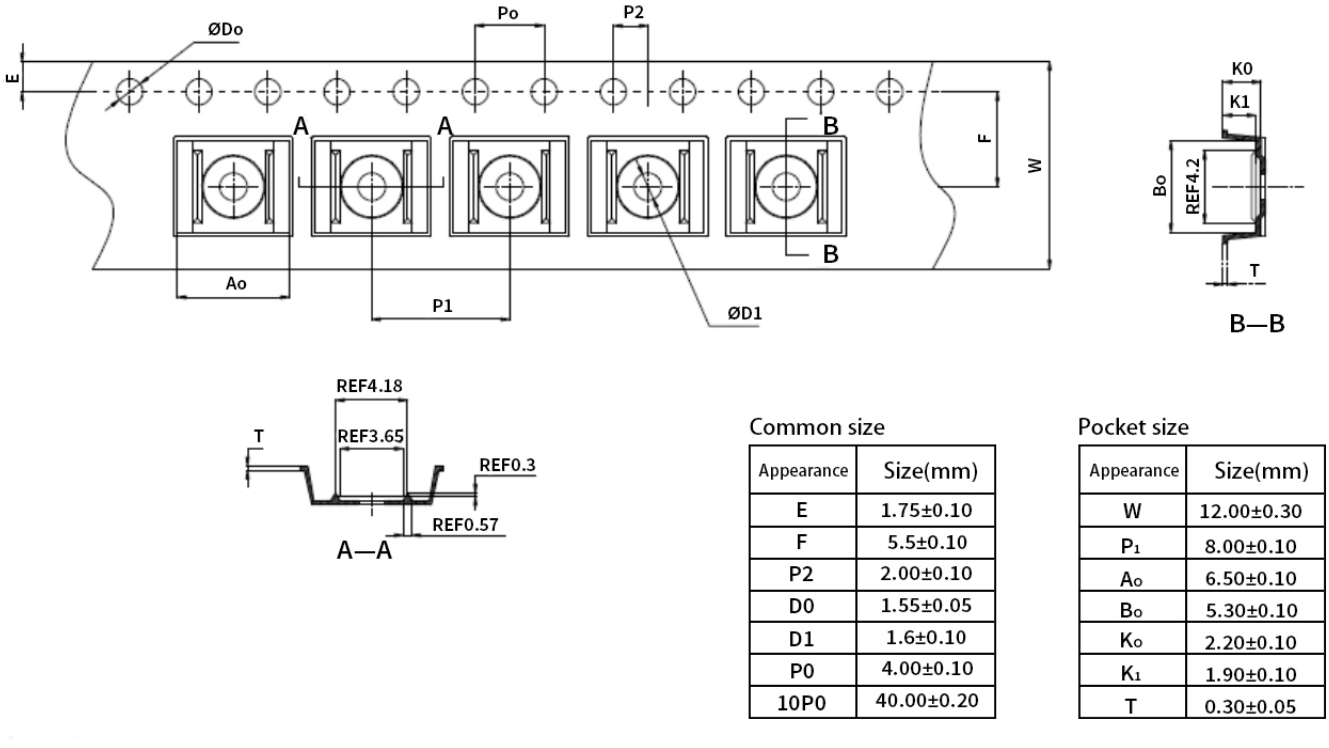




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SMALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



Common size

Appearance	Size(mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Pocket size

Appearance	Size(mm)
W	12.00±0.30
P_1	8.00±0.10
A_o	6.50±0.10
B_o	5.30±0.10
K_o	2.20±0.10
K_1	1.90±0.10
T	0.30±0.05

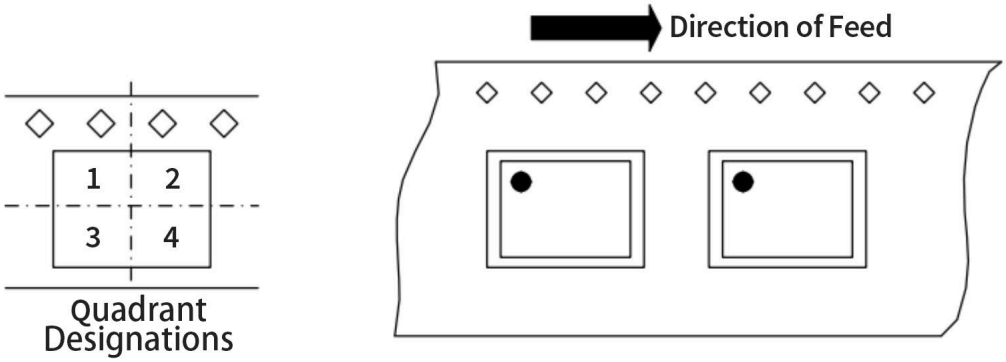
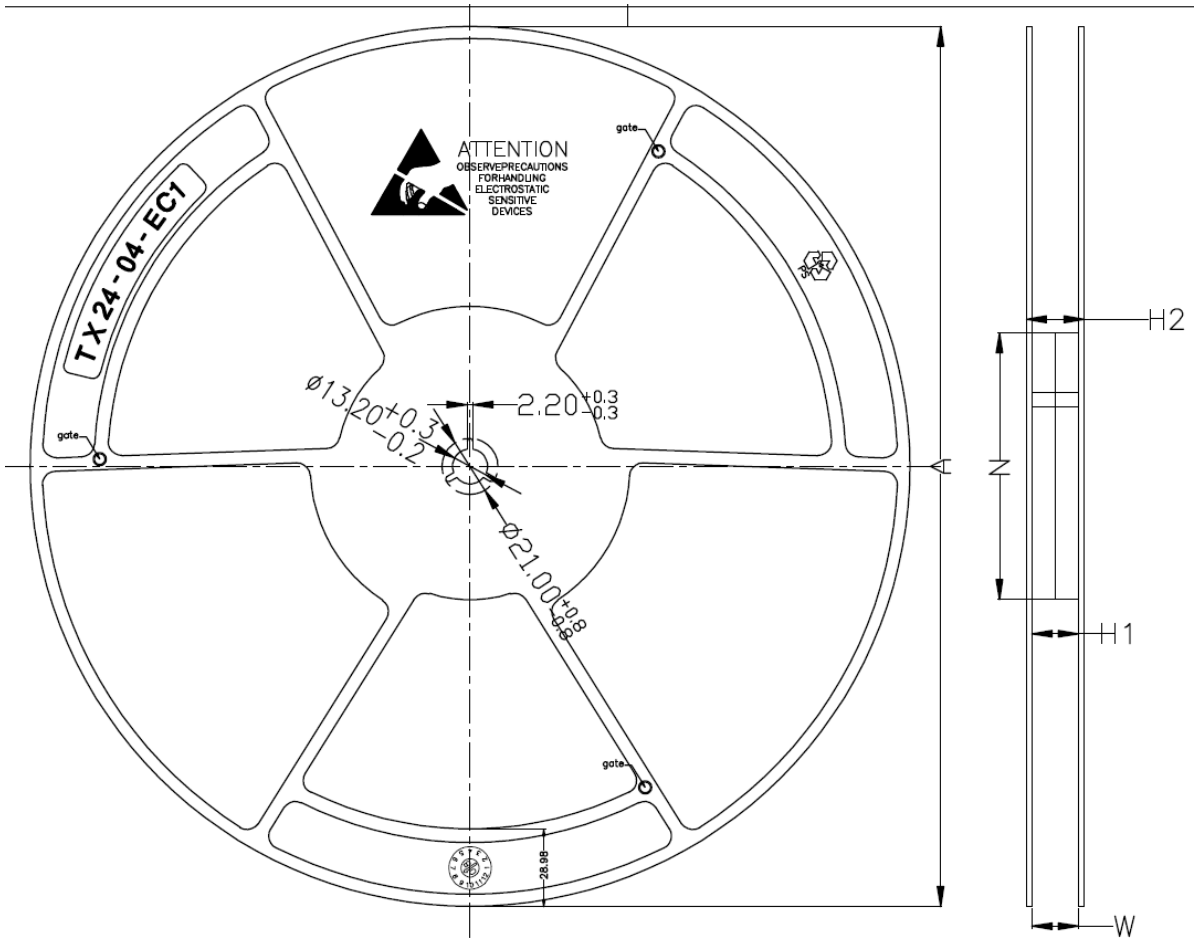
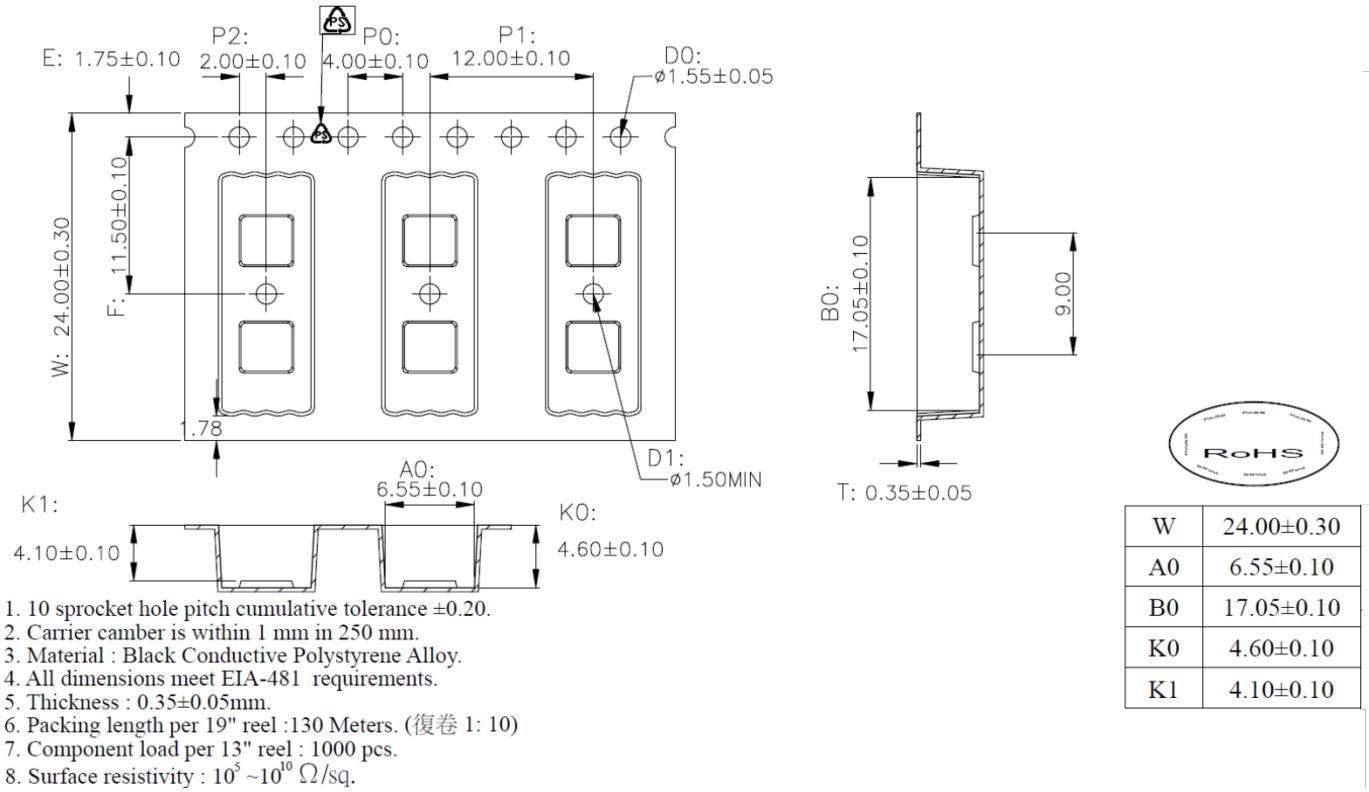


Figure 13.2 Tape and Reel Information of SOP8



PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA $^{+2}_{-2}$	øN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
24MM	330	100	24.4	28.6	24.4

NOTES:
1. MATERIAL:DISSIPATIVE(BLACK)
2. FLANGE WARPAGE:3 MM MAXIMUM 5
3. ALL DIMENSIONS ARE IN MM
4. ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5. GENERAL TOLERANCE: ±0.25 MM



W	24.00±0.30
A0	6.55±0.10
B0	17.05±0.10
K0	4.60±0.10
K1	4.10±0.10

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.35±0.05mm.
6. Packing length per 19" reel :130 Meters. (復卷 1: 10)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : 10^5 ~10^{10} Ω/sq.

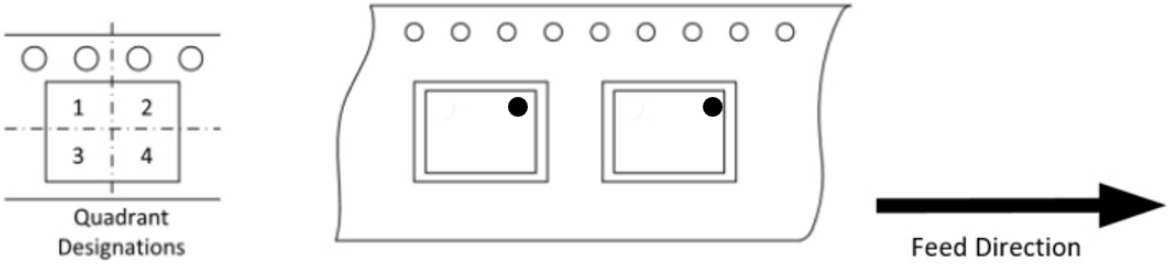


Figure 13.3 Tape and Reel Information of SOP8 (600mil)

14. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/5/10
1.1	Updated the format of Chapter 3. CMTI is divided into “$CMTI_L$” and “$CMTI_H$” in section 6.2, 6.3 and 6.4. Added a note for “ITH+” and “ITH-” in section 6.5. Updated DTI from “28” to “24” in section 7.1. Updated “Overvoltage Category per IEC60664-1” in section 7.1. Updated the withstand isolation voltage from 8kv to 7.5kv. Updated regulatory information in section 7.4. Added notes for NSI7221 under special application conditions in Chapter 9.	2024/12/26

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