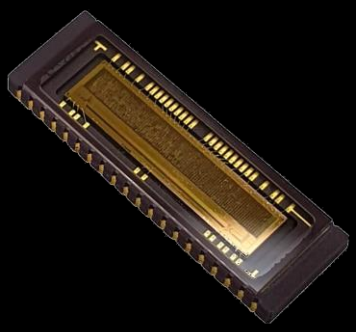
NEWSIGHT IMAGING
WHERE TECHNOLOGY SHINES

3D Machine Vision

NSI3000

CMOS Image Sensor



Line sensor of 2048 ultra- sensitive pixels
Super resolution virtual line of 8192 pixels

Perfect fit for applications like Robotics, Lidar, fast camera, bar code reader

The NSI3000 is a 2048X1 imager chip with virtual resolution of 8192X1, and physical resolution of 2048X8 to be used in Laser Lidar, Barcode readers, AR/VR and Industry 4.0 applications. The chip can be operated in two main modes: highly sensitive camera, and in high resolution mode.
The pixel array is composed of two sub-arrays:

- 4 rows of 2048 large pixels of 4x8µm, which can be used as 2048x1 effective array of large pixels of 8x16µm area using analog binning. This sub-array gives excellent sensitivity.
- 4 rows of 2048 4x4µm regular pixels, which can be used as 8192x1 effective high resolution line array of 4x4µm pixels. This sub-array gives high resolution and accuracy.

The chip can be configured in multiple operating modes using a serial interface which can be operated in two modes – simple synchronous serial interface and standard I^2C with a 16-bit dedicated protocol.
The video stream output is parallel data in 8, 9, 10, 11 or 12 bit stream in a dedicated bus which can support up to 80 MHz speed.

Specifications:

Parameter	Value
Array format	2048x8
Capture size	8192 µm x 48 µm
Scanning resolutions	2048X1, 8192X1
Pixel size	4µm x 8µm upper 4 rows 4µm x 4µm lower 4 rows
Supply Voltage	3.3 V
Power consumption	72 mW @ 7.5MHz
Input clock frequency	80 MHz
A/D converter	8-12 bits column parallel single slope
Down-sampling	N/A
Video output format	Parallel 8-12 bits data
Frame rate	up to 40000 fps
Readout control	Synchronous pixel clock + RDY signal
Sensitivity	50 µV/e

Key Features:

The NSI3000 features a state-of-the-art architecture, allowing extremely high sensitivity, while keeping low power consumption. The following are the product highlights.

- **Sensor Array**
  - Scanning resolutions:
    - 2048x1, in high sensitivity mode
    - 8192x1, in high resolution mode
  - 4 Rows of 4µm x 8µm rectangular highly sensitive pixels
  - 4 Rows of 4µm x 4µm square pixels
  - Configurable 8-12 Bit ADC
  - Integrated CDS for fixed pattern noise reduction
  - Programmable frame rate up to 40,000 fps
  - Analog binning options to improve sensitivity and reduce noise
  - Parallel comparators architecture with automatic CDS offset correction.
  - Programmable configuration:
    - Exposure times
    - ADC accuracy
    - Scanning resolution
  - Integrated Bandgap Reference

- **Interfaces**
  - Sensor data out:
    - Configurable parallel 8-12bit synchronous frame data at speeds up to 80 MHz
  - Sensor configuration:
    - Proprietary serial interface
      or
    - Enhanced I^2C serial interface
- **Input clock frequency: up to 80 MHz**
- **Power Consumption: 72mW, at 7.5MHz, 3.3V, 23**°C
- **Operating voltage: 3.3 +/-10%**
- **Technology: 0.18 µm**
- **Operation temperature: -20 to 85 degrees Celsius**
- **Package: 40pin LCC**

Pin Diagram

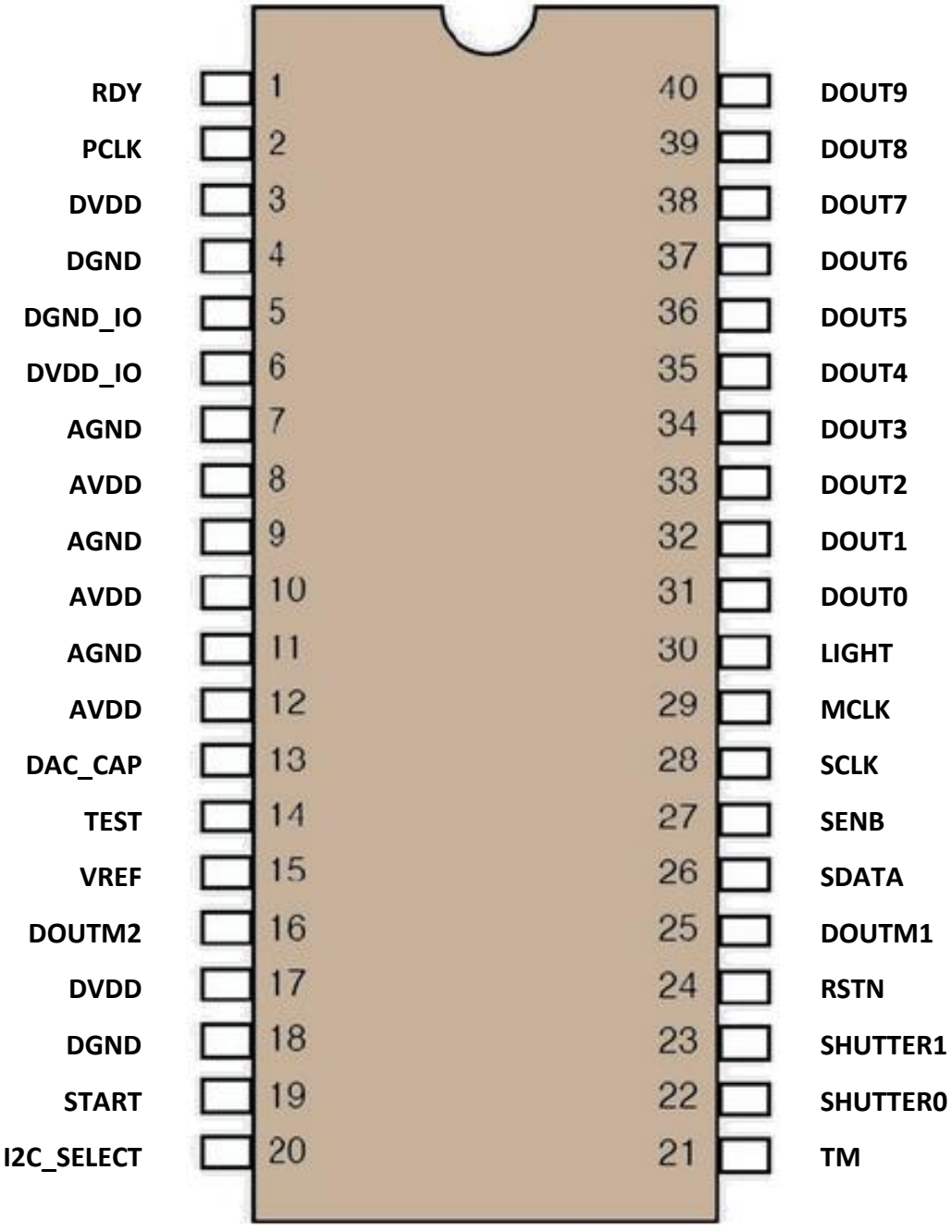


Figure 1 - LCC 40-pin package diagram

NSI3000 Pinout

Pin Name	#	I/O	Signal type	Description
RDY	1	O	Video	Parallel Data output bus valid, synchronous to PCLK output rising edge.
PCLK	2	O	Video	Output data synchronized clock
DVDD	3	P	Power	Digital power supply (3.3 V)
DGND	4	P	Power	Digital ground
DGND_IO	5	P	Power	Digital I/O ground
DVDD_IO	6	P	Power	Digital I/O power supply (3.3 V)
AGND	7	P	Power	Analog ground
AVDD	8	P	Power	Analog power supply (3.3 V)
AGND	9	P	Power	Analog ground
AVDD	10	P	Power	Analog power supply (3.3 V)
AGND	11	P	Power	Analog ground
AVDD	12	P	Power	Analog power supply (3.3 V)
DAC_CAP	13	A	Test	Ramp DAC cap input
RAMP	14	A	Test	Internal ramp input, input for bypassing the inetrnal RAMP generator
VREF	15	A	Test	Reference test voltage
DOUTM2	16	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DVDD	17	P	Power	Digital power supply (3.3 V)
DGND	18	P	Power	Digital output video data
START	19	I	Control	Start operationsignal
I2C_SELECT	20	I	Control + Test	Normal mode - select I2C interface (high) or NSI3000 propriety serial interface (low) Test mode – Row 0 reset.
TM	21	I	Control + Test	Normal mode – drive output pins to Tristate Test mode - Row 1 reset
SHUTTER0	22	I	Test	Row 0 photo-diode transfer
SHUTTER1	23	I	Test	Row 1 photo-diode transfer
RSTN	24	I	Control	Active low reset

Pin Name	#	I/O	Signal type	Description
DOUTM1	25	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
SDATA	26	I/O	Control	Serial interface data
SENB	27	I	Control	Serial interface enable
SCLK	28	I	Control	Serial interface clock
MCLK	29	I	Control	Master clock
LIGHT	30	O	Control	Light Illumination Pulse
DOUT0	31	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT1	32	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT2	33	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT3	34	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT4	35	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT5	36	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT6	37	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT7	38	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT8	39	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.
DOUT9	40	O	Video	Digital output video data, valid when RDY signal is asserted, synchronous to PCLK output rising edge.

Parallel Output Interface

Basic Timing (data only)

The data from the NSI3000 is driven out of the chip on DOUT pads. There are 12 data pads of the Video out interface. The number of valid data bits is a result of the selected ADC accuracy and can range from 8 to 12 bits. In all cases the data is aligned to the left, always using the MSB pads. The data is valid when RDY is active and is driven out with the rising edge of PCLK. The RDY signal acts as the horizontal sync signal and marks the beginning and the end of a single row.

Serial Interface

The serial interface is used for programming the NSI3000 device and setting up the operational modes and the timing of the internal pixel control signals. The serial interface also allows reading the NSI3000 configuration. When the “I2C_SELECT” pin is driven low, the chosen protocol will be the synchronous serial interface which uses 3 signals: SCLK, SDATA and SENB.

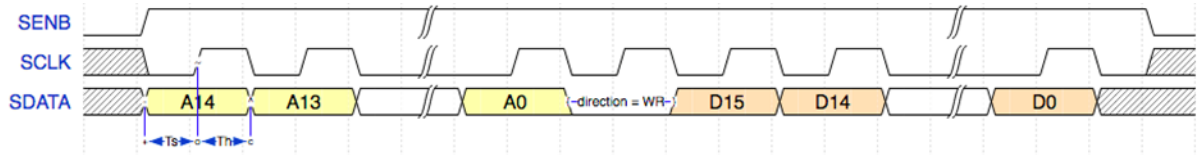
Serial Interface Signals

Signal name	Direction	Description
SENB	IN	Serial Enable: This signal must be asserted for the serial interface to function. The signal allows several NSI3000 devices to share the same SCLK and SDATA lines.
SCLK	IN	Serial interface clock signal
SDATA	IN/OUT	Bidirectional serial address and data line synchronous to SCLK

The protocol uses frames of 32 bits, 15 address bits, one direction bit and 16 data bits. The SDATA signal is sampled and driven by the NSI3000 device on the rising edge of the SCLK signal.

Serial Interface – Write Operation

A write operation starts with driving SENB high. 15 bits of address are sent to the NSI3000 on the SDATA line, MSB first. Direction bit "0", indicating a write operation, follows the address bits. 16 bits of data are sent to the NSI3000 device, MSB first. When SENB is asserted low, the transfer ends.
If SENB goes low in the middle of a transfer, the transfer is terminated and ignored.
Data is latched in the NSI3000 interface on the rising edges of SCLK, so good practice is to drive the data using the falling edges of SCLK.

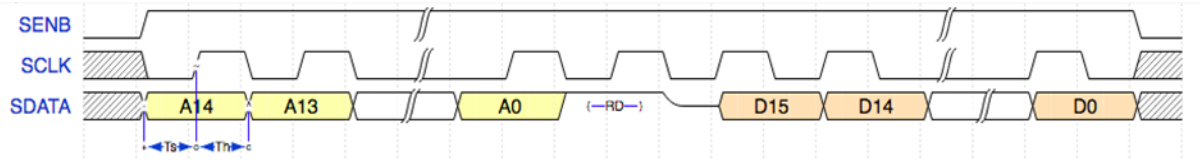


Serial Interface Write Transaction

Serial Interface – Read Operation

A read operation starts with driving SENB high. 15 bits of address are sent to the NSI3000 on the SDATA line, MSB first. Direction bit "1", indicating a read operation, follows the address bits. The driver releases the SDATA signal, to allow the NSI3000 device to drive the data out of the device. 16 bits of data are read from the NSI3000 device. When SENB is asserted low, the transfer ends.
If SENB goes low in the middle of a transfer, the transfer is terminated and ignored.

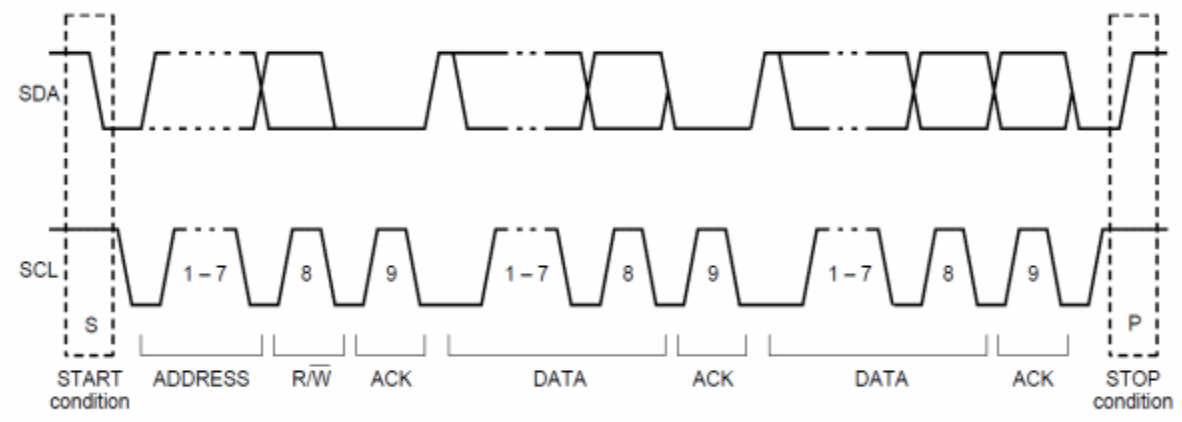
Data is driven by the NSI3000 interface on the rising edges of SCLK, so good practice is to sample the data externally using the falling edges of SCLK.



Serial Interface Read Transaction

Enhanced I²C Interface

The I2C bus protocol was invented in 1982 by Philips Semiconductor, and later enhanced by Texas Instruments. The I2C bus protocol is a Multi-Master/Multi-Slave serial bus, widely used for connecting low speed peripherals to processors and MCUs. The packet size of a standard I2C is 7-bits for address and 8-bits for data, as follows:

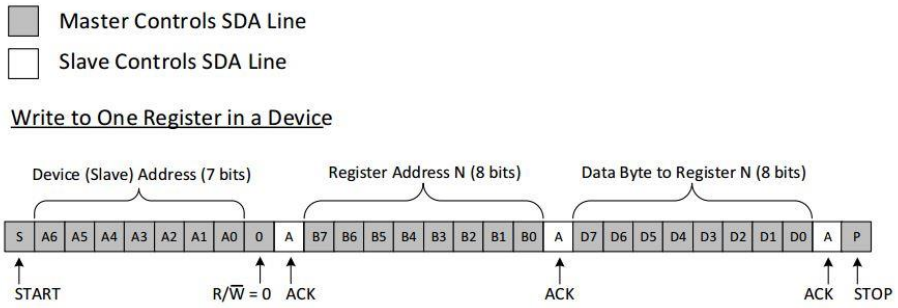


A complete I2C data transfer (courtesy of NXP semiconductors)

The NSI3000 registers can be configured using the enhanced I2C bus protocol. When the "I2C_SELECT" pin is driven high, the chosen protocol will be the I2C, and the "SCLK" and "SDATA" pins will be used to configure the chip.
The I2C implemented in NSI3000 supports only the enhanced 16-bit data and addresses, by using an encapsulation protocol over the standard I2C. 2) The NSI3000 device address is 0x3C.

Standard I2C Write Transaction

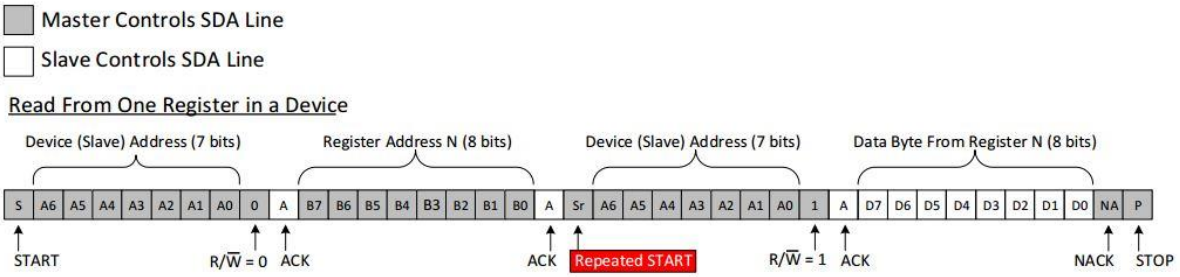
The master sends a “start” bit followed by the slave address and a “write” bit (“0”). After receiving an ACK from the slave, the master sends an 8-bit register address. After receiving an ACK from the slave, the master sends the 8-bit data to be written to the register. This transaction can continue with more write operations. The slave increments the address for each data byte received. The sequence ends with the master sending a “stop” bit.



Write transaction to a device register (courtesy of Texas Instruments)

Standard I2C Read Transaction

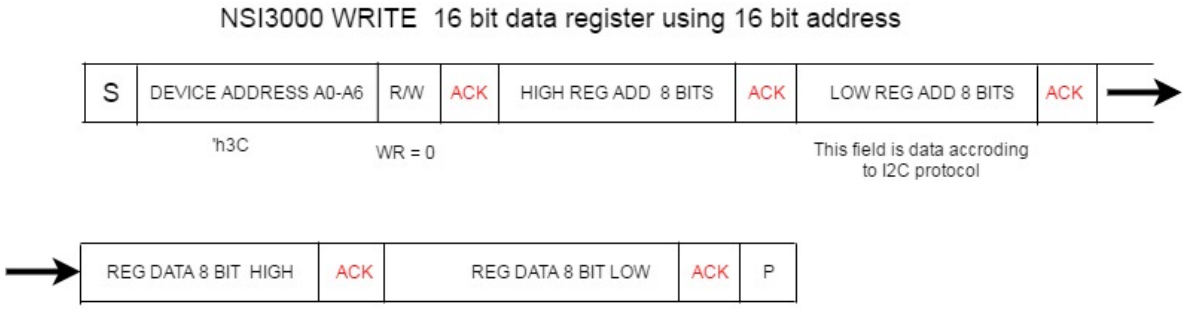
The master sends a “start” bit followed by the slave address and a “write” bit (“0”). After receiving an ACK from the slave, the master sends an 8-bit register address. After receiving an ACK from the slave, the master sends again a “start” bit followed by the slave address and a “read” bit (“1”). The slave sends the 8-bit data from the register. This transaction can continue with more read operations. The slave increments the address for each data byte transmitted. The sequence ends with the master sending a “NACK” + “stop” bit.



Read transaction from a device register (courtesy of Texas Instruments)

Enhanced I2C Write Transaction

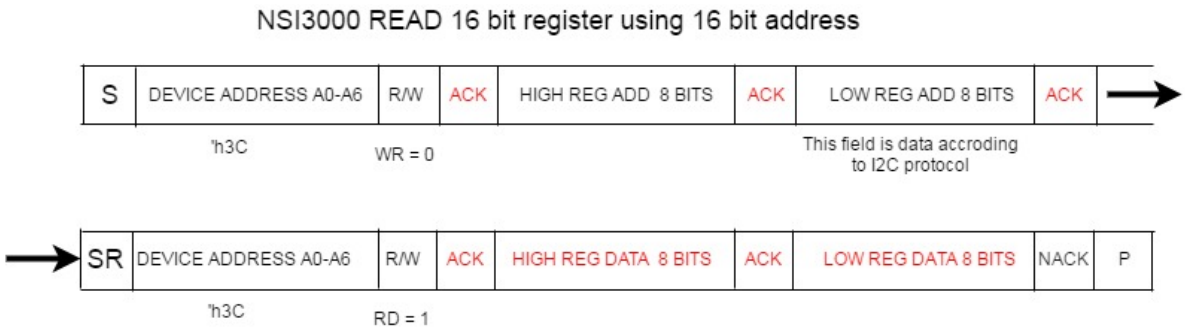
The master sends a “start” bit followed by the NSI3000 address and a “write” bit (“0”). After receiving an ACK from the chip, the master sends the *upper* 8-bit address of the register. After receiving an ACK from the chip, the master – instead of sending the 8-bit data to be written to the register – sends the *lower* 8-bit address of the register, followed by two 8-bit data write transactions.



Enhanced 16-bit write transaction to a sensor register

Enhanced I2C Read Transaction

The master sends a “start” bit followed by the NSI3000 address and a “write” bit (“0”). After receiving an ACK from the chip, the master sends the *upper* 8-bit address of the register. After receiving an ACK from the chip, the master sends the *lower* 8-bit address of the register. The master sends again a “start” bit followed by the chip address and a “read” bit (“1”). The chip sends the upper 8-bit data from the addressed register, followed by the lower 8-bit data. The sequence ends with the master sending a “NACK” + “stop” bit.



Enhanced 16-bit read transaction from a sensor register

Timing Characteristics

Parameter	Min	Type	Max	Unit
MCLK – Operating frequency			80	MHz
SCLK – Serial input clock frequency	MCLK/8			MHz
SDATA, SENB setup time (before SCLK)			4	ns
SDATA, SENB hold time (after SCLK)	0.5			ns
SDATA delay (after SCLK)			4	ns
DOUT delay (after PCLK)			3	ns
RDY delay (after PCLK)			3	ns

Table 1 - Electro – Optical Characteristics