NS4990 DataSheet V1.1

ShenZhen Nsiway Technology Co., Ltd

2010,09

Change History

DATA	VERSION	AUTHOR	CHAGE EXPLAIN
2010，09	V1.1		Page 20 “The Package of DFN(3×3)-8” Page 21 “The Package of DFN(2×2)-8”

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FIGURE LISTS

TABLE LISTS

General Description

The NS4990 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.30 watts of continuous average power to an 8Ω BTL load and 2 watts of continuous average power to a 4Ω BTL load with less than 1% distortion (THD+N) from a 5VDC power supply.

The NS4990 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The NS4990 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown pin to be driven in a likewise manner to enable shutdown. The NS4990 contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions. The NS4990 is unity-gain stable and can be configured by external gain-setting resistors

Features

- Improved PSRR at 217Hz & 1KHz 70dB
- Power Output at 5.0V, 1% THD+N, 4Ω 2W (typ)
- Power Output at 5.0V,1% THD+N,8Ω 1.3W (typ)
- Power Output at 3.6V,1% THD+N,4Ω 950mW (typ)
- Power Output at 3.6V,1% THD+N,8Ω 650mW (typ)
- Shutdown Current 0.1μA (typ)
- 2.20- 5.5V operation
- Available in space-saving packages: DFN(2×2)-8 and DFN(3×3)-8

Applications

- Portable computers
- Desktop computers
- Low voltage audio systems

Typical Application Circuit

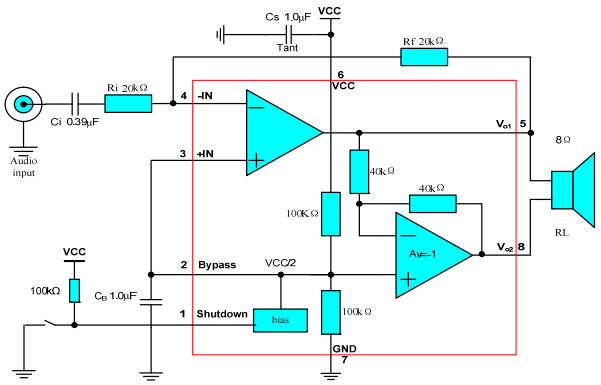


Figure1. typical Audio Amplifier Application Circuit

Absolute Maximum Ratings

Table1. Chip Limit Parameter Table

Name	Parameter
Supply Voltage	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to VDD +0.3V
ESD Susceptibility	2000V
Junction Temperature	150°C
Thermal Resistance	
θJA	210°C/W
θJC	56°C/W

WARNING: In addition to limits or any other conditions, the chip may be damaged.

Electrical Characteristics

Table2. Electrical Characteristics（VDD＝5.0V，TA＝25oC）

Symbol	Parameter	Conditions	NS4990		Units
			Typical	Max	(Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V,I_O=0A, No load	2.4	5	mA
		V_{IN}=0V,I_O=0A, 8Ω load	2.8	6	mA
I_{OFF}	Shutdown Current		0.1	1.5	uA
V_{OS}	Outpt Offset Voltage		3.7	20	mV
R_O	Resistor Output		8.5	10	KΩ
P_O	Output Power,8Ω Load	THD+N≤1%,f=1KHz	1.3		W
	Output Power4Ω Load	THD+N≤1%,f=1KHz	2.00		
T_D	Wake-up time		100		mS
THD+N	Total Harmonic Distortion+Noise	P_O=0.5W_{RMS},f=1KHz	0.1	0.2	%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine P-P Input terminated With 10Ω	63(f=217 Hz)67(f=1KHz)	60 (min)	dB

Table3. Electrical Characteristics（VDD＝3.6V，TA＝25oC）

Symbol	Parameter	Conditions	NS4990		Units (Limits)
			Typical	Limit	
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V,I_O=0A, No load	1.8	5	mA
		V_{IN}=0V,I_O=0A, 8Ω load	2.2	6	mA
I_{OFF}	Shutdown Current		0.1	1.5	uA
V_{OS}	Outpt Offset Voltage		3.7	20	mV
R_O	Resistor Output		8.2	10	KΩ
P_O	Output Power,8Ω Load	THD+N≤1%,f=1KHz	650		mW
	Output Power4Ω Load	THD+N≤1%,f=1KHz	950		
T_D	Wake-up time		75		mS
THD+N	Total Harmonic Distortion+Noise	P_O=0.5W_{RMS},f=1KHz	0.1	0.2 (max)	%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine P-P Input terminated With 10Ω	63(f=217 Hz) 68(f=1K Hz)	60 (min)	dB

Table4. Electrical Characteristics（VDD＝2.5V，TA＝25oC）

Symbol	Parameter	Conditions	NS4990		Units (Limits)
			Typical	Limit	
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V,I_O=0A, No load	1.5	5	mA
		V_{IN}=0V,I_O=0A, 8Ω load	2	6	mA
I_{OFF}	Shutdown Current		0.1	2	uA
V_{OS}	Outpt Offset Voltage		3.7	20	mV
R_O	Resistor Output		8.5	10	KΩ
P_O	Output Power,8Ω Load	THD+N≤1%,f=1KHz	280		mW
	Output Power4Ω Load	THD+N≤1%,f=1KHz	360		
T_D	Wake-up time		70		mS
THD+N	Total Harmonic Distortion+Noise	P_O=0.5W_{RMS},f=1KHz	0.1	0.2 (max)	%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine P-P Input terminated With 4Ω	63(f=217 Hz) 68(f=1K Hz)	60 (min)	dB

Pin Configuration

Pin Layout

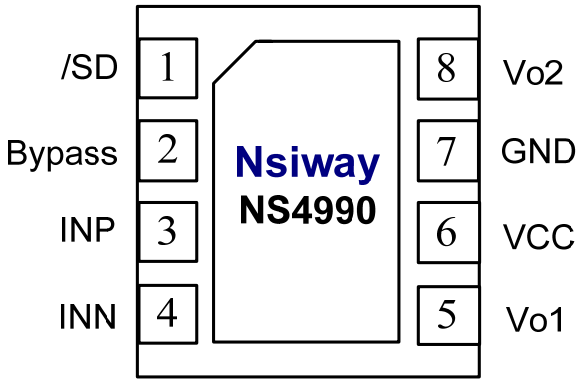


Figure2. DFN(2×2)-8 and DFN(3×3)-8 Package Pin Distribution (top view)

Pin Discription

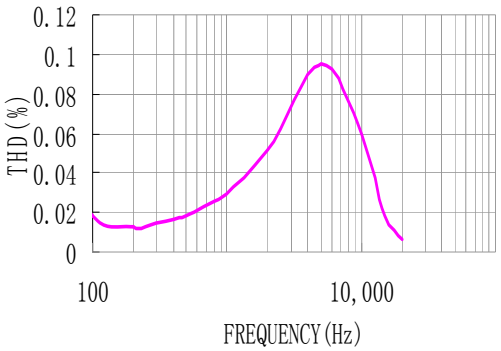
Table5. Pin Discription

Pin NO.	Pin Name	Description
1	/SD	The device enters in shutdown mode when a low level is applied on this pin
2	BYP	Bypass capacitor pin which provides the common mode voltage
3	+IN	Positive input of the first amplifier, receives the common mode voltage
4	-IN	Negative input of the first amplifier, receives the audio input signal
5	Vo1	Negative output
6	VDD	Analog VDD input supply.
7	GND	Ground connection for circuitry.
8	Vo2	Positive output

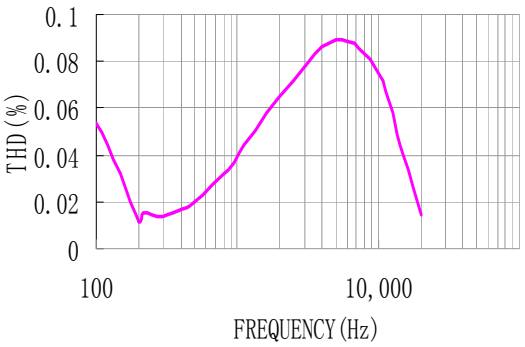
Typical Characteristics

THD, THD+N,S/N

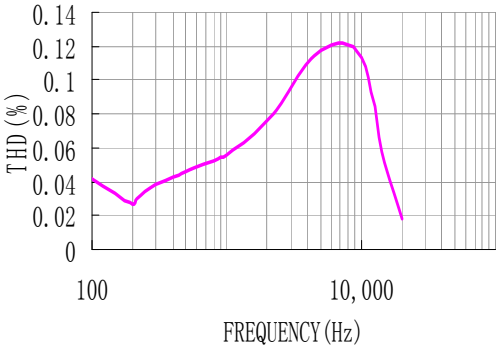
THD vs Frequency
T=25℃, Vdd=5V, RL=8Ω, and Po=500mW



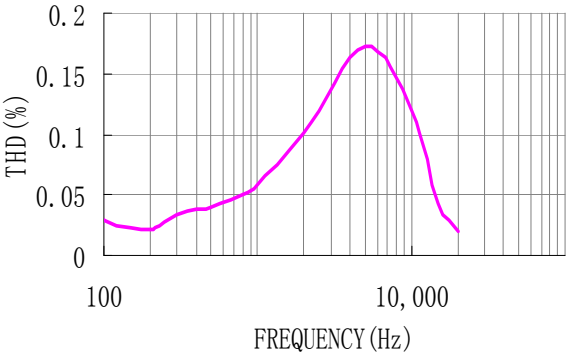
THD vs Frequency
T=25℃, Vdd=3.3V, RL=8Ω, and Po=425mW



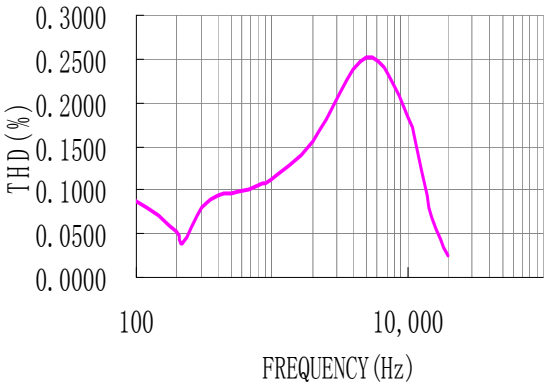
THD vs Frequency
T=25℃, Vdd=2.5V, RL=8Ω, and Po=150mW



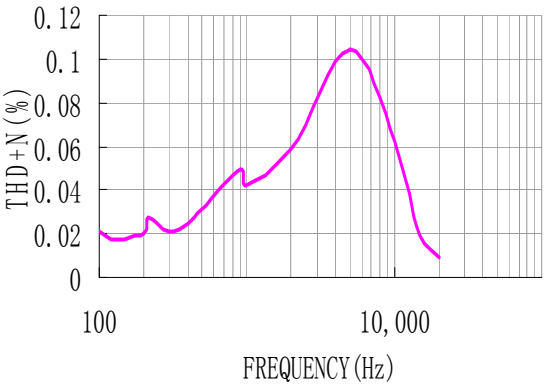
THD vs Frequency
T=25℃, Vdd=3.3V, RL=4Ω, and Po=425mW



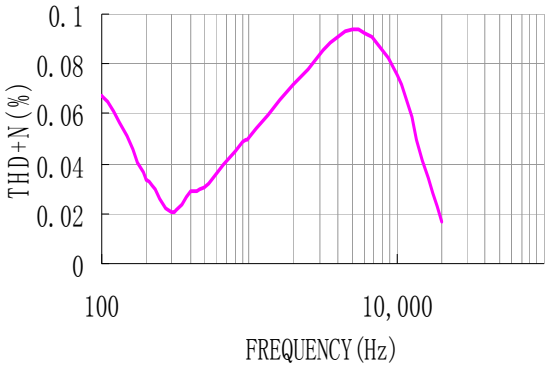
THD vs Frequency
T=25℃, Vdd=2.5V, RL=4Ω, and Po=150mW



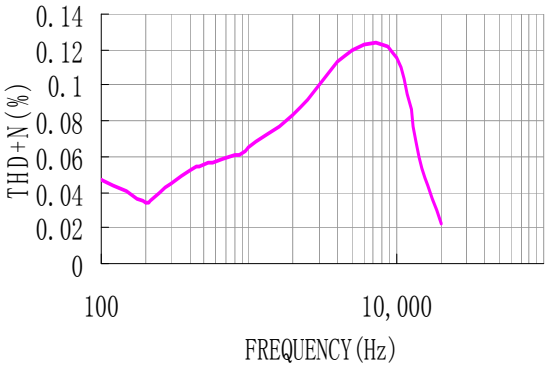
THD+N vs Frequency
T=25℃, Vdd=5V, RL=8Ω, and Po=500mW



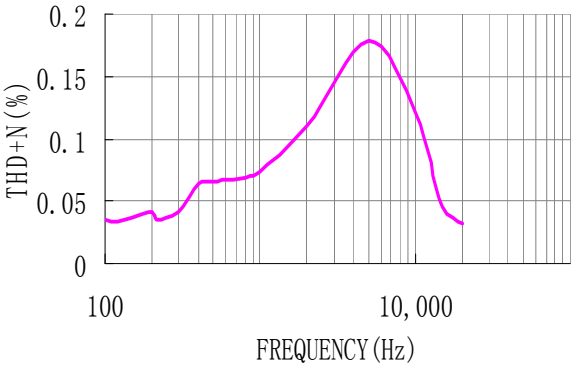
THD+N vs Frequency
T=25℃, Vdd=3.3V, RL=8Ω, and Po=425mW



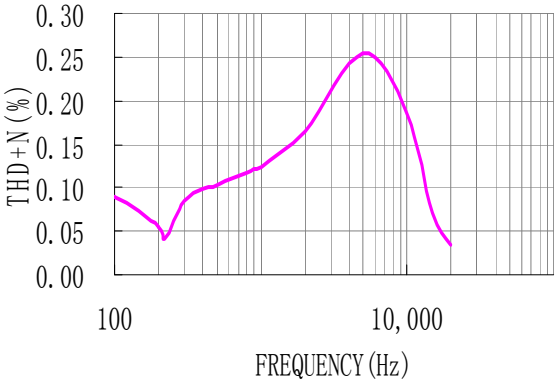
THD+N vs Frequency
T=25℃, Vdd=2.5V, RL=8Ω, and Po=150mW



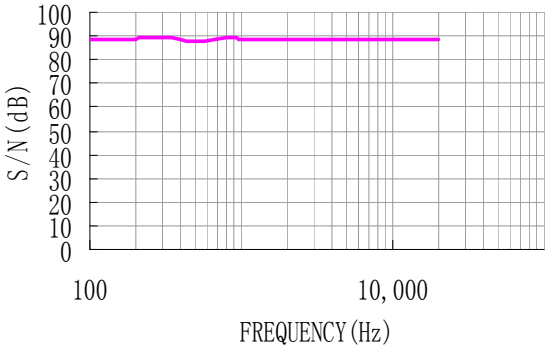
THD+N vs Frequency
T=25℃, Vdd=3.3V, RL=4Ω, and Po=425mW



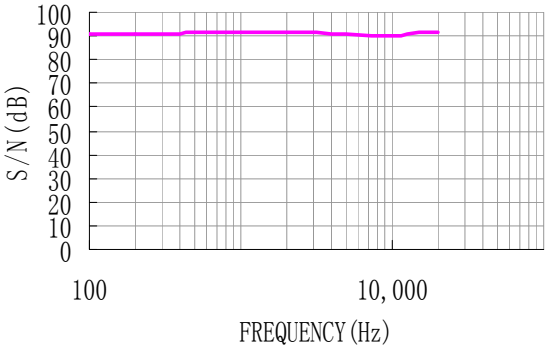
THD+N vs Frequency
T=25℃, Vdd=2.5V, RL=4Ω, and Po=150mW



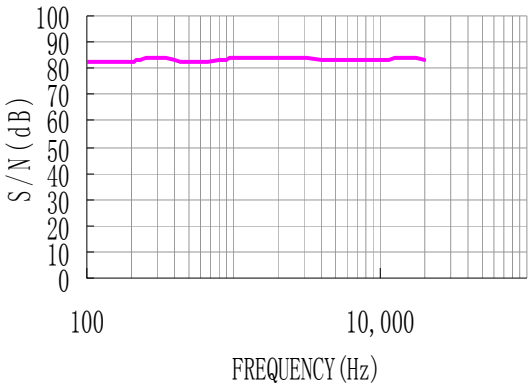
S/N vs Frequency
T=25℃, Vdd=5V, RL=8Ω, and Po=500mW



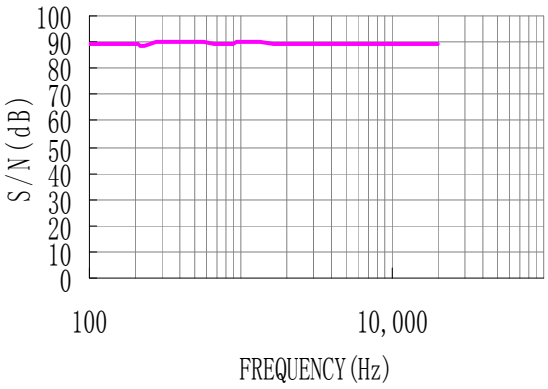
S/N vs Frequency
T=25℃, Vdd=3.3V, RL=8Ω, and Po=425mW



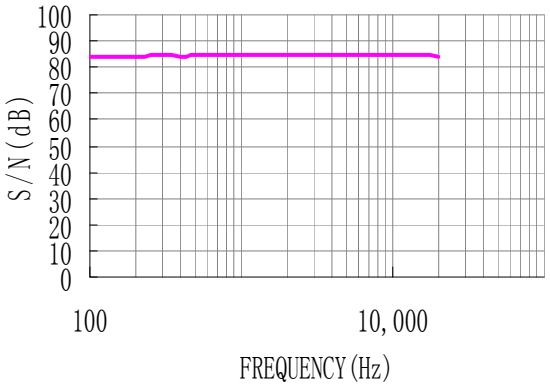
S/N vs Frequency
T=25℃, Vdd=2.5V, RL=8Ω, and Po=150mW



S/N vs Frequency
T=25℃, Vdd=3.3V, RL=4Ω, and Po=425mW

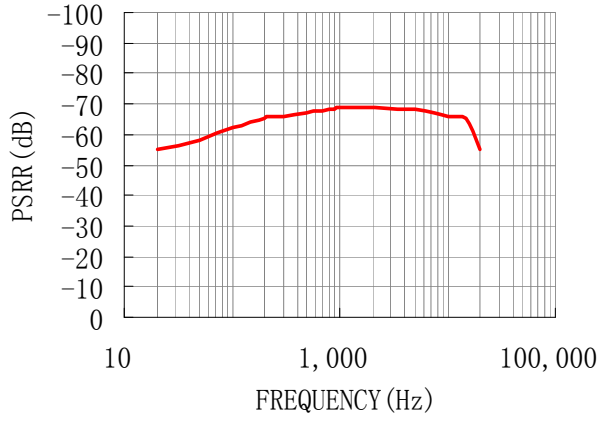


S/N vs Frequency
T=25℃, Vdd=2.5V, RL=4Ω, and Po=150mW

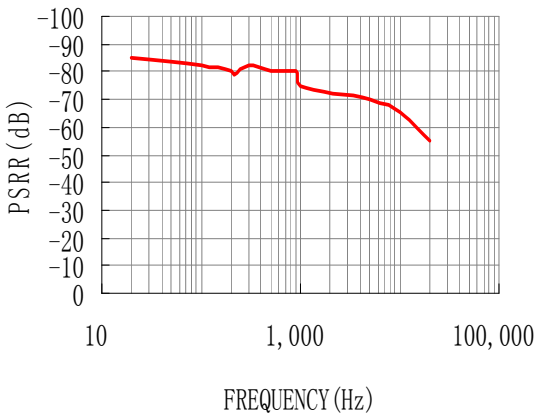


Power Supply Rejection Ratio (PSRR)

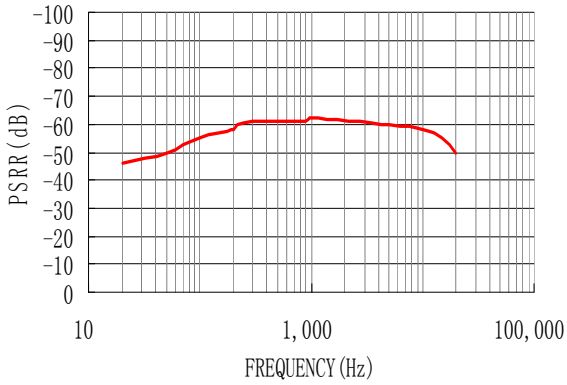
PSRR vs Frequency
VDD=5V, RL=8Ω, 输入接10Ω电阻



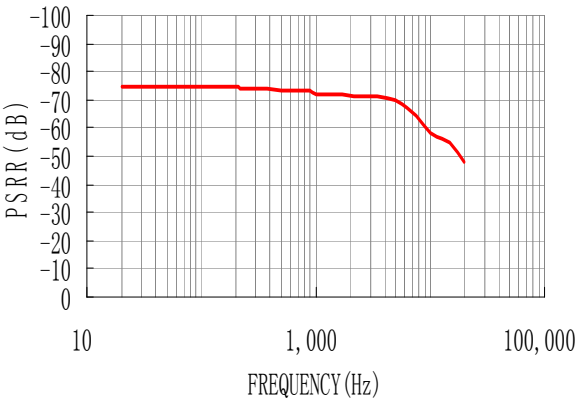
PSRR vs Frequency
VDD=5V, RL=8Ω, 输入悬空



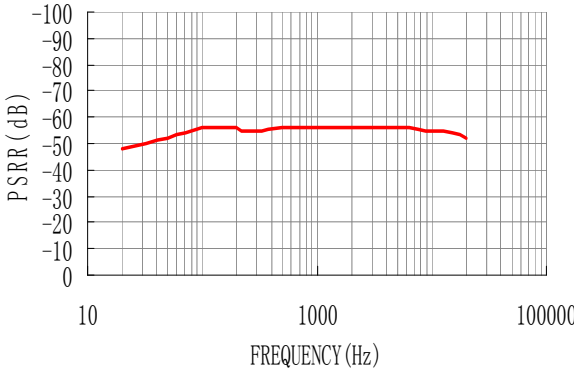
PSRR vs Frequency
VDD=3.3V, RL=8Ω, 输入接10Ω电阻



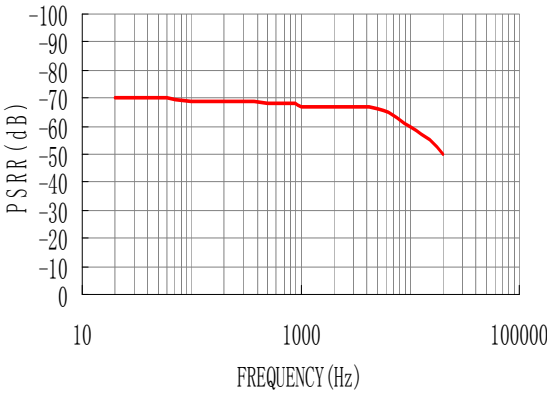
PSRR vs Frequency
VDD=3.3V, RL=8Ω, 输入悬空



PSRR vs Frequency
VDD=2.5V, RL=8Ω, 输入接10Ω电阻

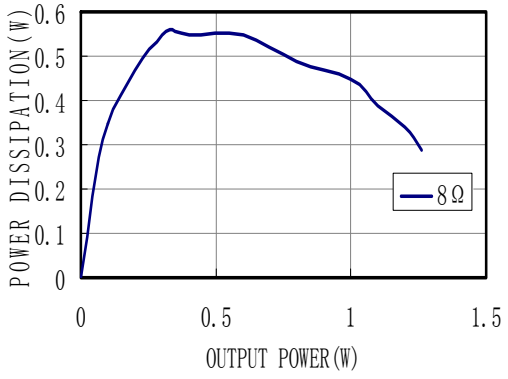


PSRR vs Frequency
VDD=2.5V, RL=8Ω, 输入悬空

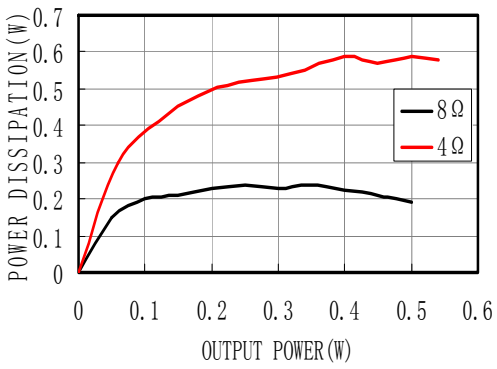


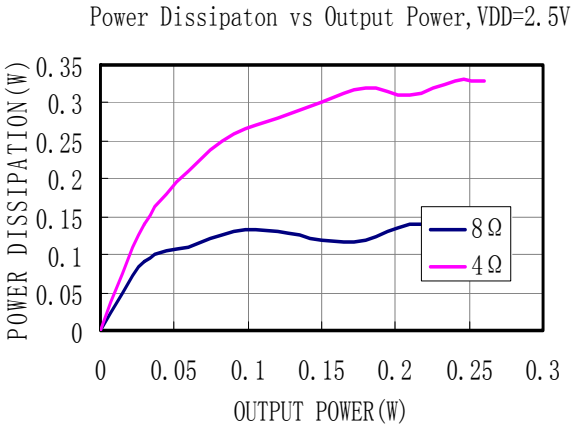
Power Dissipation

Power Dissipaton vs Output Power, VDD=5V

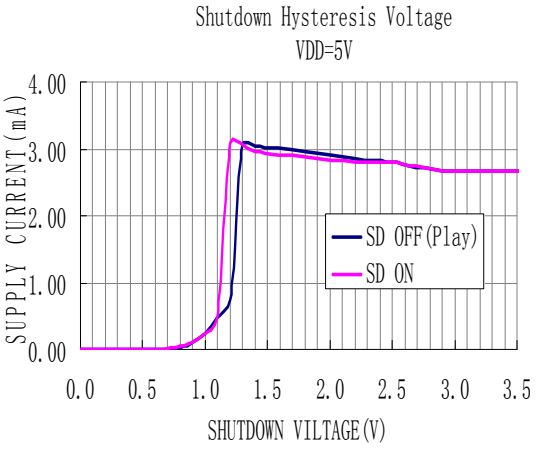


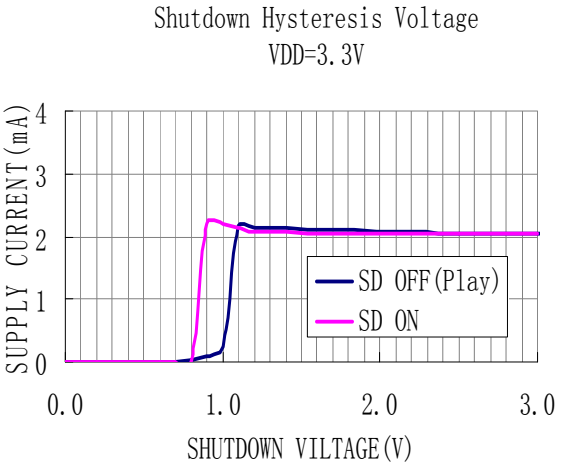
Power Dissipaton vs Output Power, VDD=3.3V

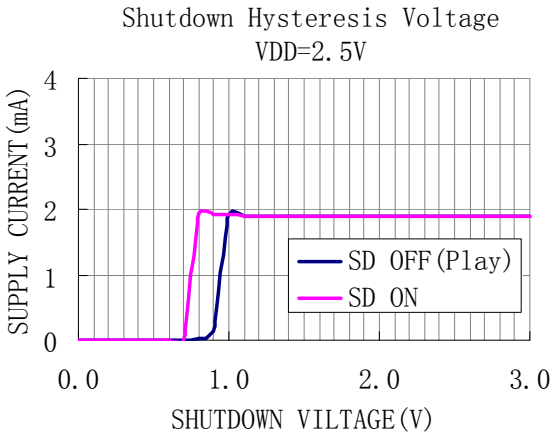




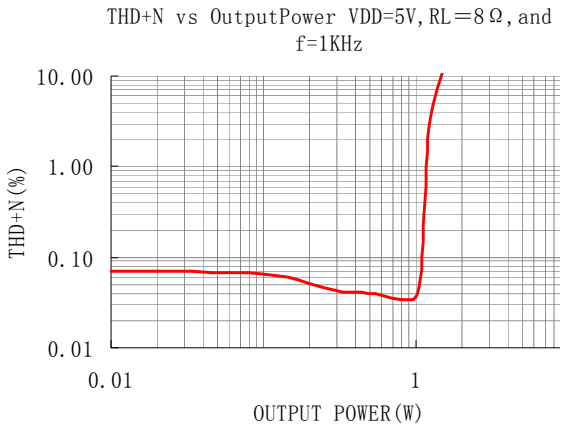
Shut Down Hysteresis

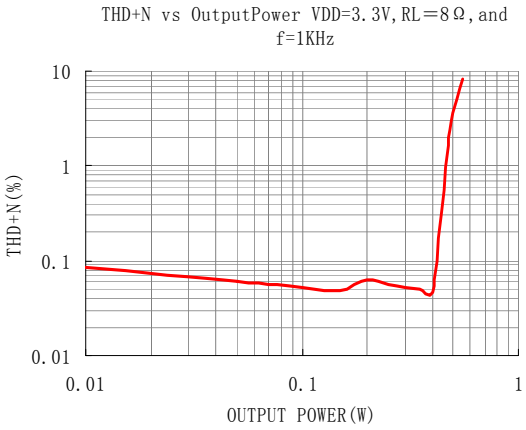


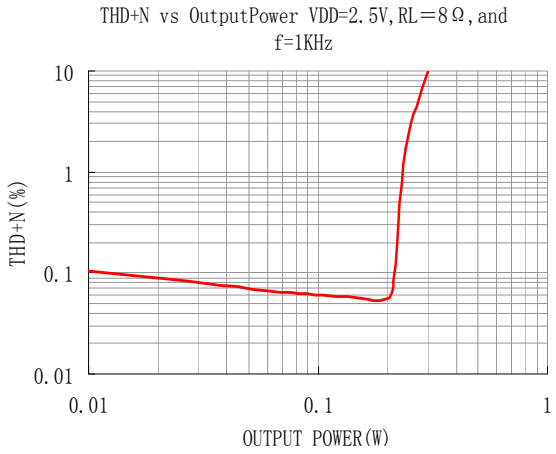


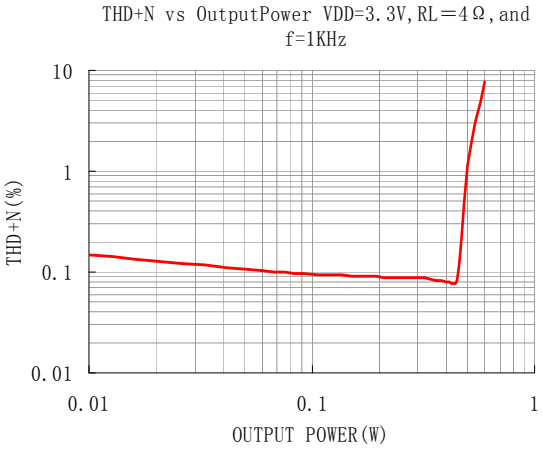


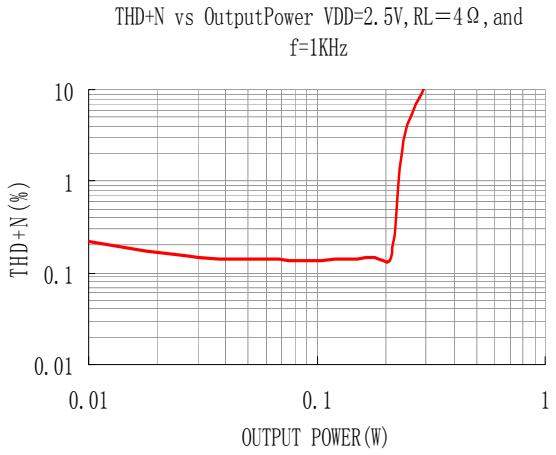
Output Power

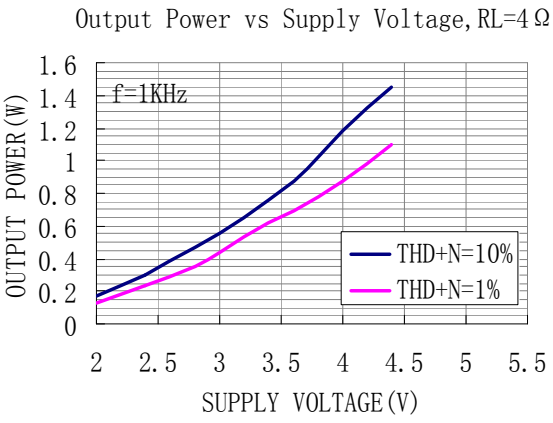


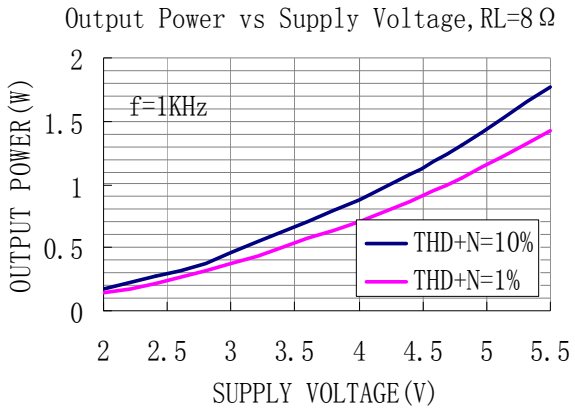


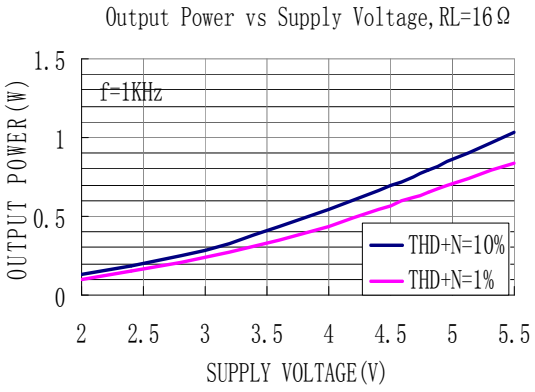












Application Information

BLOCK DIAGRAM

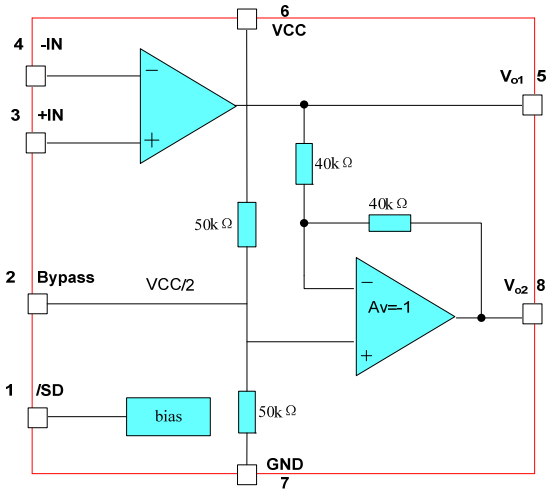


Figure3. The block diagram of NS4990

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the NS4990 has two internal operational amplifiers. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of Rf to Ri while
the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 \times \frac{R_f}{R_i}$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier

configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section.

A bridge configuration, such as the one used in NS4990,also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the NS4990 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier.

The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4 \times \frac{V_{DD}^2}{2\pi^2 R_L} \qquad (1)$$

It is critical that the maximum junction temperature TJMAX of 150°C is not exceeded. TJMAX can be determined from the power derating curves by using PDMAX and the PC board foil area. By adding copper foil, the thermal resistance of the application can be reduced from the free air value of θJA, resulting in higher PDMAX values without thermal shutdown protection circuitry being activated. Additional copper foil can be added to any of the leads connected to the NS4990. It is especially effective when connected to VDD, GND, and the output pins. Refer to the application information on the NS4990 reference design board for an example of good heat sinking. If TJMAX still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10μF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the NS4990. The selection of a bypass capacitor, especially CB, is dependent upon PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the NS4990 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. In addition, the NS4990 contains a Shutdown Mode pin (LD and MH packages only), allowing the designer to designate whether the part will be driven into shutdown with a high level logic signal or a low level logic signal. This allows the designer maximum flexibility in device use, as the Shutdown Mode pin may simply be tied permanently to either VDD or GND to set the NS4990 as either a "shutdown-high" device or a "shutdown-low" device, respectively. The device may then be placed into shutdown mode by toggling the Shutdown pin to the same state as the Shutdown Mode pin. For simplicity's sake, this is called "shutdown same", as the NS4990 enters shutdown mode whenever the two pins are in the same logic state. The MM package lacks this Shutdown Mode feature, and is permanently fixed as a 'shutdown-low' device. The trigger point for either shutdown high or shutdown low is shown as a typical value in the Supply Current vs Shutdown Voltage graphs in the Typical Performance Characteristics section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1μA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the NS4990 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality. The NS4990 is unity-gain stable which gives the designer maximum system flexibility. The NS4990 should be used in low gain configurations to minimize THD+N+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, Audio Power Amplifier Design, for a more complete explanation of proper gain selection. Besides gain, one of the major considerations is the closedloop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, Ci, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 VDD). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, CB, is the most critical component to minimize turn-on pops since it determines how fast the NS4990 turns on. The slower the NS4990's outputs ramp to their quiescent DC voltage (nominally 1/2 VDD), the smaller the turn-on pop. Choosing CB equal to 1.0μF along with a small value of Ci (in the range of 0.1μF to 0.39μF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with CB equal to 0.1μF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of CB equal to 1.0μF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1Wrms
Load Impedance	8Ω
Input Level	1Vrms
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found.

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the NS4990 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 2.

$$A_{VD} \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{ORMS} / V_{INRMS} \qquad (2)$$

$$R_f / R_i = A_{VD} / 2$$

From Equation 2, the minimum AVD is 2.83; use AVD = 3.Since the desired input impedance was 20kΩ, and with a AVD impedance of 2, a ratio of 1.5:1 of Rf to Ri results in an allocation of Ri = 20kΩ and Rf = 30kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

$$f_L = 100Hz / 5 = 20Hz$$

$$f_H = 20KHz \times 5 = 100KHz$$

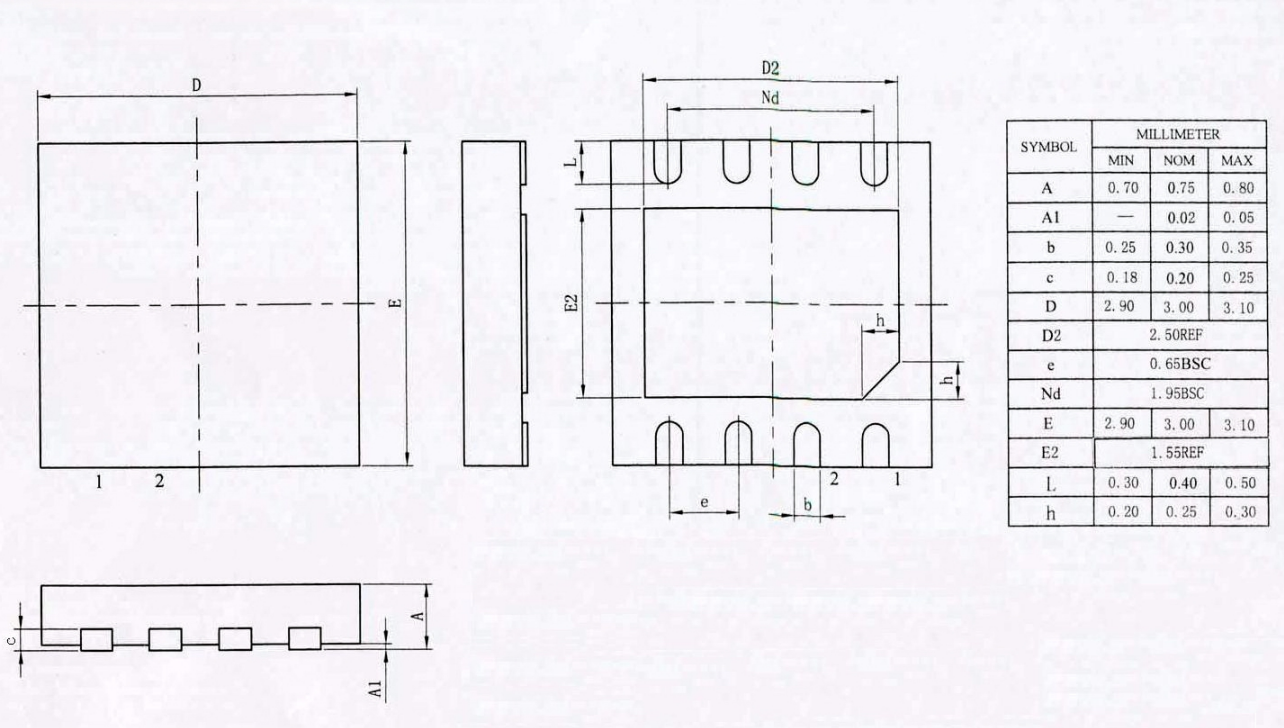
As stated in the External Components section, Ri in conjunction with Ci create a highpass filter.

$$C_i \geq 1/(2\pi \times 20K\Omega \times 20Hz) = 0.397uf$$

Use 0.39uf.The high frequency pole is determined by the product of the desired frequency pole, fH, and the differential gain, AVD. With a AVD = 3 and fH = 100kHz, the resulting GBWP = 300kHz which is much smaller than the NS4990 GBWP of 2.5MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the NS4990 can still be used without running into bandwidth limitations.

Physical Size of Chip Package

The Package of DFN(3×3)-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.50REF		
e	0.65BSC		
Nd	1.95BSC		
E	2.90	3.00	3.10
E2	1.55REF		
L	0.30	0.40	0.50
h	0.20	0.25	0.30

Figure4. The Package of DFN(3×3)-8

The Package of DFN(2×2)-8

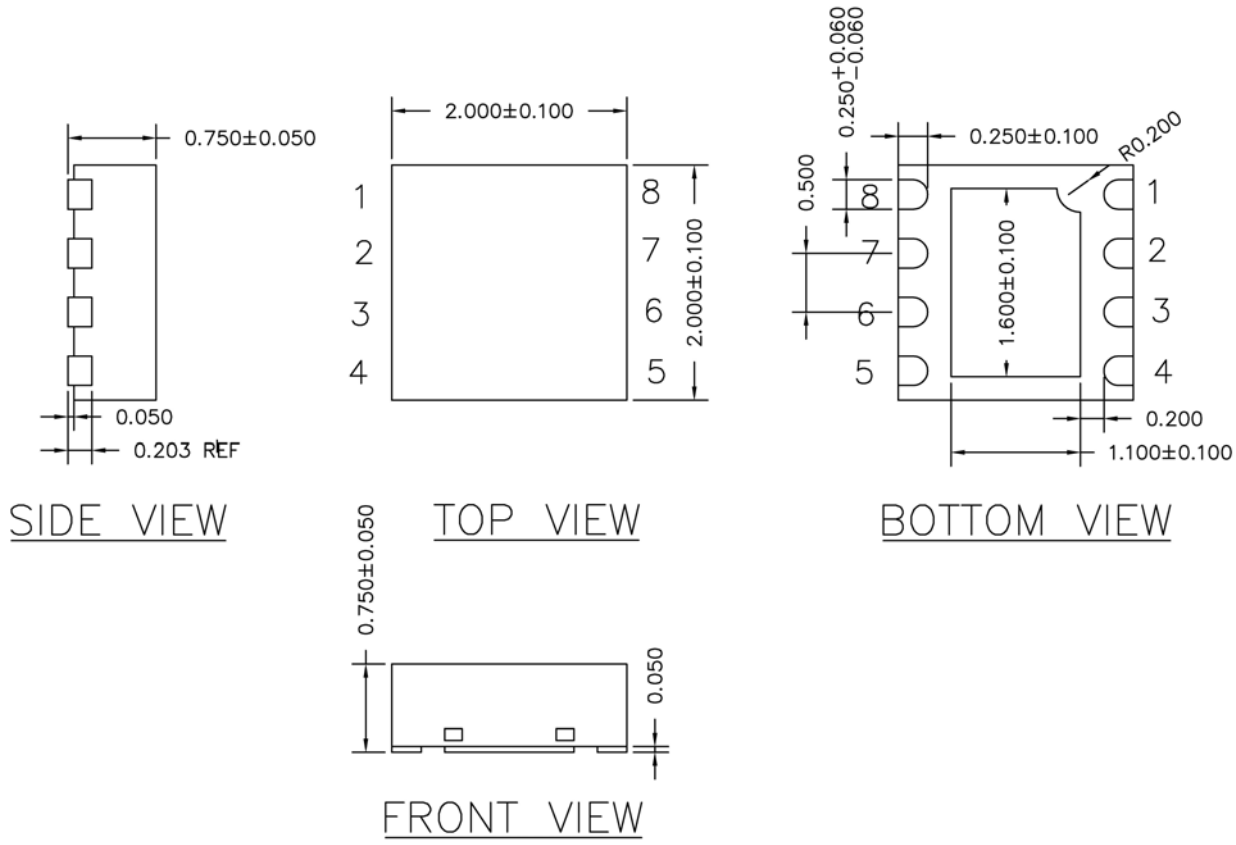


Figure5. The Package of DFN(2×2)-8