Power Modules
Passivated Assembled Circuit Elements, 50A

Available
RoHS* COMPLIANT

FEATURES

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1600 V_{RRM}/V_{DRM}
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL approved file E320098

PACE-PAK (D-19 Modified)

DESCRIPTION

The NP500 series of integrated power circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

PRODUCT SUMMARY	
I_O	50A
Type	Modules - Thyristor,Standard
Package	PACE-PAK (D-19 modified)
Circuit	Single phase, hybrid bridge common cathode, Single phase, hybrid bridge doubler connection, Single phase, all SCR bridge

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUE	UNIT
I_O	80°C	50	A
I_{TSM}, I_{FSM}	50 Hz	550	A
	60 Hz	576	
I^2t	50 Hz	1510	A^2s
	60 Hz	1380	
$I^2\sqrt{t}$		15125	$A^2\sqrt{t}$
V_{RRM}	Range	400 to 1600	V
V_{ISOL}		2500	V
T_J		-40 to 125	°C
T_{stg}			

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM} MAXIMUM AT T_J MAXIMUM mA
NP501/NP501W/NP501S	400	500	10
NP502/NP502W/NP502S	800	900	
NP503/NP503W/NP503S	1000	1100	
NP504/NP504W/NP504S	1200	1300	
NP505/NP505W/NP505S	1600	1700	

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUE	UNIT
Maximum DC output current at case temperature	I_O	Full bridge circuits			50	A
					80	°C
Maximum peak, one cycle non-reptitive on-state or forward current	I_{TSM}, I_{FSM}	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	550	A
		t = 8.3ms			576	
		t = 10ms	100%V_{RRM} reapplied		460	
		t = 8.3ms			484	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied		1510	kA^2s
		t = 8.3ms			1380	
		t = 10ms	100%V_{RRM} reapplied		1058	
		t = 8.3ms			972	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied I^2t for time tx = $I^2\sqrt{t} \cdot \sqrt{t}x$			15125	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$<I< π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.83	V
High level value of threshold voltage	$V_{T(TO)2}$	(I> π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.03	
Low level value of on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$<I< π x $I_{T(AV)}$), $T_J = T_J$ maximum			9.61	mΩ
High level value of on-state slope resistance	r_{t2}	(I> π x $I_{T(AV)}$), $T_J = T_J$ maximum			7.01	
Maximum on-state voltage drop	V_{TM}	I_{TM} =150A		T_J = 25 °C	1.4	V
Maximum forward voltage drop	V_{FM}	I_{FM} =150A		T_J = 25 °C	1.4	V
Maximum non-repetitive rate of rise of turned-on current	dI/dt	T_J = 125 °C from 0.67 V_{DRM} I_{TM} = 150A, I_g = 500 mA, t_r < 0.5 µs, tp > 6µs			200	A/µs
Maximum holding current	I_H	T_J = 25°C anode supply = 6V, resistive load			130	mA
Maximum latching current	I_L				250	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum critical rate of rise of off-state voltage	dV/dt	T_J = 125°C, exponential to 0.67 V_{DRM}, gate open	200	V/µs
Maximum peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	I_{RRM}, I_{DRM},	T_J = 125°C, gate open circuit	10	mA
Maximum peak reverse leakage current	I_{RRM}	T_J = 25°C	20	µA
RMS isolation voltage	I_{ISOL}	50 Hz, circuit to base, all terminals shorted, T_J = 25 °C, t = 1s	2500	V

TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNIT
Maximum peak gate power	P_{GM}			8	W
Maximum average gate power	$P_{G(AV)}$			2	
Maximum peak positive gate current	I_{GM}			2	A
Maximum peak negative gate voltage	$-V_{GM}$			10	V
Maximum gate voltage required to trigger	V_{GT}	T_J = -40°C	Anode supply = 6V resistive load	3	V
		T_J = 25°C		2	
		T_J = 125°C		1	
Maximum gate current required to trigger	I_{GT}	T_J = -40°C		90	mA
		T_J = 25°C		60	
		T_J = 125°C		35	
Maximum gate voltage that will not trigger	V_{GD}	T_J = 125°C, rated V_{DRM} applied		0.2	V
Maximum gate current that will not trigger	I_{GD}			2	mA

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum junction operating and storage temperature range	T_J, T_{stg}		-40 to 125	°C
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	1.00	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth and greased	0.10	
Mounting torque, base to heatsink (1)			4	Nm
Approximate weight			58	g
			2.0	oz.
Case style			PACK-PAK (D-19 modified)	

Note

(1) A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound

Ordering Information Table

Device code

N	P	50	5	W
①	②	③	④	⑤

1 - Nell Power semiconductors product

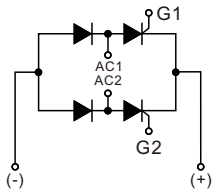
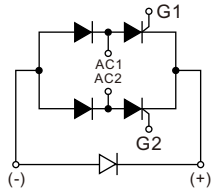
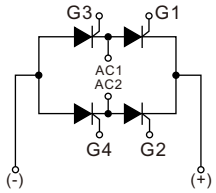
2 - Module type

3 - Current rating, 50 = 50A DC

4 - Voltage code
1 = 400V 4 = 1200V
2 = 800V 5 = 1600V
3 = 1000V

5 - Circuit configuration
Blank = Single Phase, Hybrid Bridge Common Cathode
W = Single Phase, Hybrid Bridge Common Cathode with a freewheeling diode
S = Single Phase, all SCR Bridge

CIRCUIT CONFIGURATION

CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	SCHEMATIC DIAGRAM	TERMINAL POSITIONS
Single phase, hybrid bridge common cathode	Blank		
Single phase, hybrid bridge common cathode with a freewheeling diode	W		
single phase, all SCR bridge	S		

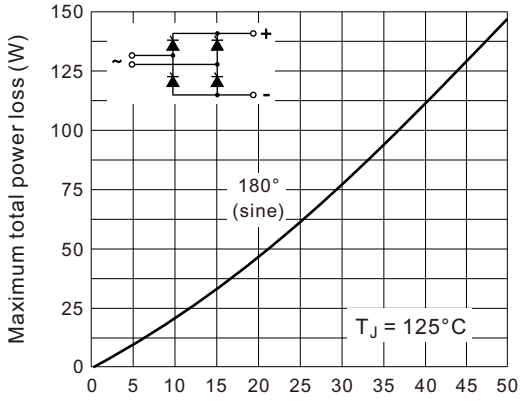
CODING(1)

CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	BASIC SERIES
Single phase, hybrid bridge common cathode	Blank	NP50X
Single phase, hybrid bridge common cathode with a freewheeling diode	W	NP50XW
single phase, all SCR bridge	S	NP50XS

Note

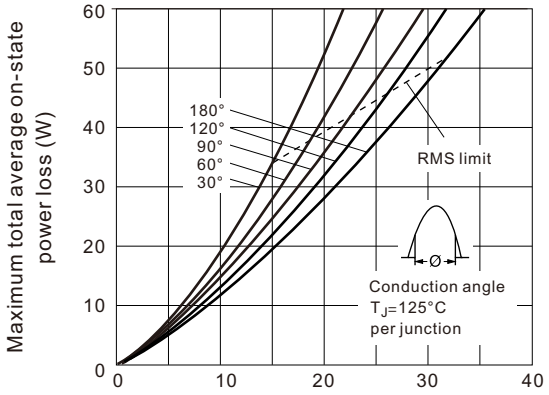
(1) To complete code refer to voltage Ratings table, i.e.: For 1600V of NP50XW, complete code is NP505W.

Fig.1 Total Power Loss



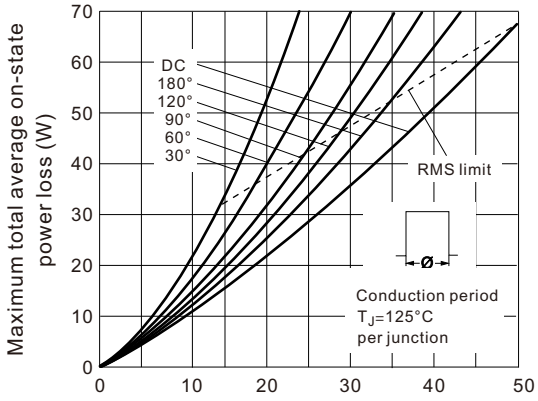
Total output current (A)

Fig.2 On-state power loss characteristics



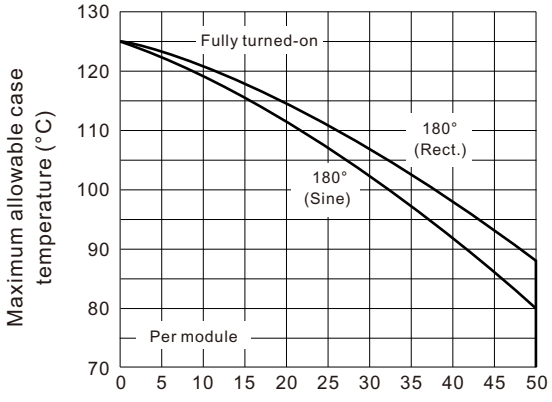
Average on-state current (A)

Fig.3 On-state power loss characteristics



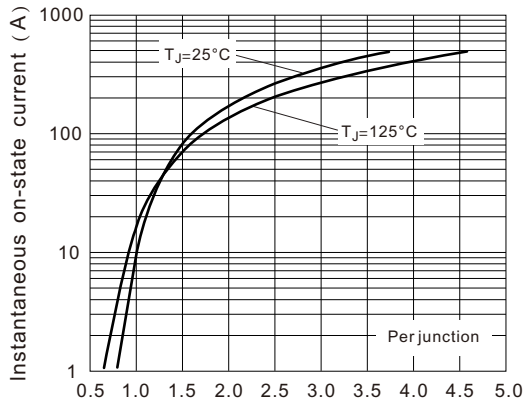
Average on-state current (A)

Fig.4 Current ratings characteristics



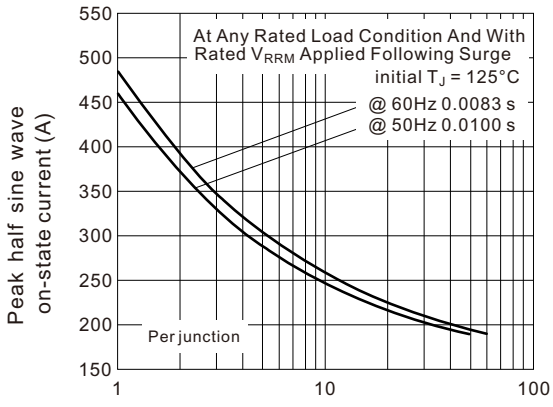
Total output current (A)

Fig.5 On-state voltage drop characteristics



Instantaneous on-state voltage (V)

Fig.6 Maximum non-repetitive surge current



Number of equal amplitude half cycle current pulses (N)

Fig.7 Maximum non-repetitive surge current

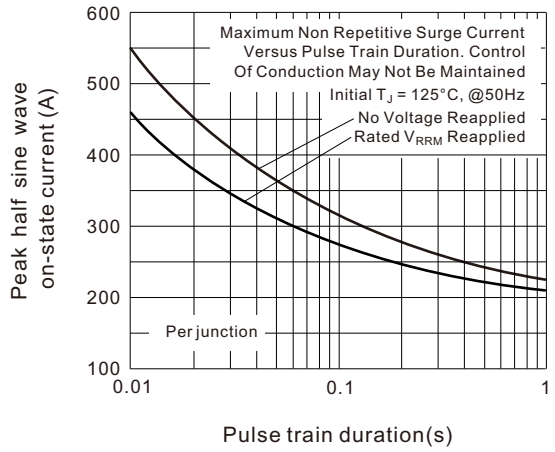


Fig.8 Thermal Impedance Z_{thJC} characteristics

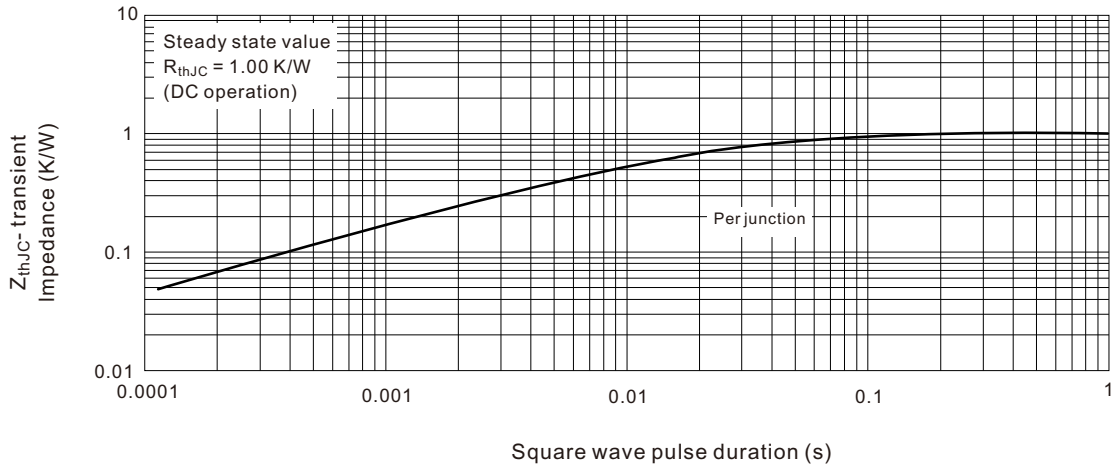
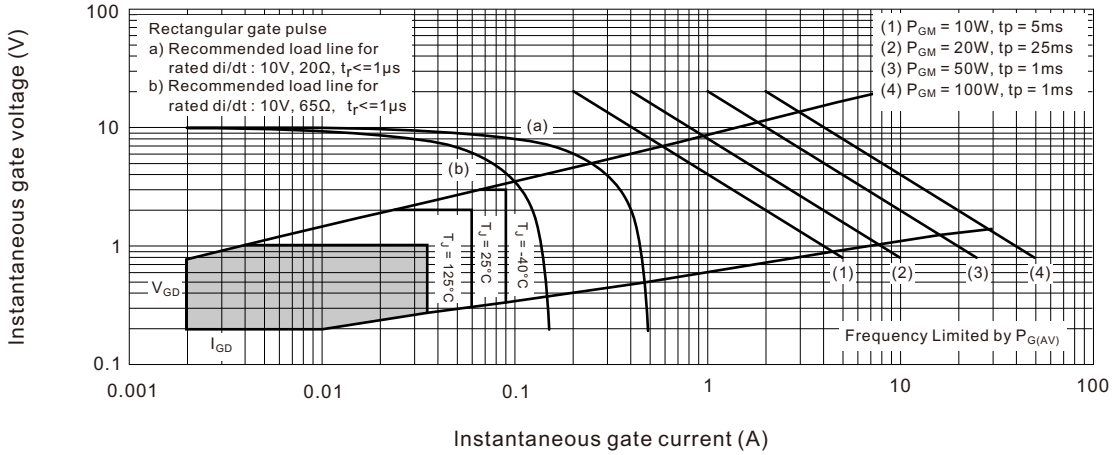
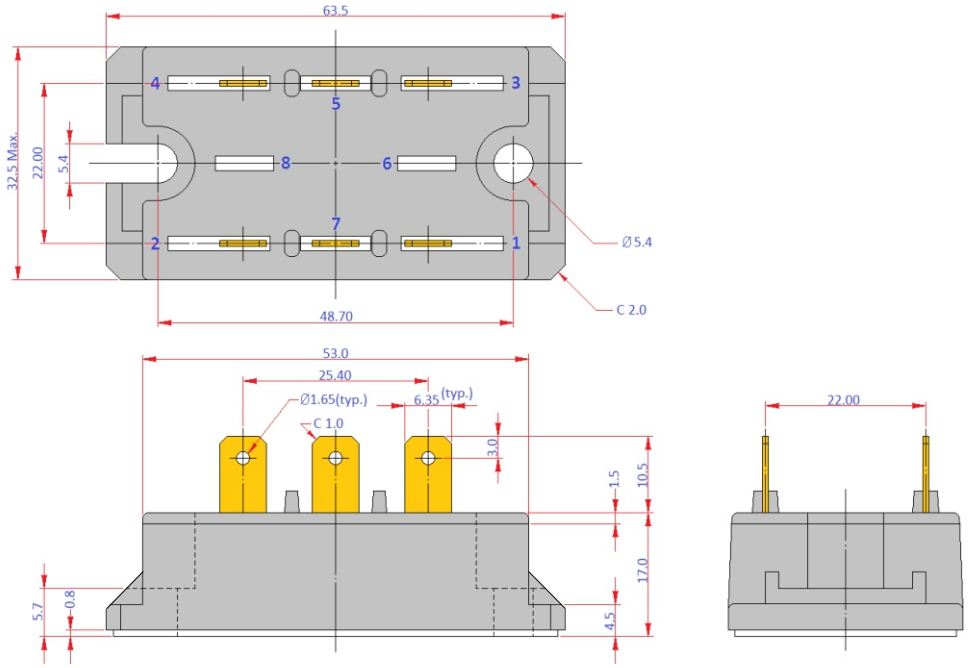


Fig.9 Gate characteristics



D-19 PACK-PAK (Modified)



All dimensions in millimeters