National Semiconductor

February 1996

NM29N16
16 MBit (2M x 8 Bit) CMOS NAND FLASH E²PROM

General Description

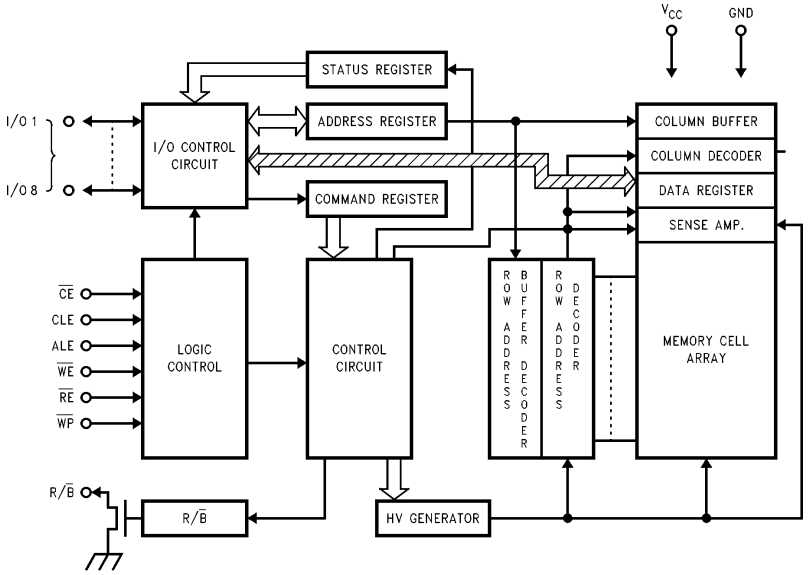
The NM29N16 is a 16 Mbit (2 Mbyte) NAND FLASH. The device is organized as an array of 512 blocks, each consisting of 16 pages. Each page contains 264 bytes. All commands and data are sent through eight I/O pins. To read data, a page is first transferred out of the array to an on-chip buffer. Sending successive read pulses ($\overline{RE}$ low) reads out successive bytes of data. The erase operation is implemented in either a single block (4 kbytes) or on multiple blocks at the same time. Programming the device requires sending address and data information to the on-board buffer and then issuing the program command. Typical program time for 264 bytes is 400 μs. All erase and program operations are internally timed.

The NM29N16 incorporates a number of features that make it ideal for portable applications requiring high density storage. These features include single 5V operation, high read/write endurance (250k cycle), and low current operation (15 mA during reads). The device comes in a TSOP Type II package which meets the requirements of PCMCIA cards. The NM29N16 is suited for numerous applications such as Solid State Drives (SSD), Audio Recording, and Image Storage for digital cameras.

Features

- Single 5V ±10% power supply
- Write/Erase endurance of 250,000 cycles, target of 1,000,000 cycles
- Fast Erase/Program Times
  - — Average Program Time of 400 μs/264 bytes
  - — Typical Block Erase Time of 6 ms
- Organized as 512 blocks, each consisting of 16 pages of 264 bytes
  - — Read/Program in pages of 264 bytes
  - — Erase in Blocks of 4 kbytes
- High Performance Read Access times
  - — Initial 25 μs page transfer
  - — Sequential 80 ns access
- Low Operating Current (typical)
  - — Typical Read current of 15 mA
  - — Typical Program current of 40 mA
  - — Typical Erase current of 20 mA
  - — Standby current less than 100 μA (CMOS)
- Command Register for Mode Control:
  - — Read
  - — Auto Page Program
  - — Auto Block Erase
  - —Reset
  - —Suspend/Resume
  - —Status Read
- 400 mil TSOP Type II Package
- JEDEC standard pinout

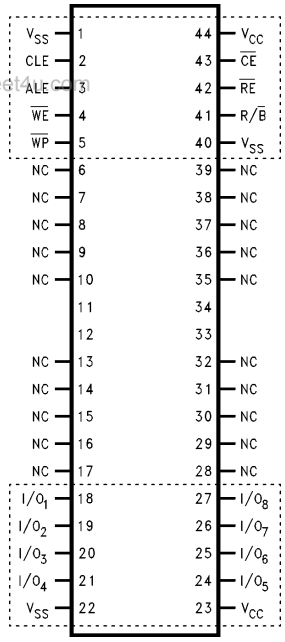
Block Diagram



TL/D/11915–1

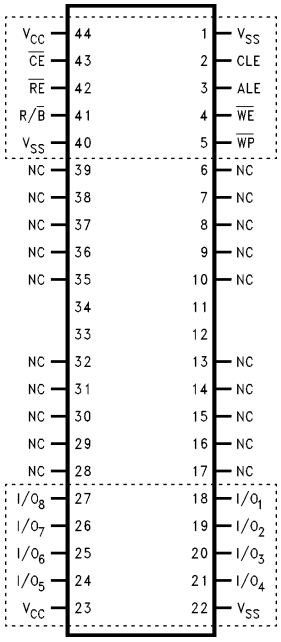
Pin Connection (Top View)

NM29N16S



TL/D/11915–2

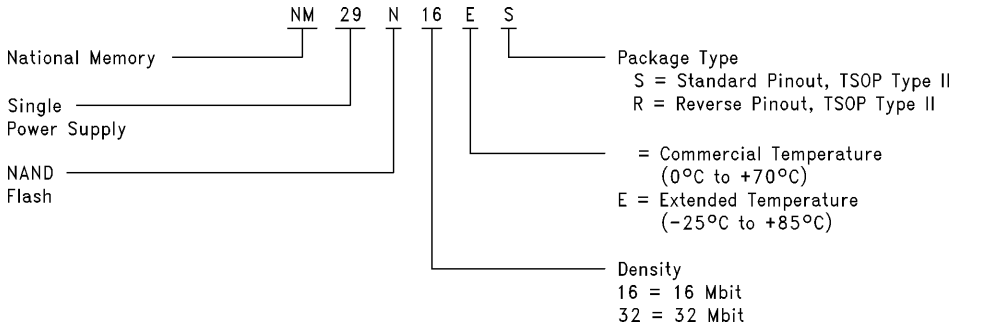
NM29N16R



TL/D/11915–3

Pin Assignment

I/O_{I-8}	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
$R/\overline{B}$	Ready/Busy
V_{CC}/V_{SS}	Power Supply/Ground



TL/D/11915–85

Number of Valid Blocks (1)

Symbol	Parameter	NM29N16			Units
		Min	Typ	Max	
N_{VB}	Valid Block Number	502	508	512	Blocks

Note 1: The NM29N16S/R may include unusable blocks. Refer to notification (17) toward the end of this document.

Capacitance* (T_A = +25°C, f = 1 MHz)

Symbol	Parameter	Condition	Min	Type	Max	Units
C_{IN}	Input	V_{IN} = 0V		5	10	pF
C_{OUT}	Output	V_{OUT} = 0V		5	10	pF

*This parameter is periodically sampled and is not 100% tested

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply (V_{CC})	−0.6V to 7.0V
Input Voltage (V_{IN})	−0.6V to 7.0V
Input/Output Voltage ($V_{I/O}$)	−0.6V to V_{CC} ±0.5V (≤7V)
Power Dissipation (P_D)	0.5W
Soldering Temperature (T_{solder}) (10 seconds)	260°C
Storage Temperature (T_{stg})	−55°C to 150°C
Operating Temperature (T_{opr})	0°C to 70°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Power Supply (V_{CC})	4.5	5.0	5.5	V
High Level Input Voltage (V_{IH})	2.4		V_{CC} + 0.5	V
Low Level Input Voltage (V_{IL})	−0.3*		0.8	V

* −2V (Pulse Width < 20 ns)

DC Operating Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V to V_{CC}				±10	μA
I_{CC01}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	t_{CYCLE} = 80 ns		15	30	mA
I_{CC02}	Operating Current (Serial Read)		t_{CYCLE} = 1 μs			5	mA
I_{CC03}	Operating Current (Command Input)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC04}	Operating Current (Data Input)	t_{CYCLE} = 80 ns			50	70	mA
I_{CC05}	Operating Current (Address Input)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC06}	Operating Current (Register Read)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC07}	Programming Current				40	60	mA
I_{CC08}	Erasing Current				20	40	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}				1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2V				100	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA		2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA				0.4	V
$I_{OL}(R/\overline{B})$	Output Current of (R/$\overline{B}$) Pin	V_{OL} = 0.4V			10		mA

Pin Functions

The NM29N16 is a sequential access memory which utilizes time sharing input of address and data information.

Command Latch Enable: CLE The CLE input signal is used to control the input of commands into the internal command register. The command is latched into the command register from the I/O port at the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE The ALE signal is used to control the input of either address information or input data into the internal address/data register. Address information is latched at the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable : $\overline{CE}$ The device goes into a low power standby mode during a read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in a busy state (R/$\overline{B}$ = L) such as during a program or erase operation and will not go into standby mode if a $\overline{CE}$ high signal is input.

Write Enable : $\overline{WE}$ The $\overline{WE}$ signal is used to strobe data into the I/O port.

Read Enable: $\overline{RE}$ The $\overline{RE}$ signal strobes data output. Data is available t_{REA} after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address + 1) with this falling edge.

I/O Port: I/O 1–8 The I/O 1–8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect : $\overline{WP}$ The $\overline{WP}$ signal is used to protect the device from inadvertent programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when the input signals are invalid.

Ready/Busy: R/$\overline{B}$ The R/$\overline{B}$ output signal is used to indicate the operating condition of the device. The R/$\overline{B}$ signal is in a busy state (R/$\overline{B}$ = L) during the program, erase or read operations and will return to a ready state (R/$\overline{B}$ = H) after completion. The output buffer of this signal is an open drain.

AC Test Conditions

Input Level	2.4V/0.4V
Input Comparison Level	2.2V/0.8V
Output Data Comparison Level	2.0V/0.8V
Output Load	1TTL & C_L (100 pF)

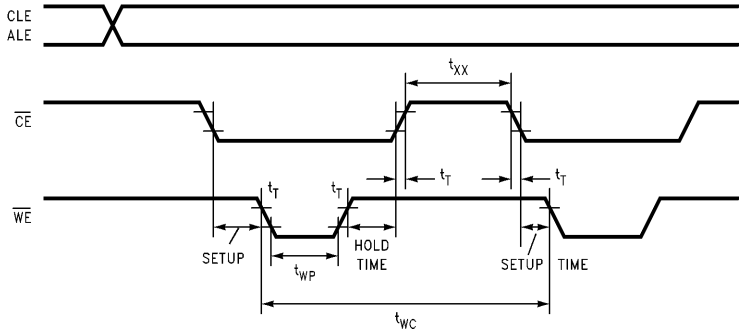
AC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Min	Max	Unit	Notes
t_{CLS}	CLE Setup Time	20		ns	
t_{CLH}	CLE Hold Time	40		ns	
t_{CS}	$\overline{CE}$ Setup Time	20		ns	
t_{CH}	$\overline{CE}$ Hold Time	40		ns	
t_{WP}	Write Pulse Width	40		ns	
t_{ALS}	ALE Setup Time	20		ns	
t_{ALH}	ALE Hold Time	40		ns	
t_{DS}	Data Setup Time	30		ns	
t_{DH}	Data Hold Time	20		ns	
t_{WC}	Write Cycle Time	80		ns	(1)
t_{WH}	$\overline{WE}$ High Hold Time	20		ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Falling Edge	100		ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20		ns	
t_{RC}	Read Cycle Time	80		ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)		45	ns	
t_{CEH}	$\overline{CE}$ High Time at the Last Address in Serial Read Cycle	250		ns	(3)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)		90	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	5	20	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance		30	ns	
t_{REH}	$\overline{RE}$ High Hold Time	20		ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Rising Edge	0		ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)		45	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)		55	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0		ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	50		ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	50		ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (Address Register Read, ID Read)	200		ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (Address Register Read, ID Read)	200		ns	
t_R	Memory Cell Array to Starting Address		25	μs	
t_{WB}	$\overline{WE}$ High to Busy		200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ low (Read Cycle)	150		ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (At Sequential Read)		200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at Read Mode)		100+ tr(R/$\overline{B}$)	ns	(2)
t_{RST}	Device Reset Time (Read/Program/Erase/Suspend)		10/20/1500/10	μs	

AC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ±10%) (Continued)

Note 1: In case that CLE, ALE, $\overline{CE}$ are input with clock, t_{WC} exceeds 80 ns. Transition time $t_T \leq 5$ ns

$$\frac{\text{set-up time}}{20\text{ ns}} + \frac{\text{hold time}}{40\text{ ns}} + \frac{t_{WP}}{40\text{ ns}} + \frac{t_{XX}}{} + \frac{4t_T}{20\text{ ns}}$$

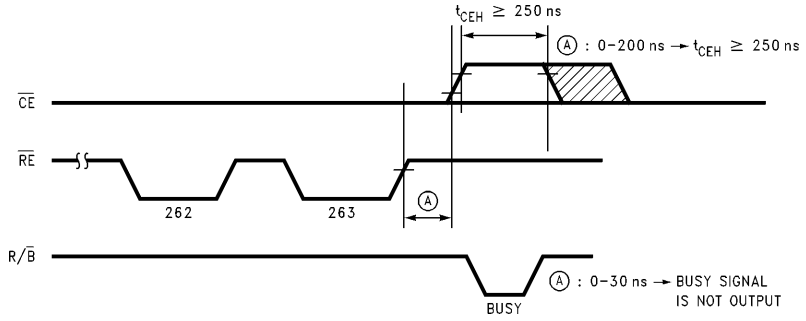


TL/D/11915–5

Note 2: $\overline{CE}$ high to Ready time depends on Pull up resister tied to R/$\overline{B}$ pin. (Refer to notification (10) toward the end of this document.)

Note 3: In the case that $\overline{CE}$ turns to a high level after accessing the last address (263) in read mode (1) or (2), $\overline{CE}$ high time must keep equal to or greater than 300 ns when the delay time of $\overline{CE}$ against $\overline{RE}$ is 0 to 200 ns as shown below.

In the second case, the device will not turn to a ''Busy'' state when the $\overline{CE}$ delay time is less than 30 ns.



TL/D/11915–6

Programming and Erasing Characteristic (T_A = 0°C to + 70°C, V_{CC} = 5V ±10%)

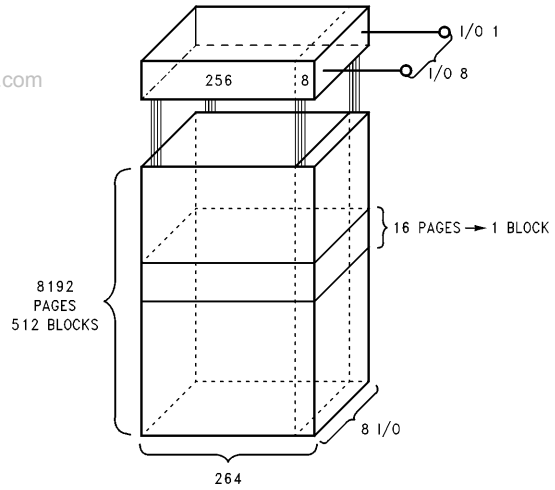
Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_{PROG}	Average Programming Time		300–1000	5000	μs	
N	Divided Number on Same Page			10	Cycles	(1)
t_{BERASE}	Block Erasing Time	6	6	100	ms	
$t_{MBERASE}$	Multi-Block Erasing Time	6–12	6–12	130	ms	(2)
t_{SR}	Suspend Input to Ready			1.5	ms	
$N_{W/E}$	Number Write/Erase Cycles			2.5×10^5	Cycles	

Note 1: Refer to the notification (16) toward the end of this document

Note 2: $t_{MBERASE}$ depends on the number of blocks to be erased (min 6 ms + 15 μs x Erase block number)

Schematic Cell Layout and Address Assignment

Programming is done in page units of 264 Bytes while the erase operation is carried out in blocks of 4 kBytes.



TL/D/11915–28

FIGURE 1. NM29N16 Schematic Cell Layout

A page consists of 264 bytes in which 256 bytes are for main memory and 8 bytes are for redundancy or other uses.

1 page = 264 bytes

1 Block = 264 bytes x 16 pages = (4k + 128) bytes

Total device density = (264 bytes) x (16 pages) x (512 block)
= 17.3 MBits (2.162 MBits)

The address is acquired through the I/O port using three consecutive clock cycles as shown in Table I.

TABLE I. Addressing

	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	I/O_8
First Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
Second Cycle	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
Third Cycle	A_{16}	A_{17}	A_{18}	A_{19}	A_{20}	*L	*L	*L

* I/O 6–8 at the third cycle must be set low

A_0–A_7 : Byte (Column) Address
A_8–A_{11} : Page Address in Block
A_{12}–A_{20} : Block Address

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read, Erase Suspend, and Reset are controlled by the twelve different command operations shown in Table III. The Address, Command Input and Data Input/Output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals as shown in Table II.

TABLE II. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	↑	H	*
Data Input	L	L	L	↑	H	*
Address Input	L	H	L	↑	H	*
Address Output	L	H	L	H	↓	*
Serial Data Output	L	L	L	H	↓	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

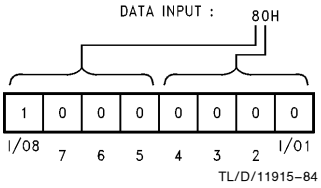
H: V_{IH}, L: V_{IL} *: V_{IH} or V_{IL}

Operation Mode: Logic and Command Tables (Continued)

TABLE III. Command Table (HEX Data)

	First Cycle	Second Cycle	Acceptable Command During Busy
Sequential Data Input	80		
Read Mode (1)	00		
Read Mode (2)	50		
Reset	FF		Yes
Auto Program	10		
Auto Block Erase	60	D0	
Suspend in Erasing	B0		Yes
Resume	D0		
Status Read	70		Yes
ID Read	90		

Bit Assignment of HEX Data (Example)



TL/D/11915–84

Once the device is set into Read mode by ''00H'' or ''50H'' command, additional Read commands are not needed for sequential page read operations. Table III shows the operation mode for Reads.

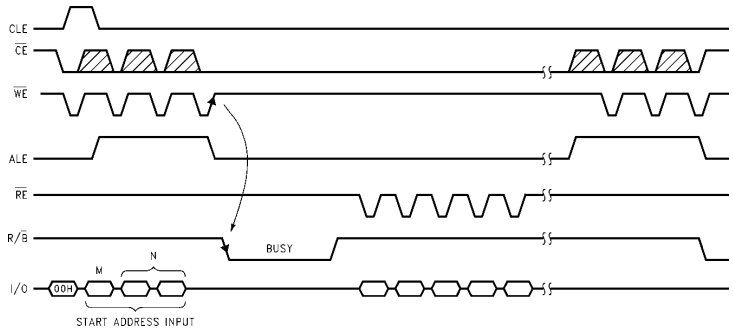
TABLE IV. Operation Mode for Reads

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O_1–I/O_8	Power
Read Mode	L	L	L	H	L	Data Output	Active
Output Deselect	L	L	L	H	H	High Impedance	Active
Standby	L	L	H	H	*	High Impedance	Standby

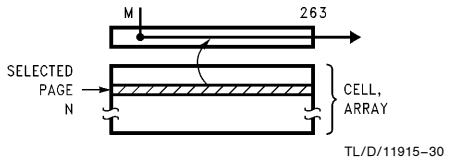
Device Operation

READ MODE (1)

The Read mode (1) is set by issuing a ''00H'' command to the command register. Refer to *Figure 2* below for timing details and block diagram.



TL/D/11915–29



TL/D/11915–30

A data transfer operation from the cell array to the register starts at the rising edge of $\overline{WE}$ in the third cycle (after latching the address information). The device will be in a busy state during this transfer period.

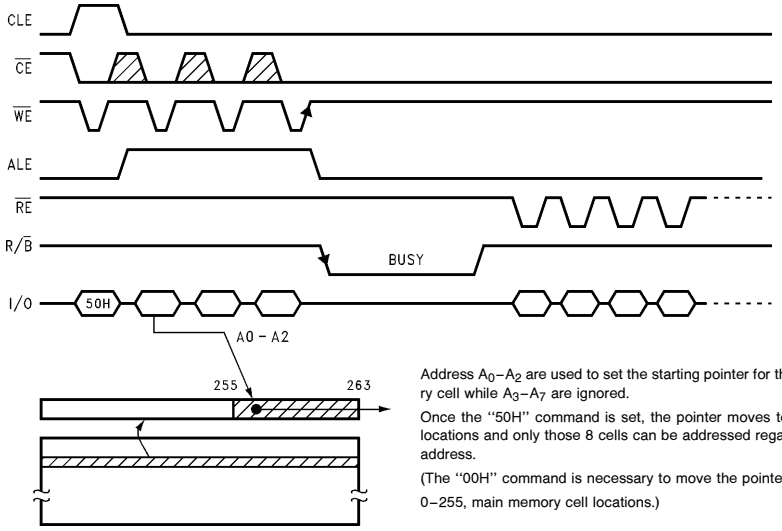
After the transfer period the device returns to a ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the designated starting pointer indicated during the address input cycle.

FIGURE 2. Read Mode (1) Operation

Device Operation (Continued)

READ MODE (2)

The Read mode (2) is the same timing as Read mode (1) but it is used to access information in the extra 8 byte redundancy area of the page. The starting pointer is therefore assigned between byte 256 and 263.



Address A_0–A_2 are used to set the starting pointer for the redundant memory cell while A_3–A_7 are ignored.

Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 8 cells can be addressed regardless of the A_3–A_7 address.

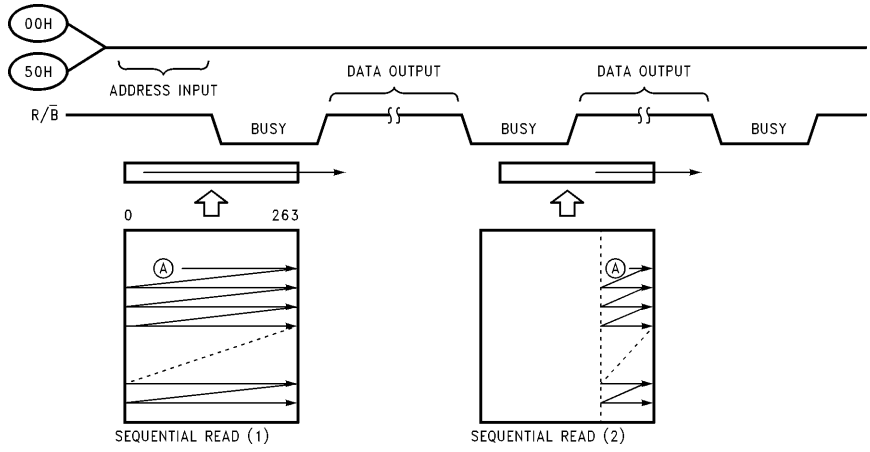
(The "00H" command is necessary to move the pointer back to the 0–255, main memory cell locations.)

TL/D/11915–31

FIGURE 3. Read Mode (2) Operation

SEQUENTIAL READ (1) (2)

This mode allows sequential read without the additional address input



TL/D/11915–32

FIGURE 4. Sequential Read

Sequential Read mode (1) outputs the address 0 to 263 while Sequential Read mode (2) outputs the redundant address location only. When the pointer reaches the last address, the device continues to output last data with each $\overline{RE}$ clcck signal.

Device Operation (Continued)

STATUS READ

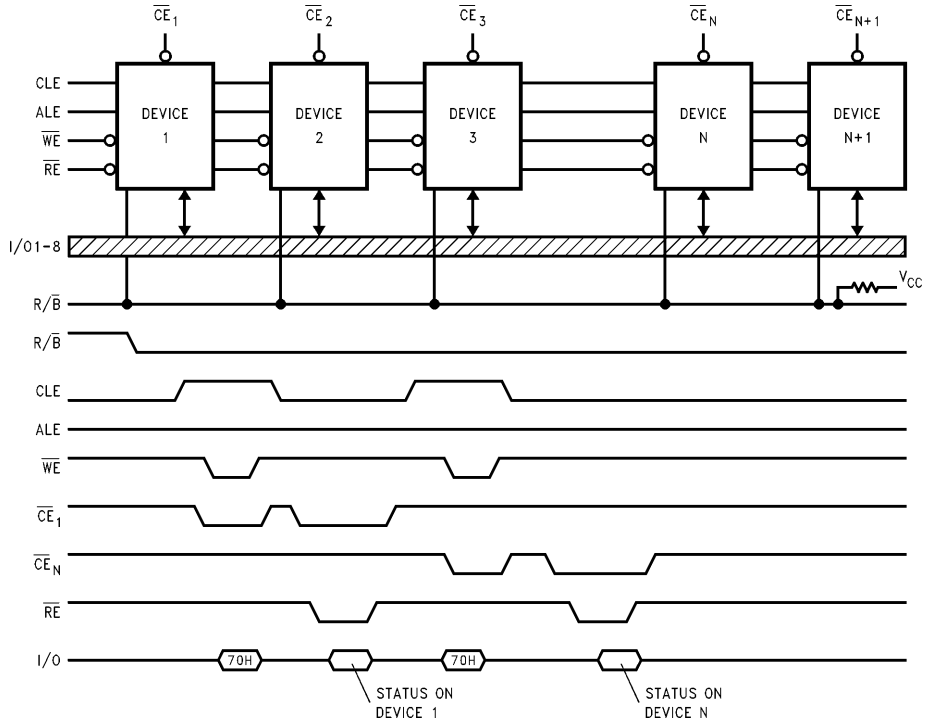
The NM29N16S/R automatically implements the execution and verification of the program and erase operations. The status read function is used to monitor the Ready/Busy status of the device, determines the pass/fail result of a program or erase operation, and determines if the device is in a suspend or protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a ''70H'' command input. The resulting information is outlined in Table V.

TABLE V. Status Output Table

	Status	Output	
I/O 1	Pass/Fail	Pass: ''0''	Fail : ''1''
I/O 2	Not Used	''0''	
I/O 3	Not Used	''0''	
I/O 4	Not Used	''0''	
I/O 5	Not Used	''0''	
I/O 6	Suspend	Suspended: ''1''	Not suspended: ''0''
I/O 7	Ready/Busy	Ready: ''1''	Busy: ''0''
I/O 8	Write Protect	Protect: ''0''	Not Protect: ''I''

The Pass/Fail status in I/O 1 is only valid when the device is in the Ready state. The device will always indicate a Pass status while in the Busy state at Read mode.

Application example with multiple devices is shown in *Figure 5* below.



TL/D/11915–33

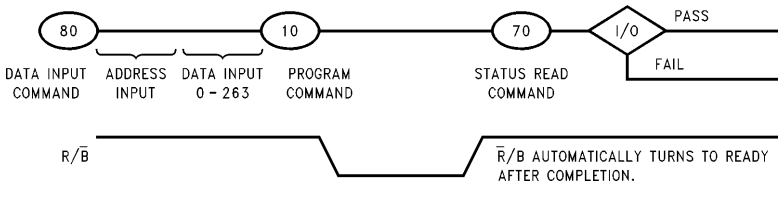
FIGURE 5. Status Read Timing Application Example

Note: If the R/$\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the status Read function can be used to determine the status of each individually selected device.

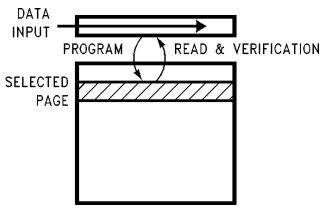
Device Operation (Continued)

AUTO PAGE PROGRAM

The NM29N16S/R implements the automatic page program operation by receiving a ''10H'' program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detail timing chart).



TL/D/11915–34



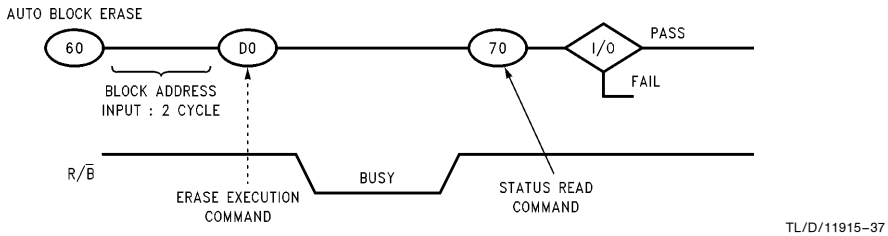
TL/D/11915–35

The data is transferred (programmed) from the register to the selected page at the rising edge of $\overline{WE}$ following the ''10H'' command input. The programmed data is transferred back to the register after programming to be automatically verified by the device. If the program does not succeed, the above program/verify operation is repeated by the device until success or the maximum loop number set in the device.

FIGURE 6. Auto Page Program

AUTO BLOCK ERASE

The block erase operation starts with the rising edge of $\overline{WE}$ after the erase execution command ''D0H'' which follows the erase setup command ''60H''. This two cycle process for erase operations acts as an extra layer protection from accidental erasure of data due to possible external noise issues. The device automatically executes the erase and verify operations.



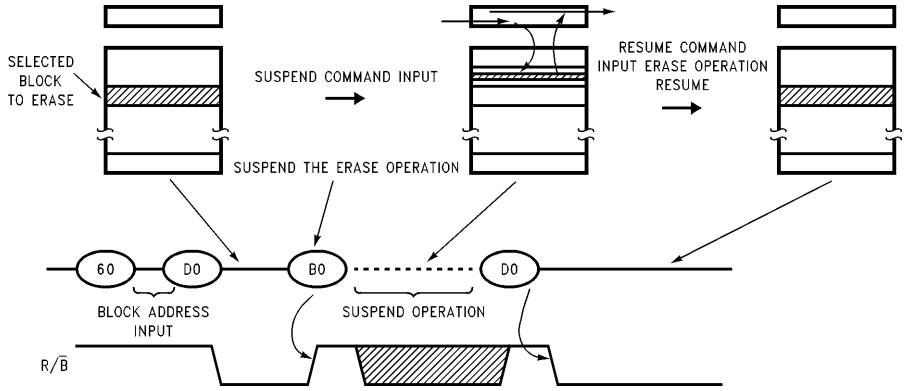
TL/D/11915–37

FIGURE 7. Auto Block Erase Operation

Device Operation (Continued)

SUSPEND/RESUME

Because an erase operation can keep the device in a busy state for an extended period of time, the NM29N16 has the ability to suspend the erase operation to allow program or read operations to be performed on the device. The block diagram and command sequence on this operation are shown as below. (Refer to the detail timing chart).



TL/D/11915–40

FIGURE 8. Suspend/Resume Erase Operation

The B0...D0 suspend/resume cycle can be repeated up to 20 times during an erase operation. After the resume command input, the erase operation continues from the point at which it left off and does not have to restart.

Device Operation (Continued)

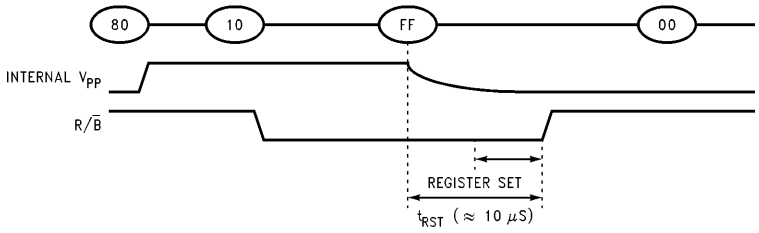
RESET

The reset mode compulsorily stops all operations. For example, in the case of a program or erase operation, the regulated voltage is discharged to 0V and the device will go to a wait state. The address and data register are set as follows after a reset:

- Address Register: All ''0''
- Data Register: All ''1''
- Operation Mode: Wait State

The response after ''FFH'' reset command input during each operation is as follows:

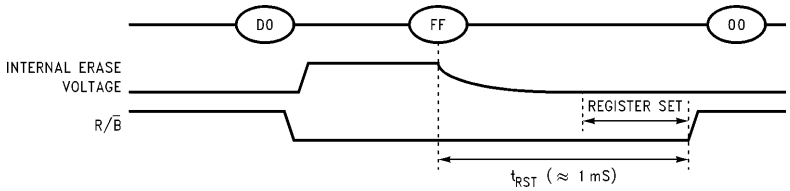
- In the case that reset (FFH) command is input during programming:



TL/D/11915–41

FIGURE 9. Reset During Programming

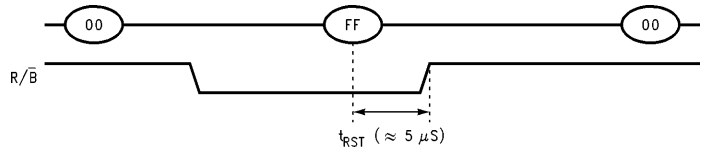
- In the case that reset (FFH) command is input during erasing:



TL/D/11915–42

FIGURE 10. Reset During Erasing

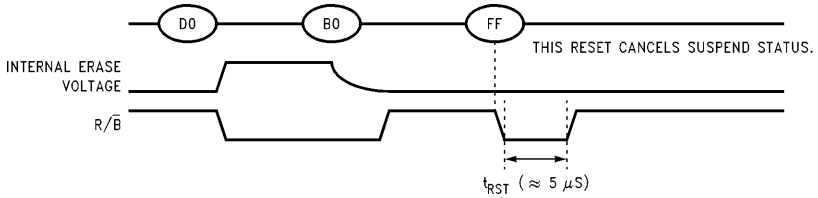
- In the case that reset (FFH) command is input during read operation:



TL/D/11915–43

FIGURE 11. Reset During Read

- In the case that reset (FFH) command is input during suspend:

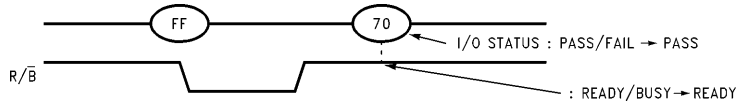


TL/D/11915–44

FIGURE 12. Reset During Suspend

Device Operation (Continued)

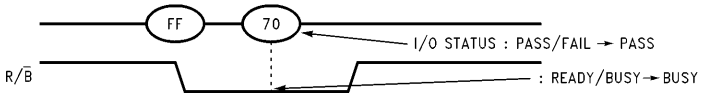
- In the case that the status read command (70H) is input after reset:



TL/D/11915–45

FIGURE 13. Read After Reset

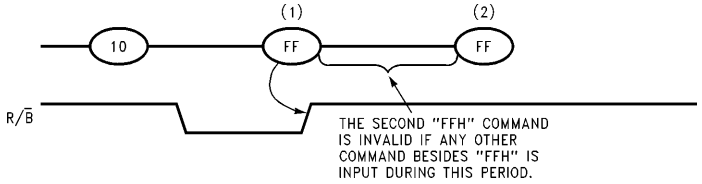
- However the following operation is prohibited. If the following operation is executed, set up for address and data register can not be guaranteed.



TL/D/11915–46

FIGURE 14. Prohibited Reset

- In the case that the reset command is input in succession:

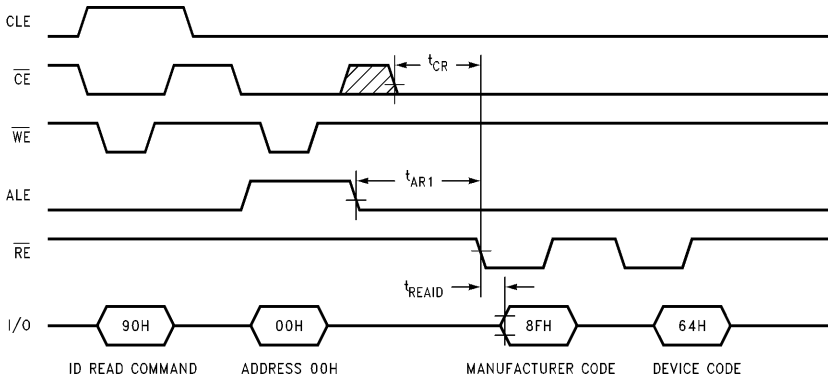


TL/D/11915–47

FIGURE 15. Consecutive Resets

ID READ

The NM29N16S/R contains an ID code to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:



TL/D/11915–48

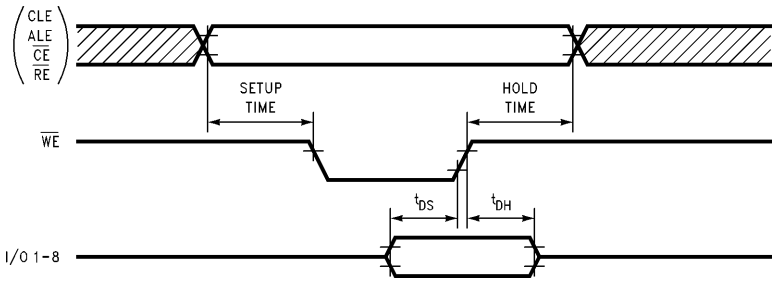
TABLE VI. Code Table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker Code	1	0	0	0	1	1	1	1	8FH
Device Code	0	1	1	0	0	1	0	0	64H

Refer to the timing specifications for the access time of t_{READ}, t_{CR}, t_{AR2}.

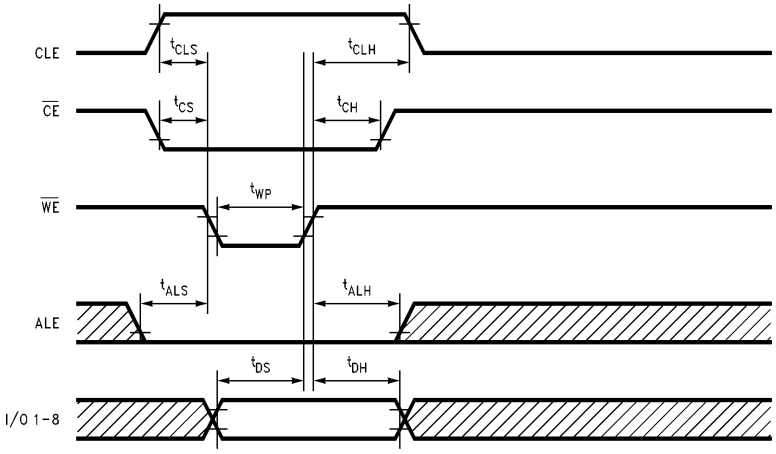
Timing Diagrams

Latch Timing Chart for Command/Address/Data



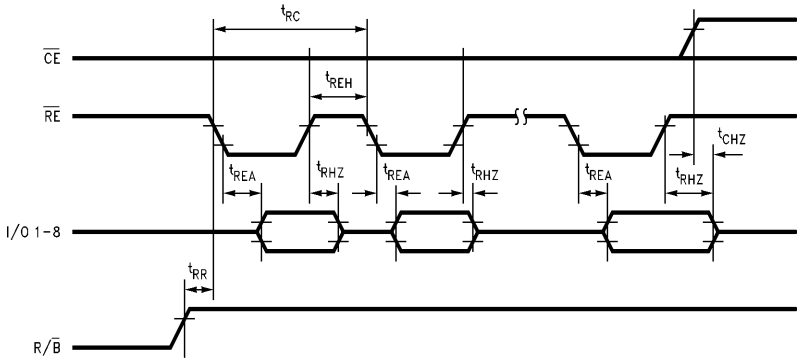
TL/D/11915–7

Command Input Cycle



TL/D/11915–8

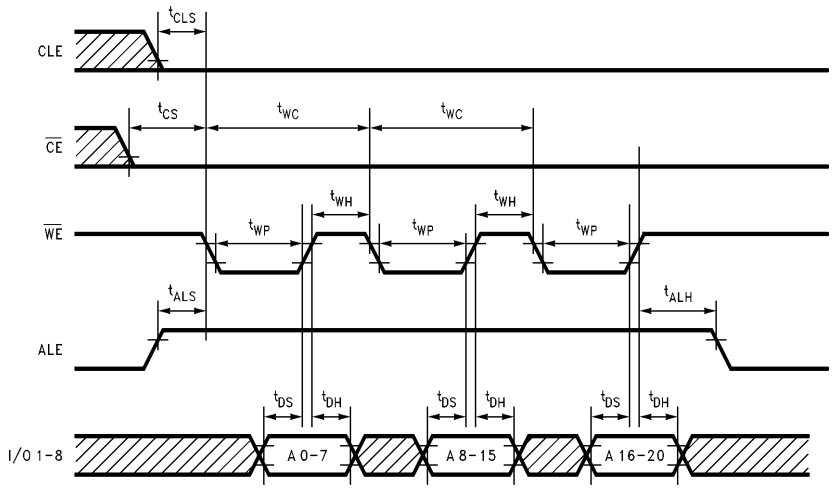
Serial Read Cycle



TL/D/11915–26

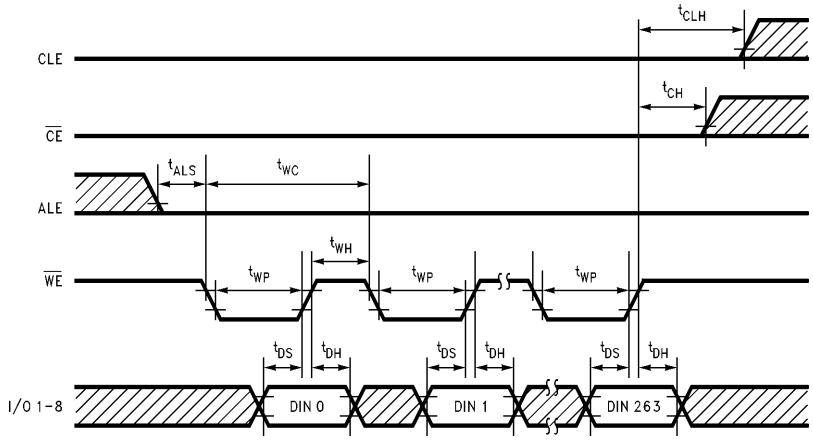
Timing Diagrams (Continued)

Address Input Cycle



TL/D/11915–9

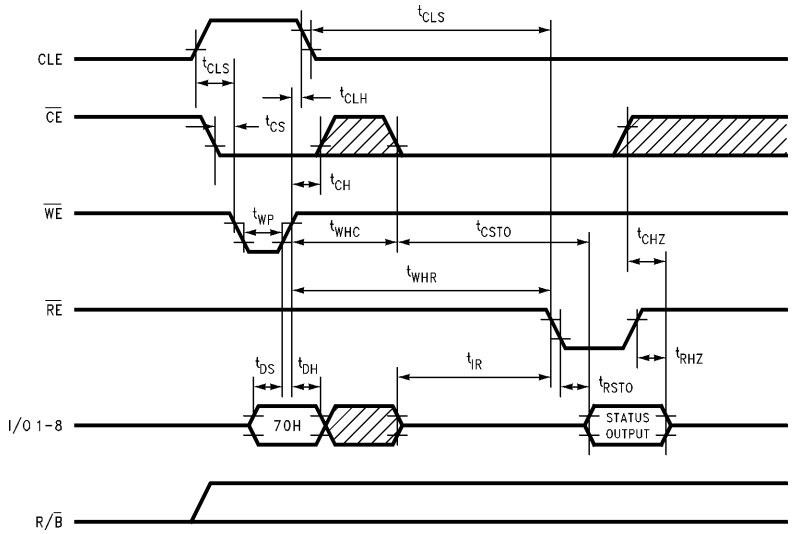
Data Input Cycle



TL/D/11915–10

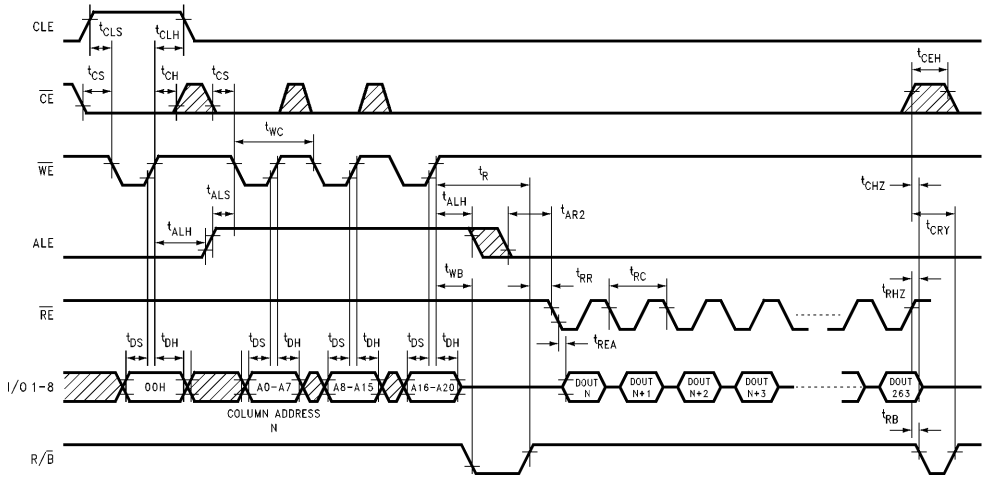
Timing Diagrams (Continued)

Status Read Cycle



TL/D/11915–11

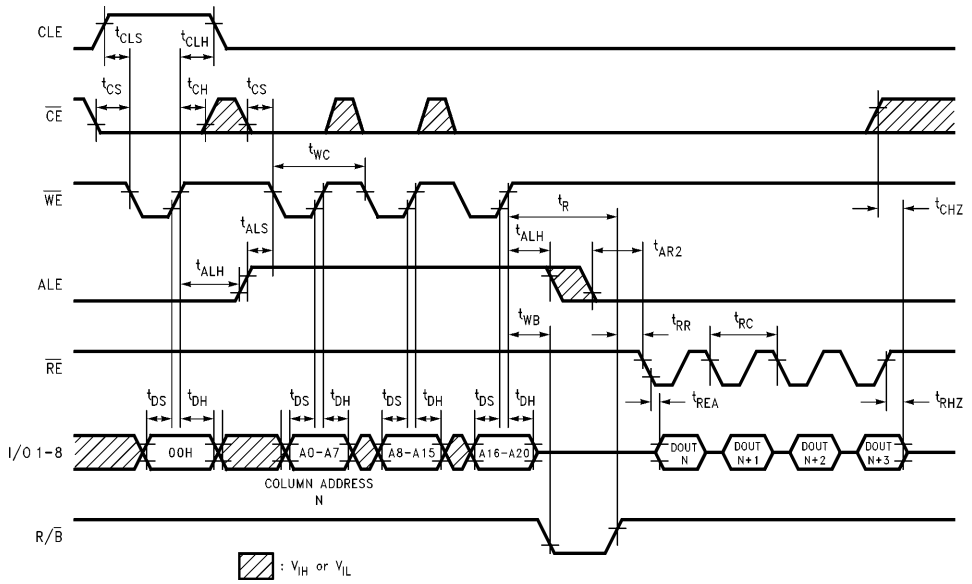
Read Cycle (1)



TL/D/11915–12

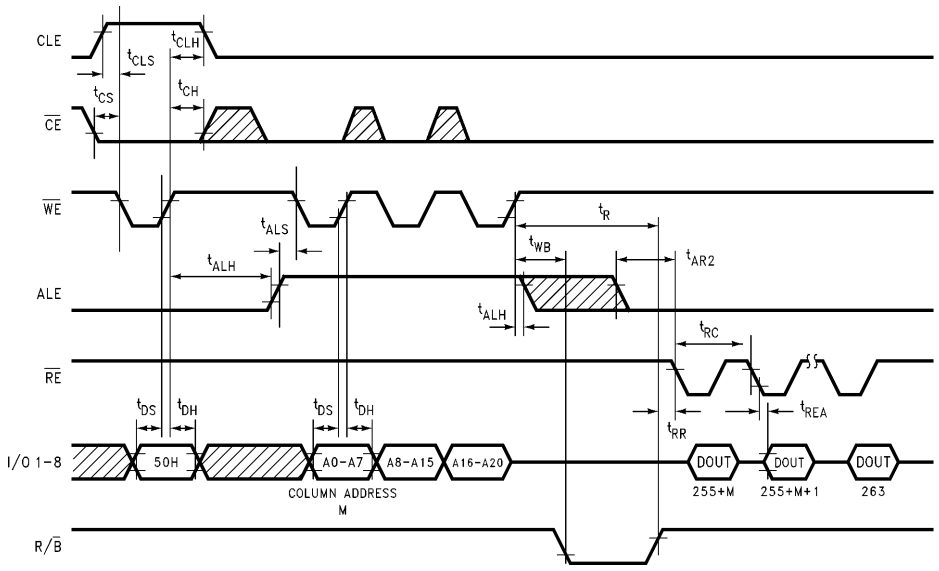
Timing Diagrams (Continued)

Read Cycle (1): Terminated by $\overline{CE}$



TL/D/11915–13

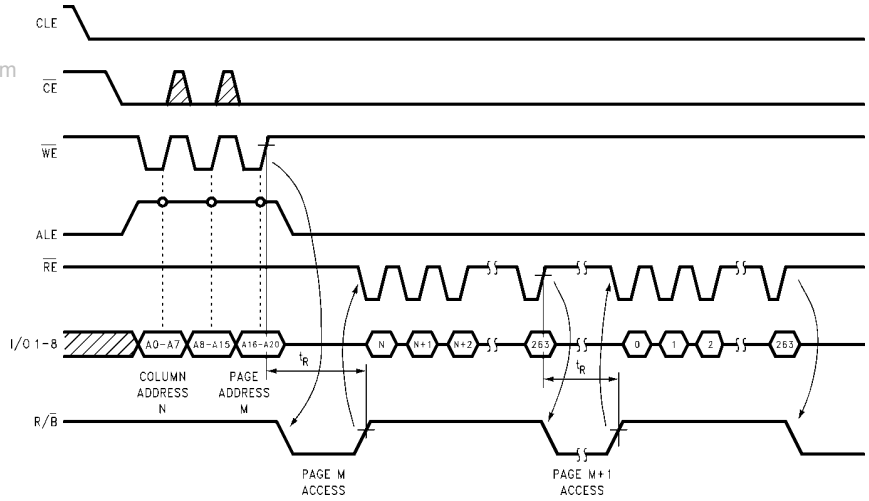
Read Cycle (2)



TL/D/11915–14

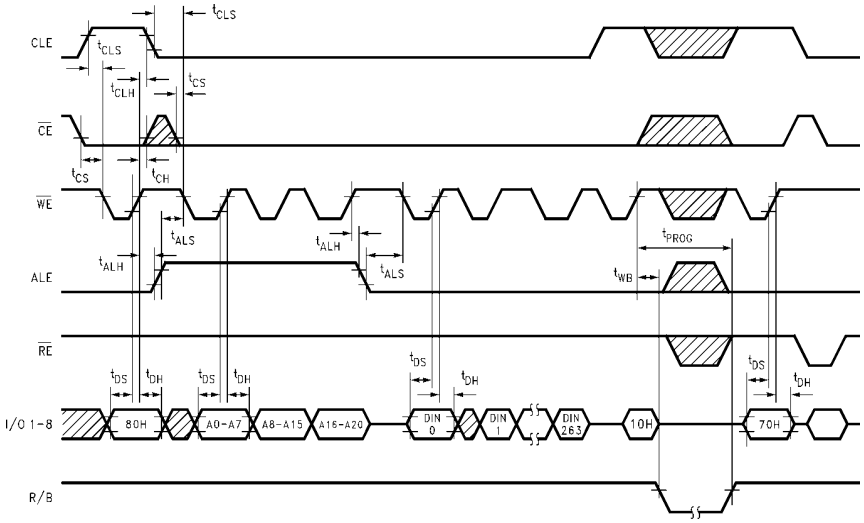
Timing Diagrams (Continued)

Sequential Read Timing



TL/D/11915–15

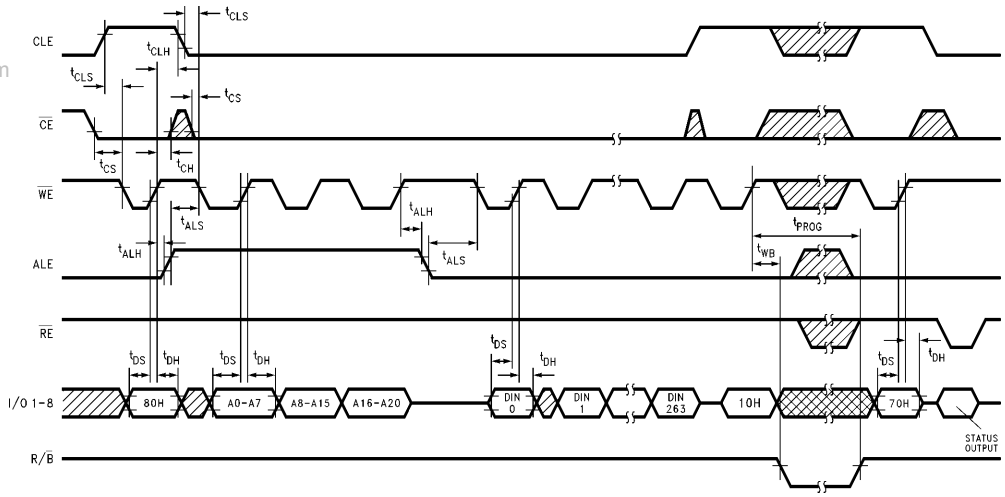
Auto Program Timing Chart



TL/D/11915–16

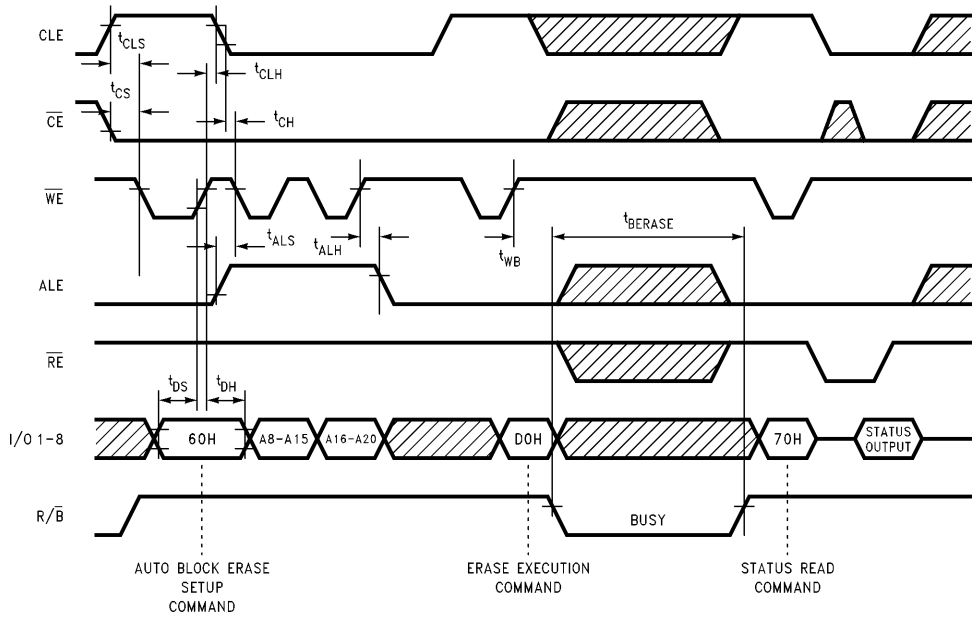
Timing Diagrams (Continued)

Auto Program



TL/D/11915–17

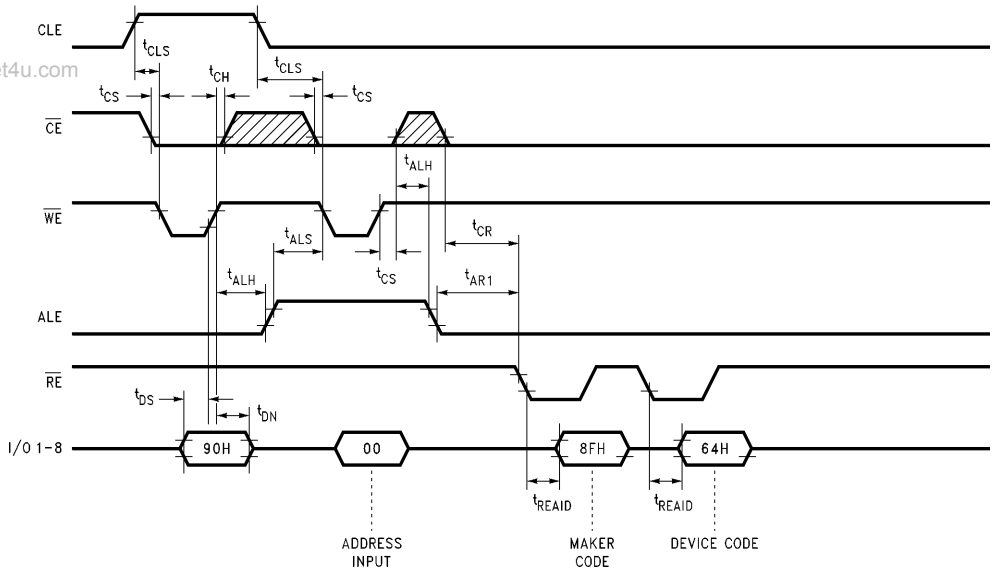
Auto Block Erase Timing



TL/D/11915–19

Timing Diagrams (Continued)

ID Read Operation



TL/D/11915–24

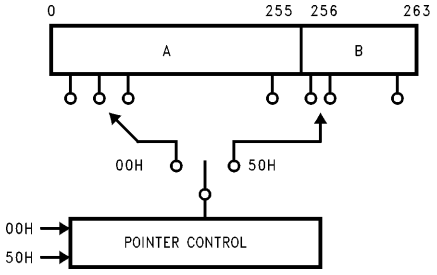
Supplementary Device Operation

(1) PROHIBITION OF UNSPECIFIED COMMANDS

The operation commands are listed in Table III. Data input as a command other than the specified commands in Table III is prohibited. Stored data may be corrupted if an unspeclfied command is entered during the command cycle.

(2) POINTER CONTROL FOR "00H", "50H"

The NM29N16S/R has two read modes to set the destination of the pointer in either the maln memory area of a page or the redundancy area. The pointer can be designated at any location between 0 and 255 in read mode (1) and between 256 and 263 in read mode (2). *Figure 16* shows the block diagram of their operations.



TL/D/11915–49

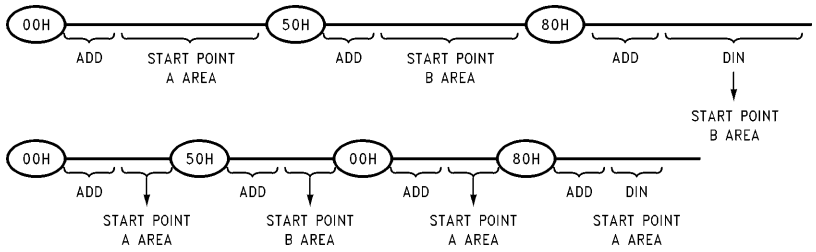
FIGURE 16. Pointer Control

Supplementary Device Operation (Continued)

The pointer is set to region ''A'' by the ''00H'' command and to region ''B'' by the ''50H'' command.

(Example)

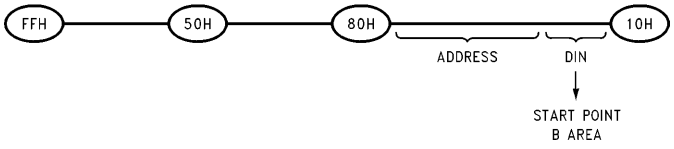
The ''00H'' command needs to be input to set the pointer back to region ''A'' when the pointer exists in region ''B''.



TL/D/11915–50

FIGURE 17. Example for Pointer Set

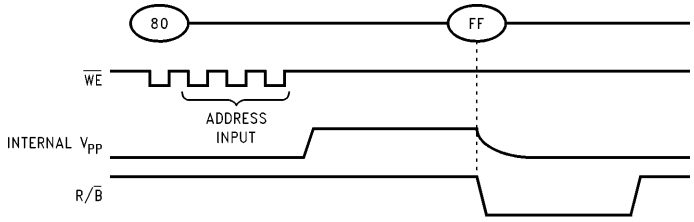
In case of programming into region ''B'' only by setting the start point in region ''B'' with ''50H'' command, it is necessary to reset the content of data register to ''1'' by ''FFH'' command.



TL/D/11915–25

(3) ACCEPTABLE COMMANDS AFTER SERIAL INPUT COMMAND OF "80H"

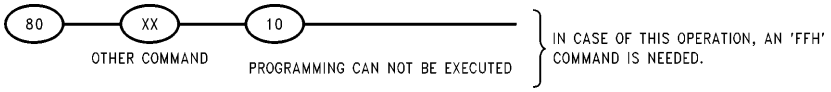
Once the serial input command (''80H'') is input, do not input any command other than the program execution command (''10H'') or the reset command (''FFH'') during programming.



TL/D/11915–51

FIGURE 18. Reset After Serial Input

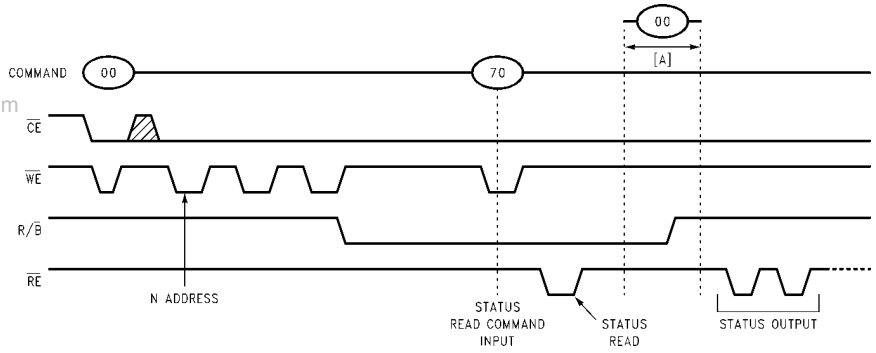
If a command other than ''10H'' or ''FFH'' is input, the program operation is not performed.



TL/D/11915–52

Supplementary Device Operation (Continued)

(4) STATUS READ DURING READ OPERATION

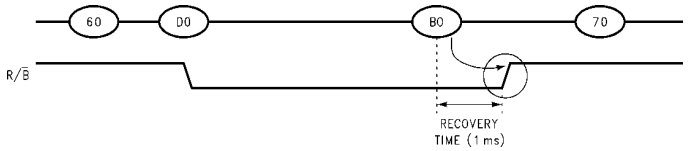


TL/D/11915–53

The device status can be read out by inputting the status read command ''70H'' during the read mode. Once the device is set to the status read mode after the ''70H'' command input, the device does not return to the read mode. Therefore, the status read during the read operation is prohibited. However, when the read command ''00H'' is input during [A], the status mode is reset, then the device returns to the read mode. In this case, the data output starts from N address without address input.

(5) SUSPEND COMMAND ''B0H''

The following issues need to be observed when the device is interrupted by a ''B0H'' command during block erasing.



TL/D/11915–54

Although the device status changes from busy to ready after ''B0H'' is input, the following two cases cannot be recognized.

— After a ''B0H'' command input, Busy ⟶ Ready

— After an erase operation is finished with ''D0H'', Busy ⟶ Ready

Therefore, the device status needs to be checked to see whether or not the ''B0H'' command has been accepted by issuing a ''70H'' command after the device goes to ready.

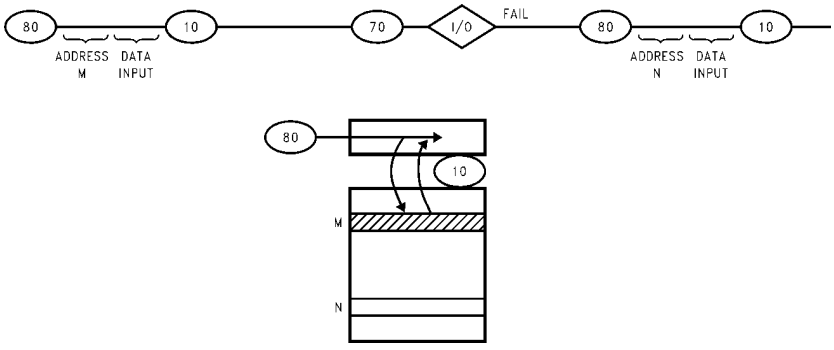
The device responds as follows when a ''D0H'' command (Resume) is input instead of ''70H''.

— ''B0H'' has been accepted : Erase operation is executed. (The device is busy.)

— ''B0H'' has not been accepted. (Erase operation has been completed) : ''D0H'' command cannot be accepted. (The device is in ready.)

Each case above is confirmed by monitoring the R/$\overline{B}$ signal.

(6) PROGRAM FAIL



TL/D/11915–55

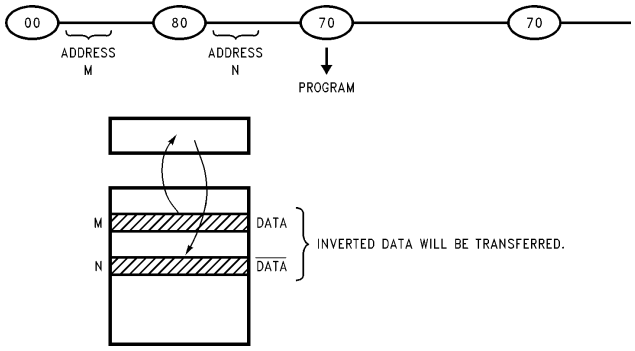
FIGURE 19. Program Fail

When the programming result for the page address M is ''Fail'', do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of ''80H'' command, address and data input is necessary.

Supplementary Device Operation (Continued)

(7) DATA TRANSFER

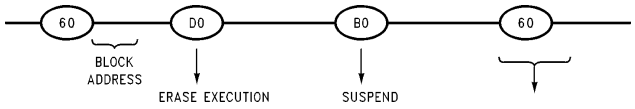
The data in page Address M cannot be automatically transferred to page address N. If the following sequence is executed, the data will be inverted (i.e., ''1'' data will become ''0'' and ''0'' will become ''1'').



TL/D/11915–56

FIGURE 20. Page to Page Transfer

(8) BLOCK ERASE AFTER SUSPEND COMMAND "B0H"

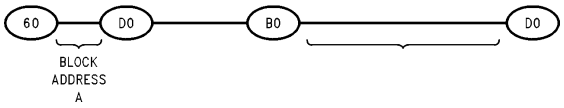


TL/D/11915–57

A block erase command is prohibited when the device has been suspended by inputting ''B0H'' during a block erase or multi-block erase operation. Only a program or read operation is allowed during this erase suspend interruption.

(9) INTERRUPTION OF AN ERASING BLOCK

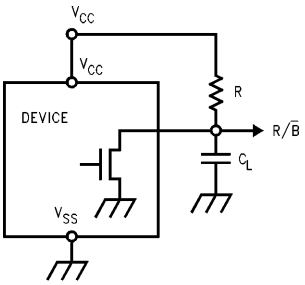
After a ''B0H'' command input, neither a program nor a read operation is allowed for the accessed block which is currently in an erase operation.



TL/D/11915–58

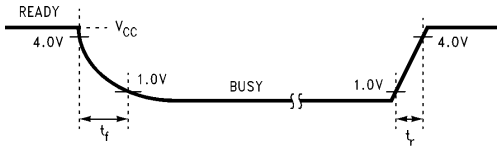
(10) R/$\overline{B}$: TERMINATION FOR THE READY/BUSY PIN (R/$\overline{B}$)

A pull-up resistor needs to be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.

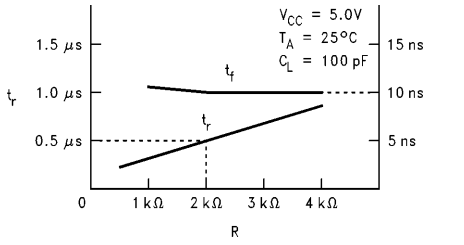


TL/D/11915–61

This data may vary by device. We recommend that you use this data as a reference when selecting a resistor value.



TL/D/11915–62



TL/D/11915–63

FIGURE 21. Ready/Busy Pin Termination

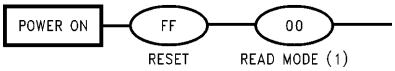
Supplementary Device Operation (Continued)

(11) STATUS AFTER POWER ON

Although the device is set to read mode after power-up, the following sequence is recommended because each input signal may not be stable at power on.

- Operation mode : Read mode (1)
- Address register : All "0"
- Data register : Indeterminacy
- High voltage generation circuit : Off state

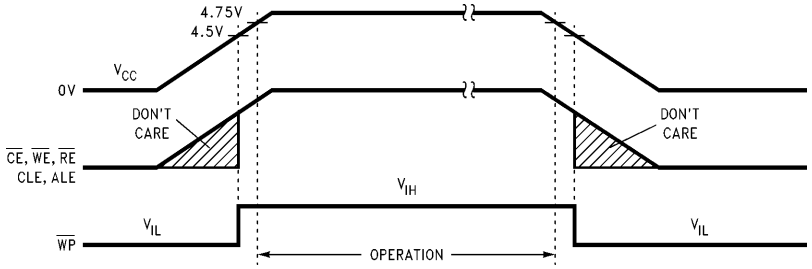
Recommended sequence



TL/D/11915–64

(12) POWER ON/OFF SEQUENCE

The $\overline{WP}$ signal is useful for protecting against data corruption at power on/off. The following timing is recommended:



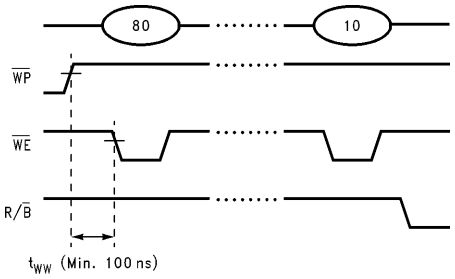
TL/D/11915–65

FIGURE 22. NM29N16 Power On/Off Sequence

(13) NOTIFICATION FOR $\overline{WP}$ SIGNAL

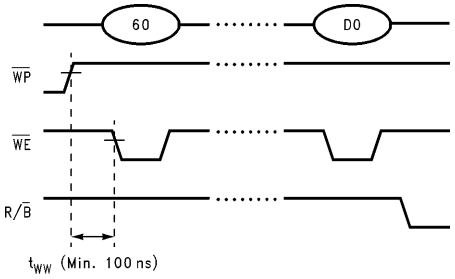
The erase and program operations are reset when $\overline{WP}$ goes low. The $\overline{WP}$ signal must be kept at a high level before 80H/60H commands may be input. If $\overline{WP}$ goes high after the 80H/60H commands are input, the program and erase operation cannot be guaranteed.

Program



TL/D/11915–66

Erase



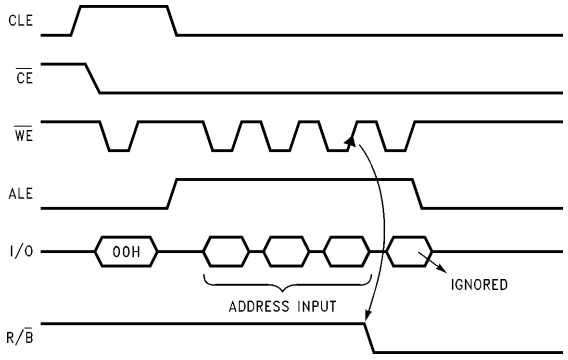
TL/D/11915–67

Supplementary Device Operation (Continued)

(14) IN THE CASE THAT 4 ADDRESS CYCLES ARE INPUT

Although the device may acquire the fourth address, it is ignored inside the chip.

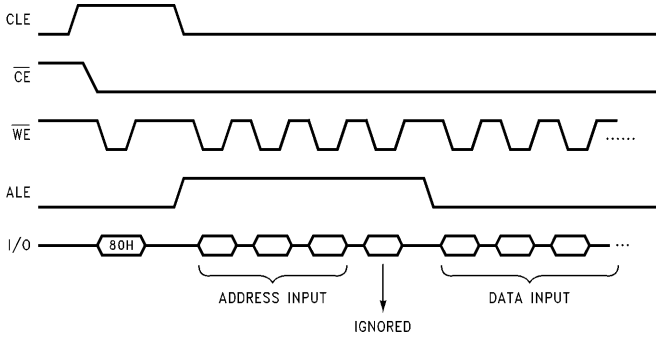
At Read operation:



TL/D/11915–71

FIGURE 23

At programming operation:

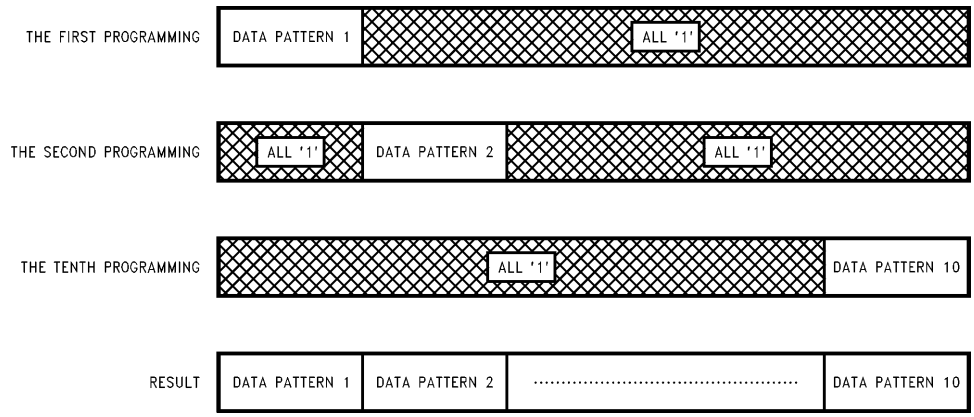


TL/D/11915–72

FIGURE 24

(15) DIVIDED PROGRAM IN THE SAME PAGE (PARTIAL PAGE PROGRAM)

The device allows a page to be divided typically into 10 segments and to program each page segment selectively as follows:



TL/D/11915–73

FIGURE 25

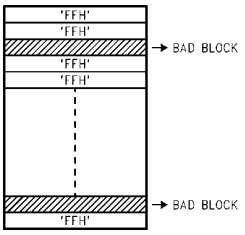
Note: The input data of unprogrammed or previously programmed page segments must be "1". (i.e., Mask all page bytes outside the segment to be programmed with "1" data.)

Supplementary Device Operation (Continued)

(16) UNUSABLE BLOCK IDENTIFICATION

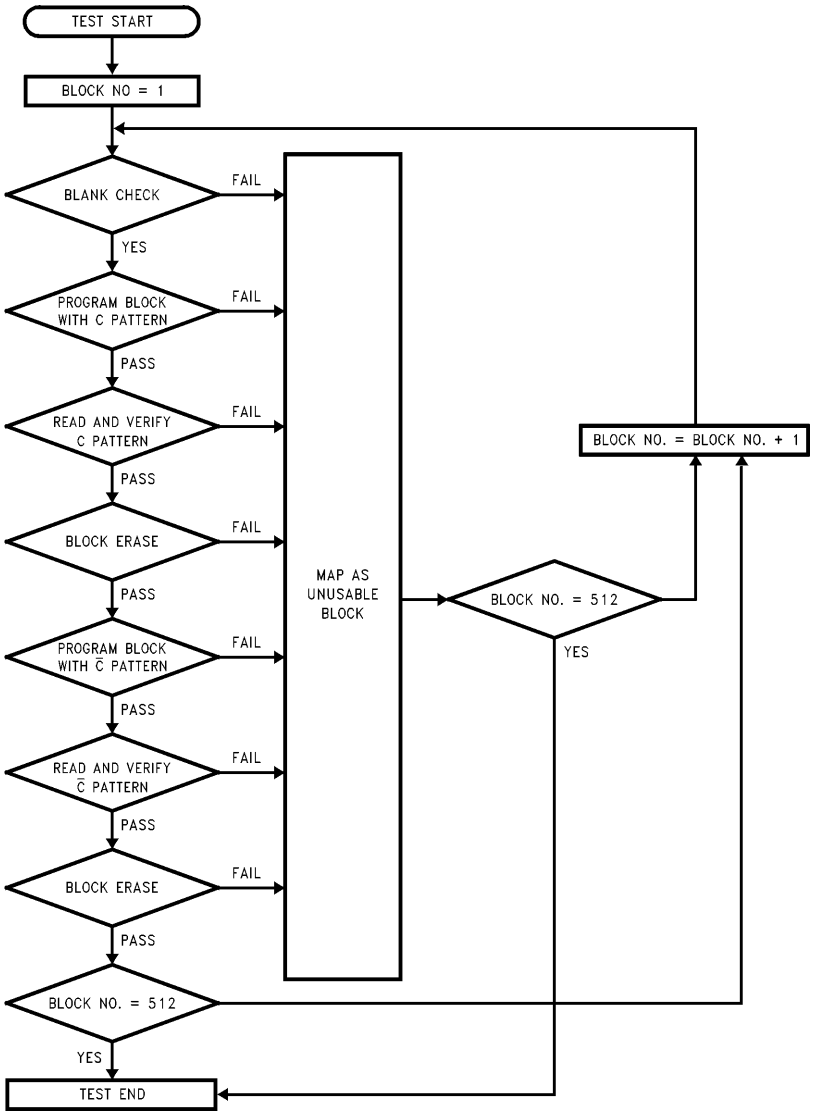
The NM29N16 may contain unusable blocks. To simplify identification, usable or good blocks leave the factory in the erased state. On initial power up (after board assembly), reading all the bytes in a usable block will result in FFH being read out. Unusable or bad blocks will read out some data other than FFH. These blocks should be mapped out of the system and not used. The valid number of blocks is as follows:

	Min	Typ	Max	Unit
Number of good blocks	502	508	512	Block



TL/D/11915–83

C: Checkboard Pattern, AAH
$\overline{C}$: Inverse Checkerboard Pattern, 55H
Blank Check: Usable blocks will read out 'FFH' for all bytes in block



TL/D/11915–4

FIGURE 26. Identification of Unusable Blocks at Initial Power Up

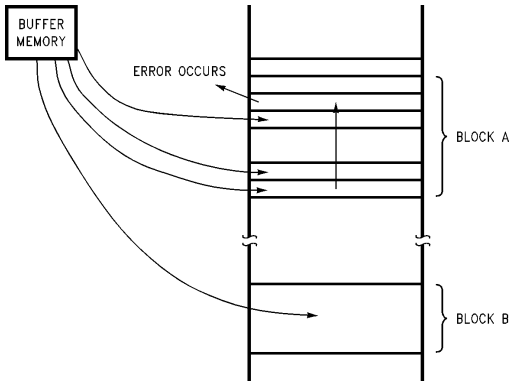
Supplementary Device Operation (Continued)

(17) ERROR IN PROGRAM OR ERASE OPERATION (FAIL AT STATUS READ)

The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs:

Program

When the error happens in Block A, try to reprogram the data into another Block B by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a ''bad block'' table or other appropriate scheme).



TL/D/11915–75

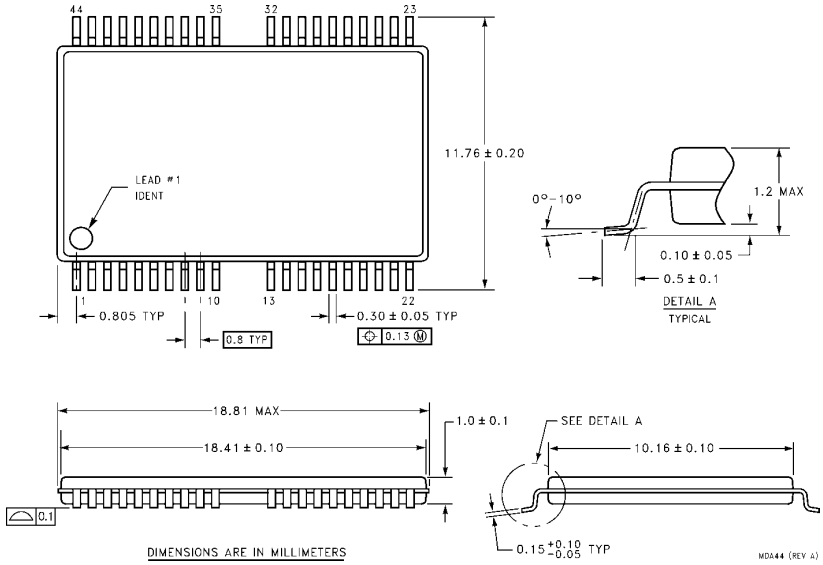
Erase

When the error oocurs after an erase operation, prevent future accesses to this bad block (again by creating or updating a table within the system or other appropriate scheme).

Physical Dimensions millimeters

Output Drawings

Plastic TSOP

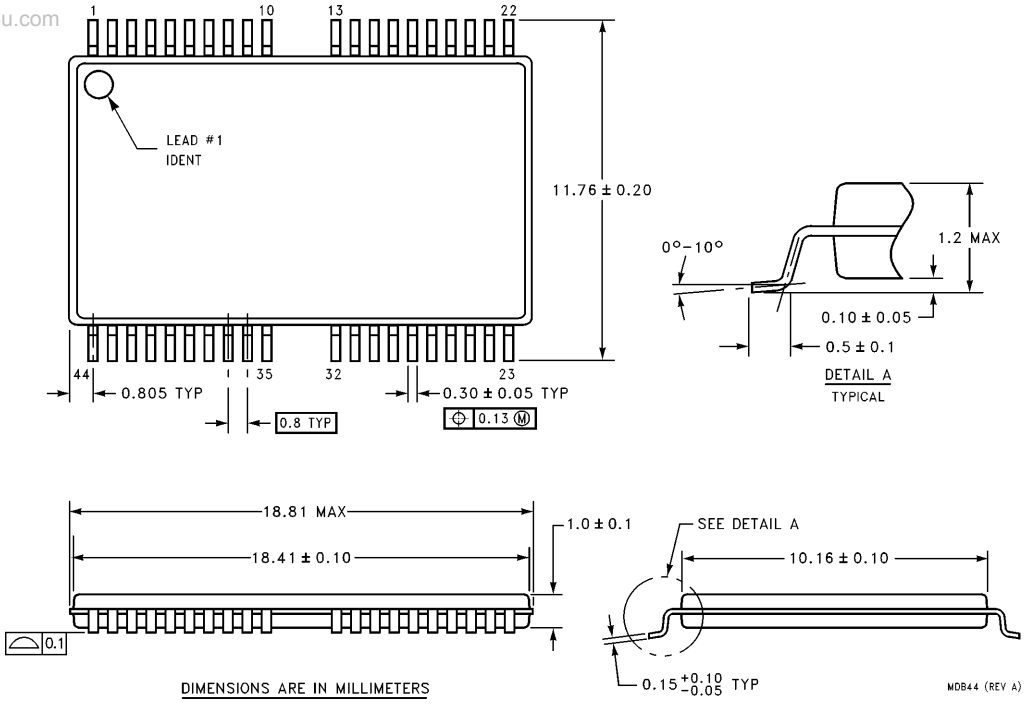


Plastic Thin Small Outline Package (S)
Order Number NM29N16S
NS Package Number NMDA0044

Physical Dimensions millimeters (Continued)

Output Drawings

Plastic TSOP



Reversed Plastic Thin Small Outline Package (R)
Order Number NM29N16R
NS Package Number NMDB0044

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408