NuMicro® Family

1T 8051-based Microcontroller

NM18002 Series
Preliminary Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

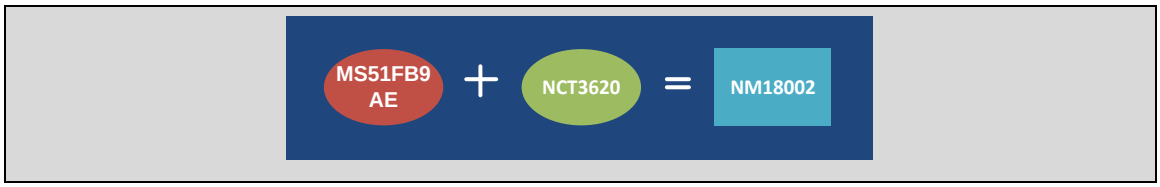
The NM18002 series is embedded with an 8-bit high performance 1T 8051-based microcontroller and a monolithic H-bridge gate driver for driving high-side P-channel and low-side N-channel power MOSFETs. It is designed for single phase BDC or BLDC motor driver applications which operate up to 28V.

The 8-bit MCU provides rich peripherals including 256 bytes of SRAM, 1K bytes of auxiliary RAM (XRAM), 16K bytes of APROM, 1K bytes of LDROM, 128 bytes of SPROM, up to 9 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UART, one I^2C, INT0, GPIO interrupt and one 12-bit ADC with 4 inputs. The peripherals are equipped with 18 sources with 4-level-priority interrupts capability.

This gate driver integrates a 5V linear voltage regulator with maximum 50mA output current capability and an Under Voltage Lock Out (UVLO) circuit which prevents malfunction when VCC is lower than the specified threshold voltage. It provides two sets of analog comparator(ACMP) for the signal conditioning of the Hall sensors and the shunt resistor signal. Besides, there is an embedded open-drain output which can transfer the low-voltage signal to high voltage by external pull-up resistor to VCC.

Additionally, the NM18002 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

NM18002 is the combination of MCU MS51FB9AE and Gate Driver NCT3620. User may refer to the TRM of MS51FB9AE and the datasheet of NCT3620 for the detailed specification. The MS51FB9AE BSP is also for NM18002 software developing.



2 FEATURES

- Recommended operation Supply Voltage VIN Range from 8 to 28V
- Gate Driver
  - 6 ~ 28V Operate Supply Voltage Range
  - Pre driver for external high side P-ch and low side N-ch MOSFET
  - Integrated one 5V LDO
  - Integrated two analog comparators (ACMP) with offset < 10mV
  - HV_OD high voltage open driven output with the voltage capability up to 28V
  - Protection:
    - UVLO (VCC Under Voltage Lockout)
    - Short-through Protection
- MCU Core
  - Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller.
  - Instruction set fully compatible with MCS-51.
  - 4-priority-level interrupts capability.
  - Dual Data Pointers (DPTRs).
- Memory
  - 16K bytes of APROM for User Code.
  - 1K bytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP)
  - Flash Memory accumulated with pages of 128 bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash
  - An additional 128 bytes security protection memory SPROM
  - 256ytes on-chip RAM.
  - Additional 1K bytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
- Clock Control
  - Default 16 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 °C, 3.3 V), ±2% in -20~105°C.
  - Selectable 24 MHz high-speed internal oscillator (HIRC).
  - 10 kHz low-speed internal oscillator (LIRC) calibrating to ±10% typically.
- I/O Port
  - Four I/O modes:
    - Quasi-bidirectional mode
    - Push-Pull Output mode
    - Open-Drain Output mode

- Input only with high impendence mode
- Schmitt trigger input / TTL mode selectable.
- Each I/O pin configured as interrupt source with edge/level trigger setting
- Standard interrupt pins INT0
- Supports high drive and high sink current I/O
- I/O pin internal pull-up or pull-down resistor enabled in input mode.
- Each GPIO enabling the pin interrupt function will also enable the wake-up function

- Timer
  - Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051.
  - One 16-bit Timer2 provides input capture module two input pins.
  - One 16-bit auto-reload Timer3, which can be the baud rate clock source of UART0 and UART1.
- WDT (Watchdog Timer)
  - 6-bit free running up counter for WDT time-out interval.
  - Selectable time-out interval is 6.40 ms ~ 1.638s since WDT_CLK = 10 kHz (LIRC).
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM(Enhanced PWM Generator)
  - Up To 6 output pins can be selected
  - Supports maximum clock source frequency up to 24 MHz
  - Supports independent mode for PWM output
  - Supports complementary mode for 3 complementary paired PWM output channels
  - Supports 16-bit resolution PWM counter
  - Supports mask function and tri-state enable for each PWM pin
  - PWM0 module support Dead-time insertion with 8-bit resolution
  - PWM0 module Supports brake function
  - PWM0 module Supports trigger ADC
- UART
  - Supports up to 2 UARTs: UART0 & UART1
  - Full-duplex asynchronous communications
  - Programmable 9th bit.
  - TXD and RXD of UART0 pins exchangeable via software.
- I2C
  - 1 sets of I2C devices
  - Master/Slave mode

- Bidirectional data transfer between masters and slaves
- 7-bit addressing mode
- Standard mode (100 kbps) and Fast mode (400 kbps).
- Supports 8-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- Supports hold time programmable.

- 12-bit ADC (Analog-to-Digital Converter)
  - 12-bit resolution and 10-bit accuracy is guaranteed.
  - Up to 4 single-end analog input channels
  - 1 internal channels, they are band-gap voltage (VBG).
  - Up to 500 KSPS sampling rate.
  - Software Write 1 to ADCS bit.
  - External pin (STADC) trigger
  - PWM trigger
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- LVR (Low Voltage Reset)
  - LVR with 2.0V threshold voltage leve
- POR (Power On Reset)
  - POR with 1.15V threshold voltage level
- BOD (Brown-out Detector)
  - 4-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 2.7V / 2.2V)
- Security
  - 96-bit Unique ID (UID)
  - 128-bit Unique Customer ID (UCID)
  - 128-bytes security protection memory SPROM
  - Code lock for security by CONFIG
- Operating Temperature: -40℃~105℃
- Reliability: ESD HBM pass 2 kV; ESD 2 kV
- Packages:
  - 24-pin, QFN, 4mm x 4mm
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Selection Guide

3.1.1 NM18002 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	HIRC 16/24 MHz	I/O	Timer	UART	I2C	HV_OD (HV Open-drian output)	4 PWM + H-bridge Gate Drier	Analog Comp.	ADC (12-Bit)	5V LDO	ICP/ISP/AP	Package
NM18002Y	16	1	1	√	1	9	4	2	1	1	√	2	4x 12bit	1	√	QFN24 (4x4mm)

Table 3.1-1 NM18002 Series Selection Guide

3.2 Pin Configuration

3.2.1 QFN 24-Pin (4mm x 4mm) Diagram

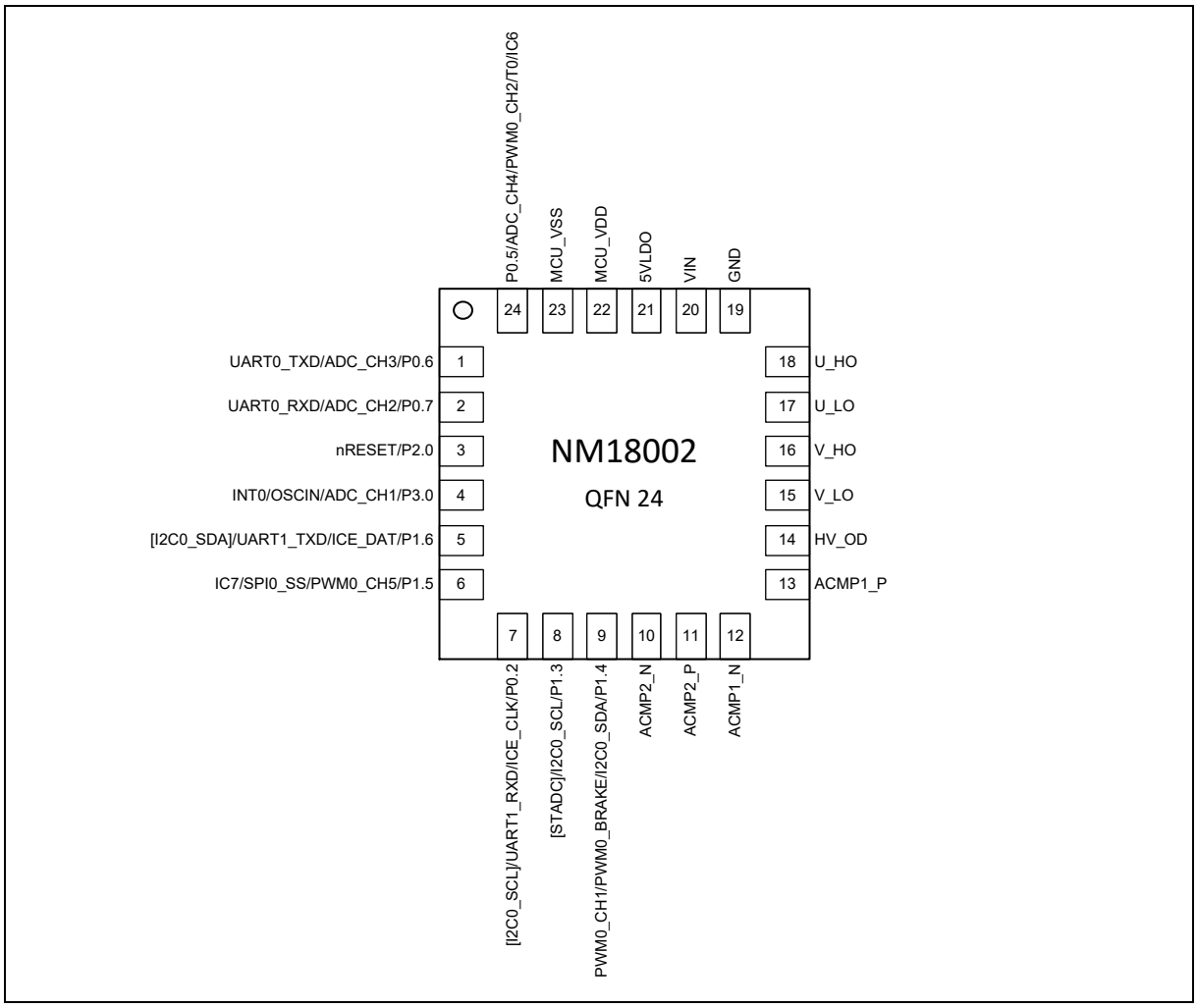


Figure 3.2-1 NM18002 QFN 24-pin Diagram

3.3 Pin Description

3.3.1 NM18002 Series QFN 24-Pin Description

MS51FB9AE TSSOP20	NCT3620 TSSOP20	NM18002 QFN24 4x4	Pin Name	Pin Type	Description
2		1	P0.6	I/O	Port 0 bit 6.
			UART0_TXD [4]	O	Serial port 0 transmit data output.
			ADC_CH3	A	ADC input channel 3.
3		2	P0.7	I/O	Port 0 bit 7.
			UART0_RXD	O	Serial port 0 receive input.
			ADC_CH2	A	ADC input channel 2.
4		3	P2.0	I	Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
			nRESET	I	nRESET pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESETpin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
5		4	P3.0	I/O	Port 3 bit 0 available when the internal oscillator is used as the system clock.
			ADC_CH1	A	ADC input channel 1.
			$\overline{\text{INT0}}$	I	External interrupt 0 input.
			OSCIN	I	If the ECLK mode is enabled, Xin is the external clock input pin.
8		5	P1.6	I/O	P1.6: Port 1 bit 6.
			ICE_DAT	I/O	ICP / OCD data input or output.
			UART1_TXD	O	Serial port 1 transmit data output.
			[I2C0_SDA] [5]	I/O	I^2C data.
10		6	P1.5	I/O	Port 1 bit 5.
			PWM0_CH5	O	PWM0 output channel 5.
			IC7	I	Input capture channel 7.
			SPI0_SS	I	SPI slave select input.
18		7	P0.2	I/O	Port 0 bit 2.
			ICE_CLK	I	ICP / OCD clock input.
			UART1_RXD	I	Serial port 1 receive input.
			[I2C0_SCL] [5]	O	I^2C clock.
12		8	P1.3	I/O	Port 1 bit 3.
			I2C0_SCL	O	I^2C clock.

			[STADC] [6]	**I**	External start ADC trigger
11		**9**	**P1.4**	**I/O**	Port 1 bit 4.
			PWM0_CH1	**O**	PWM0 output channel 1.
			I2C0_SDA	**I/O**	I^2C data.
			PWM0_BRAKE	**I**	Fault Brake input.
	11	**10**	**ACMP2_N[7]**	**A**	ACMP2 negative input
	12	**11**	**ACMP2_P[7]**	**A**	ACMP2 positive input
	13	**12**	**ACMP1_N[7]**	**A**	ACMP1 negative input
	14	**13**	**ACMP1_P[7]**	**A**	ACMP1 positive input
	15	**14**	**HV_OD**	**HO**	High voltage open drain output
	16	**15**	**V_LO**	**HO**	Low side NMOS gate driver V-phase output.
	17	**16**	**V_HO**	**HO**	High side PMOS gate driver V-phase output.
	18	**17**	**U_LO**	**HO**	Low side NMOS gate driver U-phase output.
	19	**18**	**U_HO**	**HO**	High side PMOS gate driver U-phase output.
	20	**19**	**GND**	**P**	Ground
	1	**20**	**VIN**	**HP**	Power supply voltage input
	2	**21**	**5VLDO**	**P**	5V LDO reference voltage. Recommend connect an about 10uF CAP to GND.
9		**22**	**MCU_VDD**	**P**	MCU power supply
7		**23**	**MCU_VSS**	**P**	MCU Ground
		24	**P0.5**	**I/O**	Port 0 bit 5.
			PWM0_CH2	**O**	PWM0 output channel 2.
			IC6	**I**	Input capture channel 6.
			T0	**I/O**	External count input to Timer/Counter 0 or its toggle output.
			ADC_CH4	**A**	ADC input channel 4.
	10		**FA**	**I**	With internal pull low to enable gate driver
16	**6**				PWM3 connect to U_HO.
15	**7**				PWM2 connect to U_LO.
14	**8**				PWM1 connect to V_HO.
13	**9**				PWM0 connect to V_LO.
17	**5**				P0.1 connect to LV_I
20	**3**				P0.4 connect to ACMP1_O
19	**4**				P0.3 connect to ACMP2_O

Table 3.3-1 QFN 24-Pin Description

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

[3] Input-only with the following pull high capability.

[4] UART0_TXD and UART0_RXD pins are software exchangeable by UART0PX (AUXR1.2).

[5] [I2C] alternate function remapping option. I2C pins is software switched by I2CPX (I2CON.0).

[6] [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).

[7] If ACMP is not used, the positive input must be connected with a pull-up resistor to 5VLDO and the negative input must be connected with a pull-down resistor to GND

4 BLOCK DIAGRAM

4.1 NM18002 Block Diagram

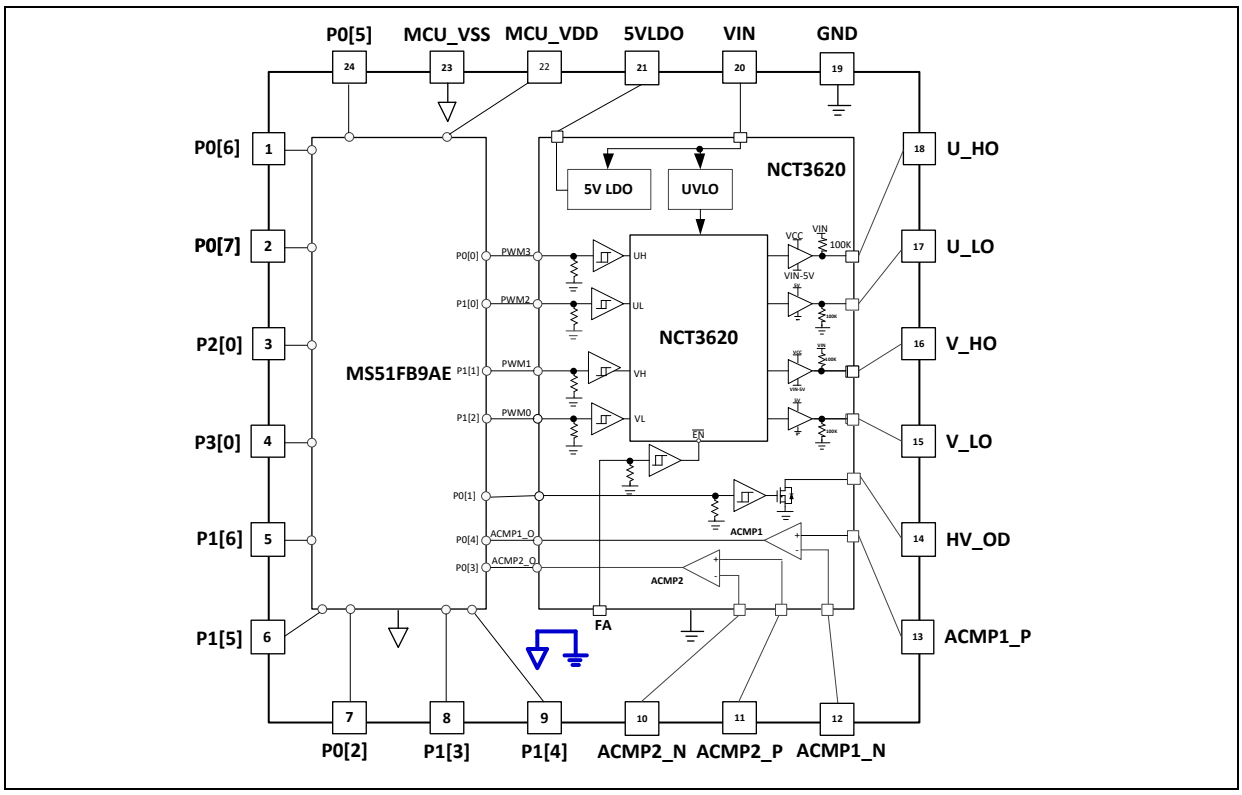


Figure 4.1-1 NM18002 Series Block Diagram

4.2 NM18002 Application Circuit

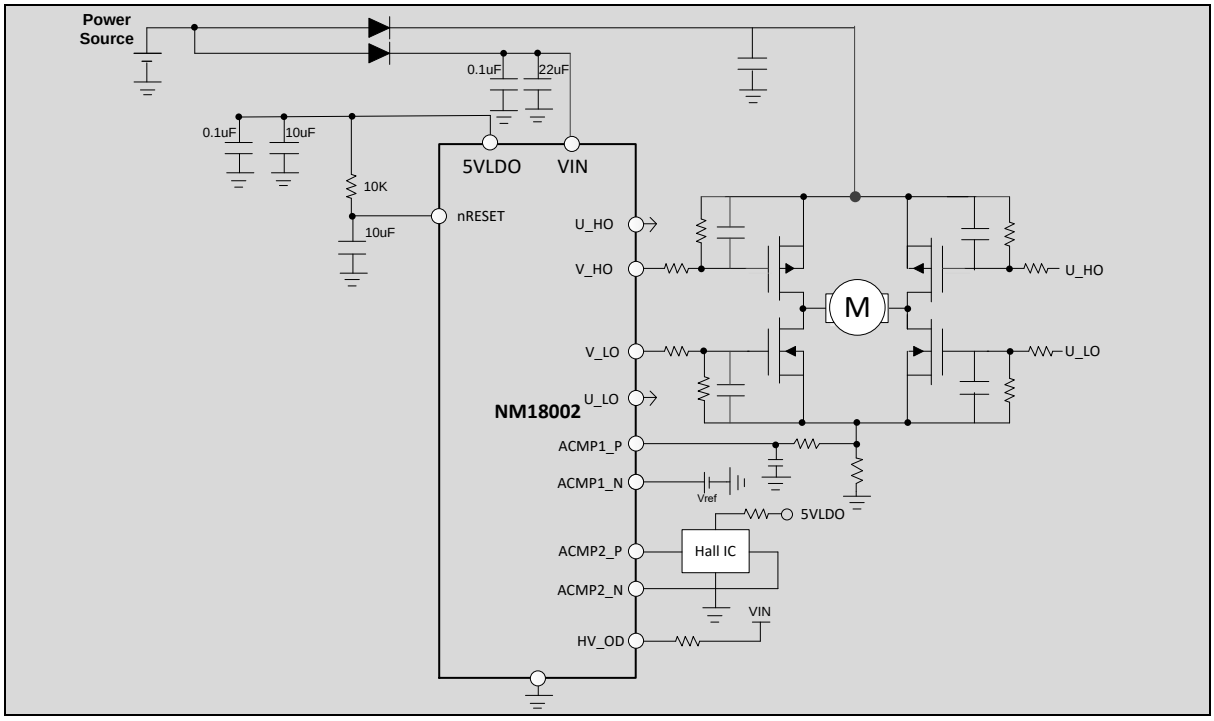


Figure 4.2-1 NM18002 Application Circuit

Note:

The circuit is a reference design. The performance may be different in applications and mass production. Therefore, users are responsible to check the circuit to meet their system function and specification.

5 NM18002 ELECTRICAL CHARACTERISTICS

The data is for reference only. Please refer to the TRM of MS51FB9AE and the datasheet of NCT3620 for the detailed electrical characteristics.

5.1 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5V, T_A = 25°C, Fsys = 16 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{BG}	Band-gap voltage[2]	1.17	1.22	1.30		T_A = 25 °C
		1.14		1.33		T_A = -40°C ~105 °C,

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. Based on characterization, tested in production.

Table 5.1-1 General operating conditions

5.2 MS51FB9AE DC Electrical Characteristics

5.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- V_{DD} = AV_{DD}
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash.

Symbol	Conditions	Fsys	Typ [6]	Max[6][7]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	3.6	4.2	4.6	4.8	mA
		24 MHz(HIRC)[1] @3.3V	3.2				
		24 MHz(HIRC)[1] @2.4V	2.9				

		16 MHz (HIRC) [1] @5.5V	3.3	3.4	3.9	4.6	
		16 MHz (HIRC) [1] @3.3V	3.1				
		16 MHz (HIRC) [1] @2.4V	2.8				
		10 kHz (LIRC)[2]	0.30	0.32	0.46	2.33	

Notes:
1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 5.2-1 Current consumption in Normal Run mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	2.8	2.9	3.2	3.8	mA
		24 MHz(HIRC)[1] @3.3V	2.4				
		24 MHz(HIRC)[1] @2.4V	2.2				
		16 MHz (HIRC)[1] @5.5V	2.2	2.5	2.6	3.2	
		16 MHz (HIRC)[1] @3.3V	1.9				
		16 MHz (HIRC)[1] @2.4V	1.8				
		10 kHz (LIRC)[2]	0.3	0.5	0.9	2.3	

Notes:
1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 5.2-2 Current consumption in Idle mode

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
	Power down mode, all peripherals disable@5.5V	6.5	6.2	9	55	µA

I_{DD_PD}	Power down mode, all peripherals disable@3.3V	6				
	Power down mode, all peripherals disable@2.4V	5.8				
	Power down mode, LVR enable all other peripherals disable	7.5	6.7	10[3]	57	
	Power down mode, LVR enable BOD enable all other peripherals disable	180	165	197	292	

Notes:

1. $AV_{DD} = V_{DD} = 3.3V$ unless otherwise specified, LVR17 disabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 5.2-3 Chip Current Consumption in Power down mode

5.2.2 Wakeup Time from Low-Power Modes

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[2][3]	Wakeup from Power down mode	Fsys = HIRC @16MHz	-	30	µs
		Fsys = HIRC @ 24MHz		30	µs

Notes:

1. Measured on a wakeup phase with a 16 MHz HIRC oscillator.
2. Based on test during characterization, not tested in production.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.

Table 5.2-4 Low-power mode wakeup timings

5.2.3 I/O DC Characteristics

5.2.3.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IL1}	Input low voltage (I/O with TTL input)	V_{SS}-0.3	-	$0.2V_{DD}$-0.1	V	
V_{IH}	Input high voltage	$0.2V_{DD}$+0.9	-	V_{DD}+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 5.2-5 I/O input characteristics

5.2.3.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.4	-	-7.5	µA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	µA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	µA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-57.2	-	-58.3	µA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-9	-	-9.6	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-	-6.6	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.2	-	-4.9	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V
		-18	-	-20	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	18	-	20	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		16	-	18	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		9.7	-	11	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:
1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 5.2-6 I/O output characteristics

5.2.3.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		45	-	65		V_{DD} = 2.4 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 5.2-7 nRESET Input Characteristics

5.3 MS51FB9AE AC Electrical Characteristics

5.3.1 Internal High Speed RC Oscillator (HIRC)

5.3.1.1 16MHz RC Oscillator (HIRC)

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	16[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20 °C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40 °C ~ -20 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:
5. Default setting value for the product
6. Based on reload value.
7. Based on characterization, tested in production.
8. Guaranteed by characterization result, not tested in production.
9. Guaranteed by design.

Table 5.3-1 16 MHz Internal High Speed RC Oscillator(HIRC) characteristics

5.3.1.2 24MHz RC Oscillator (HIRC)

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +85 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:
1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

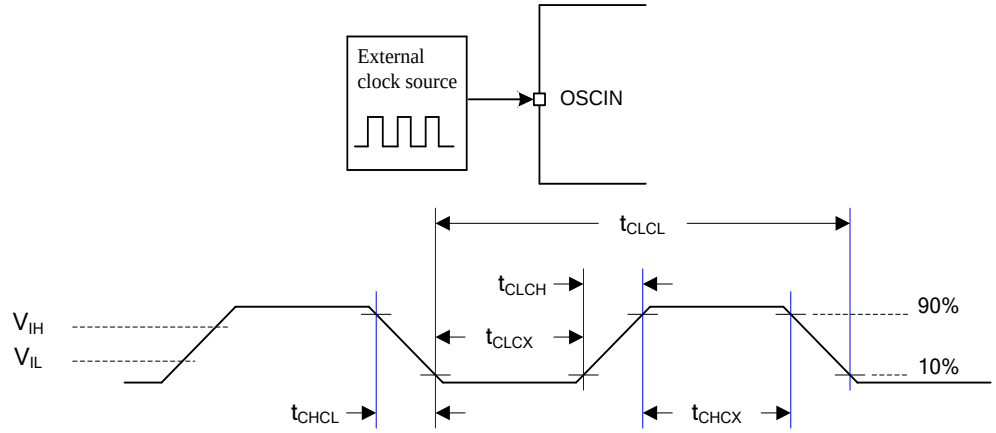
Table 5.3-2 24MHz Internal High Speed RC Oscillator(HIRC) characteristics

5.3.2 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode OSCIN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	0.7*V_{DD}	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	0.3*V_{DD}	V	

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions



Notes:

1. Guaranteed by characterization, not tested in production.

Table 5.3-3 External 4~24 MHz High Speed Clock Input Signal

5.3.3 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[1]	-	10[1]	%	T_A = 25 °C, V_{DD} = 5V
		-35[2]	-	35[2]	%	T_A=-40~105°C Without software calibration
I_{LRC}[3]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Notes:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design.

Table 5.3-4 10 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

5.3.4 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V

		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 2.4 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 2.4 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$[*3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 5.3-5 I/O AC characteristics

5.4 MS51FB9AE Analog Characteristics

5.4.1 Reset and Power Control Block Characteristics

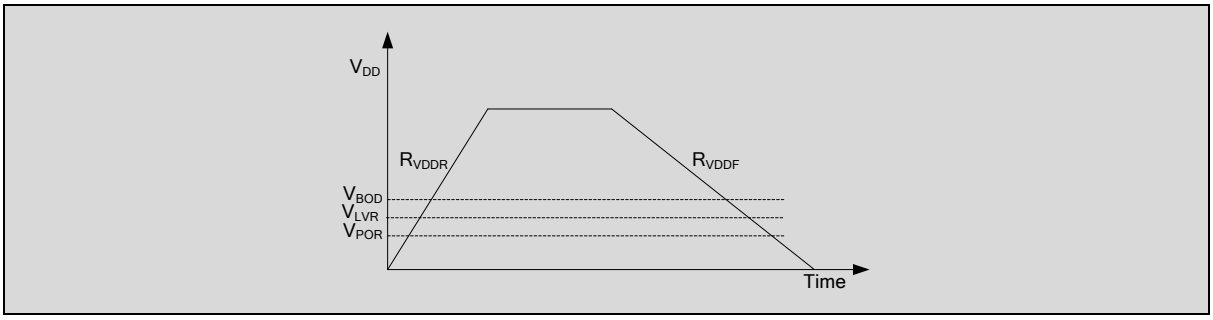
The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	0.5	2.9		AV_{DD} = 5.5V
V_{POR}	POR reset voltage	1	1.15	1.3	V	-
V_{LVR}	LVR reset voltage	1.7	2.0	2.4		-
V_{BOD}	BOD brown-out detect voltage	4.25	4.4	4.55		BOV[1:0] = [0,0]
		3.55	3.7	3.85		BOV[1:0] = [0,1]
		2.60	2.7	2.80		BOV[1:0] = [1,0]
		2.10	2.2	2.35		BOV[1:0] = [1,1]
T_{LVR_SU}[*1]	LVR startup time	60	-	80	μs	-
T_{LVR_RE}[1]	LVR respond time	0.4	-	4		Fsys = HIRC@16MHz
		180	-	350		Fsys = LIRC
T_{BOD_SU}[1]	BOD startup time	180	-	320		Fsys = HIRC@16MHz
T_{BOD_RE}[1]	BOD respond time	2.5	-	5		Fsys = HIRC@16MHz

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 5.4-1 Reset and power control unit



BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 5.4-2 Minimum Brown-out Detect Pulse Width

5.4.2 12-bit SAR ADC

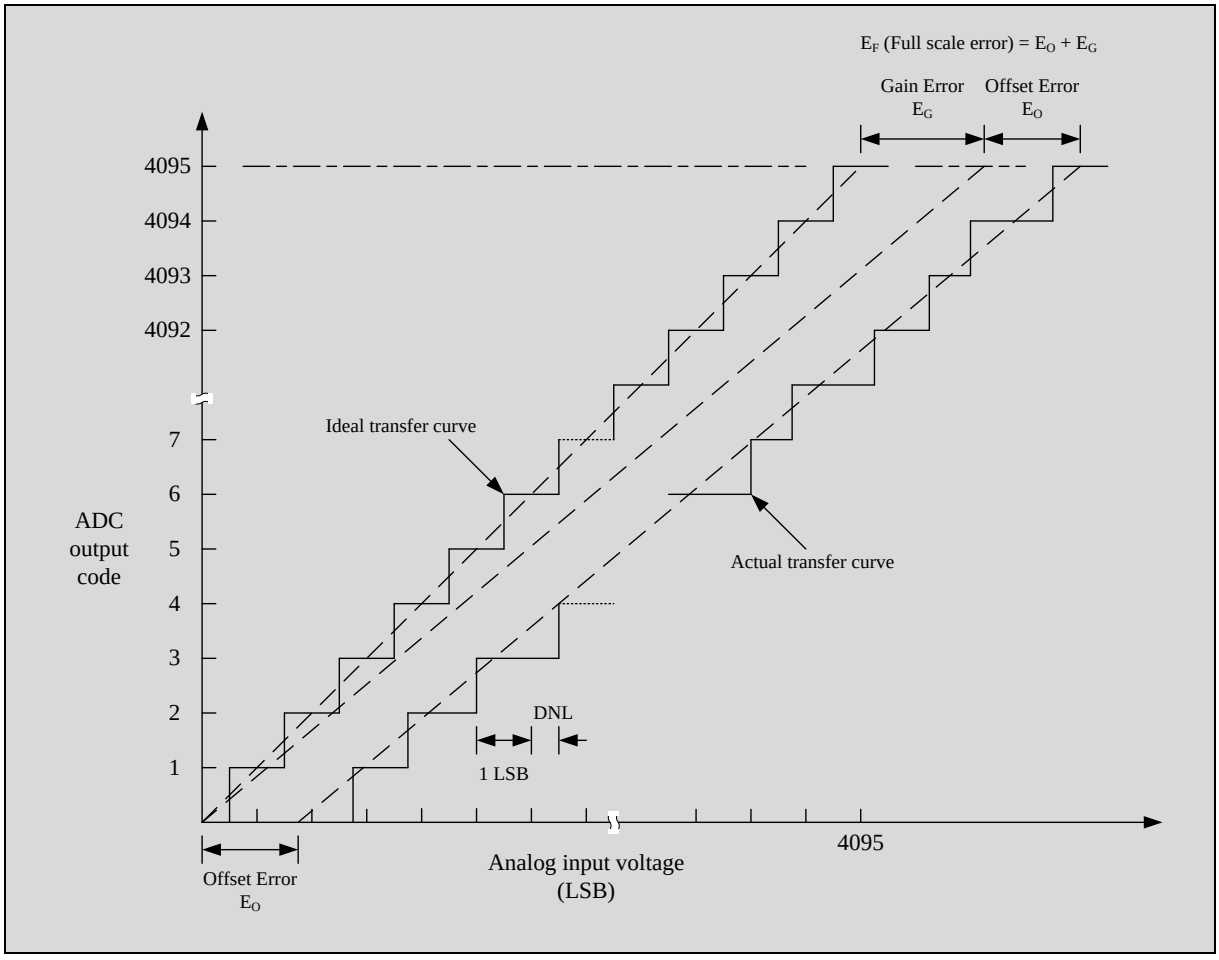
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	2.7	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{ADC} = 500 kHz $T_{CONV} = 17 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[1] $1/T_{ADC}$	ADC Clock frequency	-	500	-	kHz	
T_{SMP}	Sampling Time	1	-	38	$1/F_{ADC}$	$T_{SMP} = \frac{4 * ADCAQT + 10}{F_{ADC}}$
T_{CONV}	Conversion time	1	-	128	$1/F_{ADC}$	
T_{EN}	Enable to ready time	20	-	-	μs	
INL[*1]	Integral Non-Linearity Error	-3	-	+3	LSB	$V_{REF} = AV_{DD} = V_{DD}$

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
DNL[*1]	Differential Non-Linearity Error	-2	-	+4	LSB	V_{REF} = AV_{DD}=V_{DD}
E_G[*1]	Gain error	-3.5	-	+0.4	LSB	V_{REF} = AV_{DD}=V_{DD}
E_O[*1]$_T$	Offset error	-2	-	+2.8	LSB	V_{REF} = AV_{DD}=V_{DD}
E_A[*1]	Absolute Error	-7		+7	LSB	V_{REF} = AV_{DD}=V_{DD}

Notes:

1. Guaranteed by characterization result, not tested in production.

Table 5.4-3 ADC characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

5.5 MS51FB9AE Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25℃
T_{ERASE}	Page erase time	-	5	-	ms	
T_{PROG}	Program time	-	10	-	μs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	4	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	50	-	-	year	100 kcycle[3] T_A = 55℃
		25	-	-	year	100 kcycle[3] T_A = 85℃
		10	-	-	year	100 kcycle[3] T_A = 105℃

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 5.5-1 Flash memory characteristics

5.6 NCT3620 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
VCC	Input supply voltage.	-0.3 to 30	V
5VLDO	5V Linear regulator output	-0.3 to 6	V
U_HO V_HO	High-side PMSO driver	VCC-6V to VCC	V
U_LO V_LO	Low-side NMOS driver	-0.3V to 6V	V
HV_OD	High voltage open drain output voltage.	30	V
Other pins		-0.3 to 6	V
θ_{JA}	Thermal Resistance,	40	℃/W
θ_{JC}	Thermal Resistance,	10	℃/W
θ_{STG}	Storage Temperature	-50 to 150	℃
θ_{J}	Junction Temperature	150	℃
ESD Rating	Human Body Mode(all pins)	±2	KV
	Charge Device Mode	±500	V
	Latch-up	±100	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.7 NCT3620 Recommended Operating Conditions

PARAMETER	RATING	UNIT
VCC supply voltage	6 to 28	V
5VLDO supply Output Current	30	mA
Operating temperature	-40 to 105	℃
Junction temperature	-40 to 125	℃

Note: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

5.8 NCT3620 DC Electrical Characteristics

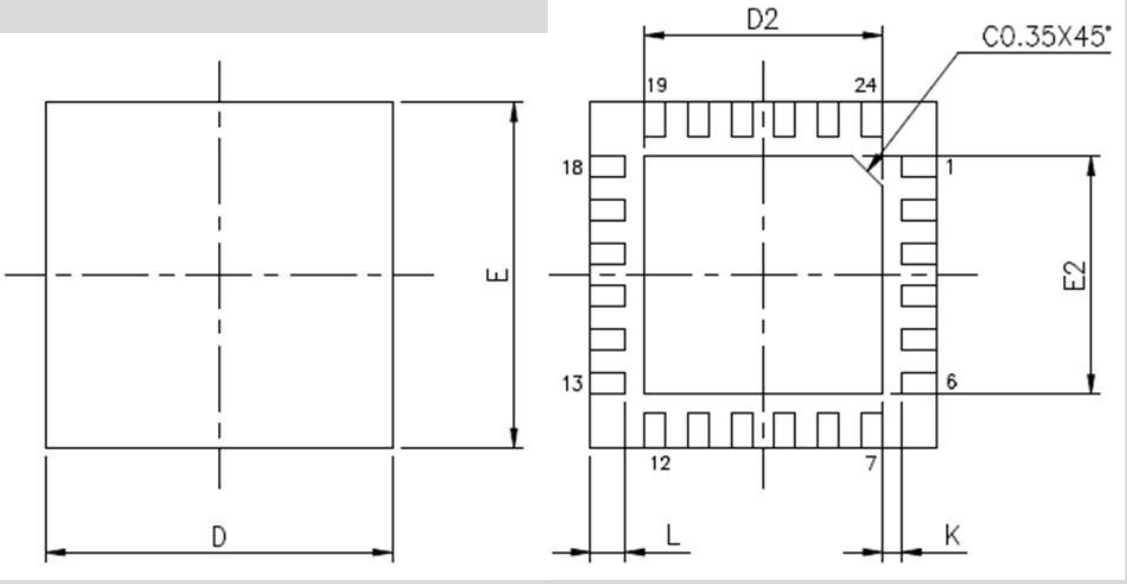
(VCC= 12V, TA = TJ = 25° C, unless otherwise specified)

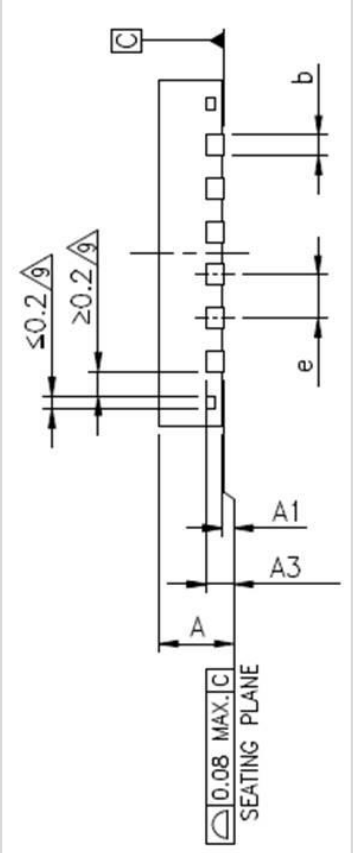
Parameter	Symbol	Test condition		Min.	Typ.	Max.	Unit
Supply voltage							
Input supply voltage	VCC			6	---	28	V
VCC UVLO turn-on threshold	UVLO+	VCC rising		3.4	3.6	3.8	V
VCC UVLO turn-off threshold	UVLO-	VCC falling		3	3.2	3.4	V
VCC Standby Current	I_{CC}	U_H,U_L,V_H,V_L=Low		200	250	300	uA
VCC operation current	I_{CCOP-1}	PWM=20KHz, PWM Duty=50%	C_L=1nF	0.6	0.8	1	mA
	I_{CCOP-2}		C_L=10nF	4.2	4.8	5.4	mA
Gate Driver							
HO Output High Voltage	V_{HOH}	I_O= - 20mA		VCC-0.7	VCC-0.5	VCC-0.2	V
HO Output Low Voltage	V_{HOL}	I_O= + 20mA		VCC-5	VCC-4.5	VCC-4	V
LO Output High Voltage	V_{LOH}	I_O= - 20mA		3.7	4	4.8	V
LO Output Low Voltage	V_{LOL}	I_O= + 20mA		0.2	0.5	0.8	V
Turn-on propagation delay	t_{on}	C_L=1nF		-	25	-	nS
Turn-off propagation delay	t_{off}	C_L=1nF		-	25	-	nS
Turn-on rise time	t_r	C_L=1nF		-	200	-	nS
Turn-off fall time	t_f	C_L=1nF		-	60	-	nS
Dead Time	t_D			400	450	500	nS
HO Pull up resistance	R_{HO}			---	100	---	KΩ
LO Pull low resistance	R_{LO}			---	100	---	KΩ
Logic Input							
High threshold voltage	V_{IH}			2.8	---	---	V
Low threshold voltage	V_{IL}			--	---	0.4	V
Input pull low Resistance	R_{IN}			---	100	---	KΩ
Comparator							
Hysteresis	V_{HYS}			---	±10	±20	mV
Internal 5VLDO							
5VLDO output voltage	$5V_{OUT}$			4.75	5	5.25	V
5V output current		VCC=28，TA = 25° C		---	---	30	mA
HV_OD							
Output Low level voltage	V_{HV_OD}	I=+10mA		---	---	0.3	V
HV_OD Off leakage current	I_{HV_OD}	HV_OD=VCC		---	---	10	uA

6 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

6.1 24-pin QFN (4 mm x 4 mm)





SYMBOL	Min	Nom	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	--	--	--
A3		0.2 REF	
b	0.18	0.25	0.3
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.6	2.7	2.75
E2	2.6	2.7	2.75
K	0.2	--	--
L	0.35	0.4	0.45

7 ORDERING INFORMATION

Part Number	Supplied As	Package Type	Operating Temperature
NM18002Y	4000 units/ T&R	QFN24, Green Package	Commercial, -40℃~105℃

8 REVISION HISTORY

Date	Revision	Description
2022.06.14	0.01	1. Preliminary version 0.001
2022.08.11	0.01	1. Rename “LD” to “HV_OD” 2. Modify ACMP pins naming.
2022.09.23	0.01	1. Modify HO Output Low Specification in Chapter 5.8 2. Modify numbers of Timer in Table 3.1-1
2022.11.08	0.02	1. Add “Package is Halogen-free, RoHS-compliant, and TSCA-compliant.” In chapter 2 and 6.
2024.02.26	0.03	1. Modify hysteresis specification of ACMP. 2. Modify the ordering information.