

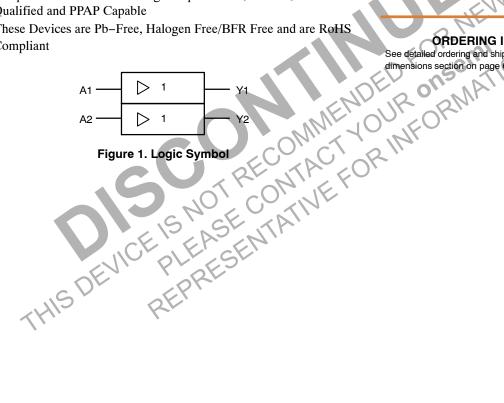
Dual Buffer

NLV27WZ16

The NLV27WZ16 is a high performance dual buffer operating from a 1.65 V to 5.5 V Supply.

Features

- \bullet Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.4 ns t_{PD} at $V_{CC} = 5 \text{ V (Typ)}$
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Sink 32 mA at 4.5 V
- Available in SC-88, and TSOP-6 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



MARKING DIAGRAMS



SC-88 **DF SUFFIX** CASE 419B-02





TSOP-6 CASE 318G-02



XXX = Specific Device Code

= Date Code* М

= Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

ee detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

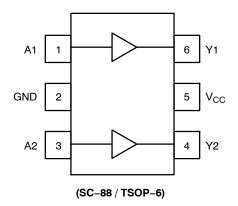


Figure 2. Pinout (Top View)

PIN ASSIGNMENT

1 A1 2 GND 3 A2 4 Y2 5 V _{CC} 6 Y1 CERERASENTATIVE FOR INFORMATION REPRESENTATIVE FOR INFORMATION		Pin	Function		A Input	Y Output
2 GND 3 A2 4 Y2 5 V _{CC} 6 Y1 REPRESENTATIVE		1	A1		L	L
3 A2 4 Y2 5 V _{CC} 6 Y1 REPRESENTATIVE FOR INFORMATION REPRESENTATIVE FOR INFORMATION		2	GND		Н	Н
4 Y2 5 V _{CC} 6 Y1 FORMATION RECONNENDED FORMATION REPRESENTATIVE FOR INFORMATION REPRESENTATIVE FOR INFORMATION		3	A2			- CM
5 V _{CC} 6 Y1 6 Y1 COMMENDED FOR MATION COMMENDED FOR MATION COMMENDED FOR MATION COMMENDED FOR MATION RECOMMENDED FOR MATION REPRESENTATIVE FOR MATIO		4	Y2			ME
6 Y1 RECOMMENDED FORMATION OF RECOMMENDED FORMATION REPRESENTATIVE FOR INFORMATION REPRESENTATIVE FOR INFORMATION		5	V _{CC}			1- 10- 1
THIS DEVICE PLEASE NTATIVE POR PRESENTATIVE PREPRESENTATIVE PREPRESENTATIVE		6	Y1		- OF	cen 10M
	THIS D	SI PICE P	NOT RESE	ECONTACT CONTACT CONTA	OURFO	RM

FUNCTION TABLE

A Input	Y Output	(6)
١	L	2510
Н	н	

MAXIMUM RATINGS

Symbol	Characteristics	Value	Units
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage Active–Mode (High or Low State) Tri–State Mode (Note 1) Power–Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} +0.5 -0.5 to +7.0 -0.5 to +7.0	V
I _{IK}	DC Input Diode Current, V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current, V _{OUT} < GND	-50	mA
I _{OUT}	DC Output Source/Sink Current	±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2) SC-88 TSOP-6	377 320	°C/W
P _D	Power Dissipation in Still Air SC–88 TSOP-6	332 390	mW
MSL	Moisture Sensitivity	Level 1	-
F _R	Flamebility Rating Oxygen Index; 28 to 34	UL 94-V-0 @ 0.125 in	ī
V _{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model (NLV) Charged Device Model	1000	V
I _{LATCHUP}	Latchup Performance (Note 4)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri–stated.

2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow per JESD51-7.

3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.

4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage Active–Mode (High or Low State) Tri–State Mode (Note 1) Power–Down Mode ($V_{\rm CC}$ = 0 V)	0 0 0	V _{CC} 5.5 5.5	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Transition Rise or Fall Rate $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V} \\ V_{CC} = 2.3 \text{ V to } 2.7 \text{ V} \\ V_{CC} = 3.0 \text{ V to } 3.6 \text{ V} \\ V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	T,	4 = 25°	С	-55°C ≤ T	_A ≤ 125°C	
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Units
V _{IH}	High-Level Input		1.65 to 1.95	0.75 x V _{CC}			0.75 x V _{CC}		V
	Voltage		2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}		
V _{IL}	Low-Level Input		1.65 to 1.95			0.25 x V _{CC}		0.25 x V _{CC}	V
	Voltage		2.3 to 5.5			0.30 x V _{CC}		0.30 x V _{CC}	
V _{ОН}	High-Level Output Voltage	$\begin{split} V_{IN} &= V_{IH} \text{ or } V_{IL} \\ I_{OH} &= -100 \mu\text{A} \\ I_{OH} &= -4 \text{ mA} \\ I_{OH} &= -8 \text{ mA} \\ I_{OH} &= -12 \text{ mA} \\ I_{OH} &= -16 \text{ mA} \\ I_{OH} &= -24 \text{ mA} \\ I_{OH} &= -32 \text{ mA} \end{split}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V _{CC} - 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V _{CC} 1.4 2.1 2.4 2.7 2.5 4.0	- - - - -	V _{CC} - 0.1 1.29 1.9 2.2 2.4 2.3 3.8	- - - - -	٧
V _{OL}	Low-Level Output Voltage	$\begin{split} &V_{IN} = V_{IH} \text{ or } V_{IL} \\ &I_{OL} = 100 \mu\text{A} \\ &I_{OL} = 4 \text{ mA} \\ &I_{OL} = 8 \text{ mA} \\ &I_{OL} = 12 \text{ mA} \\ &I_{OL} = 16 \text{ mA} \\ &I_{OL} = 24 \text{ mA} \\ &I_{OL} = 32 \text{ mA} \end{split}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	- - - -	- 0.08 0.2 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	-		±0.1	-	±1.0	μΑ
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0		74	1.0	NON	10	μΑ
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	MOF	2	1.0		10	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

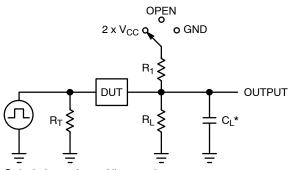
AC ELECTRICAL CHARACTERISTICS

						\sim	b				
				1	A = 25°C		-40°C ≤ 1	Γ _A ≤ 85°C	-55°C ≤ T	_A ≤ 125°C	
Symbol	Parameter	Condition	V _{CC} (V)	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay, A to Y (Figures 3 and 4)	RL = 1 M Ω , CL = 15 pF	1.65 to 1.95	(AT)	8.0	9.6	-	10.2	-	10.2	ns
	(Figures 5 and 4)	RL = 1 M Ω , CL = 15 pF	2.3 to 2.7	-	3.0	5.2	-	5.8	-	5.8	
		GC = 19 hr	3.0 to 3.6	-	2.3	3.6	_	4.0	_	4.0	
	COL	CP'	4.5 to 5.5	-	1.8	2.9	-	3.2	-	3.2	
	4119	RL = 500 Ω,	3.0 to 3.6	-	3.0	4.6	-	5.1	-	5.1	
	, ,	CL = 50 pF	4.5 to 5.5	-	2.4	3.8	_	4.2	_	4.2	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	4.0	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 3.3 V, V_{IN} = 0 V or V_{CC} 10 MHz, V_{CC} = 5.0 V, V_{IN} = 0 V or V_{CC}	11 12.5	pF

^{5.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in}$) I_{CC} . C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in}$) $I_{CC} \cdot V_{CC}$.



Test	Switch Position	C _L , pF	R_L, Ω	R ₁ , Ω
t _{PLH} / t _{PHL}	Open	See AC Characteristics Table		
t _{PLZ} / t _{PZL}	2 x V _{CC}	50	500	500
t _{PHZ} / t _{PZH}	GND	50	500	500

X = Don't Care

 C_L includes probe and jig capacitance R_T is Z_{OUT} of pulse generator (typically 50 $\Omega)$ f = 1 MHz

Figure 3. Test Circuit

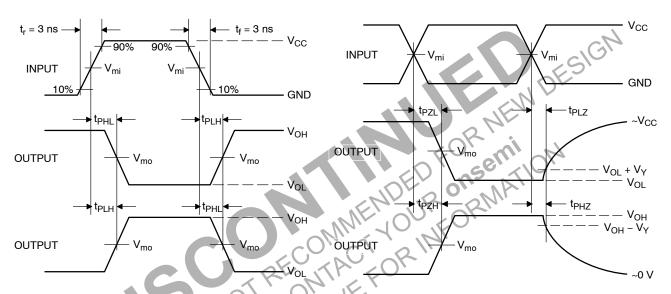


Figure 4. Switching Waveforms

	11000125	V		
V _{CC} , V	V_{mi}, V	t _{PLH} , t _{PHL}	t _{PZL} , t _{PLZ} , t _{PZH} , t _{PHZ}	V _Y , V
1.65 to 1.95	V _{CC} /2	V _{CC} /2	V _{CC} / 2	0.15
2.3 to 2.7	V _{CC} /2	V _{CC} /2	V _{CC} / 2	0.15
3.0 to 3.6	V _{CC} /2	V _{CC} /2	V _{CC} / 2	0.3
4.5 to 5.5	V _{CC} /2	V _{CC} /2	V _{CC} /2	0.3

ORDERING INFORMATION

Device	Package	Specific Device Code	Pin1 Orientation (See bellow)	Shipping [†]
NL27WZ16DFT2G-L22348	SC-88	MR	Q4	3000 / Tape & Reel
NLV27WZ16DFT2G*	SC-88	MR	Q4	3000 / Tape & Reel
NL27WZ16DTT1G	TSOP-6	MR	Q4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin 1 Orientation in Tape and Reel





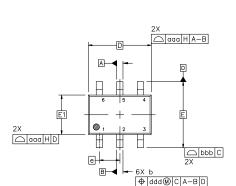
^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.





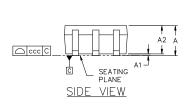
SC-88 2.00x1.25x0.90, 0.65P CASE 419B-02 **ISSUE Z**

DATE 18 APR 2024



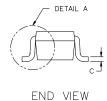
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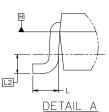
- DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
- ALL DIMENSION ARE IN MILLIMETERS.
- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20
- DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 DATUMS A AND B ARE DETERMINED AT DATUM H.
- DIMENSIONS 6 AND C APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP. 6.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 6 AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

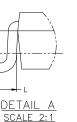


6X 0.30 -

TOP VIEW







GENERIC MARKING DIAGRAM*



DIM	MIN.	NOM.	MAX.		
Α	1.10				
A1	0.00		0.10		
A2	0.70	0.90	1.00		
b	0.15	0.20	0.25		
С	0.08	0.15	0.22		
D		2.00 BSC	;		
E	2.10 BSC				
E1	1.25 BSC				
е	0.65 BSC				
L	0.26 0.36 0.46				
L2		0.15 BSC			
aaa	0.15				
bbb	0.30				
ccc	0.10				
ddd		0.10			

MILLIMETERS

RECOMMENDED MOUNTING FOOTPRINT*

6X 0.66

2.50

FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

XXX = Specific Device Code

= Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

- *Date Code orientation and/or position may vary depending upon manufacturing location.
- *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Rep Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.			
DESCRIPTION:	SC-88 2.00x1.25x0.90, 0.65	5P	PAGE 1 OF 4		

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SC-88 2.00x1.25x0.90, 0.65P CASE 419B-02 ISSUE Z

DATE 18 APR 2024

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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NOTE 5

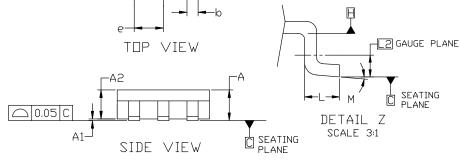
TSOP-6 3.00x1.50x0.90, 0.95P **CASE 318G ISSUE W**

DATE 26 FEB 2024

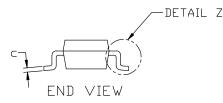


- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- CONTROLLING DIMENSION: MILLIMETERS.
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM
 LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- 4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.

 5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS						
DIM	MIN	NDM	MAX			
Α	0.90	1.00	1.10			
A1	0.01	0.06	0.10			
A2	0.80	0.90	1.00			
b	0.25	0.38	0.50			
C	0.10	0.18	0.26			
D	2.90	3.00	3.10			
Е	2.50	2.75	3.00			
E1	1.30	1.50	1.70			
е	0.85	0.95	1.05			
L	0.20	0.40	0.60			
L2	0.25 BSC					
М	0°		10°			



		-	-	6X -0.60
1				
3.20				6X ⊏0.95
<u> </u>				
	1			
		-	<u>►1</u> 0	.95 ITCH

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference manual, SDLDERRM/D.

DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repositor Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	TSOP-6 3.00x1.50x0.90, 0.95P		PAGE 1 OF 6	

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TSOP-6 3.00x1.50x0.90, 0.95P CASE 318G ISSUE W

DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code XXX = Specific Device Code

A =Assembly Location M = Date Code
Y = Year ■ = Pb-Free Package

W = Work Week
■ Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2	STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. Vz 5. V in 6. V out	STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD	STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR
STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER	STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND	STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE	STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+	STYLE 11: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1/GATE 2	STYLE 12: PIN 1. I/O 2. GROUND 3. I/O 4. I/O 5. VCC 6. I/O
STYLE 13: PIN 1. GATE 1 2. SOURCE 2 3. GATE 2 4. DRAIN 2 5. SOURCE 1 6. DRAIN 1	STYLE 14: PIN 1. ANODE 2. SOURCE 3. GATE 4. CATHODE/DRAIN 5. CATHODE/DRAIN 6. CATHODE/DRAIN	PIN 1. ANODE PIN 2. SOURCE 3. GATE 4. DRAIN	E 16: 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE	STYLE 17: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR	

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