

TFT COLOR LCD MODULE

NL12876BC26-25

39cm (15.3 Type) WXGA LVDS interface (1port)

PRELIMINARY DATA SHEET 🚍

DOD-PP-0167 (4th edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PP-0114(3).

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INTRODUCTION

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Examples: Computers, office automation equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

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Examples: Control systems for transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, medical equipment not specifically designed for life support, safety equipment, etc.

The **Specific** quality grade applies to the products developed, designed and manufactured in accordance with the standards or quality assurance program designated by a customer who requires an extremely higher level of reliability and quality for such products.

Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "Standard" unless otherwise specified in this document.



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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL12876BC26-25 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing circuit, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

• For industrial use

1.3 FEATURES

- High luminance
- High contrast
- Ultra Wide viewing angle
- Wide temperature range
- LVDS interface
- Edge light type (without inverter)



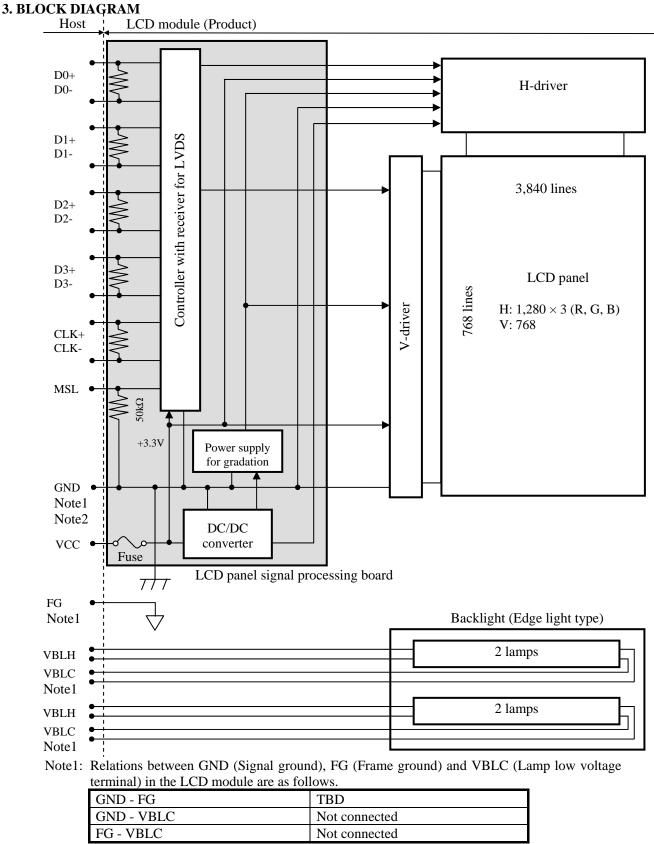
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2. GENERAL SPECIFICATIONS

Display area	$334.08 \text{ (H)} \times 200.45 \text{ (V)} \text{ mm}$			
Diagonal size of display	39cm (15.3 inches)			
Drive system	a-Si TFT active matrix			
Display color	16,777,216 colors (At 8-bit input + FRC)			
Pixel	1280 (H) × 768 (V) pixels			
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe			
Dot pitch	$0.087 (H) \times 0.261 (V) mm$			
Pixel pitch	$0.261 (H) \times 0.261 (V) mm$			
Module size	$358.0 \text{ mm (W) (typ.)} \times 226.0 \text{ mm (H) (typ.)} \times 16.8 \text{ (D) mm (max.)} $ (excluding projection)			
Weight	TBD g (typ.)			
Contrast ratio	BD (typ.)			
Viewing angle	 At the contrast ratio ≥10:1 Horizontal: Right side 85° (typ.), Left side 85° (typ.) Vertical: Up side 85° (typ.), Down side 85° (typ.) 			
Designed viewing direction	 Viewing angle with optimum grayscale (γ=2.2): normal axis (perpendicular) 			
Polarizer surface	Antiglare			
Polarizer pencil-hardness	3H (min.) [by JIS K5400]			
Color gamut	At LCD panel center (40)% (typ.) [against NTSC color space]			
Response time	$\begin{array}{c} Ton + Toff (10\% \leftrightarrow 90\%) \\ 25 \text{ms (typ.)} \end{array}$			
Luminance	At IBL= 6.0 mArms / lamp (400)cd/m ² (typ.)			
Signal system	LVDS 1port (Receiver: THC63LVDF84B, THine Electronics Inc. or equivalent) [8bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE)]			
Power supply voltage	LCD panel signal processing board: 3.3V			
Backlight	Edge light type: 4 cold cathode fluorescent lamps (without inverter)			
	At IBL=6.0mArms / lamp, Checkered flag pattern			



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Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds are connected together in customer equipment.



4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	358.0 ± 0.5 (W) × 226.0 ± 0.5 (H) × 16.8 max. (D) (excluding projection)	Note1	mm
Display area	334.08 (H) × 200.45 (V)	Note1	mm
Weight	TBD (typ.), TBD (max.)		g

Note1: See "7. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

	Parameter		Symbol	Rating	Unit	Remarks
Power supply	LCD panel signal processing board		VCC	-0.3 to +3.6	V	
voltage	Lamp v	voltage	VBLH	TBD	Vrms	
Input voltage	Display Not	-	VD	-0.3 to +3.6 and	V	-
for signals	Function Not		VF	< VCC+0.3	v	
	Storage temperature			-20 to +80	°C	-
Operating	temperature	Front surface	TopF	-10 to +70	°C	Note3
Operating	temperature	Rear surface	TopR	-10 to +70	°C	Note4
				≤ 95	%	$Ta \le 40^{\circ}C$
	Relative humidity		RH	≤ 85	%	40°C <ta≤ 50°c<="" td=""></ta≤>
Note5			КП	≤ 55	%	50°C <ta≤ 60°c<="" td=""></ta≤>
				≤ 36	%	60°C <ta≤ 70°c<="" td=""></ta≤>
	Absolute humidity Note5	AH	≤ 70 Note6	g/m ³	Ta>70°C	

Note1: D0+/-, D1+/-, D2+/-, D3+/-, CLK+/-

Note2: MSL

Note3: Measured at center of LCD panel surface (including self-heat)

Note4: Measured at center of LCD module's rear shield surface (including self-heat)

Note5: No condensation

Note6: Water amount at Ta= 70° C and RH= 36%

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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

							(Ta= 25°C)
Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VCC	3.0	3.3	3.6	V	-
Power supply current		ICC	-	(600) Note1	(900) Note2	mA	at VCC= 3.3V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VCC
Differential input	High	VTH	-	-	+100	mV	at VCM= 1.2V
threshold voltage	Low	VTL	-100	-	-	mV	Note3
Terminating resistance		RT	-	100	-	Ω	-
Input voltage for	High	VFH	0.7VCC	-	VCC	V	CMOS level
DPS and MSL signals	Low	VFL	0	-	0.3VCC	V	emos iever
Input current for	High	IFH	-	-	160	μΑ	
DPS and MSL signal	Low	IFL	-160	-	-	μΑ	-

Note1: Checkered flag pattern [by EIAJ ED-2522]

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS receiver

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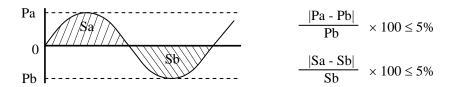


4.3.2 Backlight lamp

						$(Ta=25^{\circ}C, Note1)$
Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.0	6.0	6.5	mArms	at IBL= TBD mArms: L= (400)cd/m ² Note3, Note4
Lamp voltage	VBLH	-	(670)	-	Vrms	Note2, Note3
Lamp starting voltage	VS	(1,100)	-	-	Vrms	Ta= 25°C Note2, Note3, Note5
Lamp starting voltage		(1,600)	-	-	Vrms	Ta= -20°C Note2, Note3, Note5
Lamp oscillation frequency	FO	(38)	(43)	(48)	kHz	Note6

Note1: This product consists of 4 backlight lamps, and these specifications are for each lamp.

- Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).
- Note3: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal). When designing the inverter, evaluate asymmetric of lamp working waveform sufficiently.



Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative Sa: Waveform space for positive part, Sb: Waveform space for negative part.

- Note4: This product consists of 2 lamps. The lamp current should be measured by high-frequency current meter at the low voltage terminal.
- Note5: The inverter should be designed so that the lamp starting voltage can be maintained for more than 1 second. Otherwise the lamp may not be turned on.
- Note6: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle (See "4.8.2 Timing characteristics".)

n : Natural number (1, 2, 3)

Note7: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.



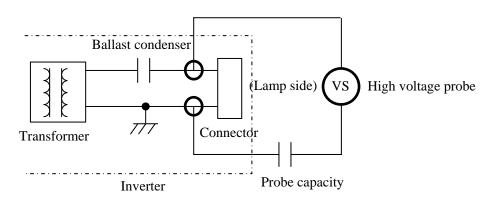
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Note8: In case of Inverter with Ballast condenser, "VS" is the voltage lebel between Ballast condenser and Connector (Refer to the below "Example of measurement"). "VS" should be designed to be more than minimum "VS". Otherwise the lamp may not be turned on because the lamp starting voltage is less than minimum "VS".

Example of measurement

Probe capacity: 3pF (Tektronix, inc.: P6015A)





4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power sup	ply voltage	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VCC	3.3V	≤ 100	mVp-p

Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuse

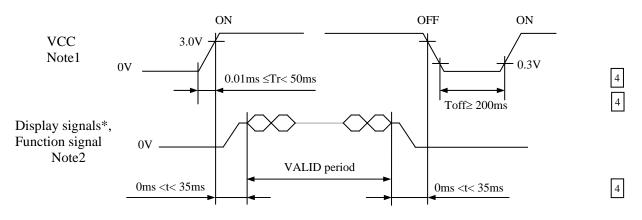
Parameter	F	use	Rating	Fusing current	Remarks
1 arameter	Туре	Supplier	Katilig	Fusing current	Remarks
VCC	(TF16SN3.15)	(KOA)	(3.15A)	(6.3A)	Note1
VCC	(11103N3.13)	.15) (KOA) (32		(0.3A)	Note1

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.



4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board

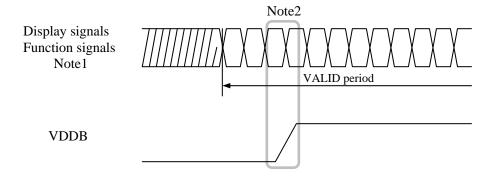


* These signals should be measured at the terminal of 100Ω resistance.

- Note1: In terms of voltage variation (voltage drop) while VCC rising edge is below 3.0V, a protection circuit may work, and then this product may not work.
- Note2: Display signals (D0+/-, D1+/-, D2+/-, D3+/- and CLK+/-) and function signal (MSL) must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. VCC should be cut when the display and function signals are stopped.

4.4.2 Inverter (Option)



- Note1: These are the display and function signals for LCD panel signal processing board.
- Note2: The backlight should be turned on within the valid period of display and function signals, in order to avoid unstable data display.



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4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side):DF14H-20P-1.25H (Hirose Electric Co., Ltd. (HRS))Adaptable plug:DF14-20S-1.25C (Hirose Electric Co., Ltd. (HRS))

Adaptable	piug:	DF14-205-1.25C (H	irose Electric Co., Ltd. (HRS))		
Pin No.	Symbol	Signal	Remarks		
1	VCC	Power supply	Note3		
2	VCC	i ower suppry	110105		
3	GND	Ground	Note3		
4	GND	Ground	1005		
5	D0-	Pixel data	Note2		
6	D0+	Tixel uata	110162		
7	GND	Ground	Note3		
8	D1-	Pixel data	Note2		
9	D1+	Tixer data	1002		
10	GND	Ground	Note3		
11	D2-	Pixel data	Note2		
12	D2+	Tixer data	1002		
13	GND	Ground	Note3		
14	CLK-	Pixel clock	Note2		
15	CLK+	I IACI CIUCK	110162		
16	GND	Ground	Note3		
17	D3-	Pixel data	Note2		
18	D3+	1 1751 Uata	110162		
19	GND	Ground	Note3		
20	MSL	Selection of LVDS Input data map	High: LVDS input map A Low or Open: LVDS input map B Note1,Note4		

Note1: See "4.6 DISPLAY COLORS AND INPUT DATA SIGNALS".

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note3: All GND and VCC terminals should be used without any non-connected lines.

Note4: See "4.5.4 Connection between receiver and transmitter for LVDS".



4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. Wrong connections will cause electric shock and also break down of the product.

CN201 plug (LCD module side): BHR-03VS-1 (J.S.T Mfg. Co., Ltd.) SM02(8.0)B-BHS-1-TB(LF)(SN), SM02(8.0)B-BHS-1-TB Adaptable socket:

			(J.S.T Mfg. Co., Ltd.)
Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.	-	Keep this pin Open.
3	VBLC	Low voltage terminal (Cold)	Cable color: White

CN202 plug (LCD module side): BHR-03VS-1 (J.S.T Mfg. Co., Ltd.) Adaptable socket: SM02(8.0)B-BHS-1-TB(LF)(SN), SM02(8.0)B-BHS-1-TB

(ISTMfg Co. Itd)

			(J.S.1 MIg. Co., Ltd.)
Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Blue
2	N.C.	-	Keep this pin Open.
3	VBLC	Low voltage terminal (Cold)	Cable color: White

CN203 plug (LCD module side): BHR-03VS-1 (J.S.T Mfg. Co., Ltd.) Adaptable socket:

SM02(8.0)B-BHS-1-TB(LF)(SN), SM02(8.0)B-BHS-1-TB (IST Mfg Co Itd)

			(J.S.1 MIg. Co., Ltd.)
Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.	-	Keep this pin Open.
3	VBLC	Low voltage terminal (Cold)	Cable color: White

CN204 plug (LCD module side): BHR-03VS-1 (J.S.T Mfg. Co., Ltd.) SM02(8.0)B-BHS-1-TB(LF)(SN), SM02(8.0)B-BHS-1-TB Adaptable socket: (ISTMfg Co. Itd.)

			(J.S.1 MIg. Co., Ltd.)
Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Blue
2	N.C.	-	Keep this pin Open.
3	VBLC	Low voltage terminal (Cold)	Cable color: White

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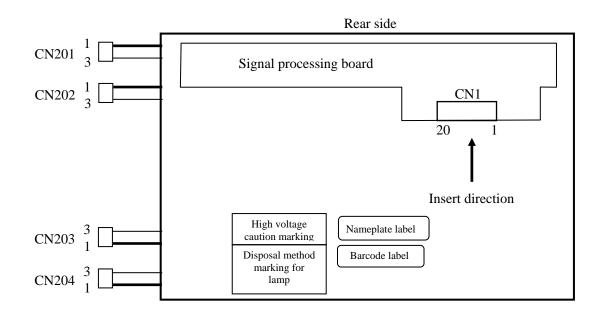
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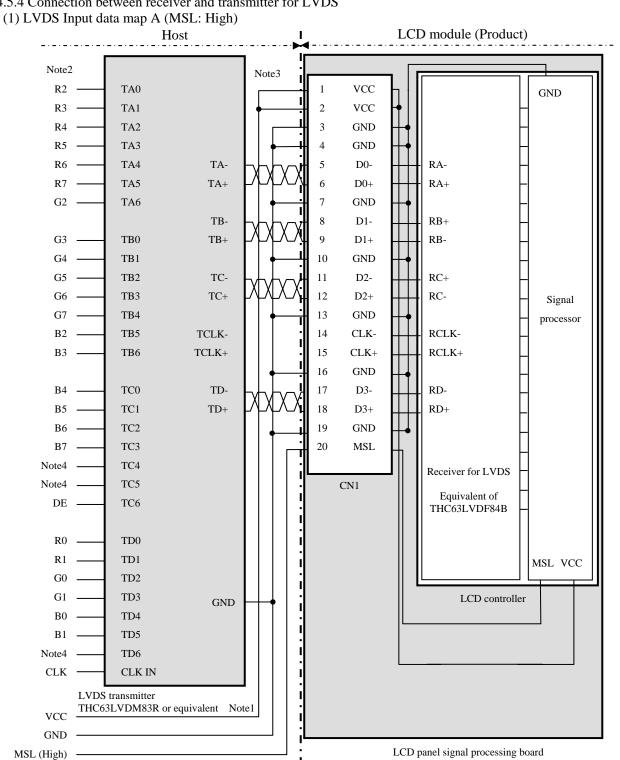
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4.5.3 Positions of plug and socket





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4.5.4 Connection between receiver and transmitter for LVDS

Note1: Recommended transmitter THC63LVDM83R (THine Electronics Inc.) or equivalent

Note2: LSB (Least Significant Bit) - R0, G0, B0 MSB (Most Significant Bit) - R7, G7, B7

- Note3: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
- Note4: Input signals to TC4, TC5 and TD6 are not used inside the product, but do not keep TC4, TC5 and TD6 open to avoid noise problem.

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PRELIMINARY

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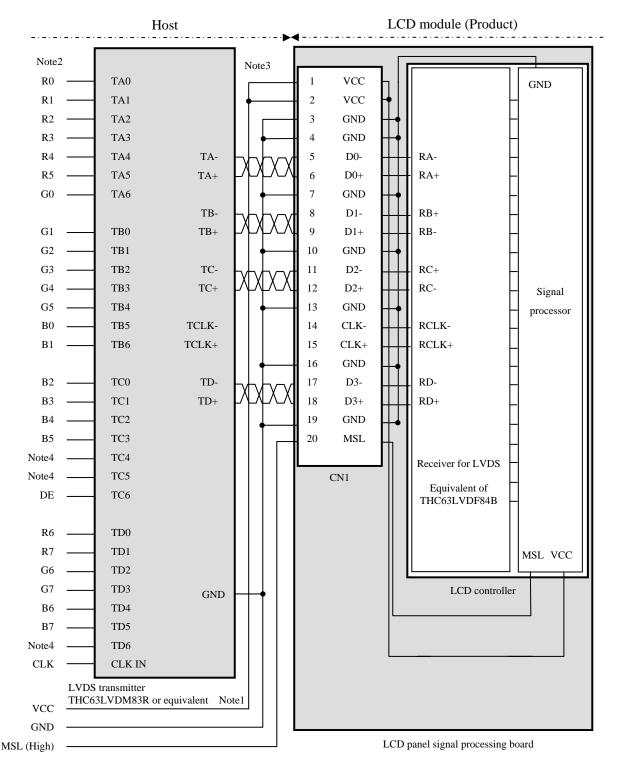
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- Note1: Recommended transmitter THC63LVDM83R (THine Electronics Inc.) or equivalent
- Note2: LSB (Least Significant Bit) R0, G0, B0 MSB (Most Significant Bit) R7, G7, B7
- Note3: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
- Note4: Input signals to TC4, TC5 and TD6 are not used inside the product, but do not keep TC4, TC5 and TD6 open to avoid noise problem.



4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display equivalent of 16,777,216 colors in 256 gray scales. Also the relation between display colors and input data signals is as the following table.

Display	colors								Data	a sig	nal	(0: I	Low	leve	el, 1	: Hi	gh le	evel)							
Display	00013	R7	R6	R5	R4	R3	R2	R 1	R0	G	7 G6	G5	G4	G3	G2	G1	G0	B7	B6	5 B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
ors	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Basic Colors	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
sic	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Ba	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
e		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
scal	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ay s	\uparrow				:	:								:								:			
Red gray scale	\downarrow				:	:								:								:			
Red	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ale		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
sce	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
ray	1				:									:								:			
Green gray scale	\downarrow				:									:								:			
Gree	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
0	_	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
le		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
sca	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Blue gray scale	1				:	:								:								:			
e gi	\downarrow				:	:								:								:			
Blu	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1



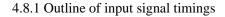
4.7 DISPLAY POSITIONS

The following table is the coordinates per pixel.

C (0,	0) B					
(C(0, 0))	C(1, 0)	• • •	C(X, 0)	• • •	C(1278, 0)	C((1279, 0)
C(0, 1)	C(1, 1)	• • •	C(X, 1)	• • •	C((1278, 1)	C((1279, 1)
•	•	•	•	•	•	•
•	•	• • •	•	• • •	•	• • •
•	•	•	•	•	•	•
C(0, Y)	C(1, Y)	• • •	C(X, Y)	• • •	C((1278, Y)	C((1279, Y)
•	•	•	•	•	•	•
•	•	• • •	•	• • •	•	•
•	•	•	•	•	•	•
C(0, 766)	C(1, 766)	•••	C(X, 766)	• • •	C((1278, 766)	C((1279, 766)
C(0, 767)	C(1,767)	• • •	C(X, 767)	• • •	C((1278, 767)	C((1279, 767)

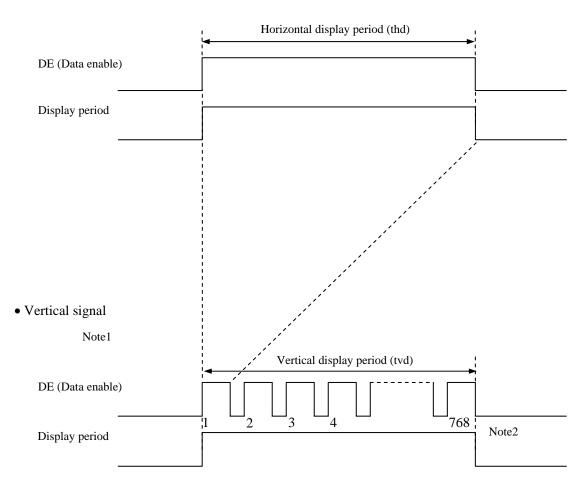


4.8 INPUT SIGNAL TIMINGS



• Horizontal signal

Note1



Note1: This diagram indicates virtual signal for set up to timing. Note2: See "**4.8.3 Input signal timing chart**" for numeration of pulse.



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4.8.2 Timing characteristics

							(Note)	l, Note2, Note3)		
	Paramete	r	Symbol	min.	typ.	max.	Unit	Remarks		
	Fre	quency	1/tc	(70)	79.5	TBD	MHz	12.579ns (typ.)		
CLK	I	Duty	-				-			
	Rise tim	ne, Fall time	-		-		ns	-		
	CLK-DATA	Setup time	-				ns			
DATA	CLK-DATA	Hold time	-		-		ns	-		
	Rise tim	ne, Fall time	-				ns			
		Cycle	th	TBD	20.93	TBD	μs	47.776kHz (typ.)		
	Horizontal	Cycle	ui	-	- 1664 -		CLK	47.770KHZ (typ.)		
		Display period	thd	1280			CLK	-		
	N 7 (* 1	Cycle	tv	TBD	16.70	TBD	ms			
DE	Vertical (One frame)	Cycle	tv	- 798		-	Н	60.0Hz (typ.)		
	(one name)	Display period	tvd		768		Н			
CL	CLK-DE	Setup time -					ns			
	CLK-DE	Hold time	-	-			ns	-		
	Rise time, Fall time						ns			

Note1: Definition of parameters is as follows.

tc=1CLK, th=1H

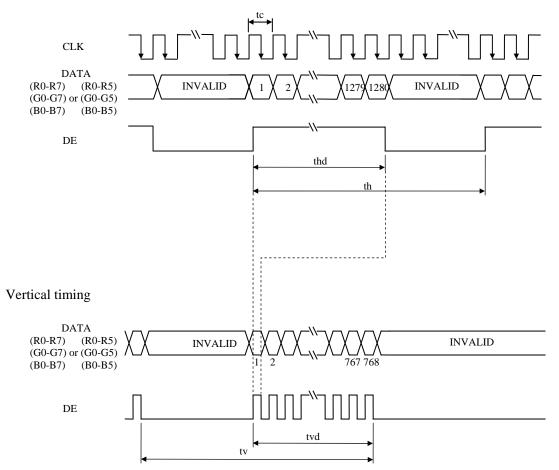
Note2: See the data sheet of LVDS transmitter.

Note3: Vertical cycle (tv) should be specified in integral multiple of Horizontal cycle (th).



4.8.3 Input signal timing chart

Horizontal timing





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4.9 OPTICS

4.9.1 Optical characteristics

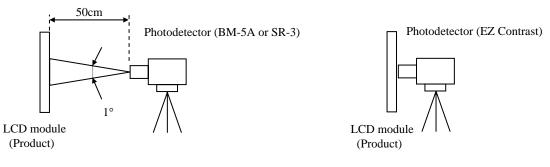
								(Note1,	Note2)	
Parameter	ſ	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument		
Luminance	e	White at center $\theta R = 0^\circ, \ \theta L = 0^\circ, \ \theta U = 0^\circ, \ \theta D = 0^\circ$	L	TBD	(400)	-	cd/m ²	BM-5A	-	
Contrast rat	tio	White/Black at center $\theta R = 0^\circ, \ \theta L = 0^\circ, \ \theta U = 0^\circ, \ \theta D = 0^\circ$	CR	TBD	TBD	-	-	BM-5A	Note3	
Luminance unif	ormity	White $\theta R = 0^\circ, \ \theta L = 0^\circ, \ \theta U = 0^\circ, \ \theta D = 0^\circ$	LU	-	TBD	TBD	-	BM-5A	Note4	
	White	x coordinate	Wx	TBD	0.313	TBD	-			
	white	y coordinate	Wy	TBD	0.329	TBD	-			4
	Red	x coordinate	Rx	-	TBD	-	-			
Chromaticity		y coordinate	Ry	-	TBD	-	-		Note5	
Cinomaticity		x coordinate	Gx	-	TBD	-	-	SR-3		
	Gleen	y coordinate	Gy	-	TBD	-	-	5K-3	Notes	
	Blue	x coordinate	Bx	-	TBD	-	-			
	Diue	y coordinate	By	-	TBD	-	-			
Color game	ut	$\theta R = 0^{\circ}, \ \theta L = 0^{\circ}, \ \theta U = 0^{\circ}, \ \theta D = 0^{\circ}$ at center, against NTSC color space	С	TBD	(40)	-	%			
Response ti	ma	White to Black	Ton	-	TBD	TBD	ms	BM-5A	Note6	
Kesponse un	lile	Black to White	Toff	-	TBD	TBD	ms	DIVI-JA	Note7	
	Right	$\theta U=0^{\circ}, \ \theta D=0^{\circ}, \ CR\geq 10$	θR	TBD	85	-	0			
V ¹	Left	$\theta U=0^{\circ}, \ \theta D=0^{\circ}, \ CR\geq 10$	θL	TBD	85	-	0	EZ	N-4-9	
Viewing angle	Up	$\theta R = 0^{\circ}, \ \theta L = 0^{\circ}, \ CR \ge 10$	θU	TBD	85	-	0	Contrast	Note8	
	Down	$\theta R = 0^{\circ}, \ \theta L = 0^{\circ}, \ CR \ge 10$	θD	TBD	85	-	0			

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta= 25°C, VCC= 3.3V, IBL= 6.0mArms/lamp, Display mode: WXGA, Horizontal cycle= 1/47.776kHz, Vertical cycle= 1/60.0Hz

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



- Note3: See "4.9.2 Definition of contrast ratio".
- Note4: See "4.9.3 Definition of luminance uniformity".
- Note5: These coordinates are found on CIE 1931 chromaticity diagram.
- Note6: Product surface temperature: TopF= TBD°C
- Note7: See "4.9.4 Definition of response times".
- Note8: See "4.9.5 Definition of viewing angles".



4.9.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

Contrast ratio (CR) = Luminance of white screen Luminance of black screen

4.9.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

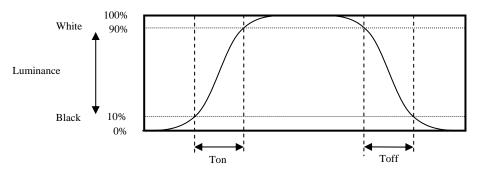
 $Luminance uniformity (LU) = \frac{Maximum luminance from (1) to (5)}{Minimum luminance from (1) to (5)}$

The luminance is measured at near the 5 points shown below.

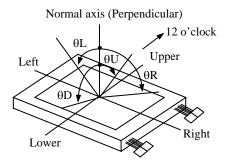
	213		6	40	1067		
128		0				2	
384				3			
501							
640		4				5	
040							

4.9.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.9.5 Definition of viewing angles





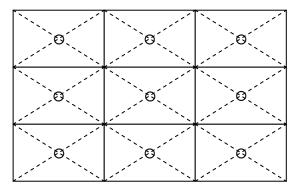
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5. RELIABILITY TESTS

Test item	Condition	(Note1 Judgement
High temperature and humidity (Operation)	 ① 60 ± 2°C, RH= 90%, 240hours ② Display data is black. 	
High temperature (Operation)	 70 ± 3°C, 240hours Display data is black. 	
Heat cycle (Operation)	 ① -10±3°C1hour 70±3°C1hour ② 50cycles, 4 hours/cycle ③ Display data is black. 	
Thermal shock (Non operation)	 ① -20 ± 3°C30minutes 80 ± 3°C30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes. 	No display malfunctions
ESD (Operation)	 150pF, 150Ω, ±10kV 9 places on a panel surface Note2 10 times each places at 1 sec interval 	
Dust (Operation)	 Sample dust: No. 15 (by JIS-Z8901)) 15 seconds stir 8 times repeat at 1 hour interval 	
Vibration (Non operation)	 ① 5 to 100Hz, 11.756m/s² ② 1 minute/cycle ③ X, Y, Z direction ④ 50 times each directions 	No display malfunctions No physical damages
Mechanical shock (Non operation)	 294m/s², 11ms ±X, ±Y, ±Z direction 3 times each directions 	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points.

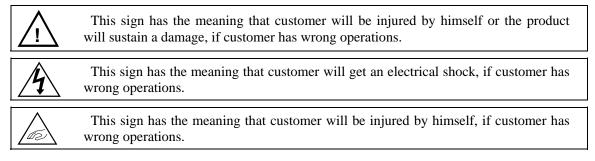




6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**



6.2 CAUTIONS

* Do not touch the working backlight. There is a danger of an electric shock.

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- * Do not touch the working backlight. There is a danger of burn injury.
- * Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 539m/s² and to be not greater 11ms, Pressure: To be not greater 19.6 N (\$\$\phi16mm jig)\$)



6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
- O not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
- ⑦ Do not push nor pull the interface connectors while the product is working.
- ③ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp.

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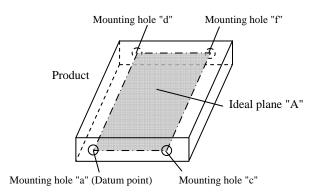
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- Properly connect the plug (backlight side) to adaptable socket (inverter side) without incomplete connection. After connecting, be careful not to hook the lamp cables because incomplete connection may occur by hooking the lamp cables. This incomplete connection may cause abnormal operation of high voltage circuit.
- If the lamp cable is attached on the metal part of the product directly, high frequency leak current to the metal part may occur, then the brightness may decrease or the lamp may not be turned on.
- When handling the product, use of an original protection sheet on the product surface (polarizer) is
 recommended for protection of product surface. Adhesive type protection sheet may change color
 or characteristics of the polarizer.
- ⁽²⁾ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal for the worst, please wash it out with soap.
- ③ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area).Bends or twist described above and undue stress to any portion may cause display mura. Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

- ① Characteristics of the LCD (such as response time, luminance, color uniformity and so on) may be changed depending on ambient temperature. If the product is stored under condition of low temperature for a long time, it may cause display mura. In this case, the product should be operated after enough time being left under condition of operating temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- (5) The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- [©] Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.
- ③ After the product is stored under condition of low temperature or dark place for a long time, the cold cathode fluorescent lamp may not be turned on under the same condition because of the general characteristic of cold cathode fluorescent lamp. In addition, when Luminance control ratio is low in pulse width modulation method inverter, the lamp may not be turned on. In this case, power should be supplied again.

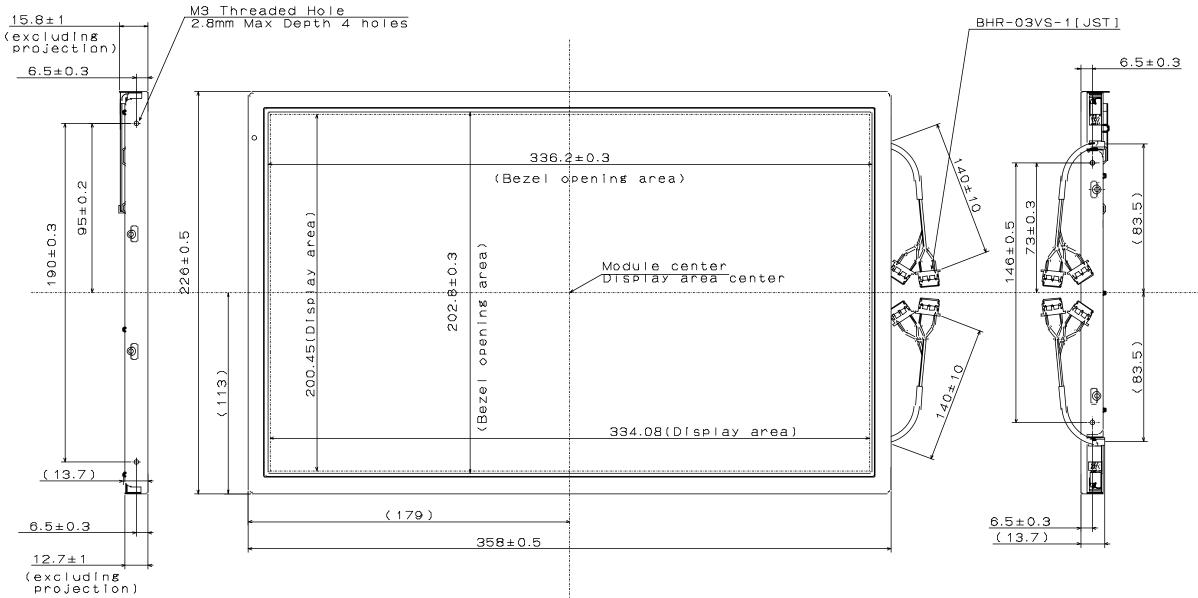
6.3.4 Other

- ① All GND and VCC terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ Pay attention not to insert foreign materials inside of the product, when using tapping screws.
- ④ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.



7. OUTLINE DRAWINGS

7.1 FRONT VIEW



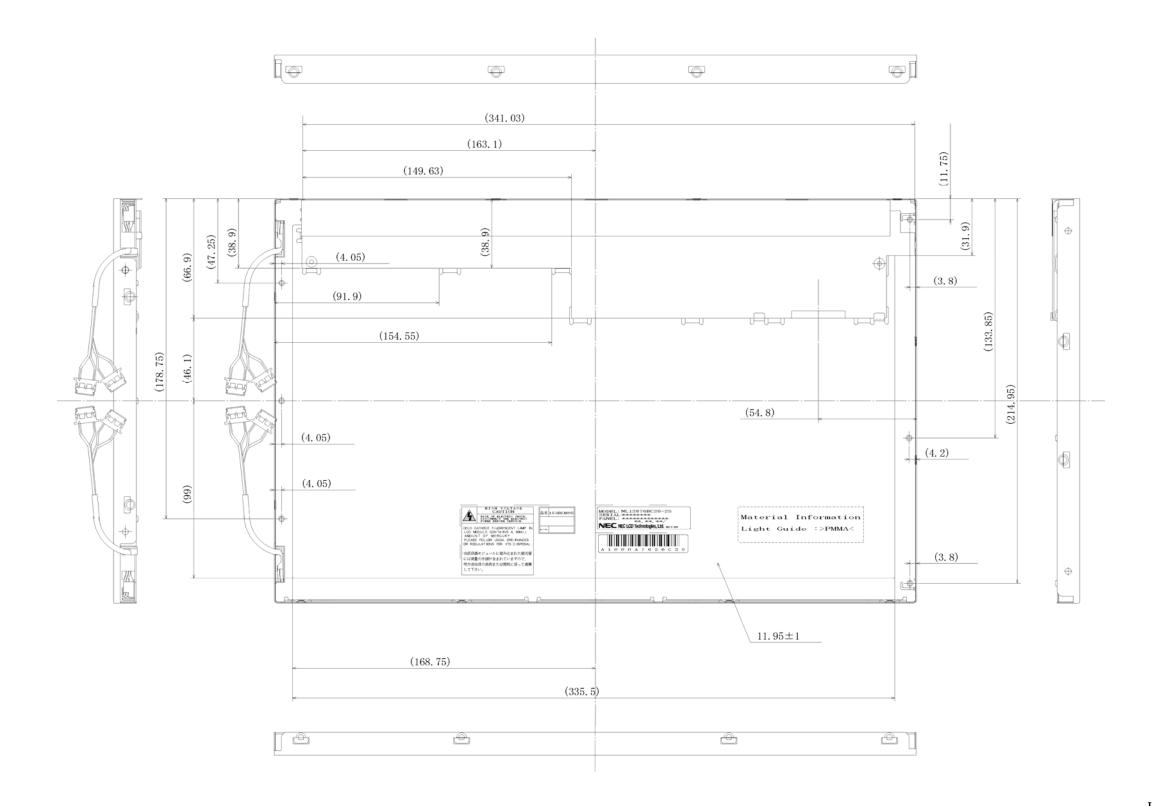
Note1: The values in parentheses are for reference. Note2: The torque for product mounting screws must never exceed TBD N·m.

Unit: mm

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7.2 REAR VIEW



Note1: The values in parentheses are for reference. Note2: The torque for product mounting screws must never exceed TBD N·m.

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Unit: mm



REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st	DOD-PP- 0063	Nov. 1, 2006	Revision contents
edition	0003	2006	New issue
			Writer Approved by Checked by Prepared by Image: Company in the second s
2nd	DOD-PP-	Nov.10,	Revision contents
edition	0091	2006	P26 Outline drawingsSummary outline drawing is changed.
			writer
			Approved by Checked by Prepared by
			T. Ogaun M. Tanaka
			T. OGAWA M. TANAKA
3rd edition	DOD-PP- 0114	Dec.01, 2006	Revision contents
	0114		PS GENERAL SPECIFICATIONS • Display area : 334.08(H) × 200.448(V)mm → 334.08(H) × 200.45(V)mm P7 MECHANICAL SPECIFICATIONS • Display area : 304.128(H) × 228.096(V)mm → 334.08(H) × 200.45(V)mm P8 LCD panel signal processing board • Power supply current : TBD mA (typ., max.) → (600) mA (typ.), (900) mA (max.) P9 Backlight lamp • Lamp current : TBD mArms (min., typ., max.) $\rightarrow 3.0$ mArms (min.), 6.0 mArms (typ.), 6.5 mArms (max.) • Lamp voltage : TBD Vrms (typ.) → (670) Vrms (typ.) • Lamp voltage : TBD Vrms (typ.) → (670) Vrms (min.) (Ta= 25°C) TBD Vrms (min.) → (1,100) Vrms (min.) (Ta= 25°C) TBD Vrms (min.) → (1,600) Vrms (min.) (Ta= 25°C) • Lamp oscillation frequency : TBD kHz (min., typ., max.) $\rightarrow (38)$ kHz (min.), (43) kHz (typ.), (48) kHz (max.) P13 Backlight lamp • CN plug (LCD module side), Adaptable socket : (addition) P19 Timing characteristics • CLK- Frequency : TBD MHz (min.), 81.0 MHz (typ.) → (70) MHz (min.), 79.5 MHz (typ.) • DE- Horizontal- Cycle : 20.84 µs (typ.), 1688 CLK (typ.) • DE- Vertical- Cycle : 16.79 ms (typ.) , 708 H (typ.) • DE- Vertical- Cycle : 16.79 ms (typ.) , 798 H (typ.) P26, P27 OUTLINE DRAWINGS • FRONT VIEW and REAR VIEW is changed. Signature of writer Approved by Checked by Prepared by T. OGAWA TO Checked by Prepared by T. OGAWA TO Checked by Prepared by

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NL12876BC26-25

REVISION HISTORY

ddi DOD-PP- coll of 7 Feb. 6. 2007 Revision contents P1 44 Outine-Structure and Principle • NL12876BC20-XX → NL12876BC20-25 PS General specifications • Di58 (D) mm (max.) (excluding protuberance) • Di68 (D) mm (max.) (excluding projection) • Laminance. Power consumption: At LBL ~ TBD mArms / lam Pb Block diagram: 50ku: (addition) PT Detailed specifications. P1 50 Block diagram: 50ku: (addition) PT Detailed specifications. • 16.8 max (D) (excluding projection) • Absolute maximum ratings-Note2: FRC→ MSL (correction) PS Flectrical characteristics-ICD panel signal processing board • Input voltage for DPS and MSL signals. • WFH: TBD (min).→07.VCC (max), VFL: TBD (max.)→ 0.3VCC (max.) • Input current for DPS and MSL signals. • FIFT: TBD → (TF158N3.15) P11 Fuse: TBD → (TF158N3.15) P12 Power supply voltage sequence.LCD panel processing board • TBD > TF158N3.15) P12 Tower supply voltage sequence.LCD panel processing board • TBD > TF158N3.15) P13 Connections and functions for interface pins-ICD panel signal processing board • TBD > (TF158N3.15) P13 Connections and functions for interface pins-ICD panel signal processing board • CN1 socket (LCD motule side) and Adaptable play (correction) P14 Backlight lamp; CD = -(CN2, CN2, CN2, CN3, CN2, CN4 P15 Positions of play and socket: drawings (addition) P16 P17 Connection between receiver and transmitter for LVDS • LVDS Input data map A and B-19pin: DPS→ GND (correction) P14 Sacklight lamp; CD = -(CN2, CN2, CN2, CN2, CN4 P15 Positions of play and socket: drawings (addition) P16 Connection between receiver and transmitter for LVDS • LVDS Input data map A and B-19pin: DPS→ GND (correction) P14 Sacklight lamp; CD = -(CN2, CN2, CN2, CN2, CN4 P15 Positions of play, CD = -(CN2, CN2, CN4, CN2, P14 • CN2; 24 SBB (M03 Significant Bit); ES, GS, B5 → R7, G7, B7 (correction) P12 Timing characteristics: • Chromaticity-W	Edition	Document number	Prepared date	Revision contents and signature						
PI. P4 Outline-Structure and Principle • NL12876BC20-X2P5 General specifications • Display color: 6 hit \rightarrow 8-bit • Module size: 17.0 (D) mm (max.) (excluding projection) • 1 (a. Rull-TBD mArms / lamp \rightarrow 6.0 mArms / lamped block diagram: 50kG (addition)P7 Detailed Specifications • Mechanical-specifications-Module size: 17.0 max (D) • 1.6 B max (D) (excluding projection)P6 Block diagram: 50kG (addition)P7 Detailed Specifications-Module size: 17.0 max (D) • 1.6 B max (D) (excluding projection)P8 Electrical characteristics-1CD panel signal processing board • lapt voltage for DPS and MSL signals: • VFH: TBD (min.)-90.7VCC (min.), VFL: TBD (max.) \rightarrow 0.3VCC (max.) • lapt urerent for DPS and MSL signals: • IFH: TBD (min.)-910 FTC TBD \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TBD \rightarrow TFF (FB) \rightarrow 0.01 ms $<$ Tr.> 50ms • TFF (FB) \rightarrow 0.01 ms $<$ Tr.>				Revision contents						
PS General specifications• Objaly color: 6-bit \rightarrow 8-bit• Module size: 17.0 (D) mm (max.) (excluding propertion)• Luminance, Power consumption: At IBL = TBD MArms / lamp \rightarrow 6.0 mArms / lamp 60 Bock diagram:50k1 (addition)P7 Detailed specifications• Mechanical - specifications-Module size: 17.0 max (D)• Mechanical - specifications-Module size: 17.0 max (D)• Absolute maximum ratings-Not2: FRC \rightarrow MSL (correction)P8 Electrical characteristics-LCD panel signal processing board• Input voltage for DPS and MSL signals:UFH: TBD (min.) \rightarrow 0.7VCC (min.), VFL: TBD (min.) \rightarrow 0.3VCC (max.)• Input corrent for DPS and MSL signals:IFH: TBD (min.) \rightarrow 0.7VCC (min.), VFL: TBD (min.) \rightarrow 0.3VCC (max.)• Input corrent for DPS and MSL signals:IFH: TBD (min.) \rightarrow 0.7VCC (min.), VFL: TBD (min.) \rightarrow 0.3VCC (max.)• Input corrent for DPS and MSL signals:IFH: TBD (min.) \rightarrow 0.700 (max)• Note8 (addition)P1 Face: TBD \rightarrow Off2: 200ms• TBD \rightarrow CTF165N3.15)P12 Power supply voltage sequence-LCD panel processing board• TBD \rightarrow CTF12: 200ms• TBD \rightarrow CTF12: 200ms <td>edition</td> <td>0107</td> <td>2007</td> <td>P1, P4 Outline-Structure and Principle</td>	edition	0107	2007	P1, P4 Outline-Structure and Principle						
 Display color: 6-bit → 8-bit Module size: 17.0 (D) rmm (max.) (excluding protuberance) → 16.8 (D) mm (max.) (excluding projection) Luminance, Power consumption: At IBL = TBD mArms / lamp→ 6.0 mArms / lar P6 Block diagram::50k (addition) P7 Detailed specifications Mechanical-specifications Mechanical-specifications Mechanical-specifications Mechanical-specifications Mechanical-specifications Mechanical-specifications Mechanical-specifications Mechanical-specifications Mechanical-specifications Methanical-specifications Methanical-specifications Methanical-specifications P8 Electrical characteristics-LCD panel signal processing board Input current for DPS and MSL signals: IFH: TBD (max.)→ 160 (max.), IFL: TBD (max.)→ 0.3VCC (max.) Input current for DPS and MSL signals: IFH: TBD (max.)→ 160 (max.), IFL: TBD (min.)→ -160 (min.) P10 Backlight lamp Note3 (addition) P11 Fuse: TBD → (TF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board TBD ≤1T< TBD → 10ff2 200ms TBD ≤1T< CTBD → 00 fms <4: 35ms Note2: FRC→ MSL (correction) P18 Socitiget lamp: (CAP <- CN201 (CN202 (CN203 (CN204)) P19 Fositions of plug and socket: drawings (addition) P16 Facklight lamp: (CAP <- CN201 (CN202 (CN203 (CN204)) P19 Fositions of plug and socket: drawings (addition) P16 Connection between receiver and transmitter for LVDS I-NDS Input data map A and B-19pit: IPB > 0KD (correction) Note4: TD6 (addition) P17 Connection between receiver and transmitter for LVDS Recommended transmitter terminal marking (correction) Note3: Mass (Most Significant Bit): RS, GS, B5→ R7, G7, B7 (correction) Note2: Measurement conditions (addition) P23 Optics - Optical characteristics Chrom										
 Module size: 17.0 (D) mm (max.) (excluding projection) → 16.8 (D) mm (max.) (excluding projection) Luminance, Power consumption: At IBL- TBD mArms / lam P6 Block diagram:50kQ (addition) P7 Detailed specifications Mechanical- specifications-Module size: 17.0 max (D) → 16.8 max (D) (excluding projection) Absolute maximum ratings-Note2: FRC- MSL (correction) P8 Electrical characteristics-LCD panel signal processing board Input voltage for DPS and MSL signals: WFH: TBD (min.)→0.7VCC (min.), VFL: TBD (max.)→0.3VCC (max.) Input corrent for DPS and MSL signals: IFH: TBD (max.)→ 160 (max.), IFL: TBD (max.)→0.3VCC (max.) P10 Backlight lamp • Note8 (addition) P11 Fase: TBD → (TF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board TBD = TT TBD→ TOT2 20ms • TBD → TOT2 20ms TBD → TOT2 20ms (TT3D)→ TOT2 (NDM) P13 Connections and functions for interface pins-LCD panel signal processing board CN socket (LCD module side) and Adaptable ping (correction) P14 Backlight lamp: (N2→ CN20)(N202,CN203,(N204 P15 Positions of plug and socket: drawings (addition) P16-P17 Connection between receiver and transmitter for LVDS LVDS Input data map A and B-19pin: DPS→ GND (correction) Note2: MSB (Most Significant Bit): FS, 55, S+ S+7, G7, B7 (correction) P17 Connection between receiver and transmitter for LVDS ECA-MSB (Most Significant Bit): FS, 55, S+3, G7, G7, B7 (correction) P12 Pointai data map A and B-19pin: DPS→ GND (correction) Note2: MSB (Most Significant Bit): FS, 55, S+3, S+7, G7, B7 (correction) P16-P17 Connection between receiver and transmitter for LVDS ECA-MSB (Most Significant Bit): FS, 55, S+3, S+7, G7, B7 (correction) P14 Edability test: Vibration and Mechani										
 → 16.8 (D) mm (max.) (excluding projection) Liminace, Power consumption: At IBL= TBD mArms / lamp→ 6.0 mArms / lamp6 Block diagram:50k0 (addition) PO Etailed specifications Mechanical -specifications-Module size: 17.0 max (D) → 16.8 max (D) (excluding projection) Absolute maximum ratings-Note2: FRC→ MSL (correction) PB Electrical characteristics-LCD panel signal processing board Input curren for DPS and MSL signals: UFH: TBD (min.)→0.7VCC (min.), VFL: TBD (max.)→ 0.3VCC (max.) Input curren for DPS and MSL signals: UFH: TBD (min.)→0.7VCC (min.), VFL: TBD (min.)→160 (min.) P10 Backlight lamp Note8 (addition) P11 Fuse: TBD→ (TF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board TBD ≤Tr: TBD→ 0.01 ms ≤Tr< 50 ms TOR <tbd> ToT> 20 ms</tbd> TOR <tbd> ToT> 20 ms</tbd> TOR <tbd> ToT> 20 ms</tbd> TOR <tbd> ToT> 20 most</tbd> Statisting tamp: Currection) P13 Sconnections and functions for interface pins-LCD panel signal processing board CNI socket (LCD module side) and Adaptable plug (correction) P14 Backlight lamp: Currect erravings (addition) P16-P17 Connection between receiver and transmitter for LVDS LVDS Input data map A and B-19pin: DPS→ GND (correction) Note3: TBC (addition) P17 Connection between receiver and transmitter for LVDS Recommended transmitter terminal marking (correction) Note3: MSB (Most Significant Bit); PS, GS, B5→ R7, G7, B7 (correction) Note2: MES (module: side) and (solitation) P24 Optics- Optical characteristics CLK: 12.579 ns (typ.), DE-Horizontal: 47.776 kHz (typ.), DE-Vertical: 60.0 kHz (addition) P24 Optics- optical characteristics CLK: 12.579 ns (typ.), DE-H										
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P7 Detailed specifications • Mechanical - specifications-Module size: 17.0 max (D) → 16.8 max (D) (excluding projection) • Absolute maximum ratings-Note2: FRC→ MSL (correction) P8 Electrical characteristics-LCD panel signal processing board • Input voltage for DPS and MSL signals: VFH: TBD (min.)→0.7VCC (min.), VFL: TBD (max.)→ 0.3VCC (max.) • Input current for DPS and MSL signals: IFH: TBD (max.)→ 160 (max.), IFL: TBD (min.)→ -160 (min.) P10 Backlight lamp • Note8 (addition) P11 Fuse: TBD → (IF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board • TBD <tc 0.01m="" tbd→="" td="" ≤tr<50ms<=""> • TBD <tc 0.01m="" tbd→="" td="" ≤tr<50ms<=""> • TBD <cc 0.01m="" tbd→="" td="" ≤tr<50ms<=""> • Note8 (addition) P13 Connections and functions for interface pins-LCD panel signal processing board • CN1 socket (LCD module side) and Adaptable plug (correction) P14 Backlight lamp: (N2→ CN201 CN202 CN203 CN204 P15 Positions of plug and socket: drawings (addition) P17 Connection between receiver and transmitter for LVDS • LVDS Input data map A and B -19pin: DPS→ GRD (correction) • Note2: MSB (Most Significant Bi): RS, (55, B5→ R7, G7, B7 (correction) P17 Connection between receiver and transmitter for LVDS <t< td=""><td></td><td></td><td></td><td>• Luminance, Power consumption: At IBL= TBD mArms / lamp\rightarrow 6.0 mArms / lamp</td></t<></cc></tc></tc>				• Luminance, Power consumption: At IBL= TBD mArms / lamp \rightarrow 6.0 mArms / lamp						
• Mechanical- specifications-Module size: 17.0 max (D) \rightarrow 16.8 max (D) (excluding projection) P8 Electrical characteristics-LCD panel signal processing board • Input voltage for DPS and MSL signals: VFH: TBD (mnx) \rightarrow 0.7VCC (min), VFL: TBD (max) \rightarrow 0.3VCC (max.) • Input current for DPS and MSL signals: IFH: TBD (max) \rightarrow 160 (max), IFL: TBD (min) \rightarrow -160 (min). P10 Backlight lamp • Notes (addition) P11 Fuse: TBD \rightarrow (TF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board • TBD <tr tbd<math="">\rightarrow 0.01 ms \leqTr < 50 ms • Toff2 TBD\rightarrow 0.01 ms \leqTr < 50 ms • Toff2 TBD\rightarrow 0.01 ms \leqTr < 50 ms • Toff2 TBD\rightarrow 0.02 ms \leqTr < 50 ms • Toff2 TBD\rightarrow 0.01 ms \leqTr < 20 ms • Toff2 TBD\rightarrow 0.01 ms \leqTr < 50 ms • Toff2 TBD\rightarrow 0.02 ms \leqTr < 0.02 ms \leqTr < 0.02 ms • Toff2 TBD\rightarrow 0.02 ms • Toff2 TBD\rightarrow 0.02 ms \leqTr < 0.02 ms • Toff2 TBD\rightarrow 0.02 ms • Toff2</tr>										
$ \rightarrow 168 \text{ max} (D) (excluding projection) • Absolute maximum ratings-Note2: FRC → MSL (correction) P8 Electrical characteristics-LCD panel signal processing board • Input voltage for DPS and MSL signals: VFH: TBD (max.) → 160 (max.), VFL: TBD (max.) → 0.3VCC (max.) • Input current for DPS and MSL signals: IFH: TBD (max.) → 160 (max.), IFL: TBD (max.) → 0.3VCC (max.) P10 Backlight Imp • Note8 (addition) P11 Fuse: TBD → CTF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board • TBD 5TI< TBD → 0.01ms 5TI< 50ms • TBD - Toff ≥ 200ms • TBD - C+ TBD → 0.01ms sTI< 50ms • Note2: FRC → MSL (correction) P13 Connections and functions for interface pins-LCD panel signal processing board • CN1 socket (LCD module side) and Adaptable ping (correction) P14 Backlight Imp; (CN2 - CN201, CN202, CN204 P15 Positions of plug and socket: drawings (addition) P16-P17 Connection between receiver and transmitter for LVDS • LVDS Input data map A and B-19pin: DPS → GND (correction) • Note2: MSB (Most Significant Bi): RS, GS, B5 → R7, G7, B7 (correction) P17 Connection between receiver and transmitter for LVDS • Recommended transmitter terminal marking (correction) • Note2: MBB (Most Significant Bi): RS, GS, B5 → R7, G7, B7 (correction) P121 Timing characteristics- • Chromaticity-Wx,Wy (typ.): TBD (typ.) → 0.313, 0.329 (typ.) (correction) P124 Optics- Optical characteristics • Chromaticity-Wx,Wy (typ.): TBD (typ.) → 0.313, 0.329 (typ.) (correction) P24 Potics- definition of response times (correction) P24$										
 Absolute maximum ratings-Note2: FRC→ MSL (correction) P8 Electrical characteristics-LCD panel signal processing board Input voltage for DPS and MSL signals: VFH: TBD (min.)→0.7VCC (min.), VFL: TBD (max.)→ 0.3VCC (max.) Input current for DPS and MSL signals: IFH: TBD (max.)→160 (max.), IFL: TBD (min.)→ -160 (min.) P10 Backlight lamp • Note8 (addition) P11 Fuse: TBD → (TF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board TBD ≤TTC TBD→ 0.01 ms ≤TT< 50ms T6f2: TBD→ Toff2 200ms T6f2: TBD→ Toff2 200ms T6f2: TBD→ Toff2 200ms T6f2: TBD→ Toff2 200ms T0f2: CLCD module side) and Adaptable plug (correction) P13 Connections and functions for interface pins-LCD panel signal processing board CNI socket (LCD module side) and Adaptable plug (correction) P14 Backlight lamp: CN2→ CN201, CN202, CN203, CN204 P15 Positions of plug and socket: drawings (addition) P16-P17 Connection between receiver and transmitter for LVDS LVDS Input data map A and B-19pin: DPS→ GND (correction) Note4: TD6 (addition) P17 Connection between receiver and transmitter for LVDS Recommended transmitter terminal marking (correction) Note2-MSB (Most Significant Bit): RS, GS, B5→ R7, G7, B7 (correction) P121 Timing characteristics-Remarks CLK: 12.579 ns (typ.), DE-Horizontal: 47.776 kHz (typ.), DE-Vertical: 60.0 kHz (addition) P23 Optics- Optical characteristics Chromaticity-Wx.Wy (typ.): TBD (typ.) → 0.313, 0.329 (typ.) (correction) Note2: MES aurement conditions (addition) P24 Potics- definition of response times (correction) P24 Reparations-Attentions Handling of the product: ③, ④ and ⑤ (addition) Char										
P8 Electrical characteristics-LCD panel signal processing board• Input voltage for DPS and MSL signals: VFR: TBD (min.) $\rightarrow 0.7VCC$ (min.), VFL: TBD (max.) $\rightarrow 0.3VCC$ (max.)• Input current for DPS and MSL signals: IFH: TBD (max.) $\rightarrow 160$ (max.), IFL: TBD (min.) $\rightarrow -160$ (min.)P10 Backlight lamp • Note8 (addition)P11 Fuse: TBD $\rightarrow (TF16SN3.15)$ P12 Power supply voltage sequence-LCD panel processing board • TBD $\preceq tree TBD \rightarrow 001m s \preceq tree some• Toff2 TBD \rightarrow 001m s \preceq tree some• Toff2 TBD \rightarrow 001m s \preceq tree some• Toff2 TBD \rightarrow 001m s \preceq tree some• Note2: FRC \rightarrow MSL (correction)P13 Connections and functions for interface pins-LCD panel signal processing board• CN1 socket (LCD module side) and Adaptable plug (correction)P14 Backlight lamp: CN2 \rightarrow CN201, CN202, CN203, CN204P15 P15 Tonnection between receiver and transmitter for LVDS• LVDS Input data map A and B-19pin: DPS \rightarrow GND (correction)P16-P17 Connection between receiver and transmitter for LVDS• LVDS Input data map A and B-19pin: DPS \rightarrow GND (correction)P17 Connection between receiver and transmitter for LVDS• Recommended transmitter terminal marking (correction)P17 Timing characteristics-Remarks• CLK: 12.579 ns (typ.), DE-Horizontal: 47.776 kHz (typ.), DE-Vertical: 60.0 kHz(addition)P23 Optics-Optical characteristics• Chromaticity-Wx,Wy (typ.): TBD (typ.) \rightarrow 0.313, 0.329 (typ.) (correction)P24 Optics- definition of response times (correction)P24 P24 Precations-Attentions• Handling of the product: \textcircled{0}, \textcircled{0} and \textcircled{0} (addition)P24 P23 Outline drawings: (change)P23 Outline drawings: (change)P34 Outline drawings: (change)P35 Outline drawings: (change)<$										
VFH: TBD (min.) $\rightarrow 0.7VCC$ (min.), VFL: TBD (max.) $\rightarrow 0.3VCC$ (max.)• Input current for DPS and MSL signals: IFH: TBD (max.) $\rightarrow 160$ (min.)P10 Backlight lamp • Note8 (addition)P11 Fuse: TBD \rightarrow (TF16SN3.15)P12 Power supply voltage sequence-LCD panel processing board • TBD \supset Tr TBD \rightarrow Toff2 200ms • TBD \supset Tr TBD \rightarrow Oms \leq 35ms • Note2: FRC \rightarrow MSL (correction)P13 Connections and functions for interface pins-LCD panel signal processing board • CN1 socket (LCD module side) and Adaptable plug (correction)P14 Backlight lamp: CN2 \rightarrow CX201(CN202,CN203,CN204P15 Positions of plug and socket: drawings (addition)P16-P17 Connection between receiver and transmitter for LVDS • LVDS Input data map A and B-19pin: DPS \rightarrow GND (correction)P17 Connection between receiver and transmitter for LVDS • Recommended transmitter terminal marking (correction) • Note2-MSB (Most Significant Bit): R5, G5, B5 \rightarrow R7, G7, B7 (correction)P21 Timing characteristics • CLK: 12.57 ps (typ.), DE-Horizontal: 47.776 kHz (typ.), DE-Vertical: 60.0 kHz (addition)P23 Optics- Optical characteristics • Chromaticity-WX.Wy (typ.): TBD (typ.) $\rightarrow 0.313, 0.329$ (typ.) (correction)P24 Optics- definition of response times (correction) P25 Reliability test-Vibration and Mechanical shock: Test condition (addition)P27-P28 Precautions-Attentions • Handling of the product: \odot , \oslash and \textcircled{O} (addition)P29-30 Outline drawings: (change)Signature of writer Approved byApproved byCharacteristics: (charge)										
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P10 Backlight lamp • Note8 (addition)P11 Fuse: TBD \rightarrow (TF165N3.15)P12 Power supply voltage sequence-LCD panel processing board • TBD \leq Tr TBD \rightarrow 0.01 ms \leq Tr \leq 50ms• TBD \leq Tr TBD \rightarrow 0.01 ms \leq Tr \leq 50ms• TBD \leq Tr TBD \rightarrow 0.01 ms \leq Tr \leq 50ms• TBD \leq Tr TBD \rightarrow 0.01 ms \leq Tr \leq 50ms• TBD \leq Tr TBD \rightarrow 0.01 ms \leq Tr \leq 50ms• TBD \leq Tr CBD \rightarrow 0.01 ms \leq Tr \leq 50ms• TBD \leq Tr CBD \rightarrow 0.01 ms \leq Tr \leq 50ms• TBD \leq Tr CBD \rightarrow 0.01 ms \leq Tr \leq 50ms• Note2: FRC \rightarrow MSL (correction)P13 Connections and functions for interface pins-LCD panel signal processing board • CN1 socket (LCD module side) and Adaptable plug (correction)P14 Backlight lamp: CN2 \rightarrow CN201, CN202, CN203, CN204P15 Positions of plug and socket: drawings (addition)P16-P17 Connection between receiver and transmitter for LVDS • LVDS Input data map A and B-19pin: DPS \rightarrow GND (correction)• Note4: TDG (addition)P17 Connection between receiver and transmitter for LVDS • Recommended transmitter terminal marking (correction)P17 Connection between receiver and transmitter for LVDS • Recommended transmitter terminal marking (correction)P21 Timing characteristics-Remarks • CLK: 12,579 ns (typ.), DE-Horizontal: 47.776 kHz (typ.), DE-Vertical: 60.0 kHz (addition)P23 Optics Optical characteristics • Chromaticity-Wx, Wy (typ.): TBD (typ.) \rightarrow 0.313, 0.329 (typ.) (correction) • Note2: Measurement conditions (addition)P24 Optics- definition of response times (correction)P25 Reliability test- Vibration and Mechanical shock: Test condition (addition)P27-P28 Precautions-Attentions • Handling of the product:				· · ·						
• Note ⁵ (addition) P11 Fuse: TBD \rightarrow (TF16SN3.15) P12 Power supply voltage sequence-LCD panel processing board • TBD \leq Tr $<$ TBD \rightarrow 0.01ms \leq Tr $<$ 50ms • Toff \geq TBD \rightarrow Toff \geq 200ms • TBD \leq CT $<$ TBD \rightarrow 0.01ms \leq Tr $<$ 55ms • Note2: FRC \rightarrow MSL (correction) P13 Connections and functions for interface pins-LCD panel signal processing board • CN1 socket (LCD module side) and Adaptable plug (correction) P14 Backlight lamp: CN2 \rightarrow CN201, CN202, CN203, CN204 P15 Positions of plug and socket: drawings (addition) P16-P17 Connection between receiver and transmitter for LVDS • LVDS Input data map A and B-19pin: DPS \rightarrow GND (correction) • Note4: TD6 (addition) P17 Connection between receiver and transmitter for LVDS • Recommended transmitter terminal marking (correction) • Note2-MSB (Most Significant Bit): RS, GS, B5 \rightarrow R7, G7, B7 (correction) P21 Timing characteristics-Remarks • CLK: 12.579 ns (typ.), DE-Horizontal: 47.776 kHz (typ.), DE-Vertical: 60.0 kHz (addition) P23 Optics- Optical characteristics • Chromaticity-Wx,Wy (typ.): TBD (typ.) \rightarrow 0.313, 0.329 (typ.) (correction) P35 Reliability test - Vibration and Mechanical shock: Test condition (addition) P24 Optics- definition of response times (correction) P25 Reliability test - Vibration and Mechanical shock:: Test condition (addition) P27-P28 Precautions-Attentions • Handling of the product: @, @ and @ (addition) P29-30 Outline drawings: (change) Signature of writer Approved by Checked by Prepared by T. Quant										
P12 Power supply voltage sequence-LCD panel processing board• TBD \leq TRD \rightarrow 0.01ms \leq Tr < 50ms										
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