NEC

TFT COLOR LCD MODULE

NL128102AC31-01E

51cm (20.1 Type)
SXGA
Analog, Full-color

SPECIFICATIONS

(First edition)

DATA SHEET

All information is subject to change without prior notice.

1st Engineering Department
Color LCD Division
Display Device Operations Unit
NEC Electron Devices
NEC Corporation

Approve		Mar. 13, 2001
Check		
Prepare		Mar. 13, 2001

INTRODUCTION

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Anti-radioactive design is not implemented in this product.

CONTENTS

1.DESCRIPTION

NL128102AC31-01E is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL128102AC31-01E has a built-in backlight with an inverter.

The 51cm(20.1" Type) diagonal display area contains 1280×1024 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has wide viewing angle and multi-scan function. Therefore, this module is so called Super Fine TFT.

2. FEATURES

- Ultra wide viewing angle with lateral electric field.
- High luminance and Low reflection
- Analog RGB signals
- Multi-scan function: e.g., SXGA, XGA, SVGA, VGA, VGA-TEXT, MAC, SUN
- Direct type backlight (twelve lamps, Inverter)
- Replaceable backlight unit and inverter
- On Screen Display
- Approved by UL1950 Third Edition (File No. E170632) and CAN/CSA-C22.2 No.950-95 (File No. E170632)

VESA: Video Electronics Standards Association
DPMS: Display Power Management Signaling
DDC1: Display Data Channel 1
DDC2B: Display Data Channel 2B

3. APPLICATIONS

- Engineering work stations, Desk-top type of PCs
- Display terminals for control system
- Monitors

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an Electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	399.4(H)×319.5(V)mm
Drive system	a-Si TFT active matrix
Display colors	full-color
Number of pixels	1280×1024
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.312(H)×0.312(V)mm
Module size	470.0(H)×382.0(V)×39.8 typ. (D) mm
Weight	2380 g(typ.)
Contrast ratio	250:1(typ.)

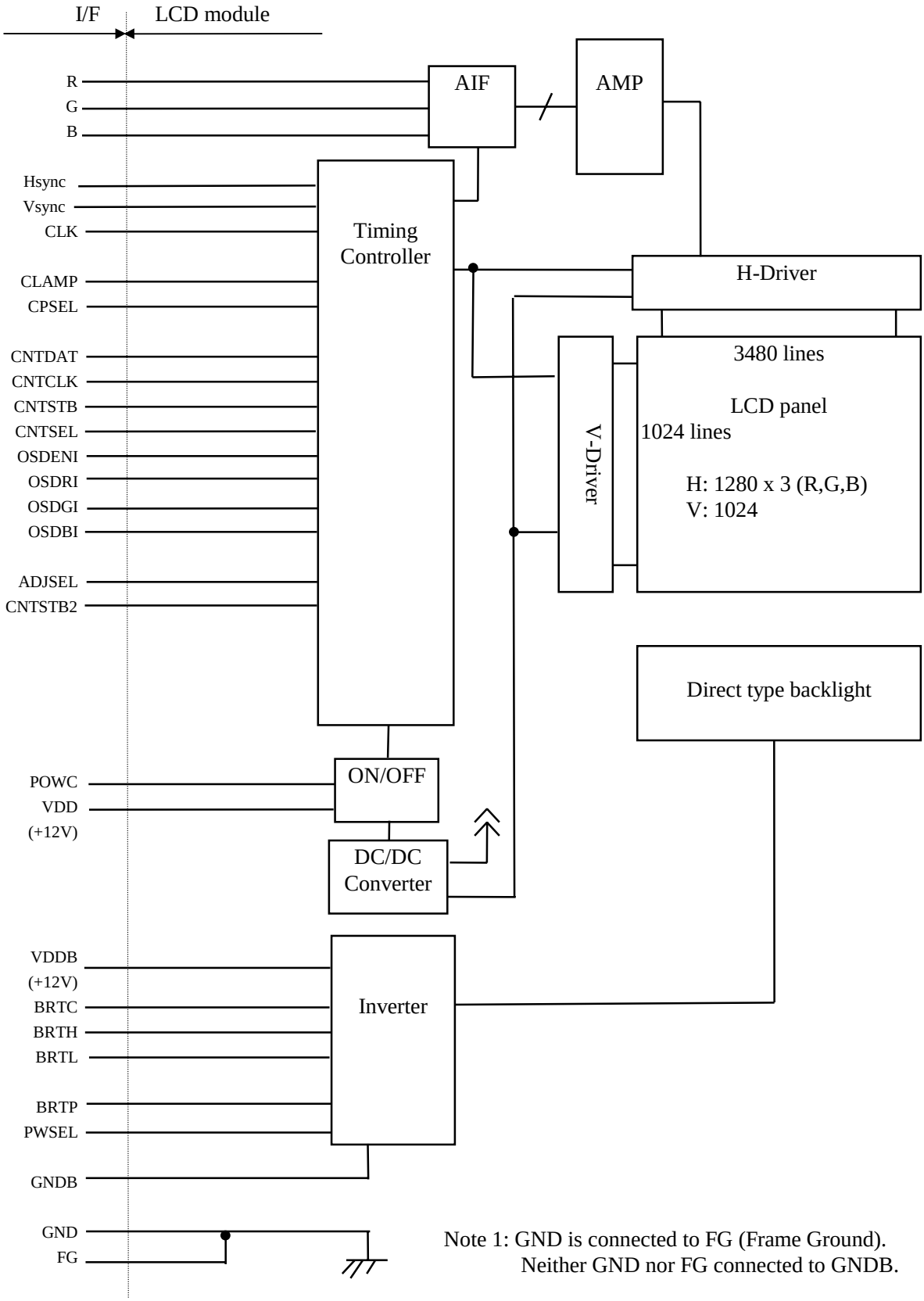
Viewing angle (more than the contrast ratio of 10:1)

- Horizontal: 85 ° (typ. , left side, right side)
- Vertical: 85 ° (typ. , up side, down side)

Optimum grayscale (γ =2.2): perpendicular

Pencil hardness	3 H（min. JIS K5400）
Color gamut	60 % (typ. At center, To NTSC)
Response time	30 ms (typ.), " black " to " white " (10% → 90%)
Luminance	250 cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals(Hsync, Vsync), Dot clock(CLK)
Supply voltage	12 V, 12 V (Logic, LCD driving, Backlight)
Backlight	Direct type: twelve cold cathode fluorescent lamps with inverter 〈Replacement parts〉 Inverter Parts No. : 201PW021 Backlight unit Parts No. : 201LHS02
Power consumption	52.1 W (typ.)

6. BLOCK DIAGRAM



Note 1: GND is connected to FG (Frame Ground).
Neither GND nor FG connected to GNDB.

7. SPECIFICATIONS

7.1 GENERAL SPECIFICATIONS

Items	Contents	Unit
Module size	470.0±1.0 (H) x 382.0±1.0 (V) x 42.5 (max.)(D)	mm
Display area	399.4 (H) x 319.5 (V)	mm
Number of dots	1280 x 3 (H) x 1024 (V)	dots
Pixel pitch	0.312 (H) x 0.312 (V)	mm
Dot pitch	0.104 (H) x 0.312 (V)	mm
Pixel arrangement	RGB (red, green, blue) vertical stripe	—
Display colors	full color	Color
Weight	2380 (typ.), 2490 (max.)	g

7.2 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Ratings	Unit	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta＝25℃
	VDDB	-0.3 to +14	V	
Logic input voltage	Vin1	-0.3 to +5.5	V	Ta＝25℃ VDD＝12V
R,G, B input voltage	Vin2	-6.0 to +6.0	V	
CLK input voltage	Vin3	-7.0 to +7.0	V	
BRTL input voltage	Vin4	-0.3 to +1.5	V	
Storage temp.	Tst	-20 to +60	℃	—
Operating temp.	Top 1	0 to +55	℃	Module front surface Note 1
	Top 2	≦ 64	℃	Module rear surface Note 2
Relative humidity (RH) Note 3	≦ 95%		%	Ta≦40 ℃
	≦ 85%		%	40＜Ta≦50 ℃
	≦ 70%		%	50＜Ta≦55 ℃
Absolute humidity Note 3	Absolute humidity (g/m^3) shall not exceed Ta=55℃, RH=70% level.		g/m^3	Ta＞55 ℃

Note 1: Measured at the surface of display area (including self heat)
Note 2: Measured at the rear shield (including self heat)
Note 3: No condensation

7.3 ELECTRICAL CHARACTERISTICS

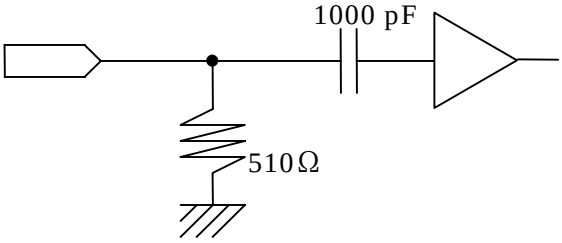
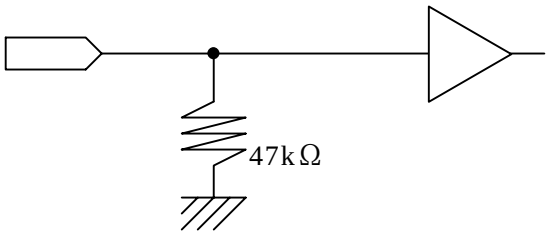
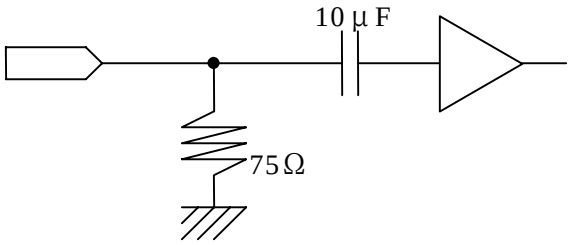
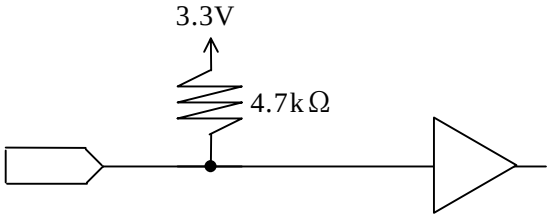
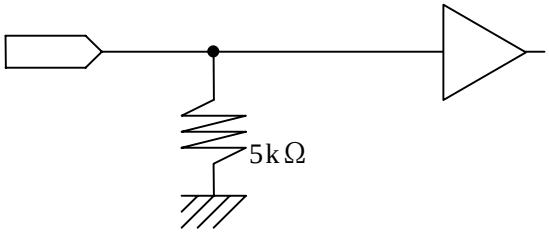
(1) Logic, LCD driving, Backlight

(Ta＝25℃)

Items	Symbols	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	10.8	12.0	13.2	V	for LCD driving
	VDDB	10.8	12.0	13.2	V	for backlight
Logic input " L " voltage	ViL1	0	—	0.8	V	for BRTP
Logic input " H " voltage	ViH1	2.0	—	5.25	V	
Logic input " L " voltage	ViL2	0	—	0.8	V	for except BRTP
Logic input " H " voltage	ViH2	2.0	—	5.25	V	
CLK input voltage	ViCLK	0.6	—	1.0	Vp-p	for CLK
CLK DC input voltage	ViDC CLK	-4.5	—	+4.5	V	
Logic input " L " current 1	IiL1	-10	—	—	μA	for Hsync, Vsync
Logic input " H " current 1	IiH1	—	—	160	μA	
Logic input " L " current 2	IiL2	-10	—	—	μA	for CNTSEL, CPSEL, and POWC
Logic input " H " current 2	IiH2	—	—	10	μA	
Logic input " L " current 3	IiL3	-10	—	—	μA	for CNTDAT, CNTSTB, CNTCLK, CLAMP, OSDENI, OSDRI, OSDGI, OSDBI, ADJDEL, CNTSTB2
Logic input " H " current 3	IiH3	—	—	1400	μA	
Logic input " L " current 4	IiL4	-1.6	—	—	μA	for BRTP
Logic input " H " current 4	IiH4	—	—	3.5	μA	
Logic input " L " current 5	IiL5	-610	—	—	μA	for BRTC, PWSEL
Logic input " H " current 5	IiH5	—	—	440	μA	
Supply current	IDDB	—	3500 note 1	4200	mA	for backlight VDDB＝12.0V (Max. luminance)
	IDD	—	839 note 1	1100	mA	for LCD driving VDD＝12.0V

Note 1: Checker flag pattern. (in EIAJ ED-2522)

(2) Input equivalent circuit

Signals	Equivalent circuit
CLK	
Hsync, Vsync CNTDAT, CNTCLK CNTSTB, CLAMP CNTSTB2	
R, G, B	
POWC, CNTSEL, CPSEL, ADJSEL	
OSDRI, OSDGI, OSDBI,OSDENI	

(3) Video signal (R, G, B) input

(Ta=25°C)

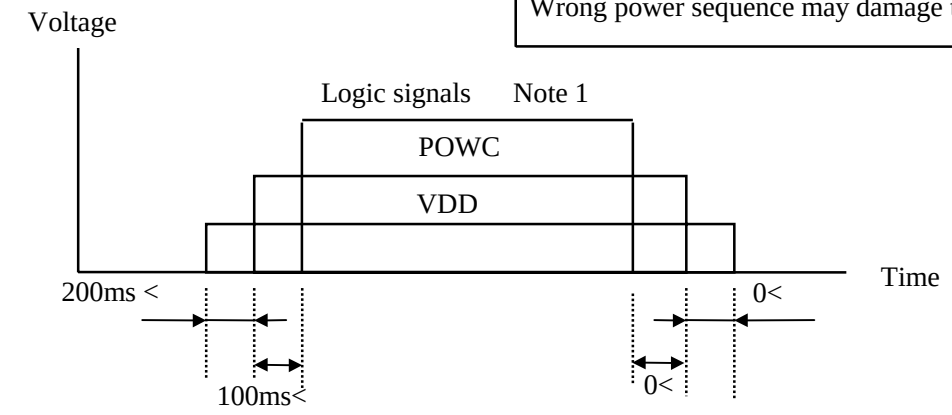
Items	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white – black)	0 (black)	0.7 (white)	Note 1	Vp-p	Need to adjust contrast if input is more than 0.7Vp-p
DC input level (black)	-3.5	—	+3.5	V	—

Note 1: Total value of video signal amplitude and sync amplitude are 1.4Vp-p max.

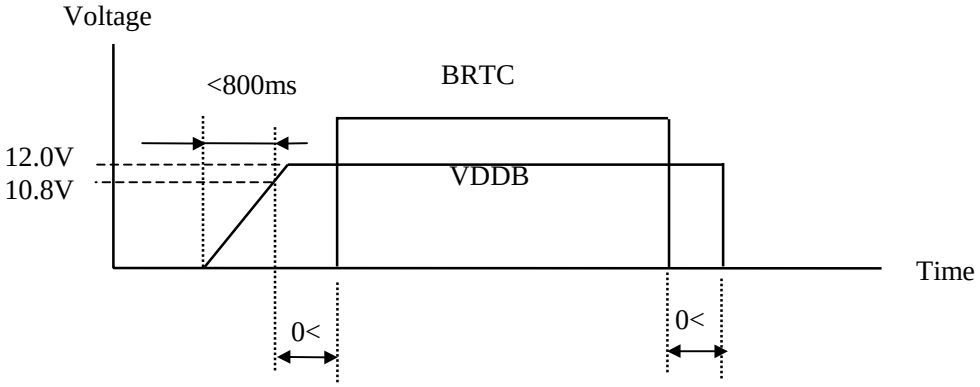
Remark: If input video signals have noise, the display may include nose. And in case that frequency is bad characteristics, the display becomes blurry indication.

7.4 POWER SUPPLY SEQUENCE

ATENTION
Wrong power sequence may damage the module.



Note 1: Synchronous signals, Control signals, CLK



(1) When VCC is not supplied, Logic signals (synchronous signals and control signals) should be "0" voltage (V). If these input voltages are higher than 0.3 V, the internal circuit will be damaged.

(2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, and Vsync is not input more than 90 ms typically.
As the display data are unstable in this period, the display maybe disordered. But the backlight works correctly even this period. So the backlight should be controlled by BRTC signal.

(3) Backlight should be turned on or off, while logic signals are supplied. The backlight power supply (VDDB) is not relative to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON /OFF without logic signals.

(4) Keep POWC signal "L" more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.

(5) Analog RGB inputs are independent from this power supply sequence.

(6) 12V for backlight should be started up within 800ms, otherwise, the protection circuit makes the backlight turn off.

(7)The backlight is turned off with safety circuit, when “L” period of BRTP signal is input more than 50 ms.

(8) Do not input “H” ACA and PWSEL, when VDD is 0V or BRTC is “L”.

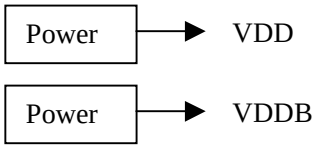
(9) Ripple of supply voltage

Supply voltage	VDD (for logic and LCD driver)	VDDB (for backligth)
Acceptable range	≦ 100 m Vp-p	≦ 200 m Vp-p

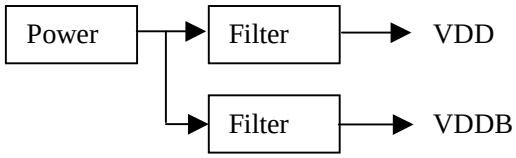
Note 1: The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

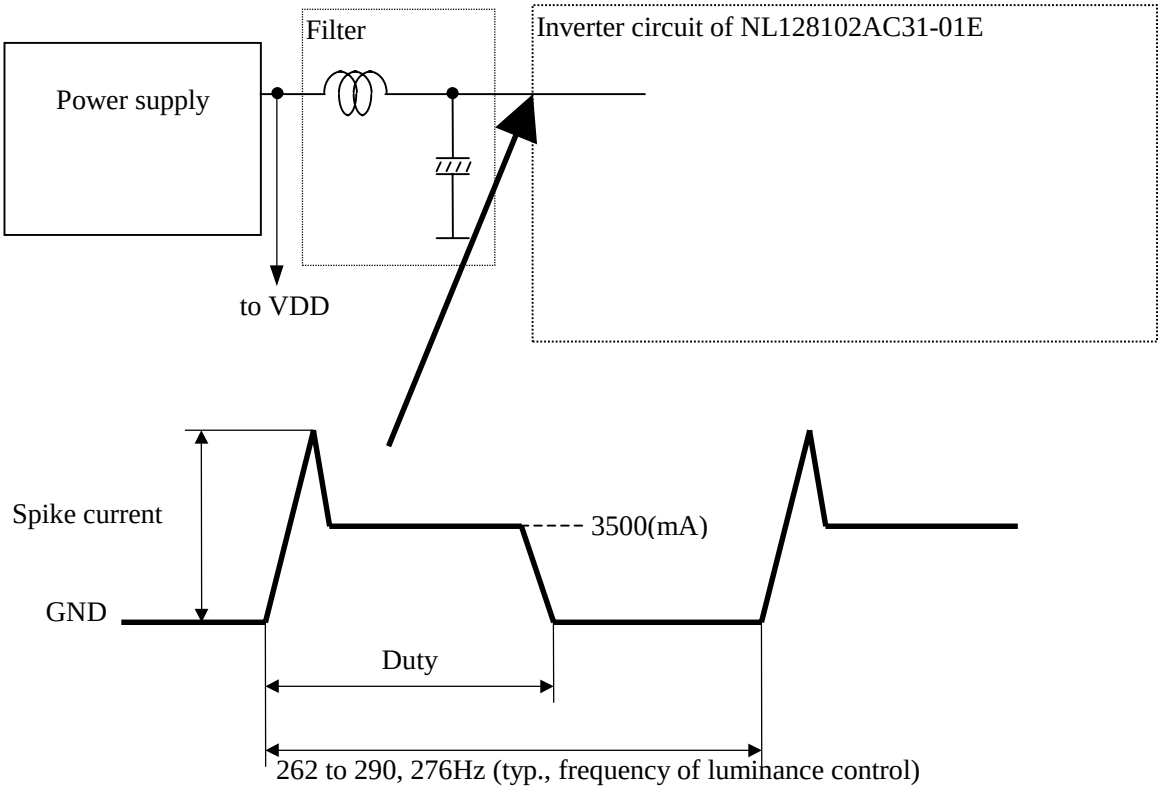
a) Separate the power supplies



b) Put the filters



(10) Inverter current wave



Maximum luminance control : 100% (Duty)
Minimum luminance control : 20% (Duty)
Luminance control frequency : 262-290Hz, 276Hz (Typ.)

Note 1: The power supply lines (VDDB and GNDB) have large ripple voltage while dimming. There is the possibility that the ripple voltage produce an acoustic noise and signal wave noise in a system circuit (e.g. audio circuit).
If the noise occurred in a system circuit, please assembles an aluminum electrolytic capacitor (5000 to 6000 μF) between the power source lines (VDDB and GNDB), and the aluminum electrolytic capacitor will be able to reduce the noise.

Note 2: Please refer to 7.6 PIN FUNCTIONS Note 2,3 “luminance control by voltage and a variable resister.”

(11) Fuse

This LCD module uses the fuses shown below.

Supply voltage	Part No.	Supplier	Ratings	Remarks
VDD	CCP2E50	KOA	2A	-
VDDB	R451007	LITTEL FUSE	7A	-

Remarks: When customer designs the power supply, above fuse specification should be considered. The power capacity should be more than 2.0 times of fuses rating. If the power capacity is smaller than 2.0 times of fuses rating, from safety point of view, enough evaluation is required for customer's application.

7.5 INTERFACE PIN CONNECTIONS

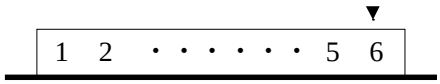
(1) CN1 socket

Part No.: MRF03-6R-SMT (coaxial type)
Adaptable plug: MRF03-6P-1.27 (For cable type) or MRF03-6PR-SMT (For board to board type)
Supplier: HIROSE ELECTRIC CO., LTD.

Coaxial cable: UL20537PF75VLAS
Supplier: Hitachi Co., Ltd.
Note: A shield of coaxial cable should be connected with GND.

Pin No.	Symbols	Pin No.	Symbols
1	B	4	Vsync
2	G	5	Hsync
3	R	6 ▼	CLK

Figure from socket view



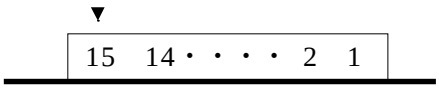
(2) CN2 socket

Part No.: IL-Z-15PL-SMTY
Adaptable plug: IL-Z-15S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	VDD	9	GND
2	VDD	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	CLAMP
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15 ▼	GND
8	CNTSTB	-	

Note 1:N.C. (No connection) must be open.

Figure from socket view



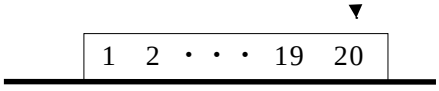
(3) CN3 socket

Part No.: DF14A-20P-1.25H
Adaptable plug: DF14-20S-1.25C
Supplier: HIROSE ELECTRIC CO., LTD.

Pin No.	Symbols	Pin No.	Symbols
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20 ▼	N.C.

Note 1:N.C. (No connection) must be open.

Figure from socket view



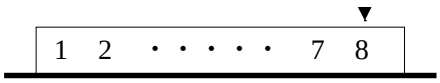
(4) CN201 socket

Part No.: DF3-8P-2H
Adaptable plug: DF3-8S-2C
Supplier: HIROSE ELECTRIC CO., LTD.

Pin No.	Symbols	Pin No.	Symbols
1	GNDB	5	VDDB
2	GNDB	6	VDDB
3	GNDB	7	VDDB
4	GNDB	8 ▼	VDDB

Note 1: N.C. (No connection) must be open.

Figure from socket view

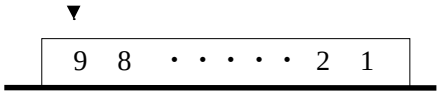


(5) CN202 socket

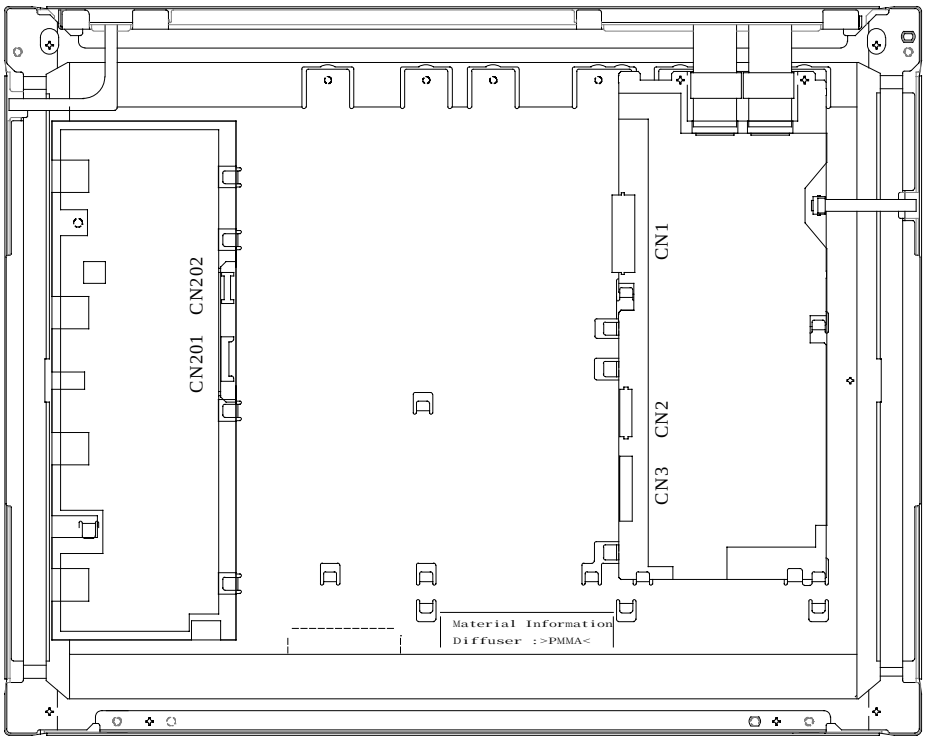
Part No.: IL-Z-9PL1-SMTY
Adaptable plug: IL-Z-9S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	GNDB	6	BRTL
2	GNDB	7	BRTP
3	N.C.	8	GNDB
4	BRTC	9 ▼	PWSEL
5	BRTH	-	

Figure from socket view



Rear view



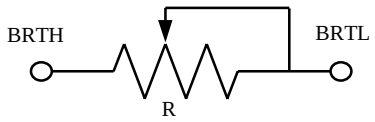
7.6 PIN FUNCTIONS

Symbols	I/O	Logic	Description
CLK	Input	Negative	Dot clock input. (ECL level) Timing signal for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	—	Red video signal input (0.7Vp-p, input impedance 75Ω)
G	Input	—	Green video signal input (0.7Vp-p, input impedance 75Ω)
B	Input	—	Blue video signal input (0.7Vp-p, input impedance 75Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "open"： Logic and LCD powers are on. "L" ： Logic and LCD powers are off. (Note 1)
CNTSEL	Input	—	Display control signal in case of serial communications.(TTL level) "H" or "Open" ：Default "L" ：External control Serial communications are set up by external control.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in **7.7 FUNCTIONS**.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTCLK is mentioned in **7.7 FUNCTIONS**.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTSTB is mentioned in **7.7 FUNCTIONS**.
CPSEL	Input	—	Clamp function select signal (TTL level) "H" or "Open"：Default "L" ：CLAMP signal is possible.(External control)
CLAMP	Input	Positive	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L".
BRTC	Input	Positive	Backlight ON/OFF control signal(TTL level) "H" or "Open" ：Backlight on "L" ：Backlight off
BRTH	Input	—	Backlight luminance control-1 Variable resistor control(Note 2) or voltage control (Note 3) These controls work in BRTP = "Open".
BRTL	Input	—	
BRTP	Input	—	Backlight luminance control-2 (TTL level) BRTP signal control (Note 4)
PWSEL	Input	—	Luminance control select signal（TTL level） "H" or "Open" ：Variable resistor control or voltage control "L" ：BRTP signal control
ADJSEL	Input	Positive	Contrast, brightness select control signal（TTL level） "H" or "Open" ：Default "L" ：External control Serial communications are set up by external control.

Symbols	I/O	Logic	Description
CNTSTB2	Input	Positive	Latch pulse2 for display control data Detail of CNTSTB2 is mentioned in **7.9 OSD FUNCTIONS**.
OSDRI	Input	—	OSD Red input （TTL level） Detail of OSDRI is mentioned in **7.9 OSD FUNCTIONS**.
OSDGI	Input	—	OSD Green input （TTL level） Detail of OSDGI is mentioned in **7.9 OSD FUNCTIONS**.
OSDBI	Input	—	OSD Blue input （TTL level） Detail of OSDBI is mentioned in **7.9 OSD FUNCTIONS**.
OSDENI	Input	Positive	OSD enable signal （TTL 0level） Detail of OSDENI is mentioned in **7.9 OSD FUNCTIONS**.
VDD	—	—	VDD (+12V±10%) power supply for logic and LCD driving.
VDDB	—	—	VDDB (+12V±10%) power supply for backlight.
GND	—	—	Ground for logic and LCD driving (VDD) GND is connected to the module GND (FG).
GNDB	—	—	Ground for backlight power supply (VDDB) GNDB is not connected to the module GND (FG).

Note 1: When POWC is "L", serial communication data is clear, please set again. When POWC is “L”, logic input signal has to be all “0V”. If more than “0.3V” is inputted, the LCD module may be broken.

Note2: Luminance control

PWM	Voltage	Variable resister
PWSEL=“L”	PWSEL= “H” or “Open” and BRTP= ”Open”	
See **7.10. OUTSIDE CONTROL FOR LUMINANCE**	BRTH should be fixed to 0V to control luminance by voltage. The range of input voltage between BRTL and GNDB is as follows. Maximum luminance (100%) : BRTL=1V Minimum luminance (30%) : BRTL=0V	The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor corresponds to the minimum of luminance.  Maximum luminance(100%) : R=10 kΩ Minimum luminance (30%) : R= 0 Ω Mating variable resistor: 10 kΩ ±5%, B curve

7.7 FUNCTIONS

This LCD module has following functions by serial data input (table 1)

（1） Expansion mode:	See table 2 and **7.8 EXPANSION FUNCTIONS**
（2） Control Display position (VERTICAL):	See table 3
（3） Control Display position (HORIZONTAL):	See table 6
（4） Control CLK delay:	See table 4
（5） Change CLK fall/rise synchronous:	See table 5
（6） Sub-Contrast control:	See table 9, 10 and **7.8.4 COLOR CONTROL FUNCTION AND GRAPH IMAGE**
（7） Sub-Brightness control:	

Set up the following items to work the above functions

(A) CLK counts of horizontal period:	See table 7
(B) CLK frequency range:	See table 8

7.7.1 HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is "L", the above functions((1)-(5))are valid. (CNTSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions((1)-(5)) are effective.

If ADJSEL is "L", the above functions((6)-(7))are valid. (ADJSEL is "H" or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB2. Once, the data is latched, the above functions((6)-(7)) are effective.

Please keep CNTSTB/2 to be "L" during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

Table 1. CNTDAT (Serial data) Composition

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19	DELAY2	CLK delay	
D20	DELAY1	CLK delay	
D21	DELAY0	CLK delay (LSB)	
D22	CKS	CLK signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	CLK counts of horizontal period (MSB)	See table 7
D33	HSE9	CLK counts of horizontal period	
D34	HSE8	CLK counts of horizontal period	
D35	HSE7	CLK counts of horizontal period	
D36	HSE6	CLK counts of horizontal period	
D37	HSE5	CLK counts of horizontal period	
D38	HSE4	CLK counts of horizontal period	
D39	HSE3	CLK counts of horizontal period	
D40	HSE2	CLK counts of horizontal period	
D41	HSE1	CLK counts of horizontal period	
D42	HSE0	CLK counts of horizontal period (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	

Table 1. CNTDAT Composition (continuation)

DATA	DATA name	Function	
AD11	DAA0	Color adjust select data (LSB)	See table 10
AD10	DAA1	Color adjust select data	
AD9	DAA2	Color adjust select data	
AD8	DAA3	Color adjust select data (MSB)	
AD7	DAD7	Color adjust data (MSB)	See table 9
AD6	DAD6	Color adjust data	
AD5	DAD5	Color adjust data	
AD4	DAD4	Color adjust data	
AD3	DAD3	Color adjust data	
AD2	DAD2	Color adjust data	
AD1	DAD1	Color adjust data	
AD0	DAD0	Color adjust data (LSB)	

Table 2. Expansion mode（VEX3 to VEX0 : 4bit）

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	SXGA	Standard Note 1
0	0	0	1	1.25	XGA	See 7.8.3 DISPLAY IMAGE
0	0	1	0	1.6	SVGA, MAC	
0	0	1	1	2.0	VGA	
0	1	0	0	2.5	VGA-TEXT	
0	1	0	1	—	Prohibit	
0	1	1	0	—	Prohibit	
0	1	1	1	—	Prohibit	
1	0	0	0	1.1	SUN	
1	0	0	1	—	Prohibit	
1	0	1	0	—	Prohibit	
1	0	1	1	—	Prohibit	
1	1	0	0	—	Prohibit	
1	1	0	1	—	Prohibit	
1	1	1	0	—	Prohibit	
1	1	1	1	—	Prohibit	

Note 1: Display mode is SXGA, when CNTSEL is "H" or open".

Table 3. Vertical display position（VD10 to VD0 : 11bit）

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] note 1
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 note 2

Note 1: The number of horizontal line between Vsync-fall and RGB data valid.
Note 2: The maximum number is based on horizontal line count of the display mode.
Note 3: Vertical position is fixed at 41H, when CNTCEL is “H” or “open”.

Table4. CLK delay（DELAY6 to DELAY0 : 7bit）

DELAY[6..0]	Delay (relative)		Unit	DELAY[6..0]	Delay (relative)		Unit	DELAY[6..0]	Delay (relative)		Unit
00H	2.10	0	ns	30H	16.74	14.64	ns	60H	31.54	29.44	ns
01H	2.42	0.32	ns	31H	17.05	14.95	ns	61H	31.87	29.77	ns
02H	2.72	0.62	ns	32H	17.34	15.24	ns	62H	32.15	30.05	ns
03H	3.03	0.93	ns	33H	17.66	15.56	ns	63H	32.45	30.35	ns
04H	3.32	1.22	ns	34H	17.94	15.84	ns	64H	32.74	30.64	ns
05H	3.65	1.55	ns	35H	18.25	16.15	ns	65H	33.05	30.95	ns
06H	3.95	1.85	ns	36H	18.53	16.43	ns	66H	33.33	31.23	ns
07H	4.30	2.20	ns	37H	18.84	16.74	ns	67H	33.65	31.55	ns
08H	4.59	2.49	ns	38H	19.15	17.05	ns	68H	33.98	31.88	ns
09H	4.89	2.79	ns	39H	19.48	17.38	ns	69H	34.29	32.19	ns
0AH	5.16	3.06	ns	3AH	19.78	17.68	ns	6AH	34.60	32.50	ns
0BH	5.47	3.37	ns	3BH	20.09	17.99	ns	6BH	34.91	32.81	ns
0CH	5.77	3.67	ns	3CH	20.41	18.31	ns	6CH	35.20	33.10	ns
0DH	6.09	3.99	ns	3DH	20.72	18.62	ns	6DH	35.50	33.40	ns
0EH	6.38	4.28	ns	3EH	21.01	18.91	ns	6EH	35.79	33.69	ns
0FH	6.70	4.60	ns	3FH	21.34	19.24	ns	6FH	36.13	34.03	ns
10H	7.02	4.92	ns	40H	21.75	19.65	ns	70H	36.41	34.31	ns
11H	7.32	5.22	ns	41H	22.07	19.97	ns	71H	36.71	34.61	ns
12H	7.61	5.51	ns	42H	22.36	20.26	ns	72H	36.99	34.89	ns
13H	7.91	5.81	ns	43H	22.65	20.55	ns	73H	37.29	35.19	ns
14H	8.22	6.12	ns	44H	22.95	20.85	ns	74H	37.60	35.50	ns
15H	8.55	6.45	ns	45H	23.27	21.17	ns	75H	37.91	35.81	ns
16H	8.83	6.73	ns	46H	23.55	21.45	ns	76H	38.21	36.11	ns
17H	9.14	7.04	ns	47H	23.99	21.89	ns	77H	38.53	36.43	ns
18H	9.47	7.37	ns	48H	24.23	22.13	ns	78H	38.87	36.77	ns
19H	9.78	7.68	ns	49H	24.54	22.44	ns	79H	39.19	37.09	ns
1AH	10.07	7.97	ns	4AH	24.83	22.73	ns	7AH	39.47	37.37	ns
1BH	10.39	8.29	ns	4BH	25.12	23.02	ns	7BH	39.78	37.68	ns
1CH	10.69	8.59	ns	4CH	25.43	23.33	ns	7CH	40.08	37.98	ns
1DH	11.01	8.91	ns	4DH	25.74	23.64	ns	7DH	40.41	38.31	ns
1EH	11.29	9.19	ns	4EH	26.04	23.94	ns	7EH	40.72	38.62	ns
1FH	11.61	9.51	ns	4FH	26.36	24.26	ns	7FH	40.97	38.87	ns
20H	11.91	9.81	ns	50H	26.66	24.56	ns				
21H	12.23	10.13	ns	51H	26.96	24.86	ns				
22H	12.52	10.42	ns	52H	27.26	25.16	ns				
23H	12.83	10.73	ns	53H	27.57	25.47	ns				
24H	13.12	11.02	ns	54H	27.86	25.76	ns				
25H	13.43	11.33	ns	55H	28.18	26.08	ns				
26H	13.71	11.61	ns	56H	28.47	26.37	ns				
27H	14.04	11.94	ns	57H	28.80	26.70	ns				
28H	14.34	12.24	ns	58H	29.10	27.00	ns				
29H	14.65	12.55	ns	59H	29.40	27.30	ns				
2AH	14.92	12.82	ns	5AH	29.69	27.59	ns				
2BH	15.22	13.12	ns	5BH	30.01	27.91	ns				
2CH	15.52	13.42	ns	5CH	30.30	28.20	ns				
2DH	15.84	13.74	ns	5DH	30.61	28.51	ns				
2EH	16.13	14.03	ns	5EH	30.90	28.80	ns				
2FH	16.44	14.34	ns	5FH	31.23	29.13	ns				

Note1: DELAY[6..0] is fixed at 00H, when CNTSEL is “H” or “open”.

note 2: This delay value is typical value at Ta=25℃. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

① Variation of CLK delay by temperature drift. (only reference) The temperature constant of CLK delay is 0.2%/℃.

Calculated example:

In case of delay time is 20ns at Ta=25℃;

(a) In case Ta rising to 50℃.

Increase of delay time → (50℃－25℃)×0.002×20ns＝+1ns

So, the total delay time is 21 ns at Ta=50℃.

(b) In case Ta falling to 0℃.

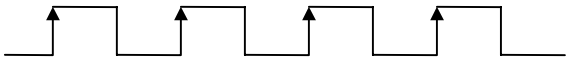
Decrease of delay time → (0℃－25℃)×0.002×20ns＝-1ns

So, the total delay time is 19 ns at Ta=0℃.

② Variation of CLK delay time against each LCD module. (only reference)

－10.5% to ＋14.4%

Table 5. CLK reverse signal

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK. 
1	DATA is sampled on falling edge of CLK. 

Note 1: CKS is "0", when CNTSEL is "H" or "open".

Table 6. Horizontal display position（HD8 to HD0 : 9bit）

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] Note 1
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
・	・	・	・	・	・	・	・	・	・
・	・	・	・	・	・	・	・	・	・
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
・	・	・	・	・	・	・	・	・	・
・	・	・	・	・	・	・	・	・	・
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Note 1: The number of CLK between Hsync-fall and RGB data valid.

Note 2: Horizontal position is set at 360 CLK, when CNTSET is "H" or "open".

Table 7. CLK counts of horizontal period（HSE10 to HSE0 : 11bit）

HSE10	**HSE9**	**HSE8**	**HSE7**	**HSE6**	**HSE5**	**HSE4**	**HSE3**	**HSE2**	**HSE1**	**HSE0**	**CLK count** Note 1
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

Note 1: The number of CLK between Hsync signals.
Note 2: CLK number is set 1688 CLK, when CNTSEL is "H" or "open".
Note 3: If setting value is different from actual input signal, it may cause to malfunction.

Table 8. CLK frequency select（MOD1 to MOD0 : 2bit）

MOD1	**MOD0**	**CLK frequency [MHz]**
0	0	90 to 135
0	1	65 to 90
1	0	50 to 65
1	1	20 to 50

Note 1: Set complying with input CLK frequency.
Note 2: CLK frequency is set 90 to 135 MHz, when CNTSEL is "H" or "open".

Table 9. Color control data（DAD7 to DAD0 : 8bit）

DAD7	**DAD6**	**DAD5**	**DAD4**	**DAD3**	**DAD2**	**DAD1**	**DAD0**	**Adjusting value**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

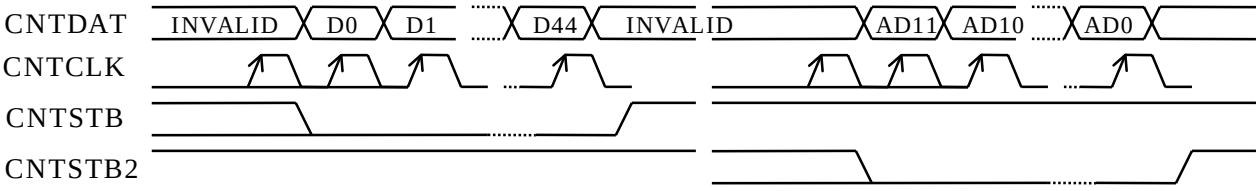
Note 1: Adjust value for selecting function above table.10.
Note 2: Different D/A-range depends on function selected.
Note 3: See more detail 7.8.4. COLOR CONTROL FUNCTIONS AND GRAPH IMAGES.

Table 10. Color adjust select data（DAA3 to DAA0 : 4bit）

DAA3	DAA2	DAA1	DAD0	Function
0	0	0	0	Prohibit
0	0	0	1	Prohibit
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	0	1	1	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

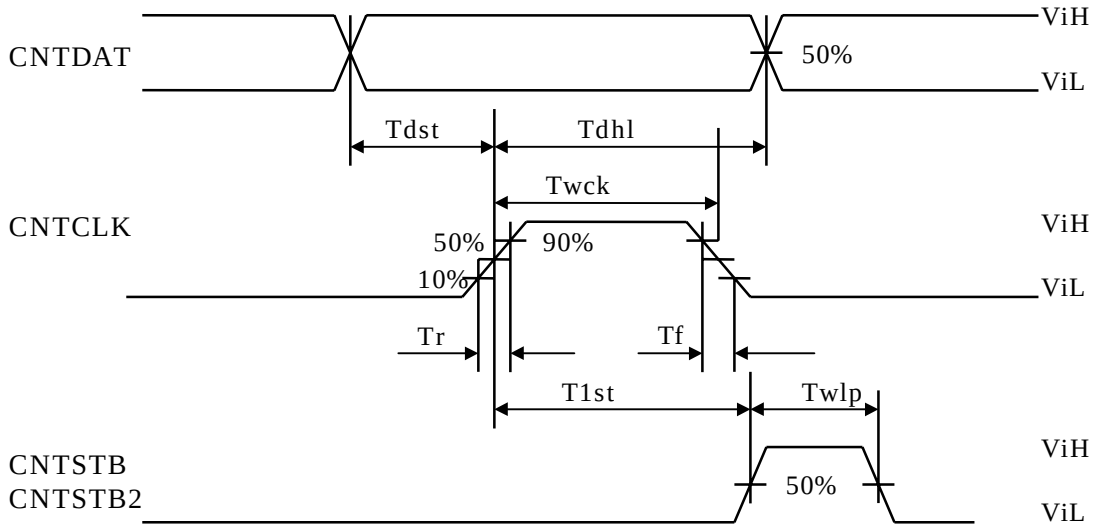
Note 1: See more detail 7.8.4. COLOR CONTROL FUNCTIONS AND GRAPH IMAGES.

7.7.2 SERIAL COMMUNICATION TIMINGS



Parameters	Symbols	Min.	Max.	Unit	Remarks
CLK pulse-width	Twck	50	—	ns	CNTCLK
CLK frequency	Fclk	—	5	MHz	
DATA set-up-time	Tdst	50	—	ns	CNTDAT
DATA hold-time	Tdhl	50	—	ns	
Latch pulse-width	Twlp	50	—	ns	CNTSTB, CNTSTB2
Latch set-up-time	T1st	50	—	ns	
Rise / fall time	Tr , Tf	—	50	ns	CNT xxx

SERIAL COMMUNICATION WAVEFORM



7.8 EXPANSION FUNCTIONS

7.8.1 HOW TO USE EXPANSION MODES

Expansion mode is a function of expanding an image. For example, VGA signal has 640×480 pixels. But, if the display data expand to 2.0 times vertically and horizontally, VGA screen image will be displayed fully on the screen of SXGA resolution.

This LCD module has the function that expands display images vertically and horizontally as shown in below table.
When each mode of input signals, which are shown at item 15. (page 34), is supplied to LCD module, display image is expanded automatically.

Please adopt expansion function after evaluating image quality, because the expanded image is relatively bad depending on displayed images.

The followings show magnification rate of each mode.

Display Mode	**Number of display data (pixels)**	**Magnification**	
		Vertical	**Horizontal** note 1
SXGA	1280 x 1024	1	1
XGA	1024 x 768	1.25	1.25
SVGA	800 x 600	1.6	1.6
VGA	640 x 480	2.0	2.0
VGA text	720 x 400	2.5	1.7
MAC	832 x 624	1.6	1.5
SUN	1152 x 900	1.1	1.1

note 1: The horizontal magnification multiples the input clock(CLK).
Input CLK = system CLK × horizontal magnification
Example: In case of SXGA and VGA, CLK frequency can be decided as follows.
SXGA: System CLK(108.0MHz)×1.0=108.0MHz
VGA : System CLK(25.175MHz)×2.0= 50.25MHz

7.8.2 SETTING SERIAL DATA FOR EXPANSION

Input signal								Module serial-data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count Number [CLK]	DSP [CLK]	Count Number [H]	DSP [H]	Calculation formula		
				(A)	(B)	—	(C)	(A)x Ver. magni	(B)x Hor. magni	=(C)
SXGA (1280 x1024)	108.0	63.981	60.02	1688	360	1066	41	(A) x 1	(B) x 1	=(C)
	117.0	71.691	67.189	1632	336	1067	41			
	125.0	75.120	71.204	1664	352	1055	28			
	130.076	76.968	72.000	1690	378	1069	42			
	135.0	78.125	72.005	1728	384	1085	58			
	135.0	79.976	75.025	1688	392	1066	41			
XGA (1024 x 768)	65*	48.363	60.004	1344	296	806	35	(A) x 1.25	(B) x 1.25	
	75*	56.476	70.069	1328	280	806	35			
	78.75*	60.023	75.029	1312	272	800	31			
MAC (832x624)	57.283*	49.725	74.5	1152	288	667	42	(A)x1.5	(B)x1.5	
SVGA (800 x 600)	36*	35.156	56.25	1024	200	625	24	(A) x 1.6	(B) x 1.6	
	40*	37.879	60.317	1056	216	628	27			
	50*	48.077	72.188	1040	184	666	29			
	49.5*	46.875	75	1056	240	666	24			
VGA (640 x 480)	25.175*	31.469	59.94	800	144	525	35	(A) x 2.0	(B) x 2.0	
	31.5*	37.861	72.809	832	168	520	31			
	31.5*	37.5	75	840	184	500	19			
	30.24*	35.0	66.667	864	160	525	42			
VGA text (720 x 400)	28.322*	31.469	70.087	900	153	449	37	(A) x 1.7	(B) x 1.7	
SUN (1152 x 900)	94.500*	61.845	66.003	1528	336	937	35	(A) x 1.1	(B) x 1.1	

*: Standard timings (Please set them up properly for correct expansion.

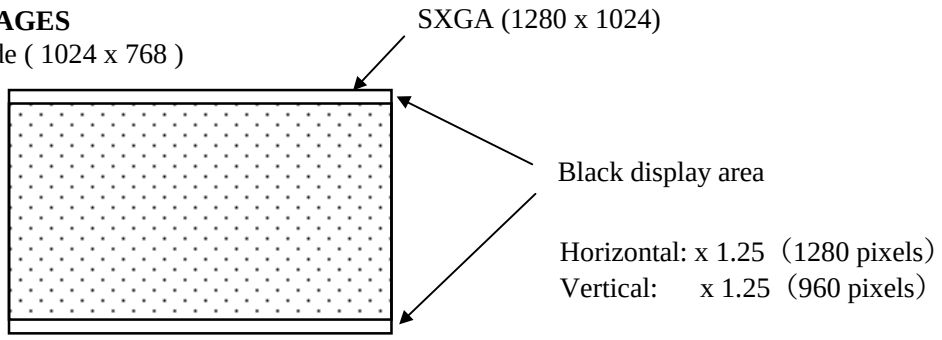
Note 1: DSP = Display Start Period. DSP is total of "pulse-width" and "back-porch".

Note 2: HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

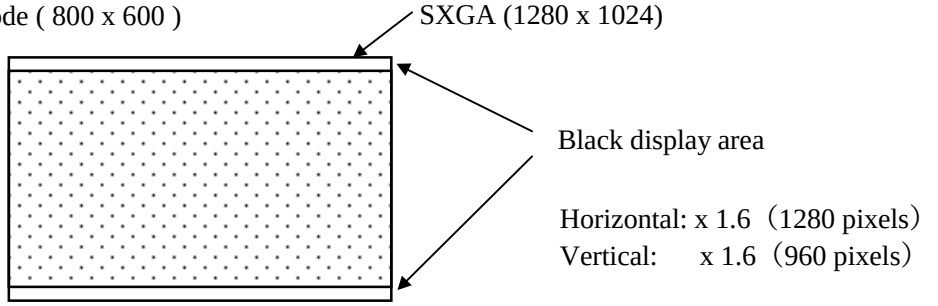
Note 3: The pulse-width of Hsync, Vsync and Back-porch are the same as SXGA-mode (Standard-mode).

7.8.3 DISPLAY IMAGES

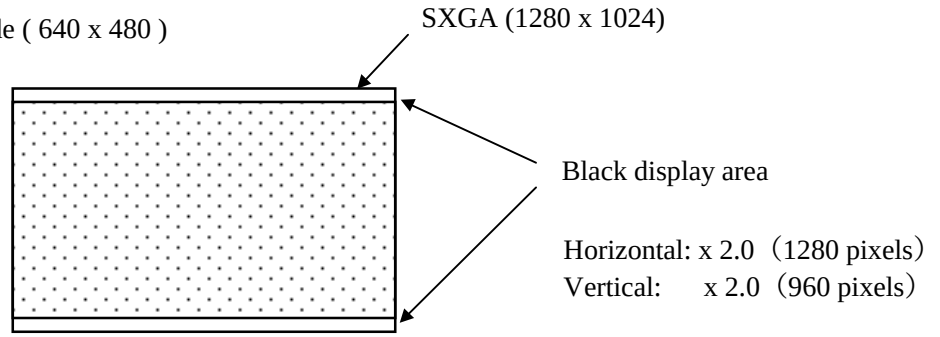
1) XGA mode (1024 x 768)



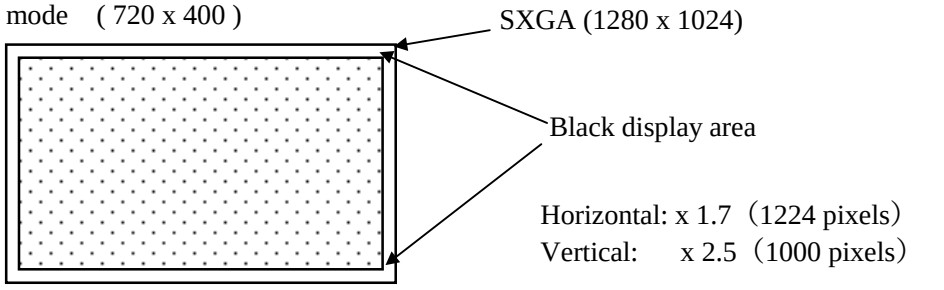
2) SVGA mode (800 x 600)



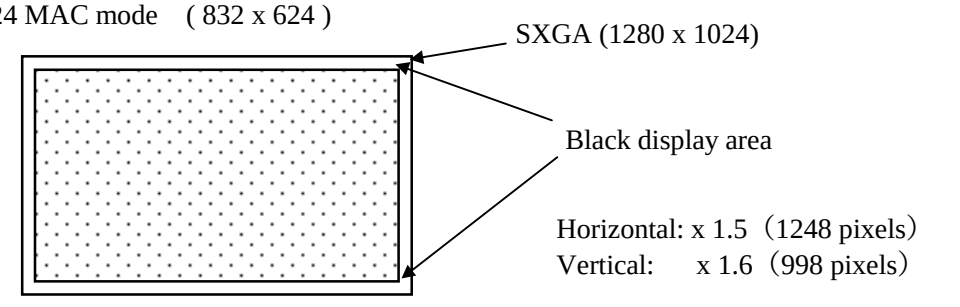
3) VGA mode (640 x 480)



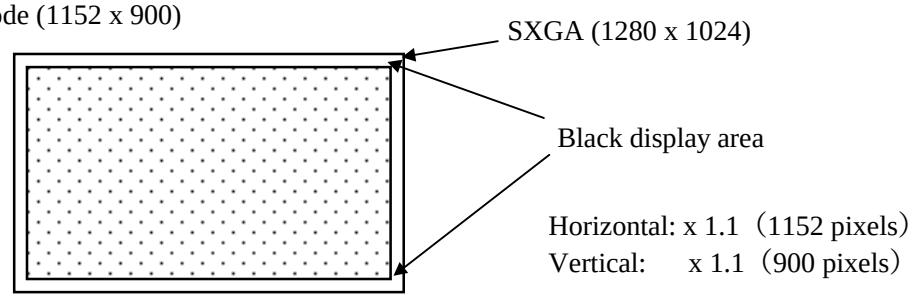
4) VGA text mode (720 x 400)



5) 832 x 624 MAC mode (832 x 624)



6) SUN mode (1152 x 900)



7.8.4 COLOR CONTROL FUNCTIONS AND GRAPHIC IMAGE

This LCD module can adjust the following functions by serial data input (table.1)

（1）Sub-contrast each R,G,B:
（2）Sub-brightness each R,G,B:

} See table 9, 10 and **7.8.4 COLOR CONTROL FUNCTION AND GRAPH IMAGE**

(1) Sub-contrast R,G,B

Sub-contrast can adjust each R/G/B with controlling the amplitude of input video signal.

Default value: 128, Valid range: 78 to 198
Contrast minimum: 78
Contrast maximum: 198
ADJSEL="H" or "Open" : Default value=128

(2) Sub-brightness R,G,B

Sub-brightness can adjust each R/G/B with adjusting the black level of input video signal.

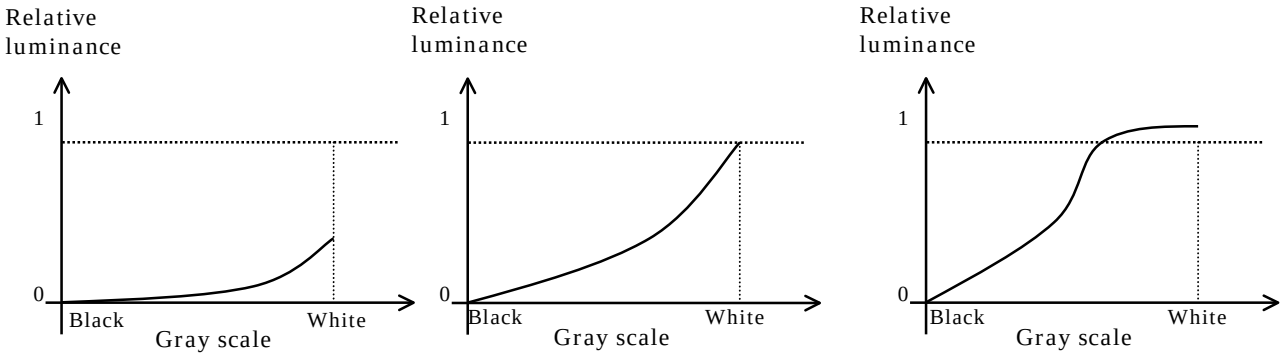
Default value: 128, Valid range: 55 to 163
Brightness minimum: 163
Brightness maximum: 55
ADJSEL="H" or "Open" : Default value=128

Note1: If the values are go over above valid range, LCD module will not be destroy. However LCD will be inferiority. Please keep values within the valid range.

Note2: Although set up the same values are set up for each LCDs, each LCD color might be slightly ill be different. And also, will be afraid to deviate values from optical characteristics. Please adopt this functions evaluating display quality.

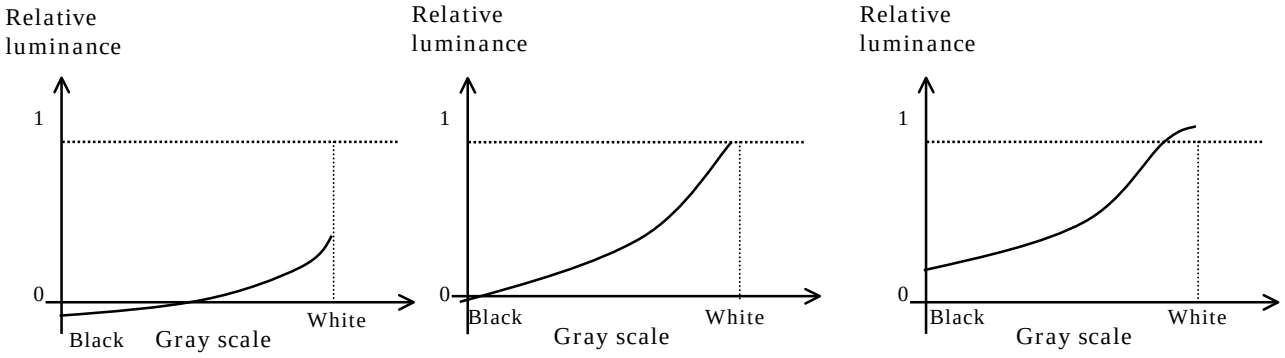
《GRAPH IMAGE》

・Sub contrast



Sub contrast
Min value ◄——— DEFAULT ———► Max value

・Sub brightness



Sub brightness
Min value ◄——— DEFAULT ———► Max value

Note 1: In case that the value of the relative luminance is over 1, the display becomes un-uniformity like Ghost.

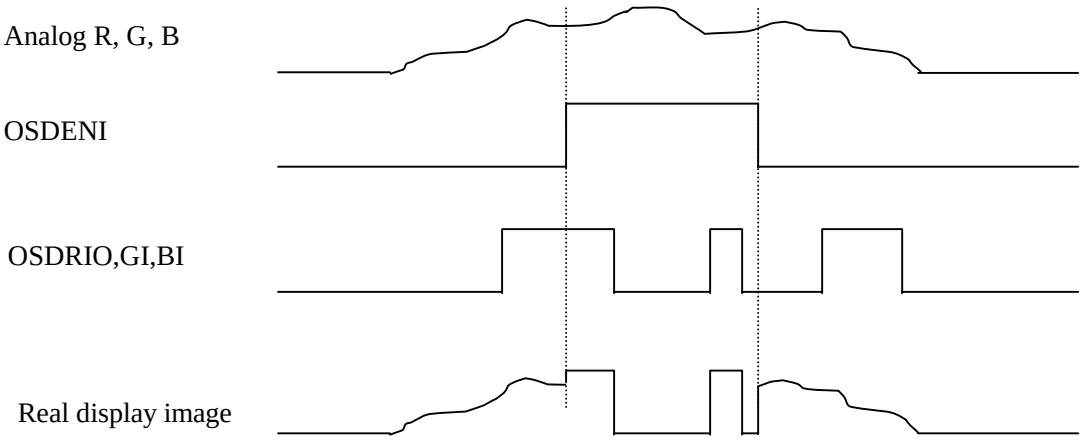
7.9 OSD FUNCTIONS

OSD (On Screen Display) is the function to display the other digital data on the input analog valid data. Possible to display 1 bit data for each R/G/B color (8 colors). OSD function is valid for the period of OSDENI

OSDRI, OSDGI, and OSDBI: digital data for OSD
OSDENI="H": OSD signal is valid
OSDENI="L": OSD signal is not valid

OSD is the sub-display for function-control and the display quality will not be guaranteed. Please adopt the OSD image evaluating display quality.

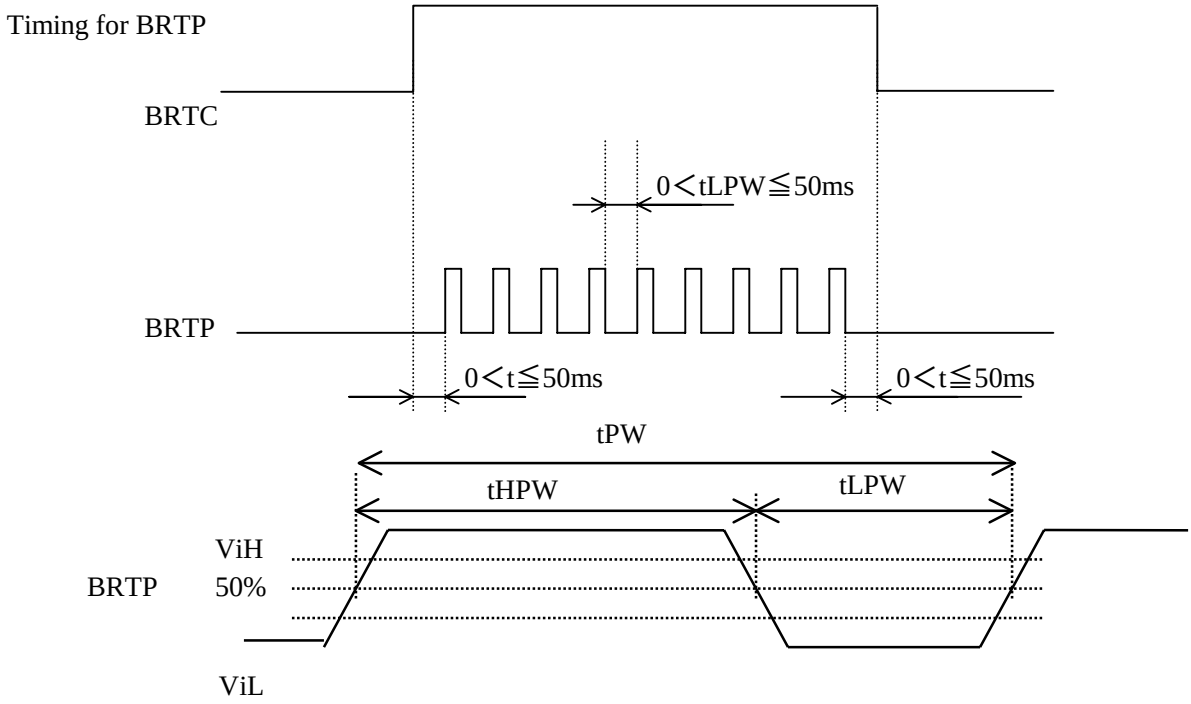
《OSD image》



7.10 OUTSIDE CONTROL FOR LUMINANCE

When PWSEL=”L”, outside control is valid. Luminance is controlled by the duty ratio of input signal of BRTP.
Duty=100%: maximum luminance
Duty=20%: minimum luminance

BRTC must not be fixed on "L", in case of PWSEL= "L" and BRTC ="H" or "Open". Otherwise, the inverter will stop to work. Once inverter stops, even if BRTP pulse comes, the backlight will not turn on again.
In this situation, please supply powers (VDDB) to the inverter again.



Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
Frequency	1/tPW	185	—	325	Hz	Note 1
“L” period	tLPW	—	—	50	ms	Note 2
Duty ratio	tHPW/tPW	20	—	100	%	Duty=100%: Luminance is maximum. Duty=20%: Luminance is minimum.
Luminance ratio	—	—	30-100	—	%	—
Input voltage	ViL	0	-	0.8	V	—
	ViH	2.0	—	5.25	V	—

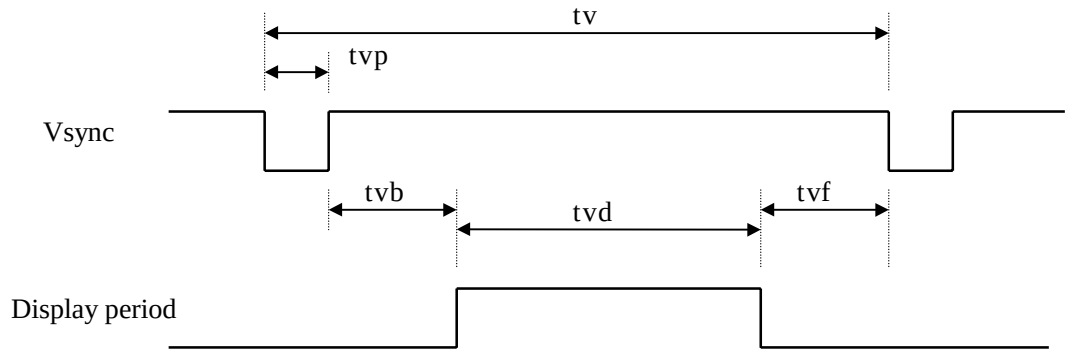
Note1: Regarding set up of frequency, refer to the below formula.
Set up frequency = Vsync frequency × (n+0.25) or (n+0.75)
Adopt the appropriate frequency after evaluating the display image quality, because the display image will be disturbed depending on frequency.
Note2: When “L” period of BRTP is longer than 50 ms, The backlight will turn off by safety circuit.

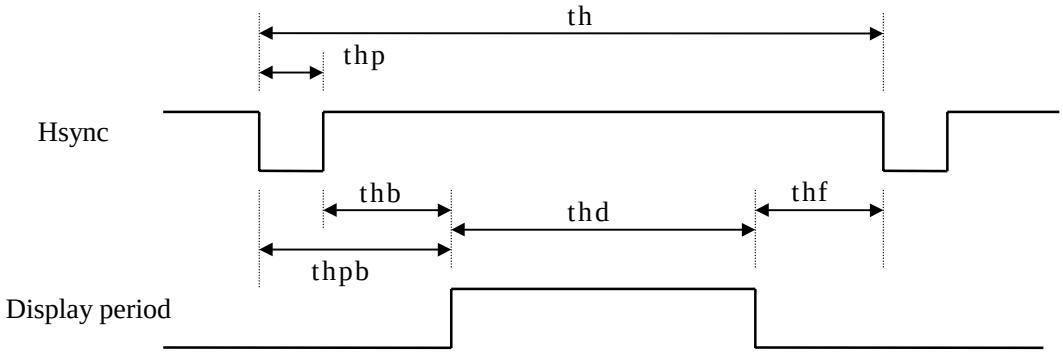
7.11 INPUT SIGNAL TIMINGS

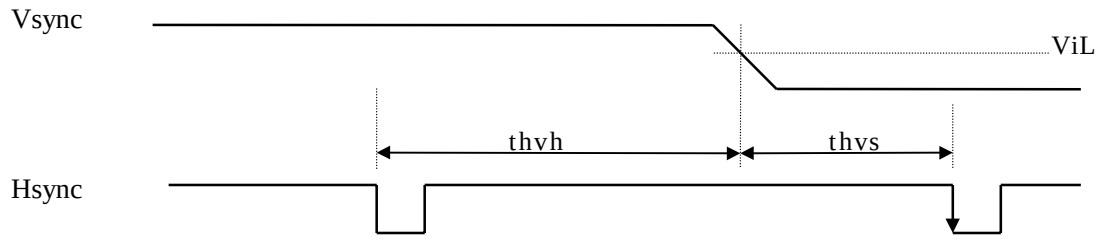
7.11.1 SXGA MODE (STANDARD)

Name		Symbols	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/tc	95.0 —	108.0 9.3	135.0 —	Mhz ns	SXGA standard
	Rise / Fall	tcrf	—	—	10	ns	—
	Pulse-width	tc / tcl	0.4	0.5	0.6	—	—
Hsync	Period	th	12.3 —	15.630 1688	17.0 —	µs CLK	63.981kHz (typ.)
	Display	thd	— —	11.852 1280	— —	µs CLK	—
	Front-porch	thf	— 10	0.444 48	— —	µs CLK	—
	Pulse-width	thp	— 16	1.037 112	— —	µs CLK	—
	Back-porch	thb	1.0 94	2.296 248	— —	µs CLK	Note 1
	Pulse-width +Back-porch	thbp	1.8	—	—	µs	—
	V-Hsync timing hold/setup time	thvh	3	—	—	ns	—
		thvs	1	—	—	CLK	—
	Rise / Fall	thrf	—	—	10	ns	—
Vsync	Period	tv	13.3 —	16.661 1066	18.5 —	ms H	60.020Hz (typ.)
	Display	tvd	— —	16.005 1024	— —	ms H	—
	Front-porch	tvf	— 1	0.016 1	— —	ms H	—
	Pulse-width	tvp	— 2	0.047 3	— —	ms H	—
	Back-porch	tvb	— 5	0.594 38	— —	ms H	—

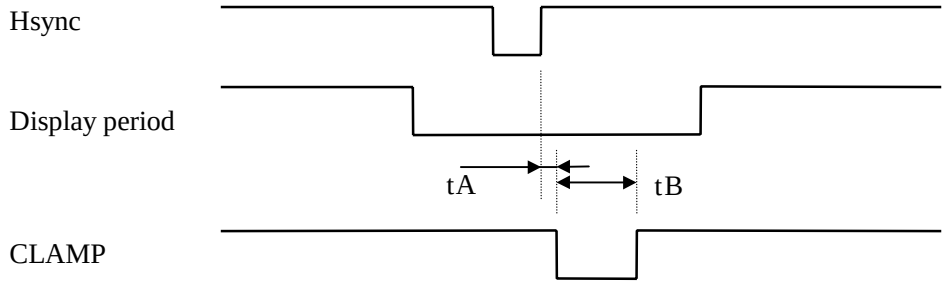
Note 1: Minimum value of Back-porch (thb) must be satisfied with both 1.0 µs and 94 CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
ViL
thvh
thvs
Hsync

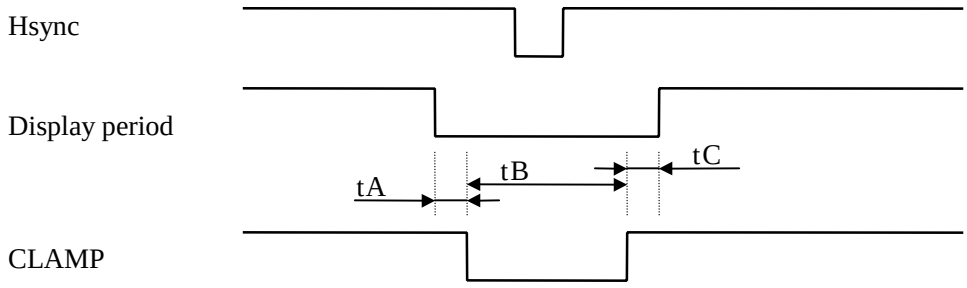
7.11.2 TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD2	tA [CLK]	tB[CLK]
0	0	2	41
0	1		27
1	0		20
1	1		15

note 1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

7.11.3 TIMING FOR INPUTTING CLAMP SIGNAL FROM OUTSIDE

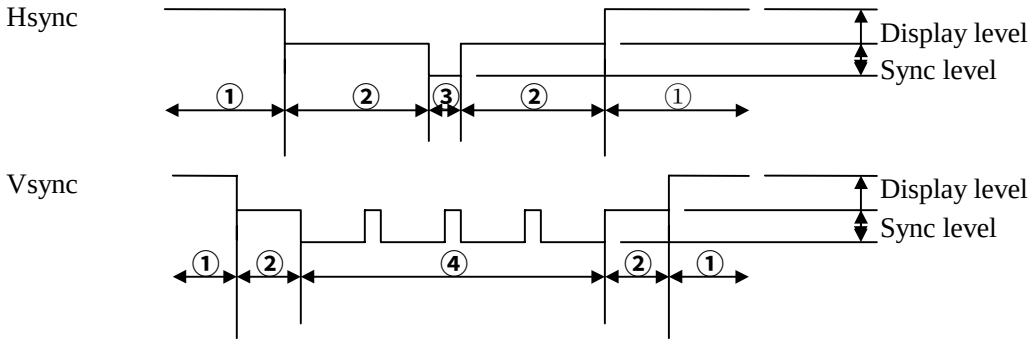


Items	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	—	—	μs	—
tB	0.3	—	—	μs	—
tC	0.2	—	—	μs	—

note 1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

note 2 : Attention for using Sync On Green signal
Clamp signals must be input during black level period as next page. If Clamp signals are input during other period, the display becomes un-uniformity.

Sync on Green Input signal timings



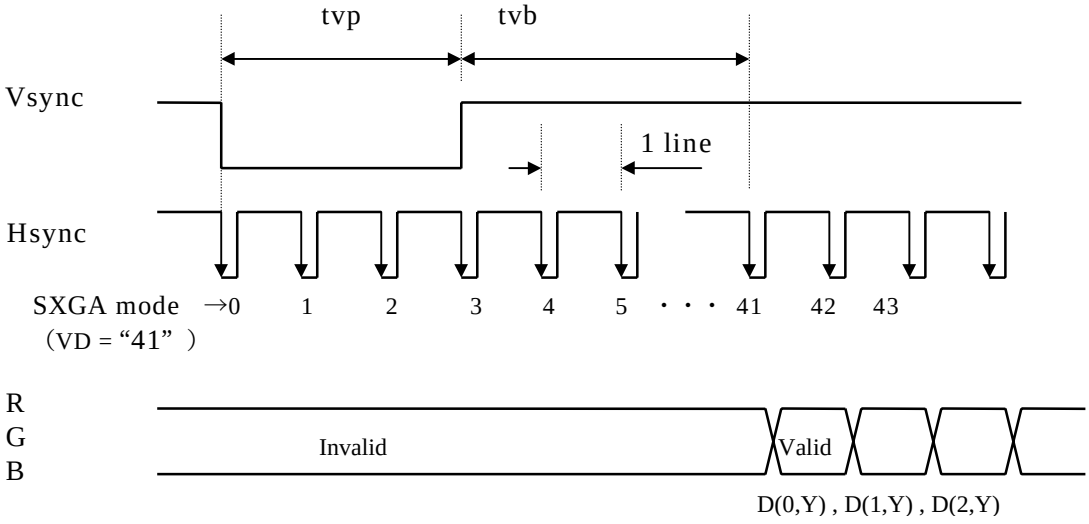
①:Display period ②:Black level period ③:Hsync period ④:Vsync period

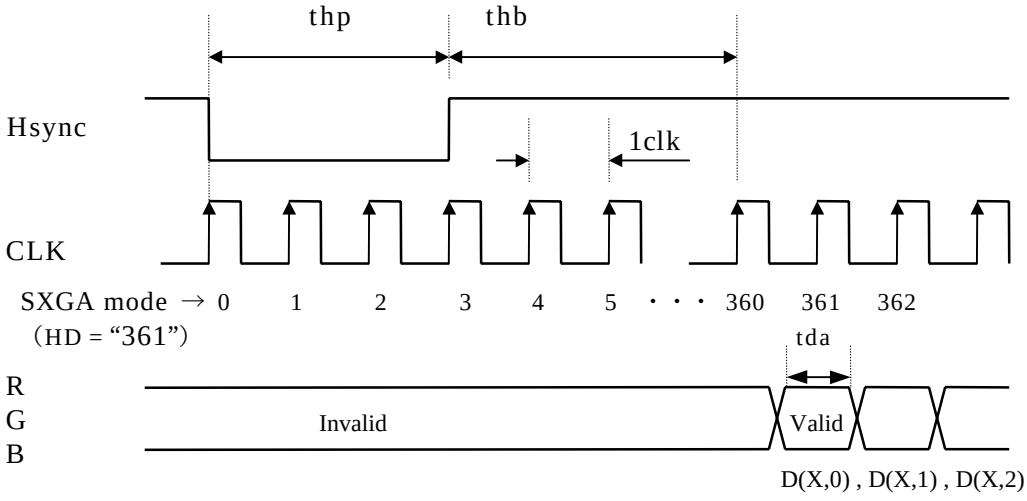
7.12 INPUT SIGNAL AND DISPLAY POSITIONS

7.12.1 SXGA STANDARD TIMINGS

Pixels

D(0,0)	D(1,0)	D(2,0)	・・・ ・・・	D(1279,0)
D(0,1)	D(1,1)	D(2,1)	・・・ ・・・	D(1279,1)
D(0,2)	D(1,2)	D(2,2)	・・・ ・・・	D(1279,2)
・ ・ ・ ・	・ ・ ・ ・	・ ・ ・ ・	・・・	・ ・ ・ ・
D(0,1023)	D(1,1023)	D(2,1023)	・・・ ・・・	D(1279,1023)





Note 1: The tda should be more than 4ns

7.13 OPTICAL CHARACTERISTICS

(Ta = 25℃, VDD = 12V, VDDB = 12V)

Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	γ=2.2 viewing angle θx±=0°, θy±=0° White／Black, at center	150	250	-	-	note 1
Luminance	Lvmax	White, at center	200	250	-	cd/m^2	note 2
Luminance uniformity	—	White	-	-	1.30	-	note 3

Reference data

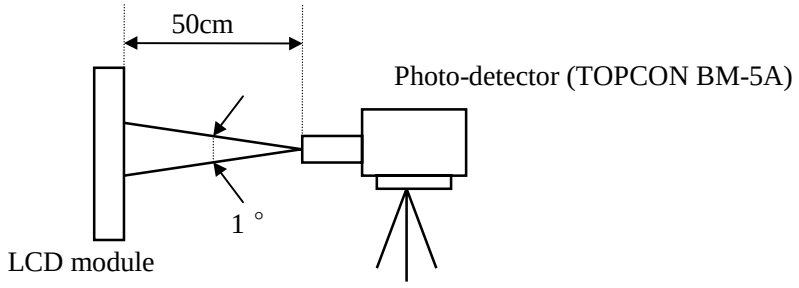
(Ta = 25℃, VDD = 12V, VDDB = 12V)

Items	Symbols	Condition		Min.	Typ.	Max.	Unit	Remarks
Chromaticity Coordinates	C	θx±=0°, θy±=0° at center, to NTSC		50	60	-	%	-
	W	White (x, y)		-	0.300, 0.315	-	-	-
	R	Red (x, y)		-	0.617, 0.339	-	-	-
	G	Green (x, y)		-	0.314, 0.580	-	-	-
	B	Blue (x, y)		-	0.143, 0.095	-	-	-
Viewing angle range (CR>10)	θ x+	CR > 10, θy±=0°		70	85	-	deg.	note 4
	θ x-			70	85	-	deg.	
	θ y+	CR > 10, θx±=0°		70	85	-	deg.	
	θ y-			70	85	-	deg.	
Viewing angle range (CR>5)	θ x+	CR > 5, θy±=0°		-	85	-	deg.	
	θ x-			-	85	-	deg.	
	θ y+	CR > 5, θx±=0°		-	85	-	deg.	
	θ y-			-	85	-	deg.	
Response time (Module surface temperature=32℃)	Ton	Black to white	0%→90%	-	35	85	ms	note 5
			10%→90%	-	30	-		
	Toff	White to black	100%→10%	-	25	55		
			90%→10%	-	23	-		
Luminance control range	—	Maximum luminance(100%)		-	30 to 100	—	%	-

note 1: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

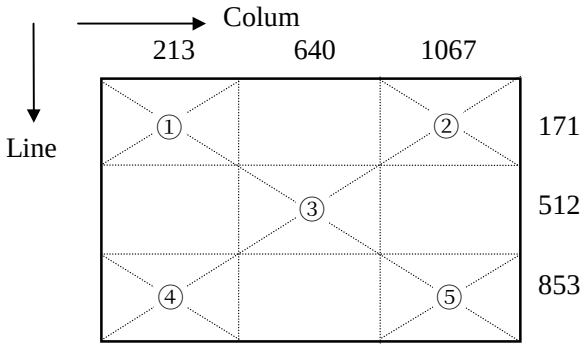
note 2: The luminance is measured after 20 minutes from lighting the backlight, with all pixels in "white". The typical value is measured after luminance saturation.



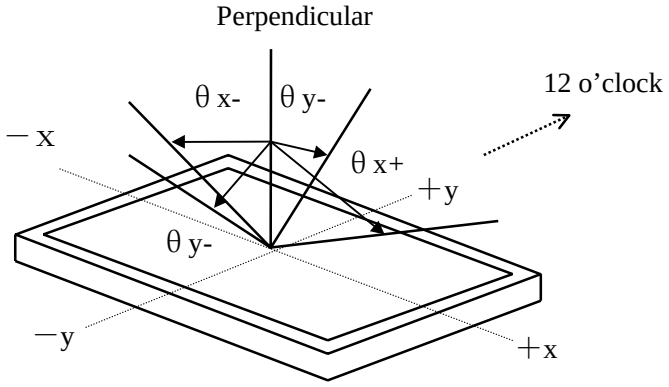
note 3: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

The luminance is measured at near the five points shown below.

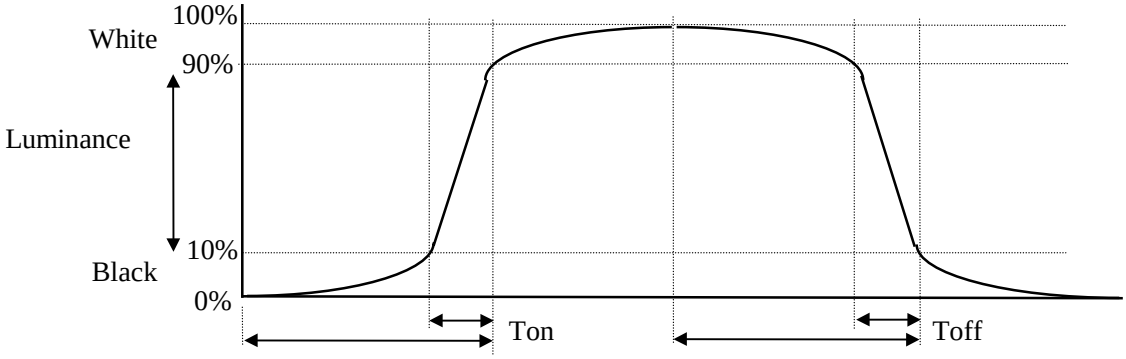


note 4: Definitions of viewing angle are as follows.



note 5: Definitions of response time are as follows.

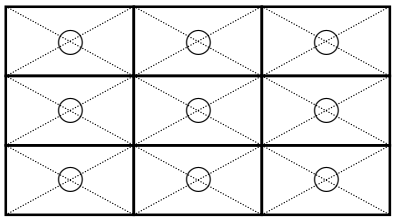
Response time is measured by Photo-detector's output level when the luminance changes "black" to "white" or "white" to "black". Definition of response times are the period between 0% and 90% (that is Ton), and one between 100% and 10% (that is Toff), of the output level.



7.14 RELIABILITY TEST

Test items	Test condition	Judgment
High temperature/humidity operation	60±2℃, RH=60% 240 hours, Display data is black.	*1
Heat cycle (operation)	① 0℃±3℃・・・1 hour 55℃±3℃・・・1 hour ② 50 cycles , 4 hours/cycle ③ Display data is black.	*1
Thermal shock (non-operation)	① -20℃±3℃・・・30 minutes 60℃±3℃・・・30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	*1
Vibration (non-operation)	① 5-100Hz, 11.76m/s^2 1 minute/cycle, X,Y,Z direction ② 10 times each direction	*1, *2
Mechanical shock (non-operation)	① 294m/s^2, 11ms X,Y,Z direction ② 3 times each direction	*1, *2
ESD (operation)	150pF, 150Ω, ±10kV 9 places on a panel *3 10 times each place at one-second intervals	*1
Dust (operation)	15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	*1

*1: No display malfunctions (display functions are checked under the same condition as out-going inspection.)
*2: No physical damages
*3: Discharge points are shown in the figure.



8. PRECAUTIONS

Because next figures and sentences are very important, please understand these contents as follows.

⚠CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

 **CAUTIONS**

Do not touch an inverter --on which a caution label is stucked-- while the LCD module is working, because of dangerous high voltage.

(1) Caution when taking out the module

① Pick the pouch only, when in taking out the module from the carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

②

 As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one or more of these signals is lost, the LCD panel would be damaged.

⑧ Do not put front side (display surface side) of the module on a desk or a table for a long time, because the display may become un-uniformity.

⑨ Don't push or rub the surface of LCD module. If you do the scratches or the rubbing marks may left on the surface of the module.

⑩ The torque for mounting screw should never exceed 0.451 N・m (4.6kgf・cm)

⑪ Do not give the stress too much on interface connectors.
The module may become function deficiency by a contact defective and damages.
Pay attention to handling at the time of matching connector connection and in the connection condition.

(3) Cautions for the atmosphere

①Dew drop atmosphere must be avoided.

②Do not store and/or operate the LCD module in high temperature and/or high humidity atmosphere. Storage in an Electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

③This module uses cold cathode fluorescent lamps. Therefore, the life-time of lamps becomes short conspicuously at low temperature.

④Do not operate the LCD module in high magnetic field.

(4) Cautions for the module characteristics

① Do not apply any fixed patterns data signal for a long time to the LCD module. It may cause image sticking. Use screen savers if the display pattern is fixed more than 30 minutes.

② The noise from the inverter circuit may be observed in the luminance control mode. This is neither defects nor malfunctions.

(5) Other cautions

① Do not disassemble and/or reassemble LCD module.

② Do not readjust variable resistors nor switches etc.

③ When returning the module for repair or etc., pack the module not to be broken. We recommend the original shipping packages.

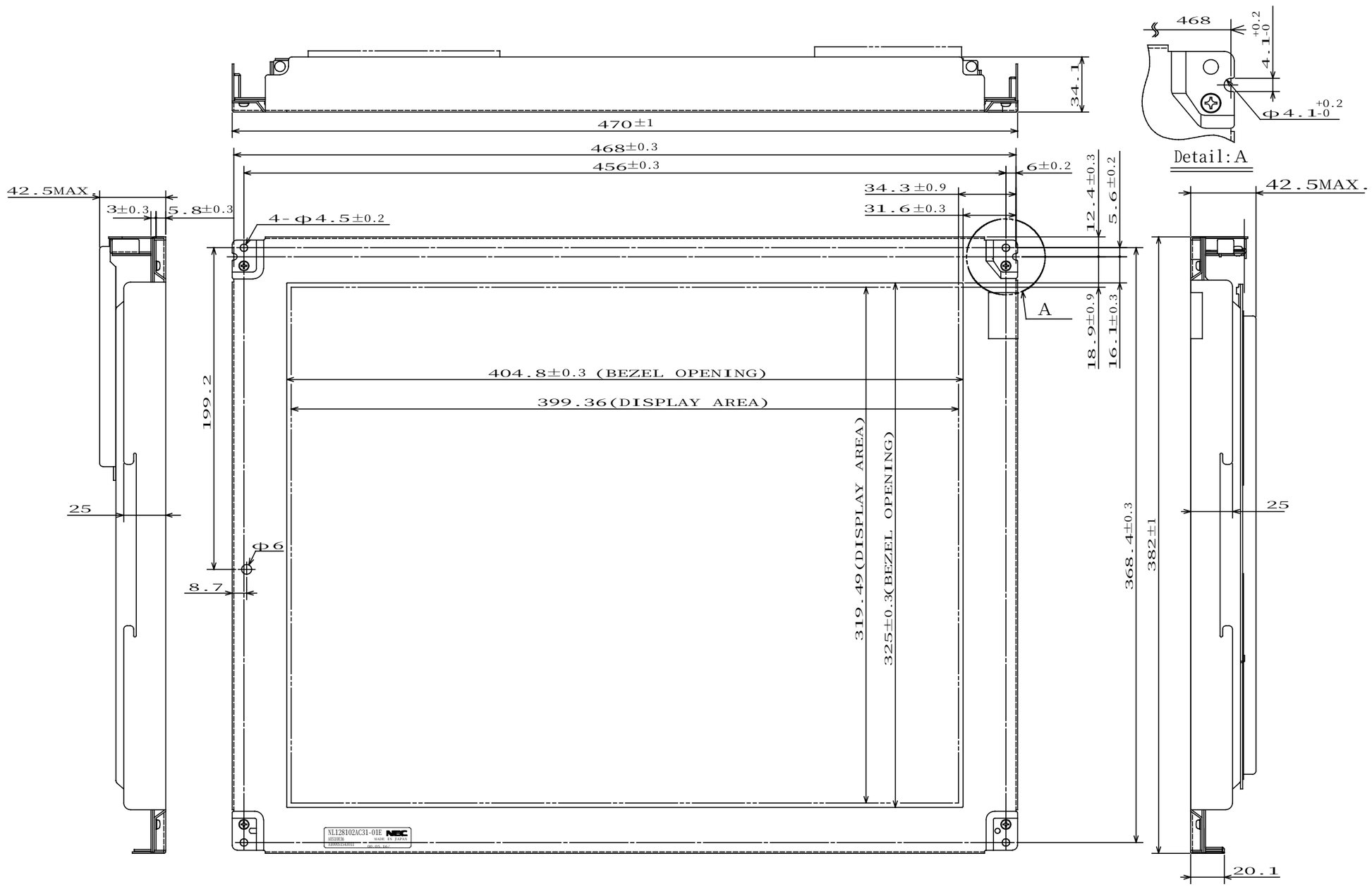
Liquid Crystal Display has the following specific characteristics. There are not defects nor malfunctions.

The ambient temperature may affect the display condition of LCD module.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

9.OUTLINE DRAWINGS

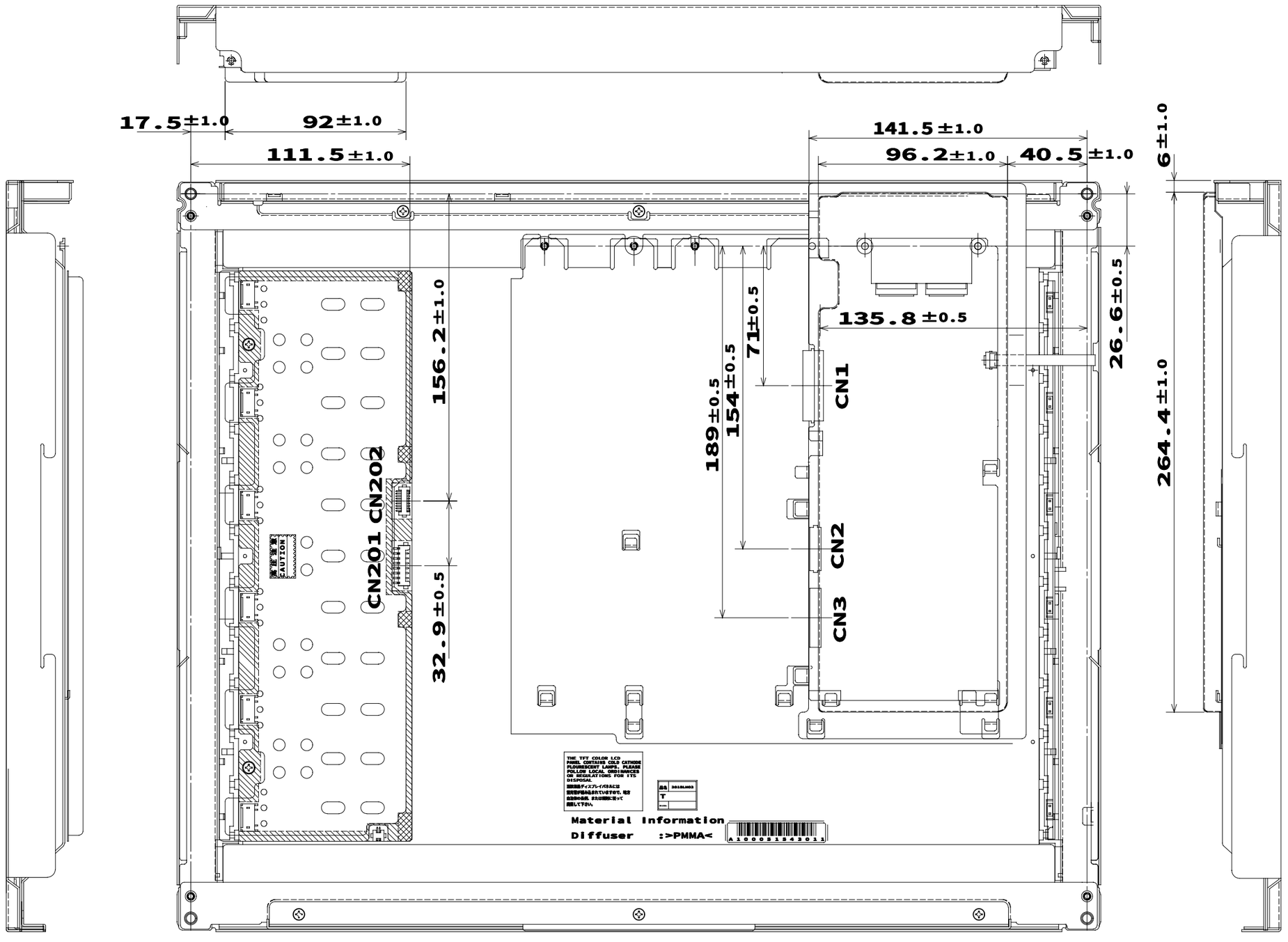
9.1 FRONT VIEW



※The torque for mounting screws should never exceed 0.42 N・m (4.3kgf・cm).

※Not shown tolerance of the dimensions are ±0.5mm.

9.2 REAR VIEW


17.5±1.0
92±1.0
111.5±1.0
141.5±1.0
96.2±1.0
40.5±1.0
6±1.0
156.2±1.0
135.8±0.5
26.6±0.5
71±0.5
189±0.5
154±0.5
CN1
CN2
CN3
CN201
CN202
32.9±0.5
264.4±1.0
CAUTION
THE TFT COLOR LCD PANEL CONTAINS COLD CATHODE FLUORESCENT LAMPS. PLEASE FOLLOW LOCAL ORDINANCES OR REGULATIONS FOR ITS DISPOSAL.
Material Information
Diffuser :>PMMA<

Revision History

Rev.	Prepared date	Revision contents and approval	Signature of writer
1st edition	Mar. 13, 2001	DOD – M – 0208 • Change part (Before - PRELIMINARY SPECIFICATIONS [DOD-H-7890] → After – DATA SHEET 1st edition) ***Note: The inside of this data sheet (1st edition) is revised the clerical error and undecided matter (TBD, etc) of PRELIMINARY SPECIFICATIONS (DOD – H - 7890). Only a changed part such as functions, characteristics value and etc that may affect a design of a customer are described especially below.*** (1) *page* 5 *lines* 9, 25 Weight 2600g(typ.) Power consumption 55.2W(typ.) → *page* 5 *lines* 9, 25 Weight 2380g(typ.) Power consumption 52.1W(typ.) (2) *page* 7 *line* 11 Weight 2600 (typ.) 2700(max.) → *page* 7 *line* 11 Weight 2380 (typ.) 2490(max.) (3) *page* 8 *line* 24 IDD – 1100 note1 1900 mA → *page* 8 *line* 24 IDD – 839 note1 1100 mA	*Approved by* *Checked by* *Prepared by* R. Kano