

WIDE BAND VIDEO SWITCH WITH I²C BUS

■ GENERAL DESCRIPTION

The NJW1321 is a Wide Band Video Switch with I²C BUS.

The NJW1321 includes switch of 4-input 2-output and 6dB amplifier. It is suitable for RGB or Y, Pb, and Pr signal because frequency range is 100MHz.

The NJW1321 includes external logic control terminals and external logic discernment terminals.

The NJW1321 is suitable for PTV, DTV, PDP and other high quality AV systems.

■ PACKAGE OUTLINE

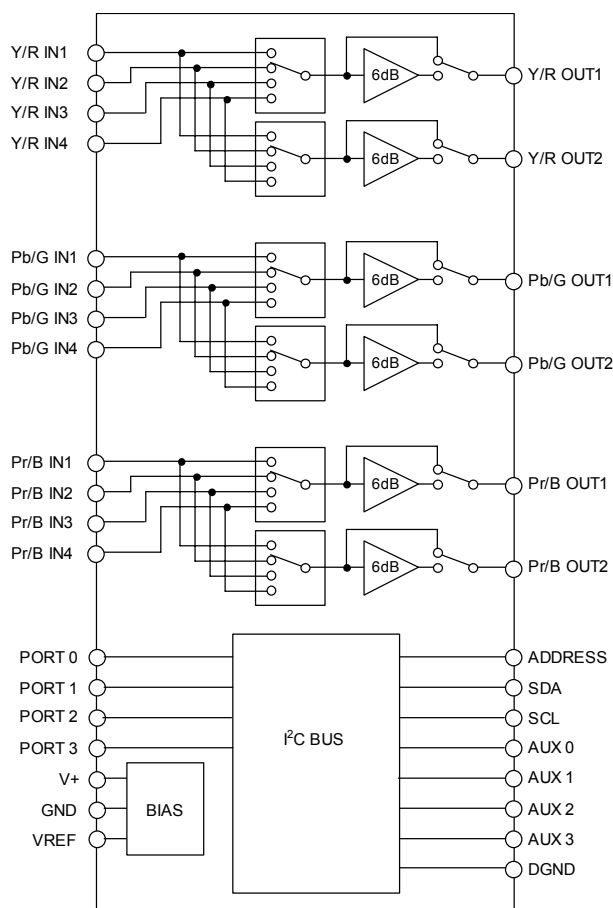


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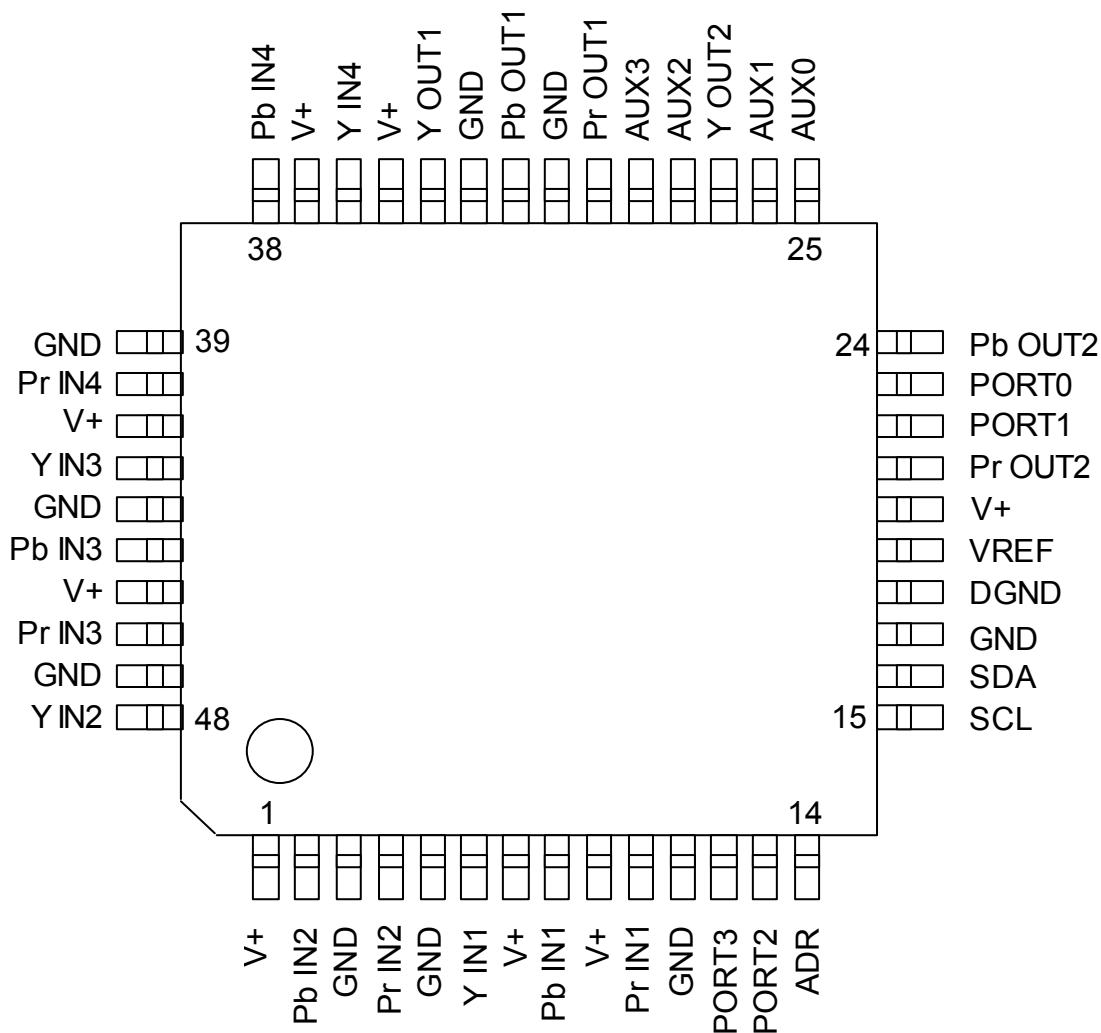
■ FEATURES

- Operating Voltage +9.0V
- I²C BUS Interface
- 4-input 2-output 3-Circuits
- Wide frequency range 0dB at 100MHz typ.
-3dB at 300MHz typ.
- Internal 6dB amplifier (Selectable Bypass or 6dB)
- External logic discernment terminal
- External logic control terminal
- Selectable slave address
- Power Save Circuit
- Bi-CMOS Technology
- Package Outline QFP48

■ BLOCK DIAGRAM



PIN CONFIGURATION



1. V+	13. PORT2	25. AUX0	37. V+
2. Pb IN2	14. ADR	26. AUX1	38. Pb IN4
3. GND	15. SCL	27. Y OUT2	39. GND
4. Pr IN2	16. SDA	28. AUX2	40. Pr IN4
5. GND	17. GND	29. AUX3	41. V+
6. Y IN1	18. DGND	30. Pr OUT1	42. Y IN3
7. V+	19. VREG	31. GND	43. GND
8. Pb IN1	20. V+	32. Pb OUT1	44. Pb IN3
9. V+	21. Pr OUT2	33. GND	45. V+
10. Pr IN1	22. PORT1	34. Y OUT1	46. Pr IN3
11. GND	23. PORT 0	35. V+	47. GND
12. PORT3	24. Pb OUT2	36. Y IN4	48. Y IN2

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	12.0	V
Power Dissipation	P _D	1875(note)	mW
Operating Temperature Range	T _{opr}	-40 to +75	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

(Note) At on a board of EIA/JEDEC specification. (76.2 × 114.3 × 1.6mm Two layers, FR-4)

■ RECOMMENDED OPEARATING CONDITION (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{opr}		8.5	9.0	9.5	V

■ ELECTRICAL CHARACTERISTICS (V⁺=9.0V, R_L=10KΩ, Ta=25°C)

●VIDEO

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I _{cc}	No signal	-	85	100	mA
Maximum Output Voltage	V _{om}	f=100kHz, THD=1%	2.0	2.5	-	Vp-p
Voltage Gain 1	Gv1	6dB Mode Vin=100kHz, 1.0Vp-p Sin signal	6.0	6.4	6.8	dB
Voltage Gain 2	Gv2	Bypass Mode Vin=100kHz, 1.0Vp-p Sin signal	-0.5	0.0	0.5	dB
Frequency Characteristic 1	Gf1	6dB Mode Vin=100MHz / 100kHz, 1.0Vp-p Sin signal	-	0	-	dB
Frequency Characteristic 2	Gf2	Bypass Mode Vin=100MHz / 100kHz, 1.0Vp-p Sin signal	-	0	-	dB
Frequency Characteristic 3	Gf3	6dB Mode Vin=300MHz / 100kHz, 1.0Vp-p Sin signal	-	-3.0	-	dB
Frequency Characteristic 4	Gf4	Bypass Mode Vin=300MHz / 100kHz, 1.0Vp-p Sin signal	-	-3.0	-	dB
Cross talk 1	CTB1	Vin=4.43MHz, 1.0Vp-p Sin signal	-	-60	-50	dB
Cross talk 2	CTB2	Vin=50MHz, 1.0Vp-p Sin signal	-	-40	-	dB
Differential Gain	DG	Vin=1.0Vp-p 10step Video signal	-	0.3	-	%
Differential Phase	DP	Vin=1.0Vp-p 10step Video signal	-	0.3	-	deg
S/N	SNv	Vin=1.0Vp-p, 100% White Video Signal	-	65	-	dB

●PORT, AUX

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PORT Input Voltage H	V _{PTH}		3.5	-	5.5	V
PORT Input Voltage M	V _{PTM}		1.4	-	2.4	V
PORY Input Voltage L	V _{PTL}		0	-	0.8	V
AUX Output Voltage H	V _{AUXH}		3.5	-	5.5	V
AUX Output Voltage M	V _{AUXM}		1.4	-	2.4	V
AUX Output Voltage L	V _{AUXL}		0	-	0.8	V
ADR Input Voltage H	V _{ADRH}		3.5	-	5.0	V
ADR Input Voltage L	V _{ADRL}		0	-	1.0	V

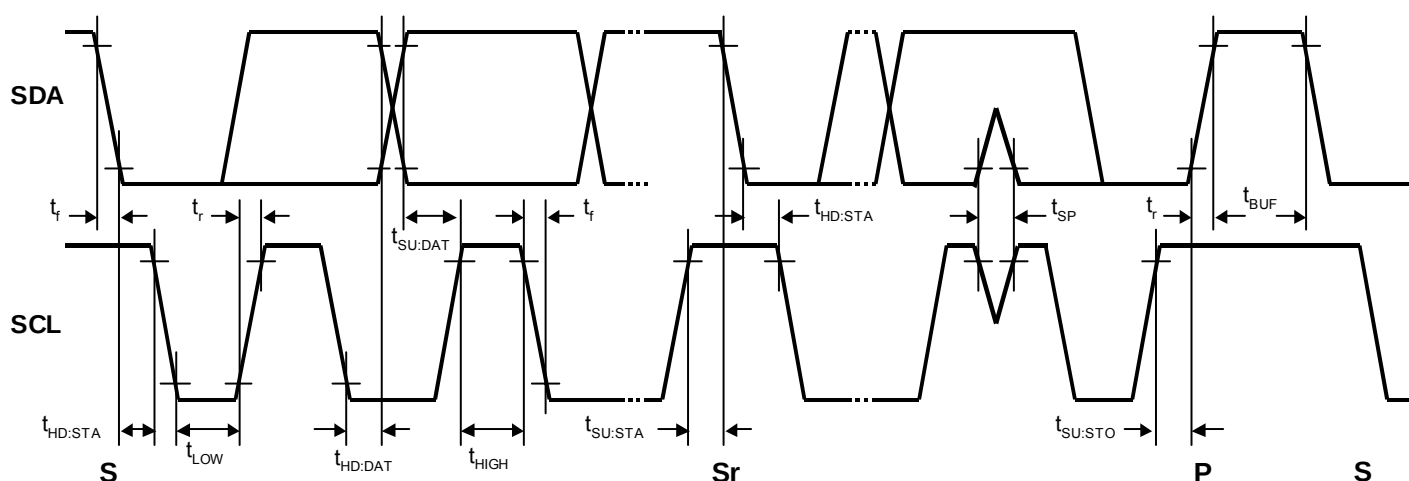
■ I²C BUS BLOCK CHARACTERISTICS (SDA,SCL)

I²C BUS Load Conditions

STANDARD MODE: Pull up resistance 4k Ω (Connected to +5V), Load capacitance 200pF (Connected to GND)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Low Level Input Voltage	V _{IL}	0.0	-	1.5	V
High Level Input Voltage	V _{IH}	2.7	-	5.5	V
LOW level Output Voltage (3mA at SDA pin)	V _{OL}	0	-	0.4	V
Output Fall Time From V _{IHmin} to V _{ILmax} with a Bus Capacitance from 10pF to 400pF	t _{of}	-	-	250	ns
Input Current each I/O pin with an Input Voltage between 0.1 and 0.9V _{DDmax}	I _i	-10	-	10	μ A
Capacitance for each I/O pin	C _i	-	-	10	pF
SCL Clock Frequency	f _{SCL}	-	-	100	kHz
Data Transfer Start Minimum Waiting Time	t _{HD:STA}	4.0	-	-	μ s
Low Level Clock Pulse Width	t _{LOW}	4.7	-	-	μ s
High Level Clock Pulse Width	t _{HIGH}	4.0	-	-	μ s
Minimum Start Preparation Waiting Time	t _{SU:STA}	4.7	-	-	μ s
Minimum Data Hold Time	t _{HD:DAT}	0	-	-	μ s
Minimum Data Preparation Time	t _{SU:DAT}	250	-	-	ns
Rise Time	t _r	-	-	1000	ns
Fall Time	t _f	-	-	300	ns
Minimum Stop Preparation Waiting Time	t _{SU:STO}	4.0	-	-	μ s
Data Change Minimum Waiting Time	t _{BUF}	4.7	-	-	μ s
Capacitive load for each bus line	C _b	-	-	400	pF
Noise Margin at the Low Level	V _{nL}	0.5	-	-	V
Noise Margin at the High Level	V _{nH}	1	-	-	V

C_b ; total capacitance of one bus line in pF.



■EQUIVALENT CIRCUIT

PIN No.	NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
6 8 10 48 2 4 42 44 46 36 38 40	Y IN1 Pb IN1 Pr IN1 Y IN2 Pb IN2 Pr IN2 Y IN3 Pb IN3 Pr IN3 Y IN4 Pb IN4 Pr IN4	Y,Pb,Pr Input RGB Input		4.4V
34 32 30 27 24 21	Y OUT1 Pb OUT1 Pr OUT1 Y OUT2 Pb OUT2 Pr OUT2	Y,Pb,Pr Output RGB Output		3.7V
23 22 13 12	PORT0 PORT1 PORT2 PORT3	Logic input terminal		-
25 26 28 29	AUX0 AUX1 AUX2 AUX3	Auxiliary 3 values voltage output terminal		0V 1.9V 5.0V

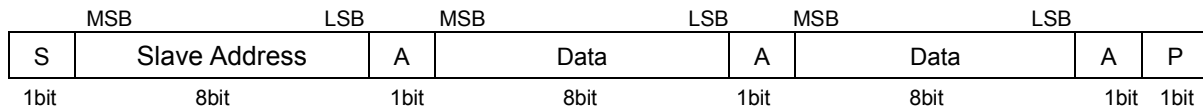
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PIN No.	NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
14	ADR	Slave address setting terminal		-
15 16	SCL SDA	I ² C clock terminal I ² C data terminal		-
19	VREF	Reference voltage terminal		4.8V
1 7 9 20 35 37 41 45	V+	Supply voltage terminal		-
3 5 11 17 31 33 39 43 47	GND	Ground terminal		-
18	DGND	Ground terminal		-

■ DEFINITION OF I²C REGISTER

◆ I²C BUS FORMAT



S: Starting Term

A: Acknowledge Bit

P: Ending Term

◆ SLAVE ADDRESS

R/W: Set the Write Mode or Read Mode.

ADR : Set the Slave Address by "ADR" terminal.

Slave Address								Hex
MSB				LSB				-
1	0	0	0	0	0	ADR	R/W	-
◆ R/W = 0 : Write Mode, ADR = 0/1								-
1	0	0	1	0	1	0	0	94(h)
1	0	0	1	0	1	1	0	96(h)
◆ R/W = 1 : Read Mode, ADR = 0/1								-
1	0	0	1	0	1	0	1	95(h)
1	0	0	1	0	1	1	1	97(h)

◆ CONTROL REGISTER TABLE

< Write Mode >

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data1	PS1	PS2	OUT1			OUT2		
Data2	AUX0		AUX1		AUX2		AUX3	

< Read Mode >

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	PORT0		PORT1		PORT2		PORT3	

◆ CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data1	0	0	0	0	0	0	0	0
Data2	0	0	0	0	0	0	0	0

■ INSTRUCTION CODE

◆ POWER SAVE, OUTPUT SETTING

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data1	PS1	PS2	OUT1			OUT2		

● PS1, PS2: Power Save Setting

Power Save		D7	D6
OUT1 ON	OUT2 ON	0	0
OUT1 ON	OUT2 OFF	0	1
OUT1 OFF	OUT2 ON	1	0
OUT1 OFF	OUT2 OFF	1	1

ON: Power Save OFF, OFF: Power Save ON (Mute)

● OUT1: Output 1 Setting

Output 1			D5	D4
YIN1	PbIN1	PrIN1	0	0
YIN2	PbIN2	PrIN2	0	1
YIN3	PbIN3	PrIN3	1	0
YIN4	PbIN4	PrIN4	1	1

Gain	D3
6dB	0
0dB	1

● OUT2: Output 2 Setting

Output 2			D2	D1
YIN1	PbIN1	PrIN1	0	0
YIN2	PbIN2	PrIN2	0	1
YIN3	PbIN3	PrIN3	1	0
YIN4	PbIN4	PrIN4	1	1

Gain	D0
6dB	0
0dB	1

◆AUX: AUXILIARY SETTING

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data2	AUX0		AUX1		AUX2		AUX3	

AUX0	D7	D6
L	0	0
M	0	1
H	1	1

AUX1	D5	D4
L	0	0
M	0	1
H	1	1

AUX2	D3	D2
L	0	0
M	0	1
H	1	1

AUX3	D1	D0
L	0	0
M	0	1
H	1	1

◆PORT: PORT SETTING

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	PORT0		PORT1		PORT2		PORT3	

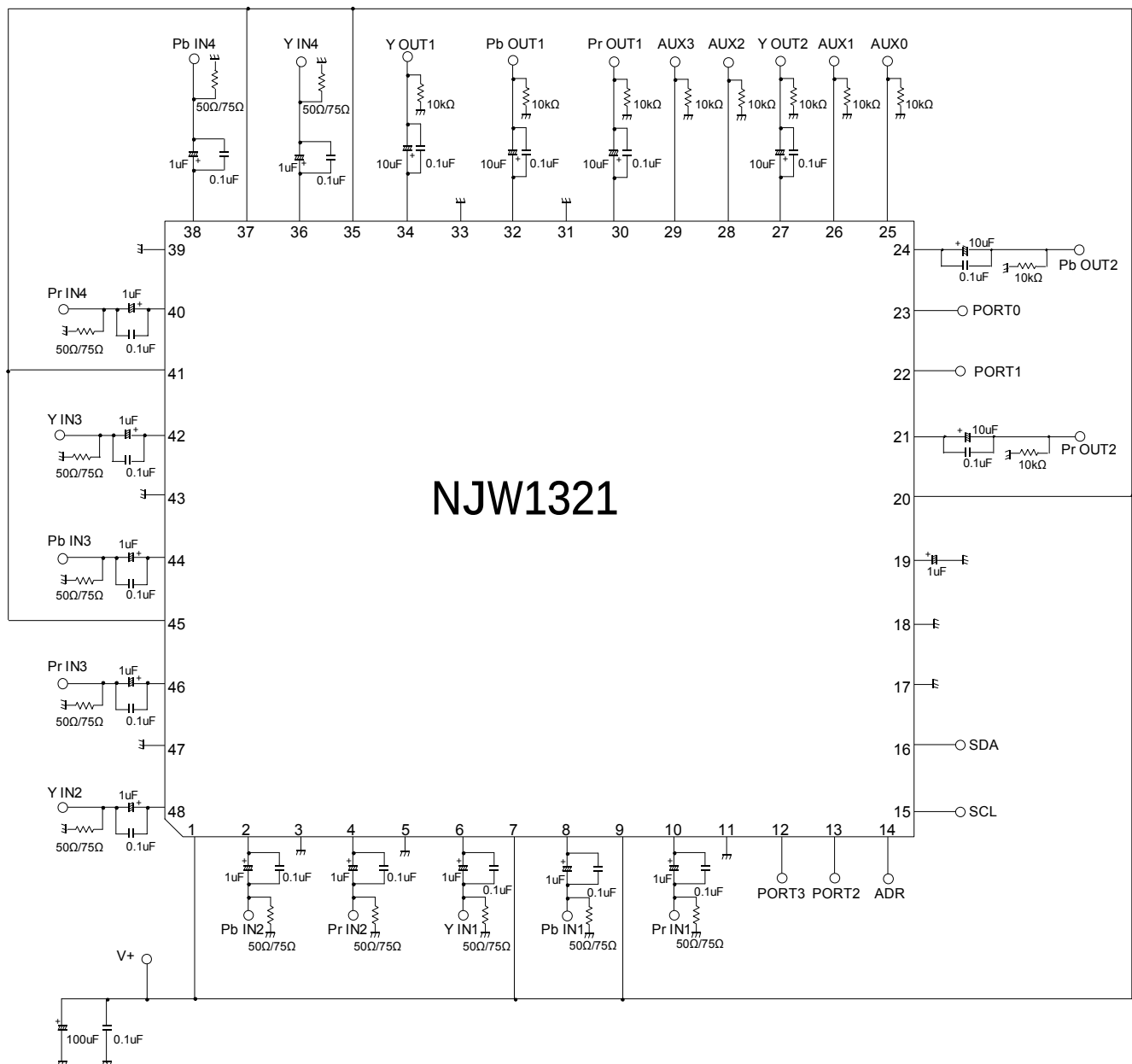
PORT0	D7	D6
OPEN	0	0
L	0	0
M	0	1
H	1	1

PORT1	D5	D4
OPEN	0	0
L	0	0
M	0	1
H	1	1

PORT2	D3	D2
OPEN	0	0
L	0	0
M	0	1
H	1	1

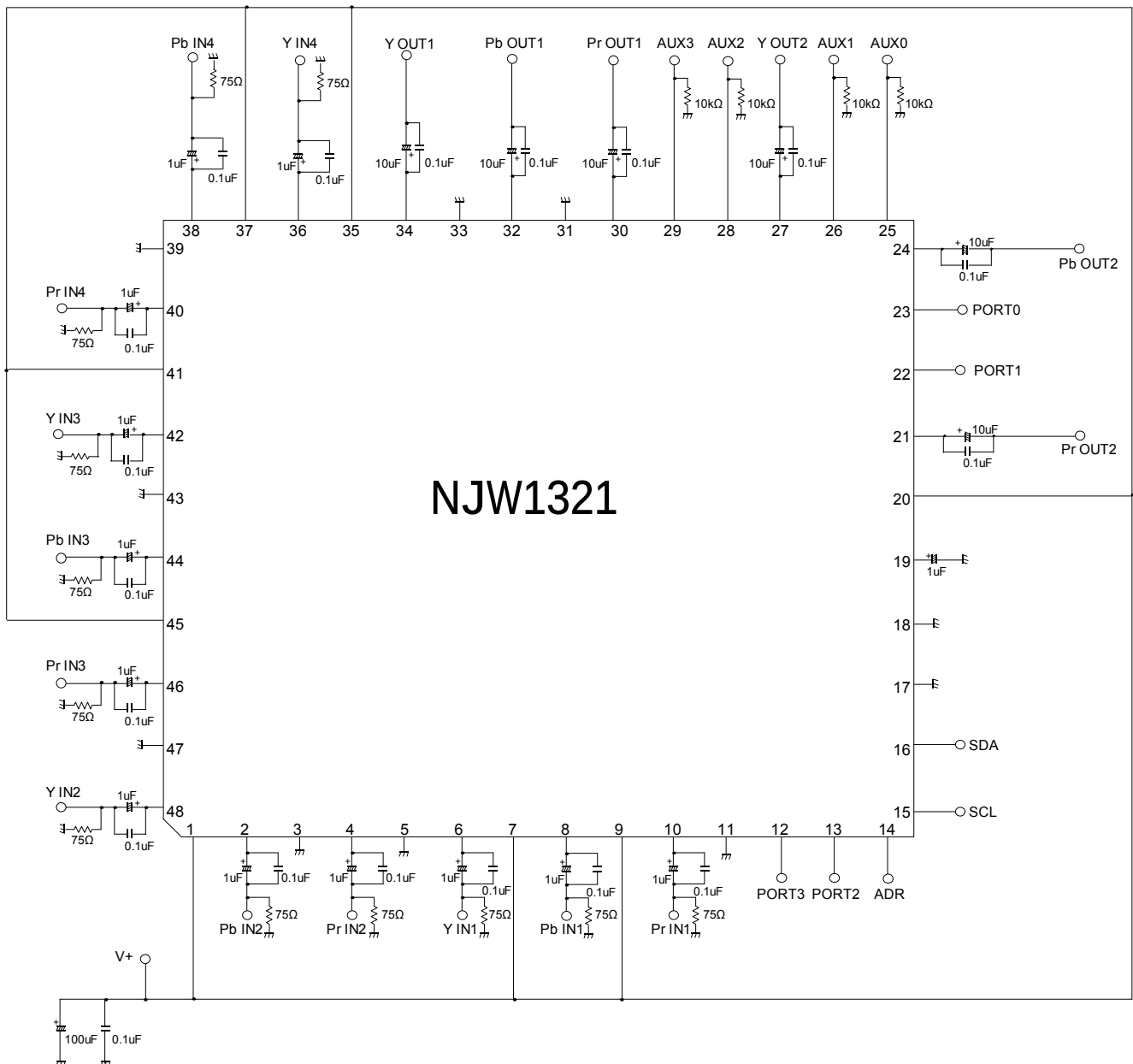
PORT3	D1	D0
OPEN	0	0
L	0	0
M	0	1
H	1	1

TEST CIRCUIT



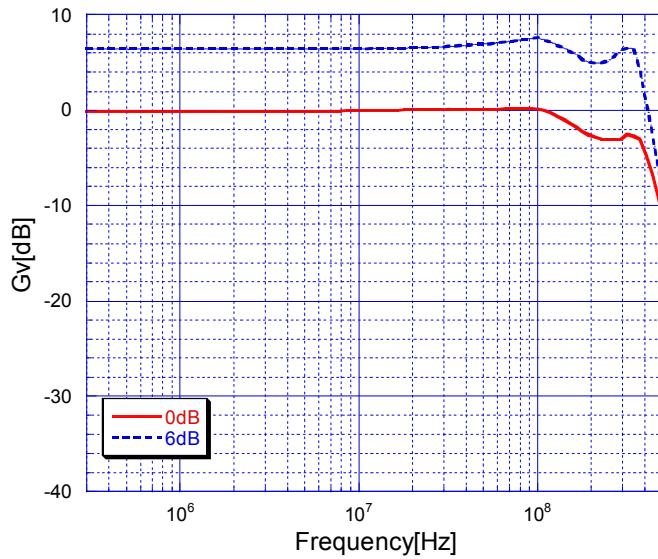
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TYPICAL CHARACTERISTICS

Voltege Gain vs. Frequency



NOTE

Please all connect V+ terminal and GND terminal.

When the power supply voltage is not impressing, please do not impress voltage to the ADR terminal.

[CAUTION]

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