AUDIO PROCESSOR

■ GENERAL DESCRIPTION

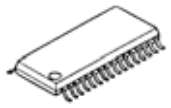
The **NJW1143A** is an audio processor which includes volume, balance, tone control, surround, simulated stereo and AGC function.

Also the **NJW1143A** features high precision characteristics about channel balance, it is less than ±1.0dB at –70dB attenuation.

All of internal status and variables are controlled by I^2C BUS. Selectable 4-slave address is applicable to multi-speaker system.

It is suitable for any TV set.

■ PACKAGE OUTLINE

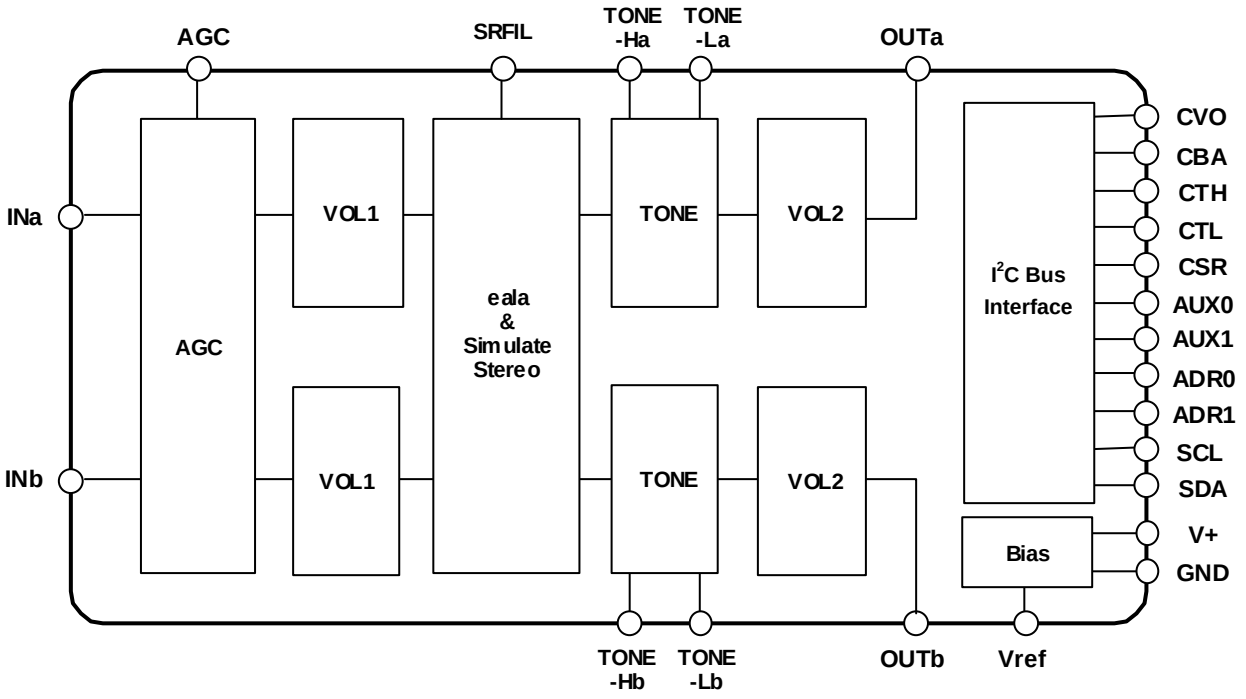


NJW1143AV

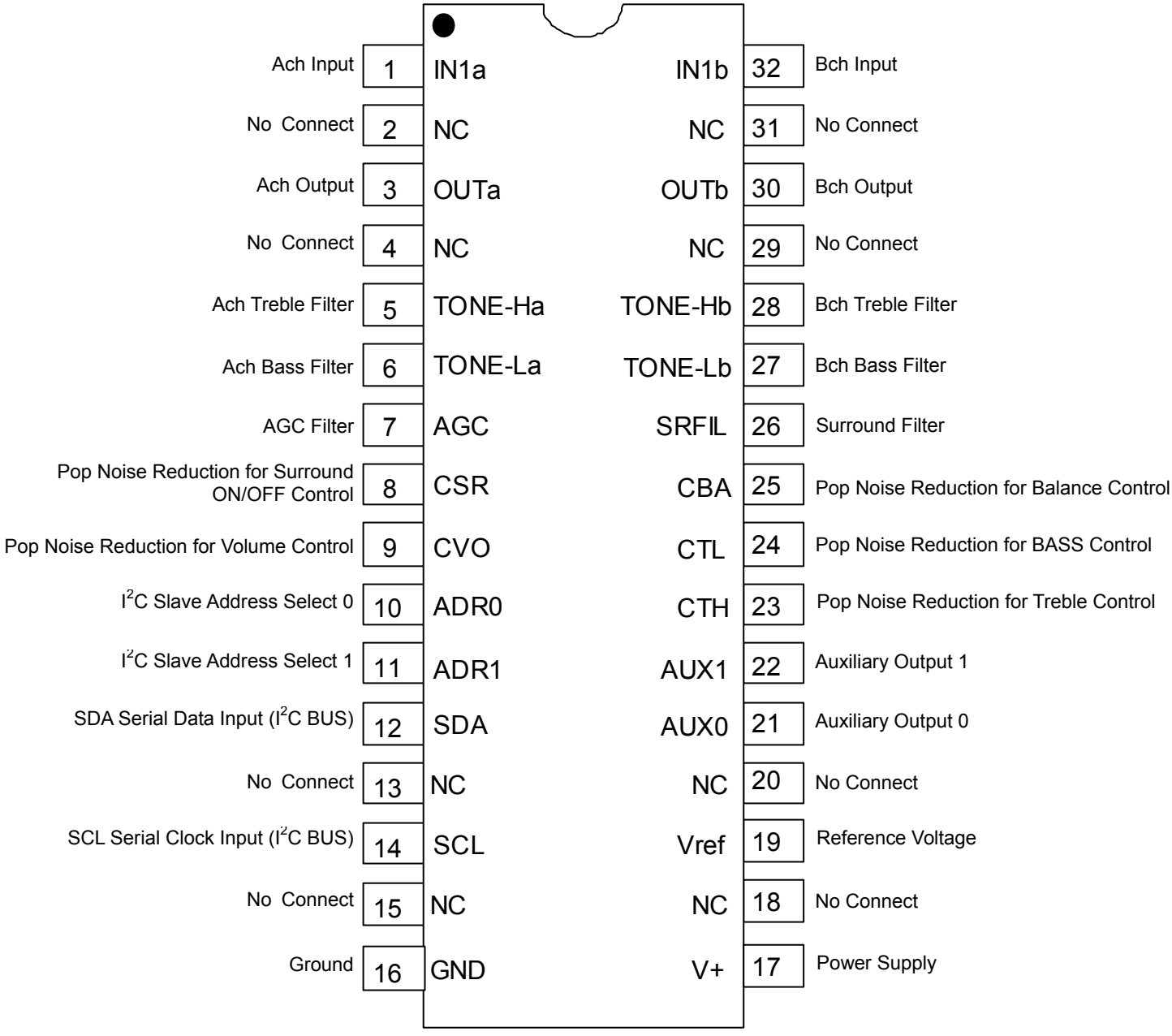
■ FEATURES

- Operating Voltage 8 to 13V
- I^2C BUS Interface
  (Fast mode applicable, Selectable 4-Slave address, 3V I/F applicable)
- Low Output Noise
- AGC Circuit (Selectable 4-stage compression level via I^2C BUS)
- "eala" (NJRC Surround)
- Simulated Surround
- Bi-CMOS Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



■ **PIN CONFIGURATION**



■ **ABSOLUTE MAXIMUM RATING** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	800 NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■ **ELECTRICAL CHARACTERISTICS** (Ta=25°C, V+=9V, Rg=600Ω, R_L=47kΩ, Vin=100mVrms/1kHz, AGC=OFF, TONE=0dB, Surround=OFF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		8.0	9.0	13.0	V
Supply Current	I_{CC}	No Signal	-	13.0	25.0	mA
Reference Voltage	V_{REF}	No Signal	4.0	4.5	5.0	V
Maximum Input Voltage	V_{IM}	VOL=-20dB,THD=10%	2.8	3.0	-	Vrms
Maximum Output Voltage	V_{OM}	OUTPUT VOL=0dB,THD=1%	-	2.5	-	Vrms
Channel Balance 1	G_{CB1}	VOL=0dB	-1.0	0.0	1.0	dB
Channel Balance 2	G_{CB2}	VOL=-70dB, Vin=1Vrms	-1.0	0.0	1.0	dB
Balance Boost A	BA_{BST}	CHS="0", BAL="11111"	-2.0	0.0	2.0	dB
Balance Cut A	BA_{CUT}	CHS="1", BAL="11111" Vin = 1Vrms	-	-	-70	dB
Balance Boost B	BB_{BST}	CHS="1", BAL="11111"	-2.0	0.0	2.0	dB
Balance Cut B	BB_{CUT}	CHS="0", BAL="11111" Vin = 1Vrms	-	-	-70	dB
Total Harmonic Distortion	THD	Vo=0.5Vrms BW=400Hz to 30kHz	-	-	0.3	%
Maximum Gain	G_{VMAX}	VOL= 0dB	-2.0	0.0	2.0	dB
Minimum Gain	G_{VMIN}	VOL= MUTE, Vin=2Vrms	-	-100	-90	dB
Channel Separation	CS	Vin = 1Vrms A-weighting	-	-80	-70	dB
Output Noise 1	V_{NO1}	VOL = 0dB A-weighting	- -	-90 (31.6)	-85 (56.2)	dBV (μVrms)
Output Noise 2	V_{NO2}	VOL = MUTE A-weighting	- -	-106 (5.0)	-96 (15.8)	dBV (μVrms)
AUX Output Voltage	V_{AUX}	Logic Output: High	4.5	-	5.5	V
		Logic Output: Low	0	-	0.5	

BW: Band Width

■ **ELECTRICAL CHARACTERISTICS** (Ta=25°C, V+=9V, Rg=600Ω, R_L=47kΩ, Vin=100mVrms/1kHz, AGC=OFF, TONE=0dB, Surround=OFF unless otherwise specified)

♦ **TONE CONTROL**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Frequency Boost	HF_{BST}	BCT="1", TREB="1111", f=10kHz	12.0	15.0	18.0	dB
High Frequency Flat	HF_{FLT}	TREB="0000", f=10kHz	-2.0	0.0	2.0	dB
High Frequency Cut	HF_{CUT}	BCT="0", TREB="1111", f=10kHz	-18.0	-15.0	-12.0	dB
Low Frequency Boost	LF_{BST}	BCB="1", BASS="1111", f=100Hz	12.0	15.0	18.0	dB
Low Frequency Flat	LF_{FLT}	BASS="0000", f=100Hz	-2.0	0.0	2.0	dB
Low Frequency Cut	LF_{CUT}	BCB="0", BASS="1111", f=100Hz	-18.0	-15.0	-12.0	dB

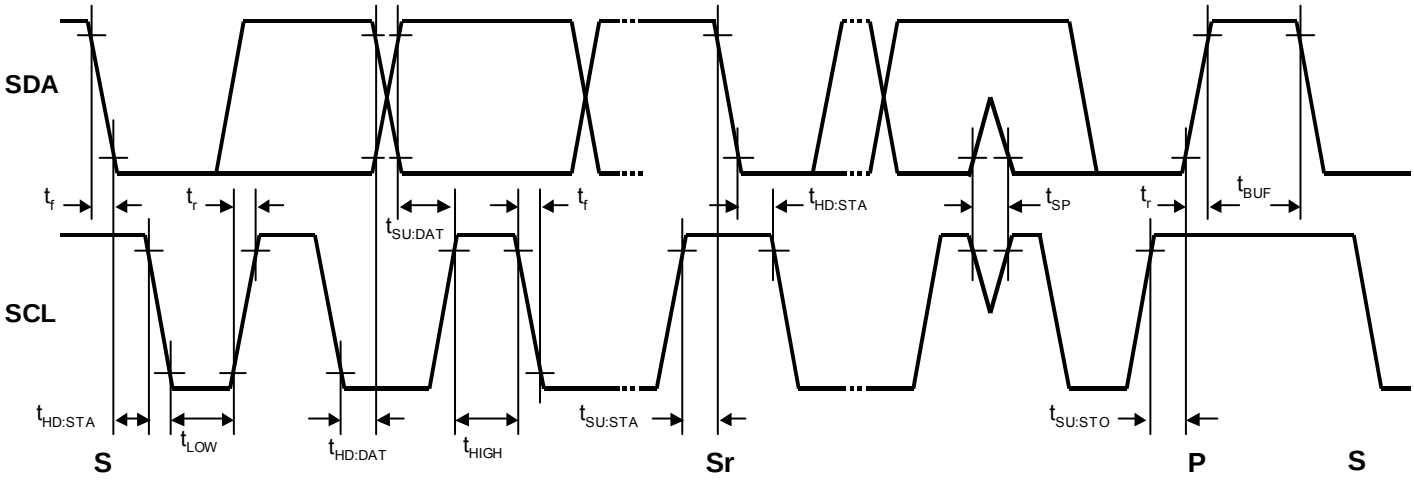
♦ **AGC CONTROL** (AGC-ON)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
AGC Boost	AGC_{BST}	Vin=50mVrms, f=1kHz	1.5	3.5	5.5	dB
AGC Flat1	AGC_{FLT1}	Vin=125mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Flat2	AGC_{FLT2}	Vin=250mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Flat3	AGC_{FLT3}	Vin=300mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Flat4	AGC_{FLT4}	Vin=400mVrms, f=1kHz	-2.5	0.0	2.5	dB
AGC Cut	AGC_{CUT}	Vin=2Vrms, f=1kHz	-14	-10	-6.0	dB

♦ **SURROUND** (SURROUND-ON)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Surround Gain1	SR_{GAIN1}	Ain→Aout, f=100Hz SUR0="1", SUR="1"	2.0	4.0	6.0	dB
Surround Gain2	SR_{GAIN2}	Ain→Bout, f=100Hz SUR0="1", SUR="1"	-6.5	-4.5	-2.5	dB
Surround Gain3	SR_{GAIN3}	Ain→Aout, f=100Hz SUR0="0", SUR="1"	6.0	8.0	10.0	dB
Surround Gain4	$SR_{GAIN\ 4}$	Ain→Bout, f=100Hz SUR0="0", SUR="1"	1.5	3.5	5.5	dB
Simulated Surround Gain1	SR_{SIM1}	Ain+Bin→Aout, f=1kHz SUR0="1", SUR="0"	1.0	3.0	5.0	dB
Simulated Surround Gain2	SR_{SIM2}	Ain+Bin→Bout, f=1kHz SUR0="1", SUR="0"	1.0	3.0	5.0	dB

■TIMING ON THE I^2C BUS (SDA,SCL)



■CHARACTERISTICS OF I/O STAGES FOR I^2C BUS (SDA,SCL)

I^2C BUS Load Conditions

STANDARD MODE : Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

FAST MODE : Pull up resistance 4kΩ (Connected to +5V), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	2.7	-	5.0	2.7	-	5.0	V
Low level output voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	-10	-	10	-10	-	10	μA

■CHARACTERISTICS OF BUS LINES (SDA,SCL) FOR I²C-BUS DEVICES

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	-	-	100	-	-	400	kHz
Hold time (repeated) START condition.	$t_{HD:STA}$	4.0	-	-	0.6	-	-	µs
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	µs
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	µs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	µs
Data hold time NOTE)	$t_{HD:DAT}$	0	-	-	0	-	-	µs
Data set-up time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	µs
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise margin at the Low level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High level	V_{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF.

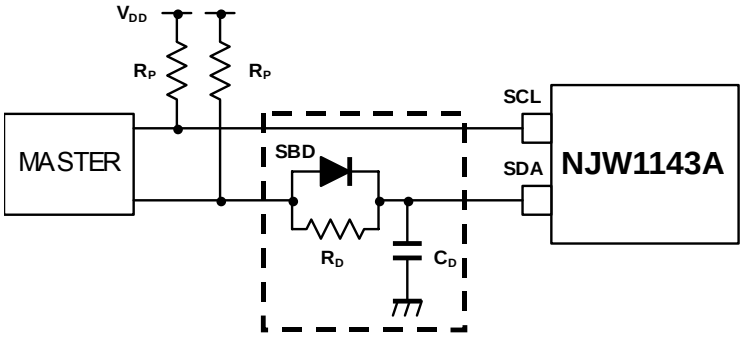
NOTE). Data hold time : $t_{HD:DAT}$

Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

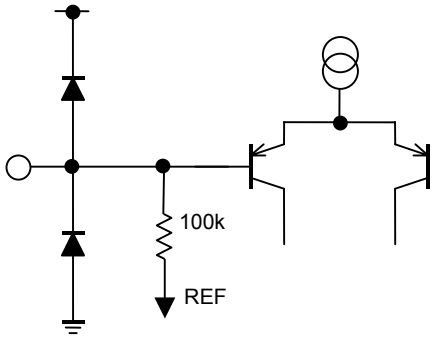
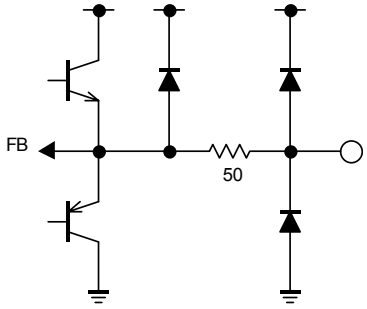
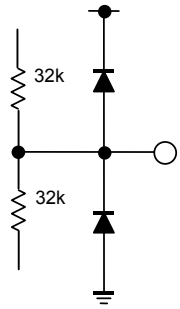
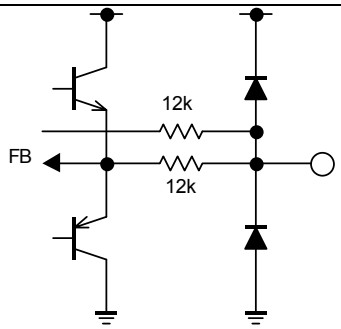
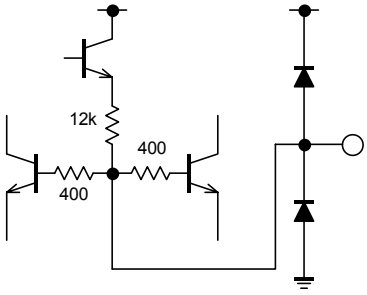
The SDA block in the NJW1143A does not hold data. Add external data-delay-circuit of the SDA terminal, in case of not providing a hold time of at least 300nsec for the SDA in the master device.
The time-consists of the data-delay-circuit of the SDA terminal are as follows.

(a) Low level → High level : $T_{LH} \approx R_P * C_D$
(b) High level → Low level : $T_{HL} \approx R_D * C_D$

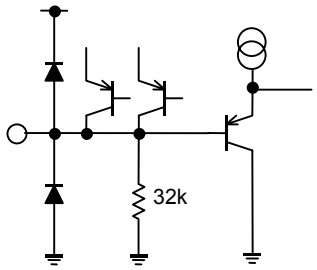
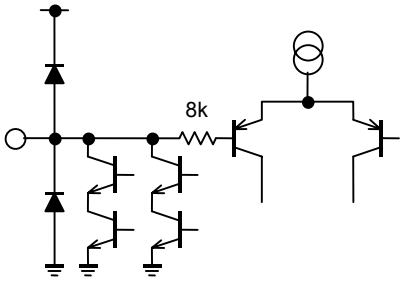
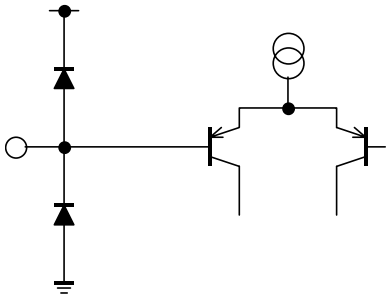
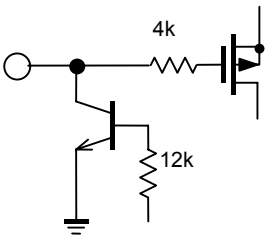
In addition, Schottky barrier diode (SBD) influences a Low level at the Acknowledge. Therefore choose the low forward voltage (Vf) as much as possible.



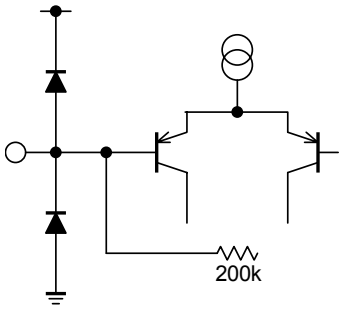
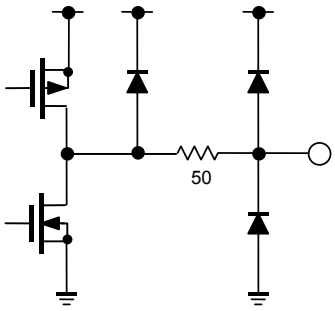
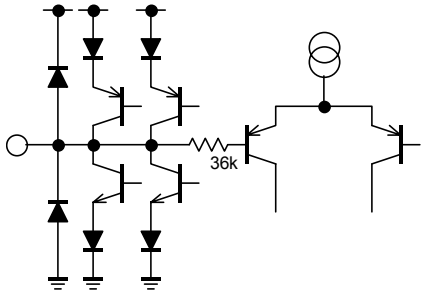
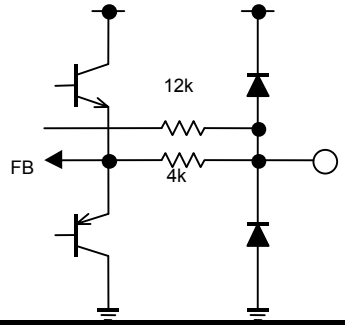
■ **TERMINAL DESCRIPTION**

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
1 32	INa INb	Ach Input terminal Bch Input terminal		$V^+/2$
3 30	OUTa OUTb	Ach Output terminal Bch Output terminal		$V^+/2$
5 28	TONE-Ha TONE-Hb	Ach Treble Filter terminal Bch Treble Filter terminal		$V^+/2$
6 27	TONE-La TONE-Lb	Ach Bass Filter terminal Bch Bass Filter terminal		$V^+/2$
7	AGC	Capacitor connection terminal for AGC attack and recovery time setting		1.4V

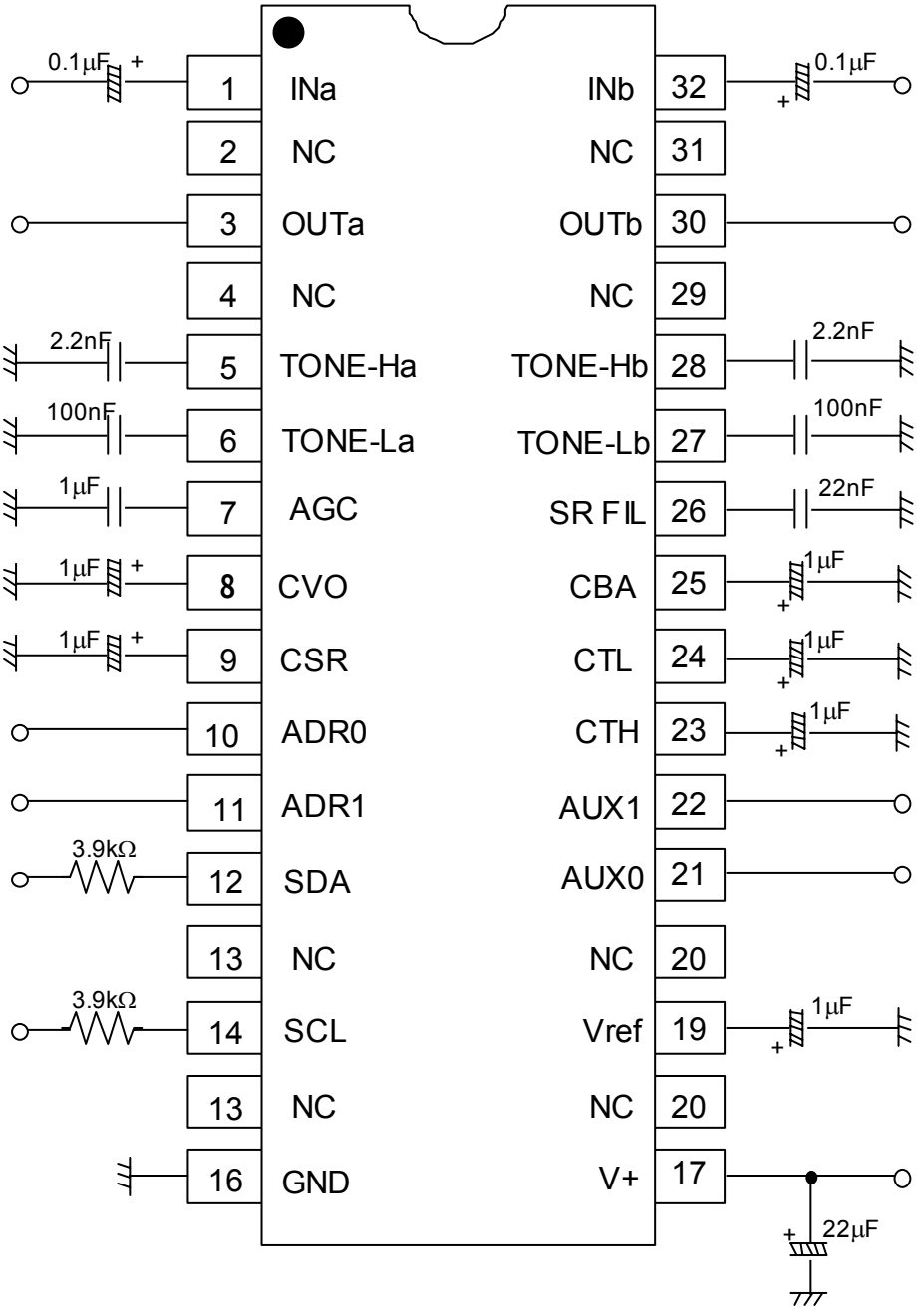
■ **TERMINAL DESCRIPTION**

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
8	CSR	Pop Noise Reduction for Surround ON/OFF Control		$V^+/2$
9	CVO	Pop Noise Reduction for Volume Control		$V^+/2$
10 11	ADR0 ADR1	I^2C Slave Address Select 0 I^2C Slave Address Select 1		-
12 14	SDA SCL	SDA Serial Data Input (I^2C BUS) SDA Serial Clock Input (I^2C BUS)		-
16	GND	Ground terminal	-	-
17	V+	Power Supply terminal	-	-

■ **TERMINAL DESCRIPTION**

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
19	Vref	Reference Voltage terminal		$V^+/2$
21 22	AUX0 AUX1	Auxiliary 2 values voltage Output terminal 0 Auxiliary 2 values voltage Output terminal 1		-
23 24 25	CTH CTL CBA	Pop Noise Reduction for Bass Control Pop Noise Reduction for Treble Control Pop Noise Reduction for Balance Control		$V^+/2$
26	SRFIL	Surround filter terminal		$V^+/2$

■ **APPLICATION CIRCUIT**



(NOTE) Separate the I^2C bus line from the following terminals for avoiding digital noise problem.

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
5	TONE-Ha	26	SR FIL	28	TONE-Hb
6	TONE-La	27	TONE-Lb	-	-

■ DEFINITION OF I²C REGISTER

● I²C BUS FORMAT

	MSB		LSB	MSB		LSB	MSB		LSB
S	Slave Address		A	Select Address		A	Data		A	P
1bit	8bit		1bit	8bit		1bit	8bit		1bit	1bit

S: Starting Term
A: Acknowledge Bit
P: Ending Term

● SLAVE ADDRESS

MSB							LSB
1	0	0	0	0	ADR1	ADR0	R/W

ADR0, ADR1: Hardware pin programmable address bits

ADR1	ADR0	Address
0	0	80H
0	1	82H
1	0	84H
1	1	86H

R/$\overline{W}$=0: Write mode for register setting
R/$\overline{W}$=1: Not available

● CONTROL REGISTER TABLE

The select address sets each function (Volume, Balance, AGC, Tone Control, Surround etc.).
The auto-increment function cycles the select address as follows.

00H→01H→02H→03H→00H

Select Address	BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00H	VOL							
01H	CHS	BAL					SUR	
02H	BCB	BASS				AGC-SW	AGC-FLAT	
03H	BCT	TREB				Don't Care	AUX1	AUX0

● CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

Select Address	BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0
02H	0	0	0	0	0	0	0	0
03H	0	0	0	0	0	0	0	0

■ I²C CONTROL COMMAND DESCRIPTION

●MASTER VOLUME CONTROL

Select Address	BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00H	VOL							

The volume controls both Ach and Bch by the 0.5dB step.
The volume is consisted of volume1 and volume2. The level is divided into half to each volume1 and volume2.

●BALANCE, AGC AND INPUT SELECTOR SETTINGS

Select Address	BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01H	CHS	BAL					SUR	

- CHS: Channel select for balance control
  "0": Ach "Bch is attenuated"
  "1": Bch "Ach is attenuated"
- BAL: Balance control for both Ach and Bch (1dB/Step)
  The balance is consisted of volume2 alone. Volume1 does not operate on balance.
- SUR : Surround Setting

Surround Setting	SUR		Remarks
	D1	**D0**	
Surround OFF	0	0	Input through
Simulated Stereo mode	0	1	For monaural signal input only
"eala" High mode	1	0	Surround Effect Small (4.0dB typ.)
"eala" Low mode	1	1	Surround Effect Large (8.0dB typ.)

●TONE CONTROL (Bass) and AGC SETTINGS

Select Address	BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
02H	BCB	BASS				AGC-SW	AGC-FLAT	

- BCB : Bass Boost or Cut
  "0" : Cut
  "1" : Boost
- BASS : BASS Level
  Cut Level : -15 to 0dB(1dB/Step)
  Boost Level : 0 to +15dB(1dB/Step)
- AGC-SW : AGC ON/OFF Switch
  "0" : AGC OFF
  "1" : AGC ON (Default : 125mVrms)
- AGC-FLAT : AGC Flat Level

AGC Flat Level	AGC-FLAT	
	D1	**D0**
125mVrms	0	0
250mVrms	0	1
375mVrms	1	0
500mVrms	1	1

●**TONE CONTROL (Treble) and FOCUS EFFECT SETTINGS**

Select Address	BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
03H	BCT	TREB				Don't Care	AUX1	AUX0

- BCT : Treble Boost or Cut
  "0" : Cut
  "1" : Boost
- TREB : Treble Level
  Cut Level : -15 to 0dB(1dB/Step)
  Boost Level : 0 to +15dB(1dB/Step)
- AUX1/AUX0: Auxiliary port High/Low
  "0": Logic output "Low"
  "1": Logic output "High"

■ **Master Volume (Select Address: 00H)**

		VOL							
Gain(dB)	HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	FF	1	1	1	1	1	1	1	1
-1	FD	1	1	1	1	1	1	0	1
-2	FB	1	1	1	1	1	0	1	1
-3	F9	1	1	1	1	1	0	0	1
-4	F7	1	1	1	1	0	1	1	1
-5	F5	1	1	1	1	0	1	0	1
-6	F3	1	1	1	1	0	0	1	1
-7	F1	1	1	1	1	0	0	0	1
-8	EF	1	1	1	0	1	1	1	1
-9	ED	1	1	1	0	1	1	0	1
-10	EB	1	1	1	0	1	0	1	1
-11	E9	1	1	1	0	1	0	0	1
-12	E7	1	1	1	0	0	1	1	1
-13	E5	1	1	1	0	0	1	0	1
-14	E3	1	1	1	0	0	0	1	1
-15	E1	1	1	1	0	0	0	0	1
-16	DF	1	1	0	1	1	1	1	1
-17	DD	1	1	0	1	1	1	0	1
-18	DB	1	1	0	1	1	0	1	1
-19	D9	1	1	0	1	1	0	0	1
-20	D7	1	1	0	1	0	1	1	1
-21	D5	1	1	0	1	0	1	0	1
-22	D3	1	1	0	1	0	0	1	1
-23	D1	1	1	0	1	0	0	0	1
-24	CF	1	1	0	0	1	1	1	1
-25	CD	1	1	0	0	1	1	0	1
-26	CB	1	1	0	0	1	0	1	1
-27	C9	1	1	0	0	1	0	0	1
-28	C7	1	1	0	0	0	1	1	1
-29	C5	1	1	0	0	0	1	0	1
-30	C3	1	1	0	0	0	0	1	1
-31	C1	1	1	0	0	0	0	0	1
-32	BF	1	0	1	1	1	1	1	1
-33	BD	1	0	1	1	1	1	0	1
-34	BB	1	0	1	1	1	0	1	1
-35	B9	1	0	1	1	1	0	0	1
-36	B7	1	0	1	1	0	1	1	1
-37	B5	1	0	1	1	0	1	0	1
-38	B3	1	0	1	1	0	0	1	1
-39	B1	1	0	1	1	0	0	0	1
-40	AF	1	0	1	0	1	1	1	1
-41	AD	1	0	1	0	1	1	0	1
-42	AB	1	0	1	0	1	0	1	1

■MASTER VOLUME (Cont'd)

		VOL							
Gain(dB)	HEX	D7	D6	D5	D4	D3	D2	D1	D0
-43	A9	1	0	1	0	1	0	0	1
-44	A7	1	0	1	0	0	1	1	1
-45	A5	1	0	1	0	0	1	0	1
-46	A3	1	0	1	0	0	0	1	1
-47	A1	1	0	1	0	0	0	0	1
-48	9F	1	0	0	1	1	1	1	1
-49	9D	1	0	0	1	1	1	0	1
-50	9B	1	0	0	1	1	0	1	1
-51	99	1	0	0	1	1	0	0	1
-52	97	1	0	0	1	0	1	1	1
-53	95	1	0	0	1	0	1	0	1
-54	93	1	0	0	1	0	0	1	1
-55	91	1	0	0	1	0	0	0	1
-56	8F	1	0	0	0	1	1	1	1
-57	8D	1	0	0	0	1	1	0	1
-58	8B	1	0	0	0	1	0	1	1
-59	89	1	0	0	0	1	0	0	1
-60	87	1	0	0	0	0	1	1	1
-61	85	1	0	0	0	0	1	0	1
-62	83	1	0	0	0	0	0	1	1
-63	81	1	0	0	0	0	0	0	1
-64	7F	0	1	1	1	1	1	1	1
-65	7D	0	1	1	1	1	1	0	1
-66	7B	0	1	1	1	1	0	1	1
-67	79	0	1	1	1	1	0	0	1
-68	77	0	1	1	1	0	1	1	1
-69	75	0	1	1	1	0	1	0	1
-70	73	0	1	1	1	0	0	1	1
-71	71	0	1	1	1	0	0	0	1
-72	6F	0	1	1	0	1	1	1	1
-73	6D	0	1	1	0	1	1	0	1
-74	6B	0	1	1	0	1	0	1	1
-75	69	0	1	1	0	1	0	0	1
-76	67	0	1	1	0	0	1	1	1
-77	65	0	1	1	0	0	1	0	1
-78	63	0	1	1	0	0	0	1	1
-79	61	0	1	1	0	0	0	0	1
-80	5F	0	1	0	1	1	1	1	1
-90	4B	0	1	0	0	1	0	1	1
-100	37	0	0	1	1	0	1	1	1
Mute	00	0	0	0	0	0	0	0	0

■ **Balance (Select Address: 01H)**

Channel Setting	CHS
	D7
Attenuated Bch Gain	0
Attenuated Ach Gain	1

Gain(dB)	BAL				
	D6	**D5**	**D4**	**D3**	**D2**
0	0	0	0	0	0
-1	0	0	0	0	1
-2	0	0	0	1	0
-3	0	0	0	1	1
-4	0	0	1	0	0
-5	0	0	1	0	1
-6	0	0	1	1	0
-7	0	0	1	1	1
-8	0	1	0	0	0
-9	0	1	0	0	1
-10	0	1	0	1	0
-11	0	1	0	1	1
-12	0	1	1	0	0
-13	0	1	1	0	1
-14	0	1	1	1	0
-15	0	1	1	1	1
-16	1	0	0	0	0
-17	1	0	0	0	1
-18	1	0	0	1	0
-19	1	0	0	1	1
-20	1	0	1	0	0
-21	1	0	1	0	1
-22	1	0	1	1	0
-23	1	0	1	1	1
-24	1	1	0	0	0
-25	1	1	0	0	1
-26	1	1	0	1	0
-27	1	1	0	1	1
-28	1	1	1	0	0
-29	1	1	1	0	1
-30	1	1	1	1	0
MUTE	1	1	1	1	1

■ **Tone Control Bass (Select Address: 02H)**

Bass Cut or Boost	BCB
	D7
Cut	0
Boost	1

		BASS			
Cut Gain(dB)	Boost Gain(dB)	**D6**	**D5**	**D4**	**D3**
-15	15	1	1	1	1
-14	14	1	1	1	0
-13	13	1	1	0	1
-12	12	1	1	0	0
-11	11	1	0	1	1
-10	10	1	0	1	0
-9	9	1	0	0	1
-8	8	1	0	0	0
-7	7	0	1	1	1
-6	6	0	1	1	0
-5	5	0	1	0	1
-4	4	0	1	0	0
-3	3	0	0	1	1
-2	2	0	0	1	0
-1	1	0	0	0	1
0	0	0	0	0	0

■ **Tone Control Treble (Select Address: 03H)**

Treble Cut or Boost	BCT
	D7
Cut	0
Boost	1

		TREB			
Cut Gain(dB)	Boost Gain(dB)	**D6**	**D5**	**D4**	**D3**
-15	15	1	1	1	1
-14	14	1	1	1	0
-13	13	1	1	0	1
-12	12	1	1	0	0
-11	11	1	0	1	1
-10	10	1	0	1	0
-9	9	1	0	0	1
-8	8	1	0	0	0
-7	7	0	1	1	1
-6	6	0	1	1	0
-5	5	0	1	0	1
-4	4	0	1	0	0
-3	3	0	0	1	1
-2	2	0	0	1	0
-1	1	0	0	0	1
0	0	0	0	0	0