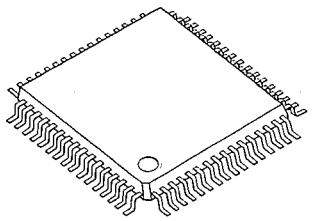
DOLBY PRO LOGIC SURROUND DECODER

■ GENERAL DESCRIPTION

The NJW1102A is a Dolby Pro Logic Surround Decoder including modified Dolby B-Type noise reduction circuit, input auto-balance controller, noise sequenoer, adaptive matrix, center and surround channel level trimmers, serial data interface and others. All of internal status and the balance of surround speakers are controlled by serial data. It performs the complete Dolby Pro Logic Surround function and surround function, such as Hall, Matrix, Simulated and others combine with the digital delay NJU9702.

(Note) Dolby and the double-D symbol are trademakes of Dolby Laboratories Licensing Corporation, San Francisco, CA94103-4813, USA.
This device is available only to licensees of Dolby Lab.
Licensing and application infromation may be obtained from Dolby Lab.

■ PACKAGE OUTLINE



NJW1102AF1

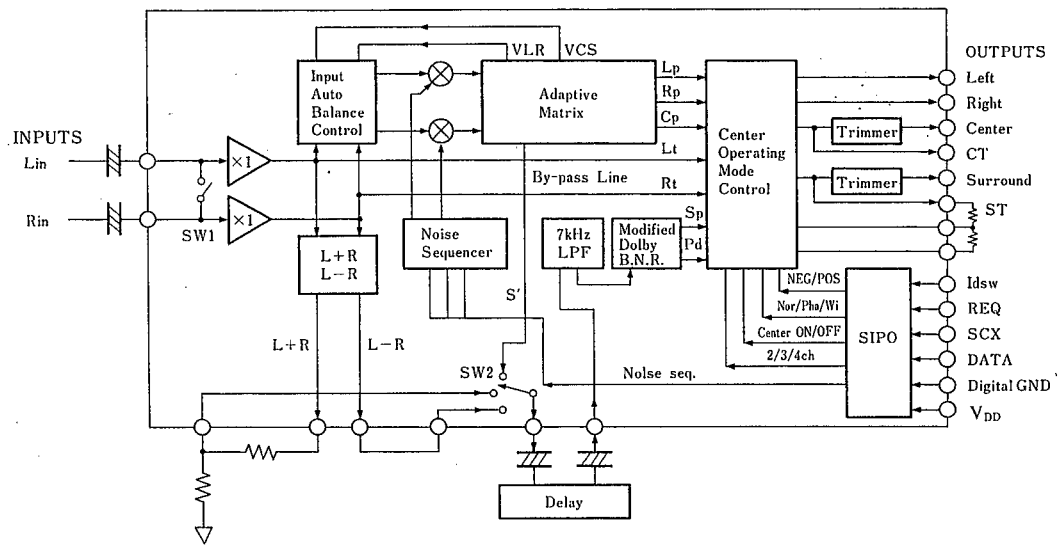
■ FEATURES

- Operating Voltage
  Analog Block V_{CC}=9−13 or ±5V
  Digital Block V_{DD}=5V
- Dolby Operating Level 300mVrms
- Center and Surround Channel Level Trimmers
  −31 to +0dB/ 1dB step (0dB=Dloby Level)
- Internal Mode Control Switch
- Bi-CMOS Technology
- Package Outline TQFP64

■ FUNCTIONS

- Input Auto-Balance
- Noise Generator And Sequencer
- Adaptive Matrix
- Pro Logic Surround Mode Conrtol : 4/3, Center ON/OFF, Normal/Phantom/Wideband
- 7kHz Low-pass Filter and Modified Dolby B Type Noise Reduction
- Center and Surround Channel Level Trimmer
- Other Surround Mode Control : S'Out Selector, Mixer And Mute Functions
- Serial Data Interface
- Optional Digital Outputs AUX1, AUX2

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	13.0	V
	V_{DD}	6.5	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

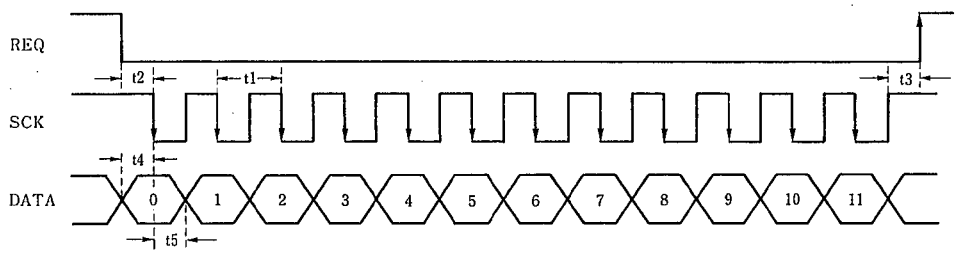
(Ta=25℃, V_{CC}=10V, V_{DD}=5V, 0dB reference is 300mVrms/1kHz at C-OUT with C ch trimmer being 0dB, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall						
Operating Voltage	V_{CC}		9	10	13	V
	V_{DD}		4.5	5.0	6.5	V
Operating Current	I_{CC}	No Signal		35	45	mA
	I_{DD}	No Signal		0.6	1.5	mA
Reference Voltage	Vref	No Signal	3.6	4.0	4.4	V
Threshold Voltage	Vthh	Digital Input High Level	$0.7V_{DD}$		V_{DD}	V
	Vthl	Digital Input Low Level	0.0		$0.3V_{DD}$	V
Input Auto Balance						
Capture Range	CPR			±5		dB
Error Correction	CER			±4		dB
Adaptive Matrix						
Output Level Accuracy Relative to C ch	△Vol	L, R, S' ch out	−0.5	0.0	0.5	dB
Matrix Rejection Relative	MR	L, R, C, S' ch out	25	40		dB
Headroom	HRAM	V_{CC}=9V at THD=1%	15	17		dB
Total Harmonic Distortion	THDAM	L, R, C, S' ch out at 4ch mode		0.050	0.200	%
		L, R ch out at 2ch mode		0.002	0.050	%
Signal to Noise Ratio	SNAM	Rg=0, weighted:CCIR/ARM at 4ch mode	75	80		dB
		L, R ch out at 2ch mode	93	100		dB
Noise Sequencer						
Output Noise Level	Vno		−15	−12.5	−10.0	dB
Output Noise Level Output Noise Level Accuracy Relative to C ch	△Vno	L, R, S' ch out	−0.5	0.0	0.5	dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Modified Noise B Type Noise Reduction						
(0dBd reference is input level at NR-IN when S out is adjusted to 0dB (300mVrms/100Hz) with S ch trimmer level being 0dB)						
Voltage Gain	VGNR	Vin=0dBd, f=100Hz		9.0		dB
Decode Response 1	DEC1	Vin=0dBd, f=1.0kHz	−1.6	−0.1	1.4	dB
Decode Response 2	DEC2	Vin=−15dBd, f=1.4kHz	−3.0	−1.5	0.0	dB
Decode Response 3	DEC3	Vin=−20dBd, f=1.4kHz	−4.9	−3.4	−1.9	dB
Decode Response 4	DEC4	Vin=−40dBd, f=5.0kHz	−6.8	−5.3	3.8	dB
Total Harmonic Distortion	THDNR	Vin=0dBd, f=1kHz		0.070	0.300	%
Headroom	HRNR	Vin=9V at THD=1%	15	17		dB
Signal to Noise	SNNR	Rg=0, weighted : CCIR/ARM	73	78		dB
Other Surround						
Total Harmonic Distortion	THDOS	Vin=0dBd, f=1kHz L+R, L−R Output		0.050	0.200	%
Headroom	HROS	V_{CC}=9V at THD=1% L+R, L−R Output	15	17		dB
Signal to Noise	SNOS	Rg=0, weighted : CCIR/ARM L+R, L−R Output	75	80		dB
Adder Gain	AG			0		dB
C.S Channel Trimmer						
Full Scale	FS	Digital Input= −31dB	−34	−31	−28	dB
Non Linearity (Note 1)	NL	Digital Input=−1, −2, −4, −8, −16dB	−0.5	0.0	0.5	dB
Optional Digital Output (AUX1, AUX2)						
Low Level Voltage	VOL	Sink Current=0.8mA, V_{DD}=5V		0.6	1.0	V
High Level Voltage	VOH	Source Current=0.5mA, V_{DD}=5V	3.5	4.0		V
Control Timing						
SCK Clock Width	t1	SCK	50			μS
REQ Set-up Time	t2	REQ-SCK	25			μS
REQ Hold Time	t3	REQ-SCK	25			μS
Data Set-up Time	t4	SCK-DATA	25			μS
Data Hold Time	t5	SCK-DATA	25			μS

(Note 1) NL=A·B/D−C
A : Measured gain value in full scale
B : Digital input value
C : Measured gain value of digital input
D : Full scale value

(Note 2) Control Timing



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