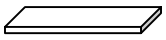
16-CHARACTER 6-LINE LCD DRIVER with JAPANESE KANJI ROM

■ GENERAL DESCRIPTION

The NJU6645 is a 16-character 6-line (16x16dots size Japanese Kanji) or 96 x 256 dots LCD driver with Japanese Kanji ROM.
It contains 8-bit parallel or serial interface, instruction decoder, character generator ROM/RAM, common and segment drivers, bleeder resistor and voltage booster.
The NJU6645 supports the character font of JIS level-1 and level-2, non-kanji and half-size character and symbol.
It is suitable for the low operation voltage and low power applications by low operating voltage 2.4 to 3.6V.

■ PACKAGE OUTLINE

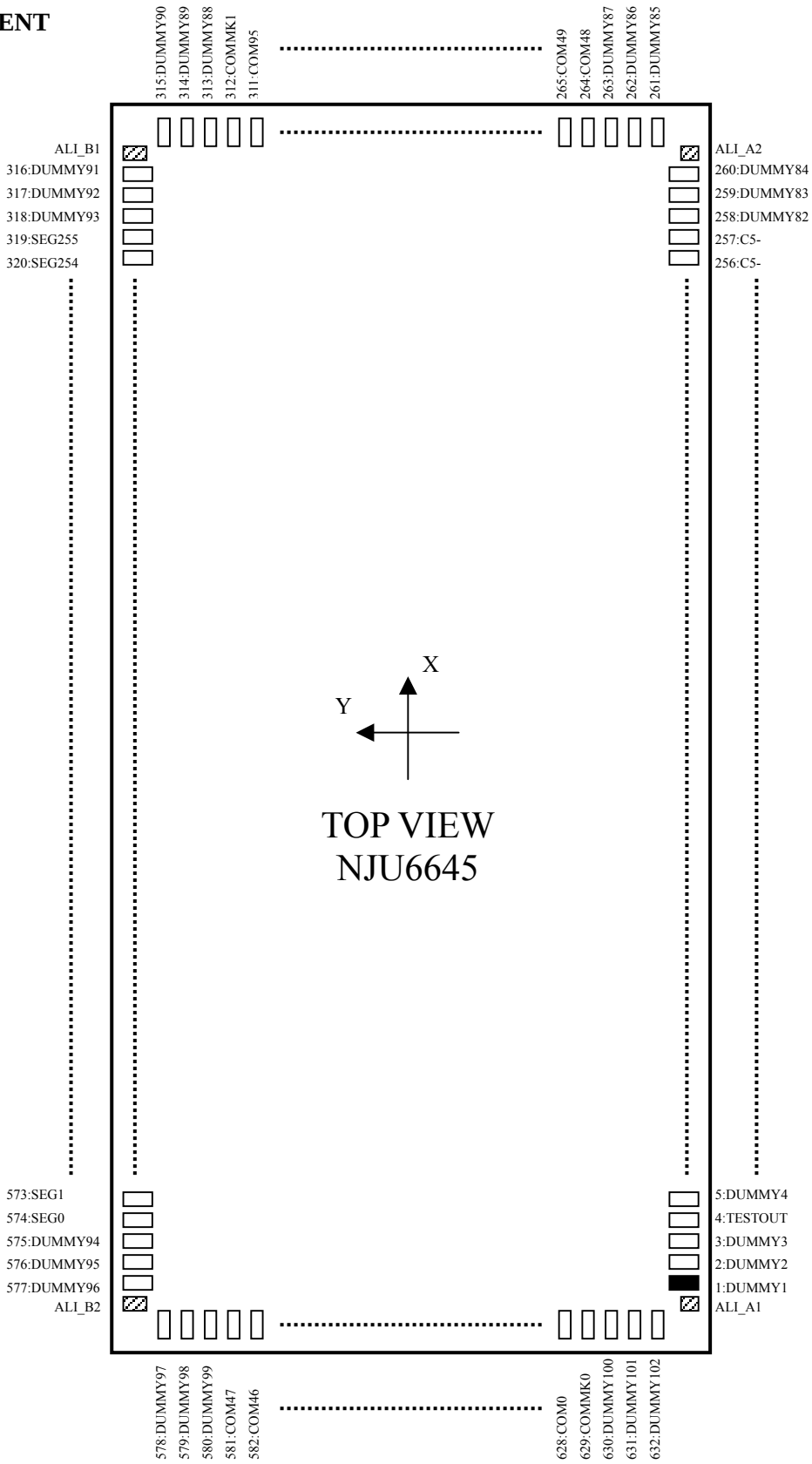


NJU6645CJ

■ FEATURES

- 16-character 6-line Kanji Character Display or 96 x 256 dots Graphic Display LCD controller driver
- LCD Driver Output : 96-common x 256-segment + 2-icon com
- 8-bit Parallel Interface
- Serial Interface
- Display Data RAM 1,536 bits at Full-size 96 Characters
- Character Generator ROM :JIS Level-1 Kanji 16 x 16 dots 2,965 fonts
  :JIS Level-2 Kanji 16 x 16 dots 3,388 fonts
  :JIS Non-Kanji 16 x 16 dots 524 fonts
  :Half Size Display 16 x 16 dots 256 fonts
- Character Generator RAM 24,576 bits 16 x 16 dots 96 fonts
- Icon Display RAM 512 bits Maximum 512 icons
- Duty Ratio 1/18, 1/34, 1/50, 1/66, 1/82, 1/98 (Programmable)
- Bias Ratio 1/4 ~ 1/11 (Programmable)
- Common and Segment driver Location order Select Function (Programmable)
- Common Wiring Select Function
- Useful Instruction Set RE Flag Set, Status Read, Display Clear, Cursor Home, Display Control, Stand-by, Cursor Control, Display / Entry Mode, Scroll Start Line, Scroll Start Row, Display Start Line, Display Duty Ratio, N-line inversion, Driver Output Control, Oscillation Control, Discharge, Boost Level, Bias Ratio, Electrical Volume, Power Control, RAM Address Set, Address Shift, RAM Data Writing / Reading
- Built-in Voltage Boost 2 to 6-time
- Built-in Electrical Volume 128-step
- Oscillation Circuit External Resistor Required
- Built-in Bleeder Resistor
- Operating Voltage +2.4 to 3.6V
- LCD Driving Voltage +4.5 to 17.0V
- Operation Temperature Range -40 to +85°C
- C-MOS Technology (P-sub)
- Package Outline Bump Chip

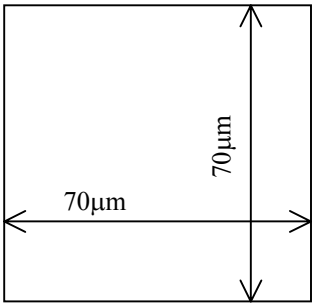
■ PAD ALIGNMENT



Chip Size	: 14.16mm x 3.16mm (T.B.D.)	Chip Center	: X=0µm, Y=0µm
Chip Thickness	: 625µm±25µm	Pad Pitch	: 50µm pitch
Bump Size	: 31µm x 130µm	Bump Height	: 17.5µm(Typ.)
Bump Material	: Au		

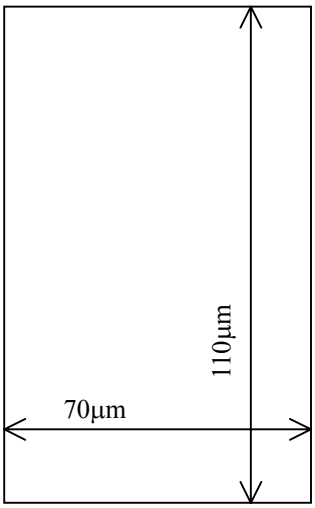
Alignment Mark

- Type A



Center Coordinates : ALI_A1 (X, Y) = (-6682, -1447)
: ALI_A2 (X, Y) = (6682, -1447)

- Type B



Center Coordinates : ALI_B1 (X, Y) = (6710, 1427)
: ALI_B2 (X, Y) = (-6710, 1427)

■ PAD COORDINATES 1

Chip Size 14.16mm x 3.16mm (Chip Center X=0μm, Y=0μm)

PAD No.	PAD name	X= μm	Y= μm
1	DUMMY1	-6475	-1412.5
2	DUMMY2	-6425	-1412.5
3	DUMMY3	-6375	-1412.5
4	TESTOUT	-6325	-1412.5
5	DUMMY4	-6275	-1412.5
6	DUMMY5	-6225	-1412.5
7	SEL68	-6175	-1412.5
8	DUMMY6	-6125	-1412.5
9	VPUP	-6075	-1412.5
10	DUMMY7	-6025	-1412.5
11	PS	-5975	-1412.5
12	DUMMY8	-5925	-1412.5
13	VPUP	-5875	-1412.5
14	DUMMY9	-5825	-1412.5
15	CSEL	-5775	-1412.5
16	DUMMY10	-5725	-1412.5
17	DUMMY11	-5675	-1412.5
18	RSTb	-5625	-1412.5
19	RSTb	-5575	-1412.5
20	DUMMY12	-5525	-1412.5
21	DUMMY13	-5475	-1412.5
22	CSb	-5425	-1412.5
23	CSb	-5375	-1412.5
24	DUMMY14	-5325	-1412.5
25	DUMMY15	-5275	-1412.5
26	RS	-5225	-1412.5
27	RS	-5175	-1412.5
28	DUMMY16	-5125	-1412.5
29	VPDN	-5075	-1412.5
30	DUMMY17	-5025	-1412.5
31	WRb/RW	-4975	-1412.5
32	WRb/RW	-4925	-1412.5
33	DUMMY18	-4875	-1412.5
34	DUMMY19	-4825	-1412.5
35	RDb/E	-4775	-1412.5
36	RDb/E	-4725	-1412.5
37	DUMMY20	-4675	-1412.5
38	VPUP	-4625	-1412.5
39	DUMMY21	-4575	-1412.5
40	D0	-4525	-1412.5
41	D0	-4475	-1412.5
42	DUMMY22	-4425	-1412.5
43	DUMMY23	-4375	-1412.5
44	D1	-4325	-1412.5
45	D1	-4275	-1412.5
46	DUMMY24	-4225	-1412.5
47	DUMMY25	-4175	-1412.5
48	D2	-4125	-1412.5
49	D2	-4075	-1412.5
50	DUMMY26	-4025	-1412.5
51	DUMMY27	-3975	-1412.5
52	D3	-3925	-1412.5
53	D3	-3875	-1412.5
54	DUMMY28	-3825	-1412.5
55	DUMMY29	-3775	-1412.5
56	D4	-3725	-1412.5
57	D4	-3675	-1412.5
58	DUMMY30	-3625	-1412.5
59	DUMMY31	-3575	-1412.5
60	D5	-3525	-1412.5
61	D5	-3475	-1412.5
62	DUMMY32	-3425	-1412.5
63	DUMMY33	-3375	-1412.5
64	D6/SCL	-3325	-1412.5
65	D6/SCL	-3275	-1412.5
66	DUMMY34	-3225	-1412.5
67	DUMMY35	-3175	-1412.5
68	D7/SDA	-3125	-1412.5
69	D7/SDA	-3075	-1412.5
70	DUMMY36	-3025	-1412.5
71	OSC2	-2975	-1412.5
72	OSC2	-2925	-1412.5
73	DUMMY37	-2875	-1412.5
74	VDD	-2825	-1412.5
75	VDD	-2775	-1412.5
76	VDD	-2725	-1412.5
77	VDD	-2675	-1412.5
78	VDD	-2625	-1412.5
79	VDD	-2575	-1412.5
80	DUMMY38	-2525	-1412.5
81	OSC1	-2475	-1412.5
82	OSC1	-2425	-1412.5
83	DUMMY39	-2375	-1412.5
84	VSS	-2325	-1412.5
85	VSS	-2275	-1412.5
86	VSS	-2225	-1412.5
87	VSS	-2175	-1412.5
88	VSS	-2125	-1412.5
89	VSS	-2075	-1412.5
90	DUMMY40	-2025	-1412.5
91	DUMMY41	-1975	-1412.5
92	VLCD	-1925	-1412.5
93	VLCD	-1875	-1412.5
94	VLCD	-1825	-1412.5
95	VLCD	-1775	-1412.5
96	VLCD	-1725	-1412.5
97	VLCD	-1675	-1412.5
98	DUMMY42	-1625	-1412.5
99	DUMMY43	-1575	-1412.5
100	V1	-1525	-1412.5

■ PAD COORDINATES 2

Chip Size 14.16mm x 3.16mm (Chip Center X=0μm, Y=0μm)

PAD No.	PAD name	X= μm	Y= μm
101	V1	-1475	-1412.5
102	V1	-1425	-1412.5
103	V1	-1375	-1412.5
104	V1	-1325	-1412.5
105	DUMMY44	-1275	-1412.5
106	DUMMY45	-1225	-1412.5
107	V2	-1175	-1412.5
108	V2	-1125	-1412.5
109	V2	-1075	-1412.5
110	V2	-1025	-1412.5
111	V2	-975	-1412.5
112	DUMMY46	-925	-1412.5
113	DUMMY47	-875	-1412.5
114	V3	-825	-1412.5
115	V3	-775	-1412.5
116	V3	-725	-1412.5
117	V3	-675	-1412.5
118	V3	-625	-1412.5
119	DUMMY48	-575	-1412.5
120	DUMMY49	-525	-1412.5
121	V4	-475	-1412.5
122	V4	-425	-1412.5
123	V4	-375	-1412.5
124	V4	-325	-1412.5
125	V4	-275	-1412.5
126	DUMMY50	-225	-1412.5
127	DUMMY51	-175	-1412.5
128	VREG	-125	-1412.5
129	VREG	-75	-1412.5
130	VREG	-25	-1412.5
131	VREG	25	-1412.5
132	VREG	75	-1412.5
133	DUMMY52	125	-1412.5
134	DUMMY53	175	-1412.5
135	VREF	225	-1412.5
136	VREF	275	-1412.5
137	VREF	325	-1412.5
138	VREF	375	-1412.5
139	DUMMY54	425	-1412.5
140	DUMMY55	475	-1412.5
141	VBA	525	-1412.5
142	VBA	575	-1412.5
143	VBA	625	-1412.5
144	VBA	675	-1412.5
145	DUMMY56	725	-1412.5
146	DUMMY57	775	-1412.5
147	VSS	825	-1412.5
148	VSS	875	-1412.5
149	VSS	925	-1412.5
150	VSS	975	-1412.5

PAD No.	PAD name	X= μm	Y= μm
151	VSS	1025	-1412.5
152	VSS	1075	-1412.5
153	DUMMY58	1125	-1412.5
154	DUMMY59	1175	-1412.5
155	VOUT	1225	-1412.5
156	VOUT	1275	-1412.5
157	VOUT	1325	-1412.5
158	VOUT	1375	-1412.5
159	VOUT	1425	-1412.5
160	VOUT	1475	-1412.5
161	DUMMY103	1525	-1412.5
162	DUMMY104	1575	-1412.5
163	VDCOUT	1625	-1412.5
164	VDCOUT	1675	-1412.5
165	VDCOUT	1725	-1412.5
166	VDCOUT	1775	-1412.5
167	VDCOUT	1825	-1412.5
168	VDCOUT	1875	-1412.5
169	VDCOUT	1925	-1412.5
170	DUMMY60	1975	-1412.5
171	DUMMY61	2025	-1412.5
172	VEE	2075	-1412.5
173	VEE	2125	-1412.5
174	VEE	2175	-1412.5
175	VEE	2225	-1412.5
176	VEE	2275	-1412.5
177	VEE	2325	-1412.5
178	DUMMY62	2375	-1412.5
179	DUMMY63	2425	-1412.5
180	C1+	2475	-1412.5
181	C1+	2525	-1412.5
182	C1+	2575	-1412.5
183	C1+	2625	-1412.5
184	C1+	2675	-1412.5
185	C1+	2725	-1412.5
186	DUMMY64	2775	-1412.5
187	DUMMY65	2825	-1412.5
188	C1-	2875	-1412.5
189	C1-	2925	-1412.5
190	C1-	2975	-1412.5
191	C1-	3025	-1412.5
192	C1-	3075	-1412.5
193	C1-	3125	-1412.5
194	DUMMY66	3175	-1412.5
195	DUMMY67	3225	-1412.5
196	C2+	3275	-1412.5
197	C2+	3325	-1412.5
198	C2+	3375	-1412.5
199	C2+	3425	-1412.5
200	C2+	3475	-1412.5

■ PAD COORDINATES 3

Chip Size 14.16mm x 3.16mm (Chip Center X=0μm, Y=0μm)

PAD No.	PAD name	X= μm	Y= μm
201	C2+	3525	-1412.5
202	DUMMY68	3575	-1412.5
203	DUMMY69	3625	-1412.5
204	C2-	3675	-1412.5
205	C2-	3725	-1412.5
206	C2-	3775	-1412.5
207	C2-	3825	-1412.5
208	C2-	3875	-1412.5
209	C2-	3925	-1412.5
210	DUMMY70	3975	-1412.5
211	DUMMY71	4025	-1412.5
212	C3+	4075	-1412.5
213	C3+	4125	-1412.5
214	C3+	4175	-1412.5
215	C3+	4225	-1412.5
216	C3+	4275	-1412.5
217	C3+	4325	-1412.5
218	DUMMY72	4375	-1412.5
219	DUMMY73	4425	-1412.5
220	C3-	4475	-1412.5
221	C3-	4525	-1412.5
222	C3-	4575	-1412.5
223	C3-	4625	-1412.5
224	C3-	4675	-1412.5
225	C3-	4725	-1412.5
226	DUMMY74	4775	-1412.5
227	DUMMY75	4825	-1412.5
228	C4+	4875	-1412.5
229	C4+	4925	-1412.5
230	C4+	4975	-1412.5
231	C4+	5025	-1412.5
232	C4+	5075	-1412.5
233	C4+	5125	-1412.5
234	DUMMY76	5175	-1412.5
235	DUMMY77	5225	-1412.5
236	C4-	5275	-1412.5
237	C4-	5325	-1412.5
238	C4-	5375	-1412.5
239	C4-	5425	-1412.5
240	C4-	5475	-1412.5
241	C4-	5525	-1412.5
242	DUMMY78	5575	-1412.5
243	DUMMY79	5625	-1412.5
244	C5+	5675	-1412.5
245	C5+	5725	-1412.5
246	C5+	5775	-1412.5
247	C5+	5825	-1412.5
248	C5+	5875	-1412.5
249	C5+	5925	-1412.5
250	DUMMY80	5975	-1412.5

PAD No.	PAD name	X= μm	Y= μm
251	DUMMY81	6025	-1412.5
252	C5-	6075	-1412.5
253	C5-	6125	-1412.5
254	C5-	6175	-1412.5
255	C5-	6225	-1412.5
256	C5-	6275	-1412.5
257	C5-	6325	-1412.5
258	DUMMY82	6375	-1412.5
259	DUMMY83	6425	-1412.5
260	DUMMY84	6475	-1412.5
261	DUMMY85	6918.5	-1352
262	DUMMY86	6918.5	-1302
263	DUMMY87	6918.5	-1252
264	COM48	6918.5	-1202
265	COM49	6918.5	-1152
266	COM50	6918.5	-1102
267	COM51	6918.5	-1052
268	COM52	6918.5	-1002
269	COM53	6918.5	-952
270	COM54	6918.5	-902
271	COM55	6918.5	-852
272	COM56	6918.5	-802
273	COM57	6918.5	-752
274	COM58	6918.5	-702
275	COM59	6918.5	-652
276	COM60	6918.5	-602
277	COM61	6918.5	-552
278	COM62	6918.5	-502
279	COM63	6918.5	-452
280	COM64	6918.5	-402
281	COM65	6918.5	-352
282	COM66	6918.5	-302
283	COM67	6918.5	-252
284	COM68	6918.5	-202
285	COM69	6918.5	-152
286	COM70	6918.5	-102
287	COM71	6918.5	-52
288	COM72	6918.5	-2
289	COM73	6918.5	48
290	COM74	6918.5	98
291	COM75	6918.5	148
292	COM76	6918.5	198
293	COM77	6918.5	248
294	COM78	6918.5	298
295	COM79	6918.5	348
296	COM80	6918.5	398
297	COM81	6918.5	448
298	COM82	6918.5	498
299	COM83	6918.5	548
300	COM84	6918.5	598

■ PAD COORDINATES 4

Chip Size 14.16mm x 3.16mm (Chip Center X=0μm, Y=0μm)

PAD No.	PAD name	X= μm	Y= μm
301	COM85	6918.5	648
302	COM86	6918.5	698
303	COM87	6918.5	748
304	COM88	6918.5	798
305	COM89	6918.5	848
306	COM90	6918.5	898
307	COM91	6918.5	948
308	COM92	6918.5	998
309	COM93	6918.5	1048
310	COM94	6918.5	1098
311	COM95	6918.5	1148
312	COMMK1	6918.5	1198
313	DUMMY88	6918.5	1248
314	DUMMY89	6918.5	1298
315	DUMMY90	6918.5	1348
316	DUMMY91	6525	1412.5
317	DUMMY92	6475	1412.5
318	DUMMY93	6425	1412.5
319	SEG255	6375	1412.5
320	SEG254	6325	1412.5
321	SEG253	6275	1412.5
322	SEG252	6225	1412.5
323	SEG251	6175	1412.5
324	SEG250	6125	1412.5
325	SEG249	6075	1412.5
326	SEG248	6025	1412.5
327	SEG247	5975	1412.5
328	SEG246	5925	1412.5
329	SEG245	5875	1412.5
330	SEG244	5825	1412.5
331	SEG243	5775	1412.5
332	SEG242	5725	1412.5
333	SEG241	5675	1412.5
334	SEG240	5625	1412.5
335	SEG239	5575	1412.5
336	SEG238	5525	1412.5
337	SEG237	5475	1412.5
338	SEG236	5425	1412.5
339	SEG235	5375	1412.5
340	SEG234	5325	1412.5
341	SEG233	5275	1412.5
342	SEG232	5225	1412.5
343	SEG231	5175	1412.5
344	SEG230	5125	1412.5
345	SEG229	5075	1412.5
346	SEG228	5025	1412.5
347	SEG227	4975	1412.5
348	SEG226	4925	1412.5
349	SEG225	4875	1412.5
350	SEG224	4825	1412.5

PAD No.	PAD name	X= μm	Y= μm
351	SEG223	4775	1412.5
352	SEG222	4725	1412.5
353	SEG221	4675	1412.5
354	SEG220	4625	1412.5
355	SEG219	4575	1412.5
356	SEG218	4525	1412.5
357	SEG217	4475	1412.5
358	SEG216	4425	1412.5
359	SEG215	4375	1412.5
360	SEG214	4325	1412.5
361	SEG213	4275	1412.5
362	SEG212	4225	1412.5
363	SEG211	4175	1412.5
364	SEG210	4125	1412.5
365	SEG209	4075	1412.5
366	SEG208	4025	1412.5
367	SEG207	3975	1412.5
368	SEG206	3925	1412.5
369	SEG205	3875	1412.5
370	SEG204	3825	1412.5
371	SEG203	3775	1412.5
372	SEG202	3725	1412.5
373	SEG201	3675	1412.5
374	SEG200	3625	1412.5
375	SEG199	3575	1412.5
376	SEG198	3525	1412.5
377	SEG197	3475	1412.5
378	SEG196	3425	1412.5
379	SEG195	3375	1412.5
380	SEG194	3325	1412.5
381	SEG193	3275	1412.5
382	SEG192	3225	1412.5
383	SEG191	3175	1412.5
384	SEG190	3125	1412.5
385	SEG189	3075	1412.5
386	SEG188	3025	1412.5
387	SEG187	2975	1412.5
388	SEG186	2925	1412.5
389	SEG185	2875	1412.5
390	SEG184	2825	1412.5
391	SEG183	2775	1412.5
392	SEG182	2725	1412.5
393	SEG181	2675	1412.5
394	SEG180	2625	1412.5
395	SEG179	2575	1412.5
396	SEG178	2525	1412.5
397	SEG177	2475	1412.5
398	SEG176	2425	1412.5
399	SEG175	2375	1412.5
400	SEG174	2325	1412.5

■ PAD COORDINATES 5

Chip Size 14.16mm x 3.16mm (Chip Center X=0μm, Y=0μm)

PAD No.	PAD name	X= μm	Y= μm
401	SEG173	2275	1412.5
402	SEG172	2225	1412.5
403	SEG171	2175	1412.5
404	SEG170	2125	1412.5
405	SEG169	2075	1412.5
406	SEG168	2025	1412.5
407	SEG167	1975	1412.5
408	SEG166	1925	1412.5
409	SEG165	1875	1412.5
410	SEG164	1825	1412.5
411	SEG163	1775	1412.5
412	SEG162	1725	1412.5
413	SEG161	1675	1412.5
414	SEG160	1625	1412.5
415	SEG159	1575	1412.5
416	SEG158	1525	1412.5
417	SEG157	1475	1412.5
418	SEG156	1425	1412.5
419	SEG155	1375	1412.5
420	SEG154	1325	1412.5
421	SEG153	1275	1412.5
422	SEG152	1225	1412.5
423	SEG151	1175	1412.5
424	SEG150	1125	1412.5
425	SEG149	1075	1412.5
426	SEG148	1025	1412.5
427	SEG147	975	1412.5
428	SEG146	925	1412.5
429	SEG145	875	1412.5
430	SEG144	825	1412.5
431	SEG143	775	1412.5
432	SEG142	725	1412.5
433	SEG141	675	1412.5
434	SEG140	625	1412.5
435	SEG139	575	1412.5
436	SEG138	525	1412.5
437	SEG137	475	1412.5
438	SEG136	425	1412.5
439	SEG135	375	1412.5
440	SEG134	325	1412.5
441	SEG133	275	1412.5
442	SEG132	225	1412.5
443	SEG131	175	1412.5
444	SEG130	125	1412.5
445	SEG129	75	1412.5
446	SEG128	25	1412.5
447	SEG127	-25	1412.5
448	SEG126	-75	1412.5
449	SEG125	-125	1412.5
450	SEG124	-175	1412.5

PAD No.	PAD name	X= μm	Y= μm
451	SEG123	-225	1412.5
452	SEG122	-275	1412.5
453	SEG121	-325	1412.5
454	SEG120	-375	1412.5
455	SEG119	-425	1412.5
456	SEG118	-475	1412.5
457	SEG117	-525	1412.5
458	SEG116	-575	1412.5
459	SEG115	-625	1412.5
460	SEG114	-675	1412.5
461	SEG113	-725	1412.5
462	SEG112	-775	1412.5
463	SEG111	-825	1412.5
464	SEG110	-875	1412.5
465	SEG109	-925	1412.5
466	SEG108	-975	1412.5
467	SEG107	-1025	1412.5
468	SEG106	-1075	1412.5
469	SEG105	-1125	1412.5
470	SEG104	-1175	1412.5
471	SEG103	-1225	1412.5
472	SEG102	-1275	1412.5
473	SEG101	-1325	1412.5
474	SEG100	-1375	1412.5
475	SEG99	-1425	1412.5
476	SEG98	-1475	1412.5
477	SEG97	-1525	1412.5
478	SEG96	-1575	1412.5
479	SEG95	-1625	1412.5
480	SEG94	-1675	1412.5
481	SEG93	-1725	1412.5
482	SEG92	-1775	1412.5
483	SEG91	-1825	1412.5
484	SEG90	-1875	1412.5
485	SEG89	-1925	1412.5
486	SEG88	-1975	1412.5
487	SEG87	-2025	1412.5
488	SEG86	-2075	1412.5
489	SEG85	-2125	1412.5
490	SEG84	-2175	1412.5
491	SEG83	-2225	1412.5
492	SEG82	-2275	1412.5
493	SEG81	-2325	1412.5
494	SEG80	-2375	1412.5
495	SEG79	-2425	1412.5
496	SEG78	-2475	1412.5
497	SEG77	-2525	1412.5
498	SEG76	-2575	1412.5
499	SEG75	-2625	1412.5
500	SEG74	-2675	1412.5

■ PAD COORDINATES 6

Chip Size 14.16mm x 3.16mm (Chip Center X=0μm, Y=0μm)

PAD No.	PAD name	X= μm	Y= μm
501	SEG73	-2725	1412.5
502	SEG72	-2775	1412.5
503	SEG71	-2825	1412.5
504	SEG70	-2875	1412.5
505	SEG69	-2925	1412.5
506	SEG68	-2975	1412.5
507	SEG67	-3025	1412.5
508	SEG66	-3075	1412.5
509	SEG65	-3125	1412.5
510	SEG64	-3175	1412.5
511	SEG63	-3225	1412.5
512	SEG62	-3275	1412.5
513	SEG61	-3325	1412.5
514	SEG60	-3375	1412.5
515	SEG59	-3425	1412.5
516	SEG58	-3475	1412.5
517	SEG57	-3525	1412.5
518	SEG56	-3575	1412.5
519	SEG55	-3625	1412.5
520	SEG54	-3675	1412.5
521	SEG53	-3725	1412.5
522	SEG52	-3775	1412.5
523	SEG51	-3825	1412.5
524	SEG50	-3875	1412.5
525	SEG49	-3925	1412.5
526	SEG48	-3975	1412.5
527	SEG47	-4025	1412.5
528	SEG46	-4075	1412.5
529	SEG45	-4125	1412.5
530	SEG44	-4175	1412.5
531	SEG43	-4225	1412.5
532	SEG42	-4275	1412.5
533	SEG41	-4325	1412.5
534	SEG40	-4375	1412.5
535	SEG39	-4425	1412.5
536	SEG38	-4475	1412.5
537	SEG37	-4525	1412.5
538	SEG36	-4575	1412.5
539	SEG35	-4625	1412.5
540	SEG34	-4675	1412.5
541	SEG33	-4725	1412.5
542	SEG32	-4775	1412.5
543	SEG31	-4825	1412.5
544	SEG30	-4875	1412.5
545	SEG29	-4925	1412.5
546	SEG28	-4975	1412.5
547	SEG27	-5025	1412.5
548	SEG26	-5075	1412.5
549	SEG25	-5125	1412.5
550	SEG24	-5175	1412.5

PAD No.	PAD name	X= μm	Y= μm
551	SEG23	-5225	1412.5
552	SEG22	-5275	1412.5
553	SEG21	-5325	1412.5
554	SEG20	-5375	1412.5
555	SEG19	-5425	1412.5
556	SEG18	-5475	1412.5
557	SEG17	-5525	1412.5
558	SEG16	-5575	1412.5
559	SEG15	-5625	1412.5
560	SEG14	-5675	1412.5
561	SEG13	-5725	1412.5
562	SEG12	-5775	1412.5
563	SEG11	-5825	1412.5
564	SEG10	-5875	1412.5
565	SEG9	-5925	1412.5
566	SEG8	-5975	1412.5
567	SEG7	-6025	1412.5
568	SEG6	-6075	1412.5
569	SEG5	-6125	1412.5
570	SEG4	-6175	1412.5
571	SEG3	-6225	1412.5
572	SEG2	-6275	1412.5
573	SEG1	-6325	1412.5
574	SEG0	-6375	1412.5
575	DUMMY94	-6425	1412.5
576	DUMMY95	-6475	1412.5
577	DUMMY96	-6525	1412.5
578	DUMMY97	-6918.5	1348
579	DUMMY98	-6918.5	1298
580	DUMMY99	-6918.5	1248
581	COM47	-6918.5	1198
582	COM46	-6918.5	1148
583	COM45	-6918.5	1098
584	COM44	-6918.5	1048
585	COM43	-6918.5	998
586	COM42	-6918.5	948
587	COM41	-6918.5	898
588	COM40	-6918.5	848
589	COM39	-6918.5	798
590	COM38	-6918.5	748
591	COM37	-6918.5	698
592	COM36	-6918.5	648
593	COM35	-6918.5	598
594	COM34	-6918.5	548
595	COM33	-6918.5	498
596	COM32	-6918.5	448
597	COM31	-6918.5	398
598	COM30	-6918.5	348
599	COM29	-6918.5	298
600	COM28	-6918.5	248

■ PAD COORDINATES 7

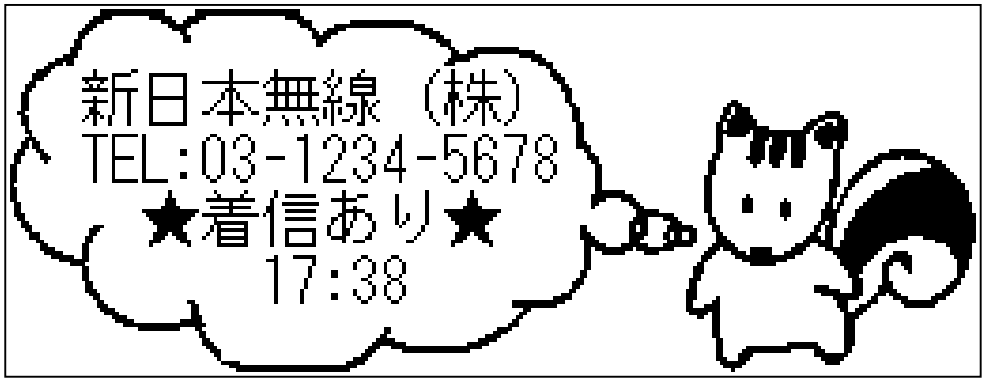
Chip Size 14.16mm x 3.16mm (Chip Center X=0μm, Y=0μm)

PAD No.	PAD name	X= μm	Y= μm
601	COM27	-6918.5	198
602	COM26	-6918.5	148
603	COM25	-6918.5	98
604	COM24	-6918.5	48
605	COM23	-6918.5	-2
606	COM22	-6918.5	-52
607	COM21	-6918.5	-102
608	COM20	-6918.5	-152
609	COM19	-6918.5	-202
610	COM18	-6918.5	-252
611	COM17	-6918.5	-302
612	COM16	-6918.5	-352
613	COM15	-6918.5	-402
614	COM14	-6918.5	-452
615	COM13	-6918.5	-502
616	COM12	-6918.5	-552
617	COM11	-6918.5	-602
618	COM10	-6918.5	-652
619	COM9	-6918.5	-702
620	COM8	-6918.5	-752
621	COM7	-6918.5	-802
622	COM6	-6918.5	-852
623	COM5	-6918.5	-902
624	COM4	-6918.5	-952
625	COM3	-6918.5	-1002
626	COM2	-6918.5	-1052
627	COM1	-6918.5	-1102
628	COM0	-6918.5	-1152
629	COMMK0	-6918.5	-1202
630	DUMMY100	-6918.5	-1252
631	DUMMY101	-6918.5	-1302
632	DUMMY102	-6918.5	-1352

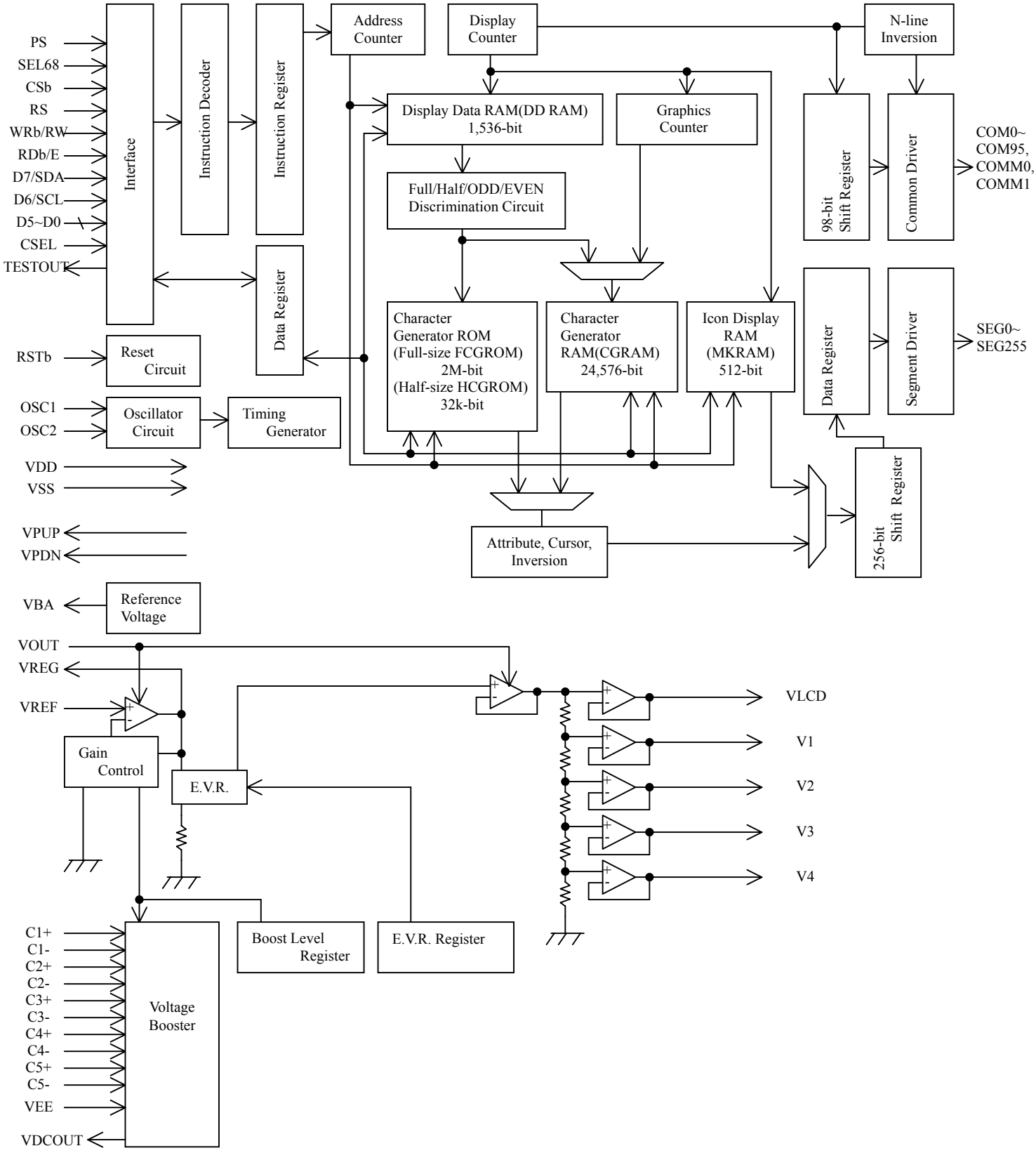
PAD No.	PAD name	X= μm	Y= μm

■ LCD DISPLAY EXAMPLE

- Mix display (Full-size / Half-size / Graphics)



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
74 to 79	VDD	Power	Power Supply (Logic, I/F) VDD=2.4 to 3.6V
84 to 89, 147 to 152	VSS	Power	GND (Logic, I/F, High voltage) VSS=0V
141 to 144	VBA	Output	Reference-Voltage Generator Output
135 to 138	VREF	Input	Voltage Regulator Input
128 to 132	VREG	Output	Voltage Regulator Output
172 to 177	VEE	Power	Voltage Booster Input VEE is normally connected to VDD.
155 to 160	VOUT	Power	High Voltage Power Supply Input (External supply) Input of LCD power supply circuit.
163 to 169	VDCOUT	Output	Voltage Booster Output Output of voltage booster circuit.
92 to 97	VLCD	Power/ Output	LCD Bias Voltages When the internal LCD power supply is used, internal LCD bias voltages (VLCD and V1~V4) are activated by the "Power Control" instruction. Stabilizing capacitors are required between each bias voltage and VSS. When the external LCD power supply is used, LCD bias voltages are externally supplied on VLCD, V1, V2, V3 and V4 individually, with the following relation maintained : VSS<V4<V3<V2<V1<VDD
100 to 104	V1		
107 to 111	V2		
114 to 118	V3		
121 to 125	V4		
9,13,38	VPUP	Power/ Output	VPUP is internally connected to VDD to fix SEL68 or PS or CSEL to "H" if necessary, and cannot be used as main power supply. VPUP should be open if not used.
29	VPDN	Power/ Output	VPDN is internally connected to VSS to fix SEL68 or PS or CSEL to "L" if necessary, and cannot be used as main GND. VPDN should be open if not used.
180 to 185	C1+	Output	Capacitor Connection for Voltage Booster
188 to 193	C1-		
196 to 201	C2+		
204 to 209	C2-		
212 to 217	C3+		
220 to 225	C3-		
228 to 233	C4+		
236 to 241	C4-		
244 to 249	C5+		
252 to 257	C5-		
81,82	OSC1	Input	Resistor Connection for Oscillation Circuit When the internal oscillator is used, connect OSC1 and VDD with an external resistor. And fix OSC2 to "H" or "L".
71,72	OSC2	Input	External Clock Input When the internal oscillator is not used, input external clock to OSC2 and leave OSC1 open.
18,19	RSTb	Input	Reset Active "L"
15	CSEL	Input	COM Output Select "L" : Both sides wiring "H" : Comb wiring

No.	SYMBOL	I/O	FUNCTION
11	PS	Input	Parallel / Serial Interface Mode Select "L" : Serial Interface "H" : Parallel Interface *In the serial interface mode (PS="L") D5 to D0 should be fixed to "H" or "L".
7	SEL68	Input	MPU Mode Select Parallel Interface (PS="H") "L" : 80-series "H" : 68-series Serial Interface (PS="L") Not used. SEL68 should be fixed to "H" or "L".
22,23	CSb	Input	Chip Select Active "L"
26,27	RS	Input	Register Select This signal interprets transferred data as display data or instruction. "L" : Instruction "H" : Display Data
31,32	WRb/RW	Input	80-series MPU Interface (PS="H", SEL68="L") Data Write (WRb) Signal Active "L" 68-series MPU Interface (PS="H", SEL68="H") Data Read or Write (RW) Signal "L" : Write "H" : Read Serial Interface (PS="L") Data Read or Write (RW) Signal
35,36	RDb/E	Input	80-series MPU Interface (PS="H", SEL68="L") Data Read (RDb) Signal Active "L" 68-series MPU Interface (PS="H", SEL68="H") Enable Signal Active "H" Serial Interface (PS="L") Not used. RDb/E should be fixed to "H" or "L".
68,69	D7/SDA	Input/ Output	Parallel Interface (PS="H") In the parallel interface mode (PS="H"), D7 to D0 are connected to 8-bit bi-directional MPU bus. D7 to D0 : 8-bit Bi-directional Bus Serial Interface (PS="L") D7 : Serial Data (SDA) D6 : Serial Clock (SCL) D5 to D0 should be fixed to "H" or "L".
64,65	D6/SCL		
60,61	D5		
56,57	D4		
52,53	D3		
48,49	D2		
44,45	D1		
40,41	D0		

No.	SYMBOL	I/O	FUNCTION
319 to 574	SEG0~ SEG255	Output	Segment Drivers Segment drivers output an one level from VLCD, V2, V3 and VSS.
264 to 311, 581 to 628	COM0~ COM95	Output	Common Drivers Common drivers output an one level from VLCD, V1, V4 and VSS.
629,312	COMMK0, COMMK1	Output	Common Drivers for Icons
4	TESTOUT	Output	For Testing
-	DUMMYx	-	Dummy PAD Dummy x is normally open.

■ FUNCTION DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel / Serial Interface Mode

The PS selects a parallel or a serial interface mode, as shown in Table 1.

Table 1 Selection of Parallel / Serial Interface Mode

PS	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D7~D0
L	Serial I/F	CSb	RS	-	WRb	-	SDA	SCL	-

Note) "-" : Fix to "H" or "L"

(1-2) Data Recognition

The data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb(RW) signals, as shown in Table 2.

Table 2 Data Recognition

Function	RS	68-series	80-series		Serial
		RW	RDb	WRb	RW
Read Instruction	0	1	0	1	1
Write Instruction	0	0	1	0	0
Read Display Data	1	1	0	1	1
Write display Data	1	0	1	0	0

(1-3) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 3.

Table 3 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	RW	D7~D0
L	80-series MPU	CSb	RS	RDb	WRb	D7~D0

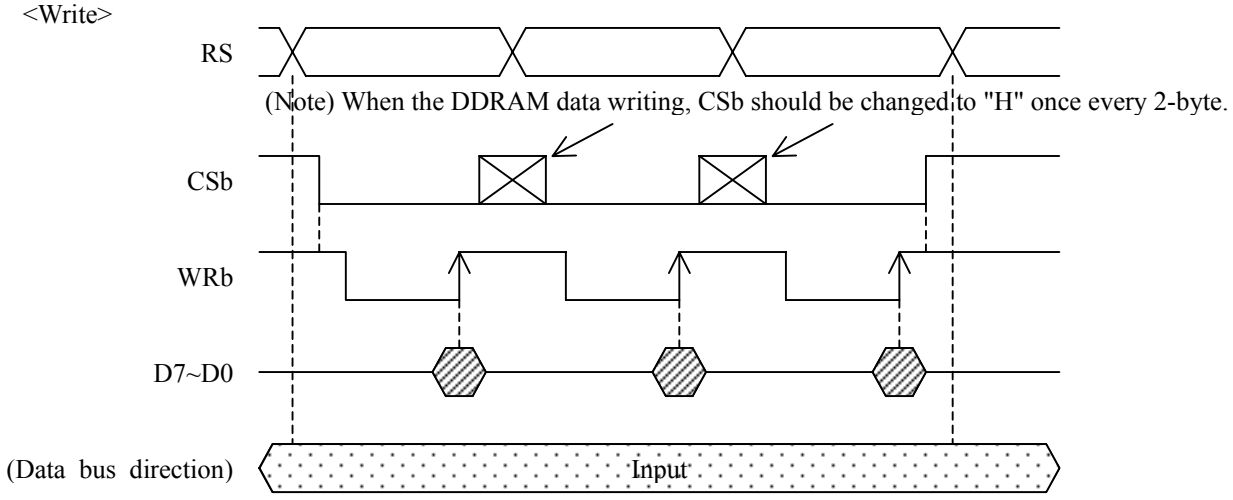
When the CSb signal is “H”, the interface is reset. The data of one character is processed by writing two times. In the DDRAM data writing, CSb is required to change to “H” once every two times. Because, it is recognized as upper 1-byte after CSb is changed from “H” to “L”.

The data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

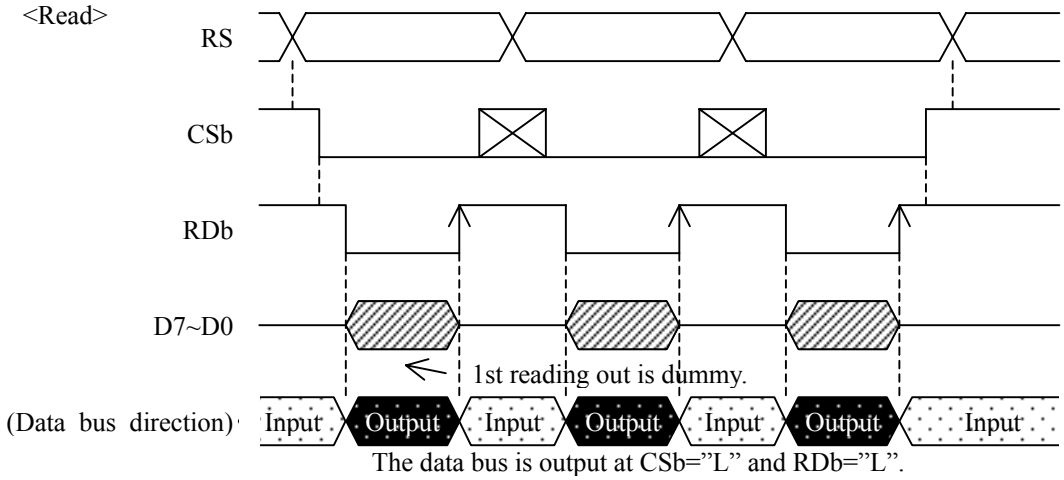
In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. Therefore a dummy data is read out by the 1st “Display Data Read” instruction. After that, the display data is read out from a specified address by the 2nd instruction. When the RS switches, it should be CSb="H".

- 80-series parallel data transmission (PS=”H”, SEL68=”L”)

<Write>



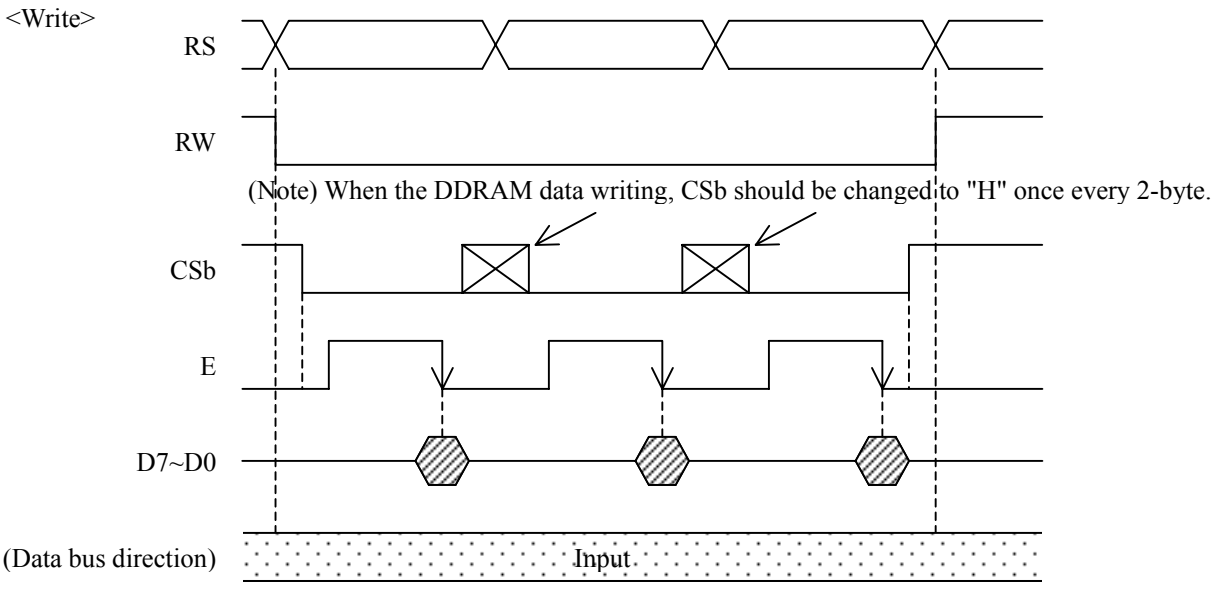
<Read>



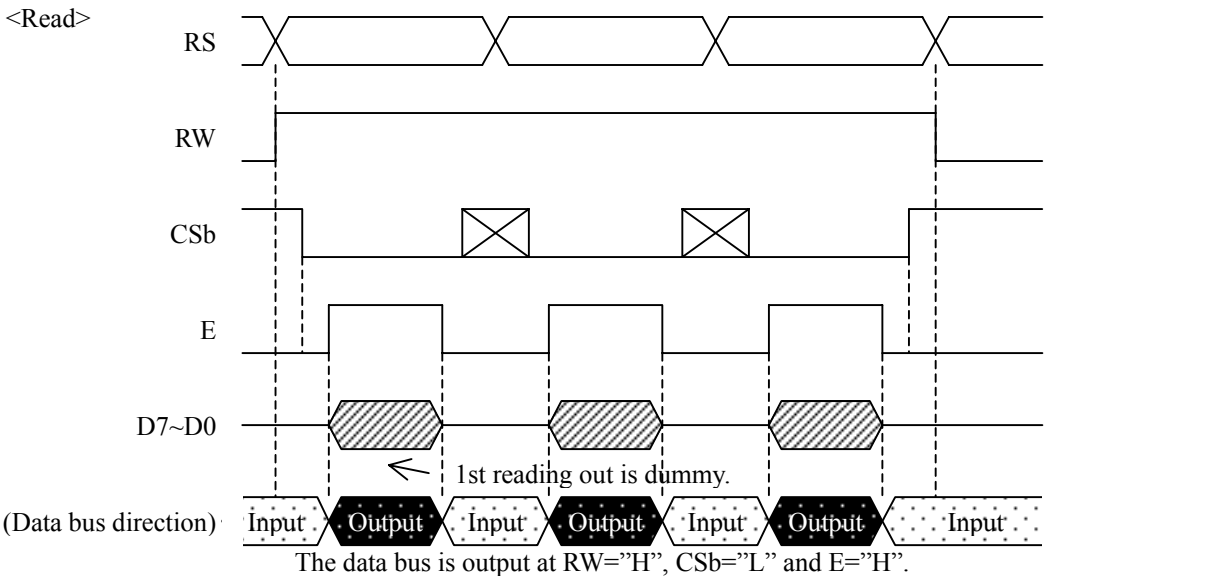
The data bus is output at CSb=”L” and RDb=”L”.

• 68-series parallel data transmission (PS="H", SEL68="H")

<Write>



<Read>



The data bus is output at RW="H", CSb="L" and E="H".

(1-4) Serial Interface

The serial interface is transmitted with 5-line. While the chip select is active (CSb="L"), the SDA and SCL are enabled. While the chip select is inactive (CSb="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. The data is interpreted as writes or reads according to the RS.

8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D7, D6,…, and D0, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

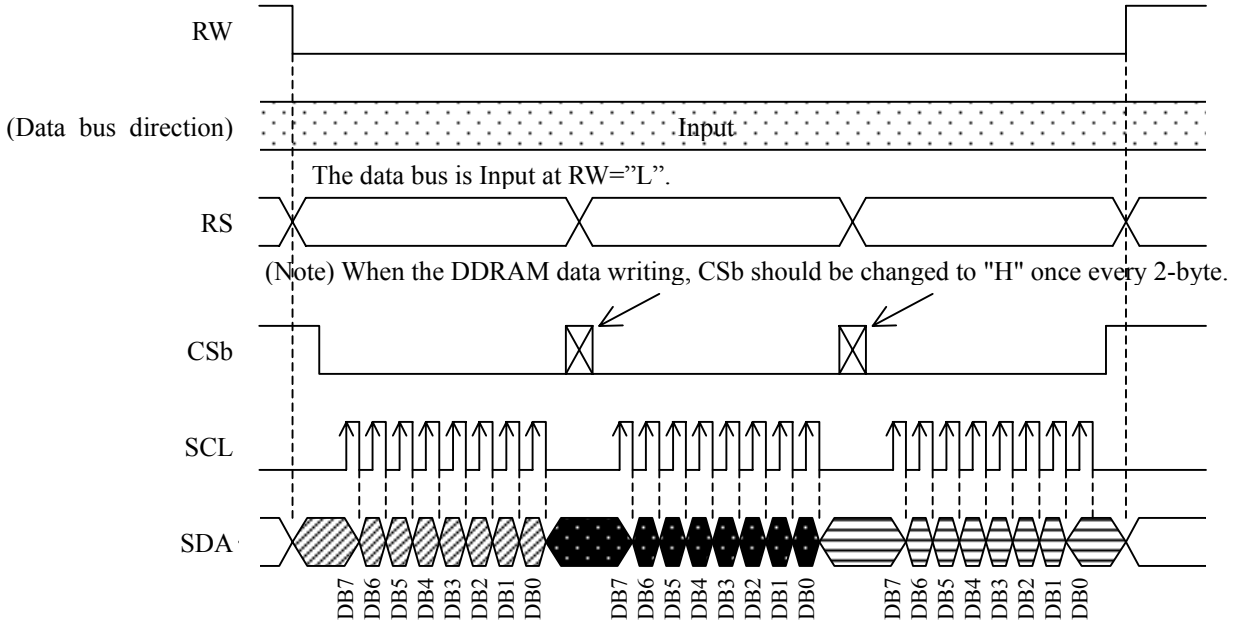
When the CSb signal is "H", the interface is reset. The data of 1-character is processed by writing 2-byte. In the DDRAM data writing, CSb is required to change to "H" once every 2-bytes. Because, it is recognized as 1-byte after CSb is changed from "H" to "L".

Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions.

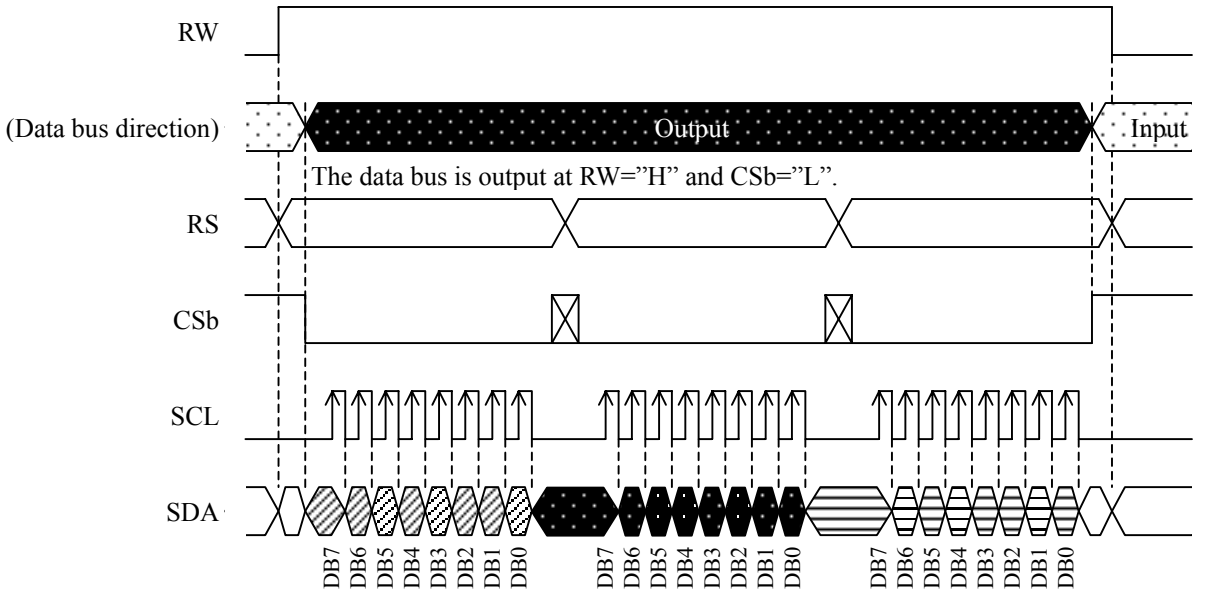
In the read mode, selected address RAM data is read out after 1-dummy as for parallel interface. When the RS and RW switches, it should be CSb="H".

• Serial data transmission (PS="L")

<Write>



<Read>



(2) ADDRESS COUNTER

The NJU6645 has the address counter of 12-bit for read/write of RAM data. The address is set by "RAM address set" instruction. In case of the RDM="0", the address is incremented after the RAM data writing and reading. In case of the RDM="1", the address is incremented only after the RAM data writing. The address doesn't change after the RAM data reading.

The address shifts as follows within range of the address DDRAM, MKRAM, and CGRAM. The DDRAM address shifts in each line.

DDRAM (1-line) : (000)H → (001)H → --- → (01F)H → (000)H
DDRAM (2-line) : (020)H → (021)H → --- → (03F)H → (020)H
DDRAM (3-line) : (040)H → (041)H → --- → (05F)H → (040)H
DDRAM (4-line) : (060)H → (061)H → --- → (07F)H → (060)H
DDRAM (5-line) : (080)H → (081)H → --- → (09F)H → (080)H
DDRAM (6-line) : (0A0)H → (0A1)H → --- → (0BF)H → (0A0)H
MKRAM : (100)H → (101)H → --- → (13F)H → (100)H
CGRAM : (200)H → (201)H → --- → (DFF)H → (200)H

The address is shifted to +1 or -1 by "address shift (ARL)" instruction. When ARL="0" is input, whenever it is input the address is shifted -1. When ARL="1" is input, whenever it is input the address is shifted +1. The address shifts as follows within range of the address DDRAM, MKRAM and CGRAM.

DDRAM (1-line) : (000)H ↔ (001)H ↔ --- ↔ (01F)H ↔ (000)H
DDRAM (2-line) : (020)H ↔ (021)H ↔ --- ↔ (03F)H ↔ (020)H
DDRAM (3-line) : (040)H ↔ (041)H ↔ --- ↔ (05F)H ↔ (040)H
DDRAM (4-line) : (060)H ↔ (061)H ↔ --- ↔ (07F)H ↔ (060)H
DDRAM (5-line) : (080)H ↔ (081)H ↔ --- ↔ (09F)H ↔ (080)H
DDRAM (6-line) : (0A0)H ↔ (0A1)H ↔ --- ↔ (0BF)H ↔ (0A0)H
MKRAM : (100)H ↔ (101)H ↔ --- ↔ (13F)H ↔ (100)H
CGRAM : (200)H ↔ (201)H ↔ --- ↔ (DFF)H ↔ (200)H

(3) DATA RAM

(3-1) RAM Address Map

Display Data RAM (DDRAM), Character Generator RAM(CGRAM), and Icon Data RAM(MKRAM) are stored at the following addresses. The address is set in the address counter by "RAM address set" instruction.

RAM Address Map

RAM ADDRESS – LOWER 8bit	RAM ADDRESS – UPPER 4bit																															
	0H											1H								2H								---	DH								EH	FH
	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0		
00H																																					*	*
01H																																					*	*
02H																																					*	*
03H																																					*	*
⋮																																					*	*
⋮																																					*	*
3EH																																					*	*
3FH																																					*	*
40H												*	*	*	*	*	*	*	*																	*	*
⋮												*	*	*	*	*	*	*	*																	*	*
⋮												*	*	*	*	*	*	*	*																	*	*
BEH												*	*	*	*	*	*	*	*																	*	*
BFH												*	*	*	*	*	*	*	*																	*	*
C0H	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																	*	*
⋮	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																	*	*
⋮	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																	*	*
FEH	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																	*	*
FFH	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*																	*	*

DDRAM address (1 address = 11-bit)

MKRAM address (1 address = 7-bit)

CGRAM address (1 address = 8-bit)

--- DDRAM (Display Data RAM)

--- MKRAM (Icon RAM)

--- CGRAM (Character Generator RAM)

* : Invalid Data

(3-2) DDRAM

Display Data RAM (DDRAM) is RAM that memorizes the attribute display data, data for the capital letters and small letters distinction, and the character-code data. RAM address uses "000H" ~ "0BFH ". The RAM Capacity has 192 addresses of 11-bit/address. At this time, the full-size data is using 2 addresses for a character, and the half-size data is using one address for a character. In the DDRAM address and the position where the panel is displayed, there are relations of the following.

Correspondence of display position on panel and DDRAM address (SEL1="0", SEL2="0")

	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F
2-line	020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F	030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F
3-line	040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F	050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F
4-line	060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F	070	071	072	073	074	075	076	077	078	079	07A	07B	07C	07D	07E	07F
5-line	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
6-line	0A0	0A1	0A2	0A3	0A4	0A5	0A6	0A7	0A8	0A9	0AA	0AB	0AC	0AD	0AE	0AF	0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF

Correspondence of display position on panel and DDRAM address (SEL1="1", SEL2="0")

	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	0A0	0A1	0A2	0A3	0A4	0A5	0A6	0A7	0A8	0A9	0AA	0AB	0AC	0AD	0AE	0AF	0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF
2-line	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
3-line	060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F	070	071	072	073	074	075	076	077	078	079	07A	07B	07C	07D	07E	07F
4-line	040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F	050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F
5-line	020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F	030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F
6-line	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F

Correspondence of display position on panel and DDRAM address (SEL1="0", SEL2="1")

	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	01F	01E	01D	01C	01B	01A	019	018	017	016	015	014	013	012	011	010	00F	00E	00D	00C	00B	00A	009	008	007	006	005	004	003	002	001	000
2-line	03F	03E	03D	03C	03B	03A	039	038	037	036	035	034	033	032	031	030	02F	02E	02D	02C	02B	02A	029	028	027	026	025	024	023	022	021	020
3-line	05F	05E	05D	05C	05B	05A	059	058	057	056	055	054	053	052	051	050	04F	04E	04D	04C	04B	04A	049	048	047	046	045	044	043	042	041	040
4-line	07F	07E	07D	07C	07B	07A	079	078	077	076	075	074	073	072	071	070	06F	06E	06D	06C	06B	06A	069	068	067	066	065	064	063	062	061	060
5-line	09F	09E	09D	09C	09B	09A	099	098	097	096	095	094	093	092	091	090	08F	08E	08D	08C	08B	08A	089	088	087	086	085	084	083	082	081	080
6-line	0BF	0BE	0BD	0BC	0BB	0BA	0B9	0B8	0B7	0B6	0B5	0B4	0B3	0B2	0B1	0B0	0AF	0AE	0AD	0AC	0AB	0AA	0A9	0A8	0A7	0A6	0A5	0A4	0A3	0A2	0A1	0A0

Correspondence of display position on panel and DDRAM address (SEL1="1", SEL2="1")

	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	0BF	0BE	0BD	0BC	0BB	0BA	0B9	0B8	0B7	0B6	0B5	0B4	0B3	0B2	0B1	0B0	0AF	0AE	0AD	0AC	0AB	0AA	0A9	0A8	0A7	0A6	0A5	0A4	0A3	0A2	0A1	0A0
2-line	09F	09E	09D	09C	09B	09A	099	098	097	096	095	094	093	092	091	090	08F	08E	08D	08C	08B	08A	089	088	087	086	085	084	083	082	081	080
3-line	07F	07E	07D	07C	07B	07A	079	078	077	076	075	074	073	072	071	070	06F	06E	06D	06C	06B	06A	069	068	067	066	065	064	063	062	061	060
4-line	05F	05E	05D	05C	05B	05A	059	058	057	056	055	054	053	052	051	050	04F	04E	04D	04C	04B	04A	049	048	047	046	045	044	043	042	041	040
5-line	03F	03E	03D	03C	03B	03A	039	038	037	036	035	034	033	032	031	030	02F	02E	02D	02C	02B	02A	029	028	027	026	025	024	023	022	021	020
6-line	01F	01E	01D	01C	01B	01A	019	018	017	016	015	014	013	012	011	010	00F	00E	00D	00C	00B	00A	009	008	007	006	005	004	003	002	001	000

Note) The DDRAM is not initialized after the power supply turns on, therefore it is necessary to execute the "Display Clear instruction" at first.

(3-3) CGRAM

The character generator RAM (CG RAM) stores any kinds of character pattern written by the user program to display user's original character pattern. RAM address uses "200H" to "DFFH". The CG RAM is able to store character of 5 x 8 dot for 4 kinds. Data "1" correspond to selection as a display, and Data "0" correspond to non-selection as a display. When the character pattern stored in CGRAM is displayed, "0100H" to "015FH" of the character-code is written in DDRAM. The following tables show the relation between the CGRAM address, data, and the displayed pattern.

Correspondence of character code and CGRAM address

	"0100"		"0101"		"0102"		"0103"		"0104"		"0105"		"0106"		"0107"		"0108"		"0109"		"010A"		"010B"		"010C"		"010D"		"010E"		"010F"	
CG Address	200	210	220	230	240	250	260	270	280	290	2A0	2B0	2C0	2D0	2E0	2F0	300	310	320	330	340	350	360	370	380	390	3A0	3B0	3C0	3D0	3E0	3F0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	20F	21F	22F	23F	24F	25F	26F	27F	28F	29F	2AF	2BF	2CF	2DF	2EF	2FF	30F	31F	32F	33F	34F	35F	36F	37F	38F	39F	3AF	3BF	3CF	3DF	3EF	3FF

	"0110"		"0111"		"0112"		"0113"		"0114"		"0115"		"0116"		"0117"		"0118"		"0119"		"011A"		"011B"		"011C"		"011D"		"011E"		"011F"	
CG Address	400	410	420	430	440	450	460	470	480	490	4A0	4B0	4C0	4D0	4E0	4F0	500	510	520	530	540	550	560	570	580	590	5A0	5B0	5C0	5D0	5E0	5F0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	40F	41F	42F	43F	44F	45F	46F	47F	48F	49F	4AF	4BF	4CF	4DF	4EF	4FF	50F	51F	52F	53F	54F	55F	56F	57F	58F	59F	5AF	5BF	5CF	5DF	5EF	5FF

	"0120"		"0121"		"0122"		"0123"		"0124"		"0125"		"0126"		"0127"		"0128"		"0129"		"012A"		"012B"		"012C"		"012D"		"012E"		"012F"	
CG Address	600	610	620	630	640	650	660	670	680	690	6A0	6B0	6C0	6D0	6E0	6F0	700	710	720	730	740	750	760	770	780	790	7A0	7B0	7C0	7D0	7E0	7F0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	60F	61F	62F	63F	64F	65F	66F	67F	68F	69F	6AF	6BF	6CF	6DF	6EF	6FF	70F	71F	72F	73F	74F	75F	76F	77F	78F	79F	7AF	7BF	7CF	7DF	7EF	7FF

	"0130"		"0131"		"0132"		"0133"		"0134"		"0135"		"0136"		"0137"		"0138"		"0139"		"013A"		"013B"		"013C"		"013D"		"013E"		"013F"	
CG Address	800	810	820	830	840	850	860	870	880	890	8A0	8B0	8C0	8D0	8E0	8F0	900	910	920	930	940	950	960	970	980	990	9A0	9B0	9C0	9D0	9E0	9F0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	80F	81F	82F	83F	84F	85F	86F	87F	88F	89F	8AF	8BF	8CF	8DF	8EF	8FF	90F	91F	92F	93F	94F	95F	96F	97F	98F	99F	9AF	9BF	9CF	9DF	9EF	9FF

	"0140"		"0141"		"0142"		"0143"		"0144"		"0145"		"0146"		"0147"		"0148"		"0149"		"014A"		"014B"		"014C"		"014D"		"014E"		"014F"	
CG Address	A00	A10	A20	A30	A40	A50	A60	A70	A80	A90	AA0	AB0	AC0	AD0	AE0	AF0	B00	B10	B20	B30	B40	B50	B60	B70	B80	B90	BA0	BB0	BC0	BD0	BE0	BF0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	A0F	A1F	A2F	A3F	A4F	A5F	A6F	A7F	A8F	A9F	AAF	ABF	ACF	ADF	AEF	AFF	B0F	B1F	B2F	B3F	B4F	B5F	B6F	B7F	B8F	B9F	BAF	BBF	BCF	BDF	BEF	BFF

	"0150"		"0151"		"0152"		"0153"		"0154"		"0155"		"0156"		"0157"		"0158"		"0159"		"015A"		"015B"		"015C"		"015D"		"015E"		"015F"	
CG Address	C00	C10	C20	C30	C40	C50	C60	C70	C80	C90	CA0	CB0	CC0	CD0	CE0	CF0	D00	D10	D20	D30	D40	D50	D60	D70	D80	D90	DA0	DB0	DC0	DD0	DE0	DF0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	C0F	C1F	C2F	C3F	C4F	C5F	C6F	C7F	C8F	C9F	CAF	CBF	CCF	CDF	CEF	CFF	D0F	D1F	D2F	D3F	D4F	D5F	D6F	D7F	D8F	D9F	DAF	DBF	DCF	DDF	DEF	DFF

Relation between the CGRAM address, data, and the displayed pattern

Character Code =”0100” (DDRAM Data)																	
		Upper Address 8bit=20H								Upper Address 8bit=21H							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Lower Address 4bit	0H	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
	1H	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
	2H	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
	3H	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	4H	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
	5H	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
	6H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	7H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	9H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	AH	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
	BH	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
	CH	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	DH	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
	EH	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
	FH	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Character Code =”0101” (DDRAM Data)																	
		Upper Address 8bit=22H								Upper Address 8bit=23H							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Lower Address 4bit	0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1H	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
	2H	0	0	1	1	1	1	1	0	0	1	1	1	1	1	0	0
	3H	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0
	4H	0	1	1	1	1	0	1	0	0	1	1	1	1	1	1	0
	5H	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	6H	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	7H	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	8H	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	9H	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	AH	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	BH	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	CH	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	DH	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
	EH	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
	FH	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Character Code =”0110” (DDRAM Data)																	
		Upper Address 8bit=40H								Upper Address 8bit=41H							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Lower Address 4bit	0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1H	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0
	2H	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
	3H	0	0	0	0	1	1	1	0	0	1	1	1	0	0	0	0
	4H	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
	5H	0	0	1	1	1	1	1	0	0	1	1	1	1	1	0	0
	6H	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	7H	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1
	8H	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1
	9H	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
	AH	0	0	1	1	1	1	1	0	0	1	1	1	1	1	0	0
	BH	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
	CH	0	0	0	0	1	1	1	0	0	1	1	1	0	0	0	0
	DH	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
	EH	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0
	FH	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note) The CGRAM is not initialized after the power supply turns on, therefore it is necessary to write data into CGRAM before display on.

(3-4) MKRAM

The icon display generator RAM (MK RAM) is RAM that stores 512 output ON/OFF settings. RAM address uses "100H" to "13FH". By storing data in this RAM, ON/OFF of each icon is set. Data "1" correspond to selection as a display, and Data "0" correspond to non-selection as a display.

Correspondence of SEG/COM terminals and MKRAM address (SEL1="0", SEL2="0")

	SEG																															
	0 : 7	8 : 15	16 : 23	24 : 31	32 : 39	40 : 47	48 : 55	56 : 63	64 : 71	72 : 79	80 : 87	88 : 95	96 : 103	104 : 111	112 : 119	120 : 127	128 : 135	136 : 143	144 : 151	152 : 159	160 : 167	168 : 175	176 : 183	184 : 191	192 : 199	200 : 207	208 : 215	216 : 223	224 : 231	232 : 239	240 : 247	248 : 255
MK COM0	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
MK COM1	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F

Correspondence of SEG/COM terminals and each bit of MKRAM address (SEL1="0", SEL2="0")

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	---	SEG248	SEG249	SEG250	SEG251	SEG252	SEG253	SEG254	SEG255
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
MK COM0		Address=100H								Address=101H								Address=102H								Address=103H							---		Address=11FH						
MK COM1		Address=120H								Address=121H								Address=122H								Address=123H							---		Address=13FH						

Note) The MKRAM is not initialized after the power supply turns on, therefore it is necessary to write data into CGRAM before display on.

Note) Correspondence to the SEG/COM terminals are changed by the "Driver Output Control instruction" (SEL1, SEL2). Refer to "(9) COMMON SHIFT DIRECTION / SEGMENT OUTPUT DIRECTION" for details.

Note) When the "Display Control instruction" is ALLON="1", display is all ON regardless of the content of RAM.

(3-5) FCGROM (Full-size font ROM)

Full-size font character generator ROM (FCGROM) generates 16 x 16 dots character pattern represented in 14-bit character codes. The NJU6645 has the Full-size font pattern of 8,128-font such as the JIS level-1, level-2 and non-kanji. Refer to "(14) Full-size / Half-size Font Mix Display" for the correspondence of the JIS code and the character code set to DDRAM.

(3-6) HCGROM (Half-size font ROM)

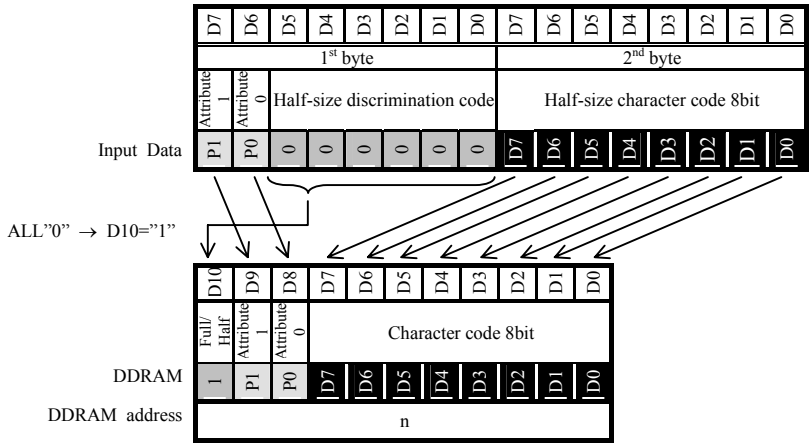
Half-size font character generator ROM (FCGROM) generates 8 x 16 dots character pattern represented in 8-bit character codes. The NJU6645 has the Half-size font pattern of 256-font. Refer to "(14) Full-size / Half-size Font Mix Display" for the correspondence of the character code set to DDRAM.

(3-7) Correspondence of the JIS Code, Input Data, RAM Data and RAM Address

(3-7-1) Write Data to DDRAM

(i) Half-size font character

The half-size data becomes the data of one character by the input data of 2-byte, and it is stored at one RAM address. When the lower 6-bit of 1st byte is all "0", it is recognized as half-size data. The attribute data is allocated in upper 2-bit in the 1st input byte. When the half-size font, "1" is stored in the MSB of RAM data as full-size/half-size discrimination bit.



Note) When the full-size character is overwritten by half-size character, the character is displayed unexpected. Therefore, when the full-size character is overwritten by half-size character, it must write two character's equivalent or rewrite all character.

- Prohibited matter

(1) In the 32nd half-size character of each line (right edge) prohibit overwriting the full-size character.

(2) In the only half left of full-size character prohibit overwriting the half-size character.

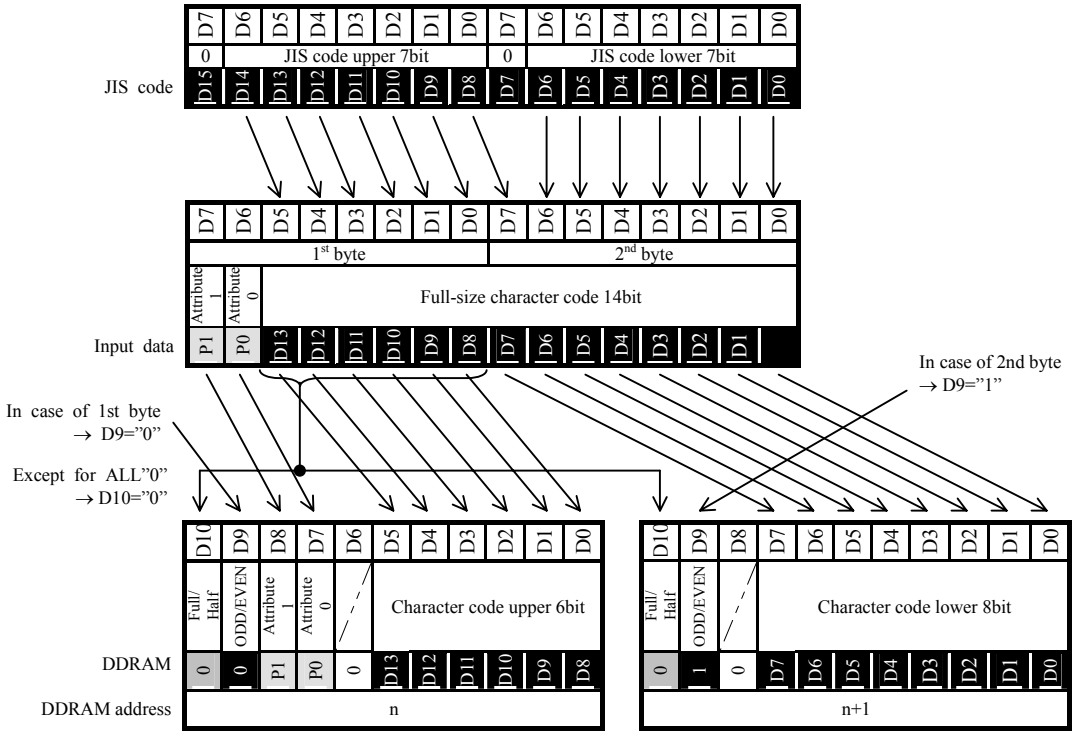
(3) In the only half right of full-size character prohibit overwriting the half-size (full-size) character.

(ii) Full-size font character

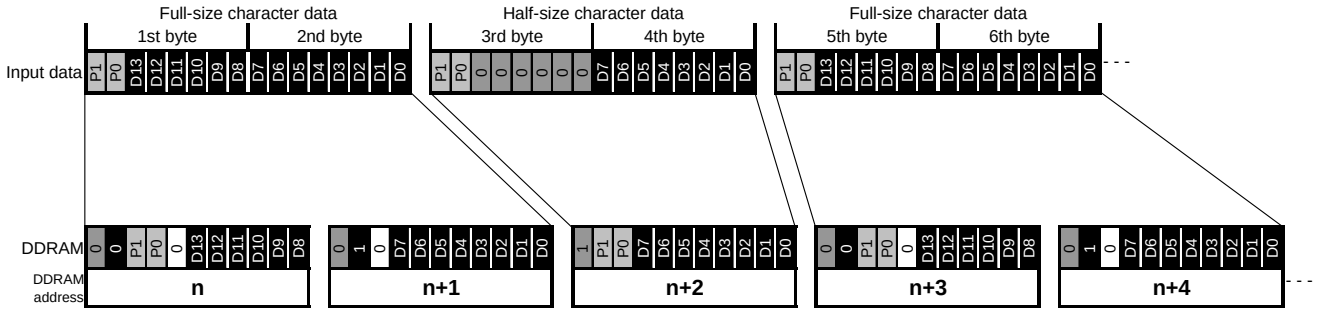
The full-size data becomes the data of 1-character by the input data of 2-byte, and it is stored at two RAM address. The attribute data is allocated in upper 2-bit in the 1st input byte. When the full-size font, “0” is stored in the MSB of RAM data as Full-size/half-size discrimination bit. And, “0” or “1” is stored in the 2nd bit of RAM as 1st byte/2nd byte discrimination data. (1st bit : “0”, 2nd bit : “1”)

The character code is 14-bit stuffed into the lower bit excluding 1-bit (code : ”0”) and 9-bit (code : ”0”) of JIS codes (16-bit).

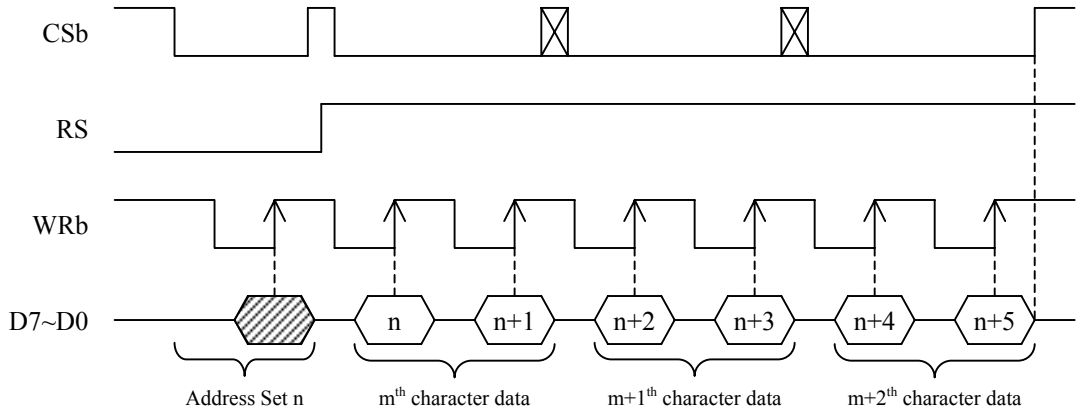
The relation between each bit allocation of JIS code and input data and the RAM is as follows.



When the DDRAM is written, the address is incremented as follows once a 1-byte in case of the full-size data, and once a 2-byte in case of the half-size data.



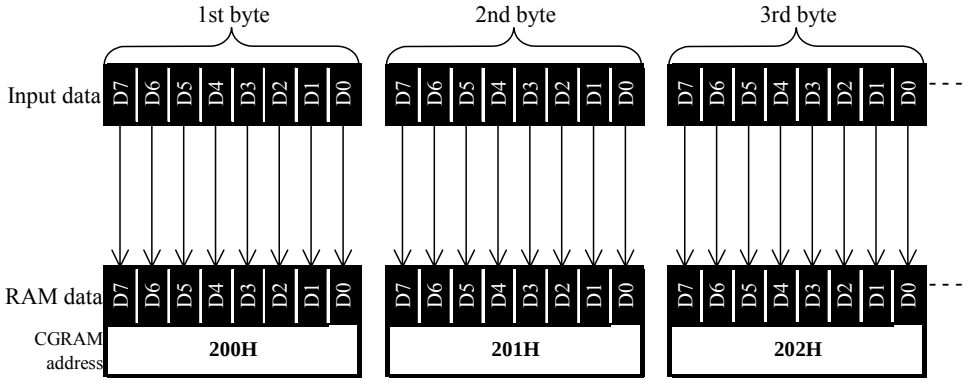
The data is recognized without fail as the first byte, immediately after CSb becomes "L". Therefore, when the DDRAM data is written, it is necessary to make CSb = "H" after it finishes writing the 2nd byte.



(3-7-2) Write Data to CGRAM

The CGRAM has 8-bit per an address, and the input value is stored in each bit as follows. The address is incremented once a 1-byte at the data writing.

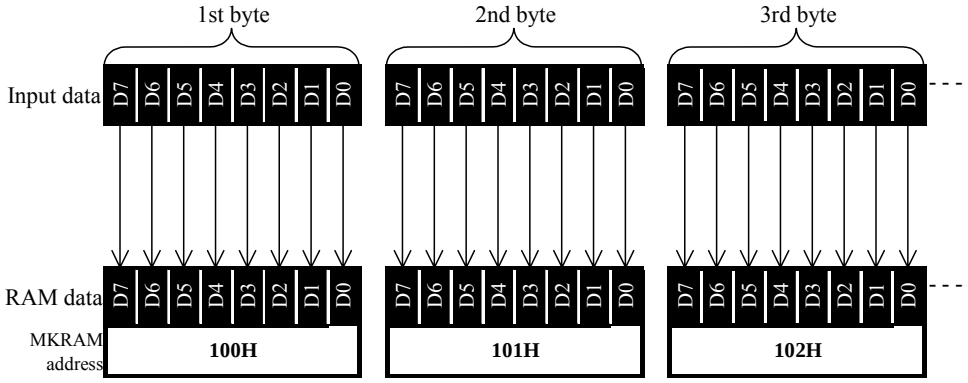
Relation between the interface, RAM data, and RAM address, in the CGRAM data writing



(3-7-3) Write Data to MKRAM

The CGRAM has 8-bit per an address, and the input value is stored in each bit as follows. The address is incremented once a 1-byte at the data writing.

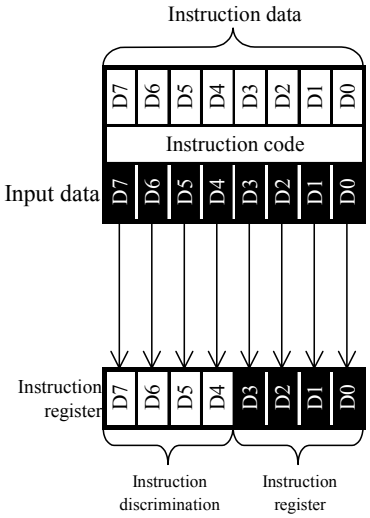
Relation between the interface, RAM data, and RAM address, in the MKRAM data writing



(3-7-4) Write to Instruction Register

The instruction set is stored in the internal instruction register by the 8-bit input in the state of RS="0", RW="0". The instruction code is applied to the item corresponding to the RE register set beforehand. Refer to "(20) Instruction table" for the correspondence of input data and the instruction.

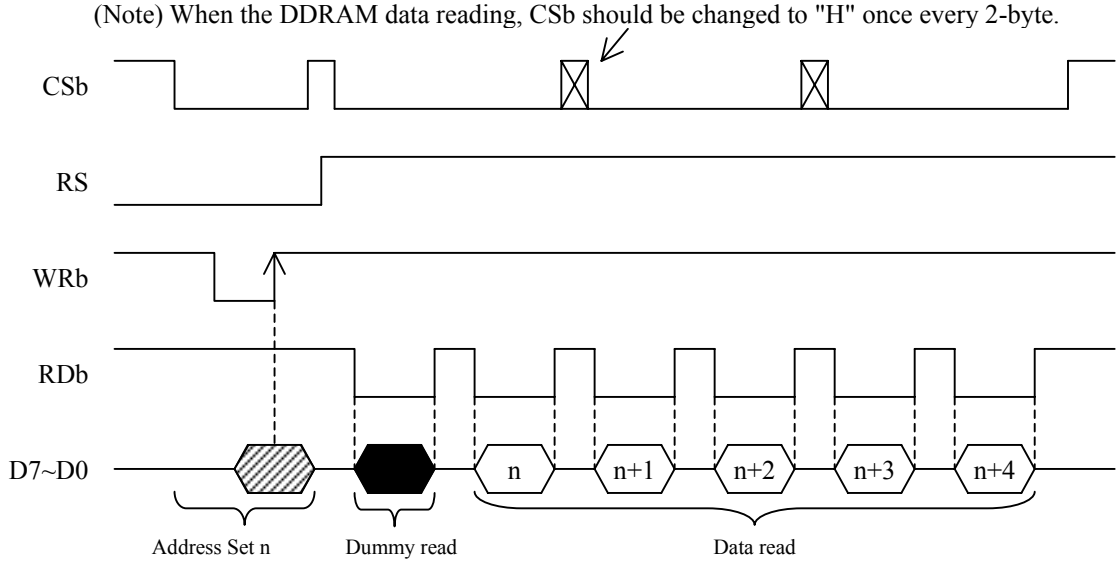
Write to instruction Register



(3-8) Read Data from RAM

The data is read out from DDRAM, CGRAM, and MKRAM. When reading data from the RAM, it is necessary to read after the address setting. The dummy reading is necessary right after the address setting. After read out, the address is incremented automatically according to the entry mode.

(Note) When the DDRAM data reading, CSb should be changed to "H" once every 2-byte.

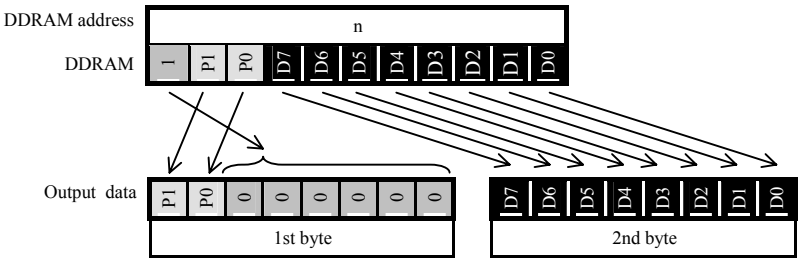


(3-8-1) Read Data from DDRAM

The DDRAM reading discriminates whether the content of the DDRAM data is full-size/half-size, and is output by an input and the same format. The data is recognized without fail as the 1st byte, immediately after CSb becomes “L”. Therefore, when the DDRAM data is read, it is necessary to make CSb = ”H” after it finishes reading the 2nd byte.

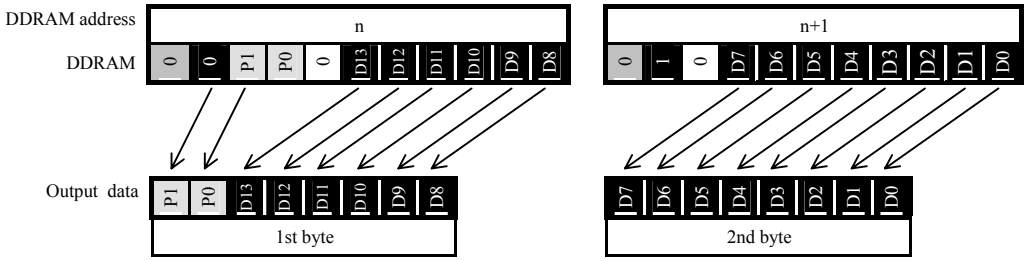
(i) Half-size font character

When the content of DDRAM data is half-size character code, the address data of one address is divided 2-byte. And after read the 2nd byte, the address is incremented according to the entry mode. The 3rd to 8th bit in 1st byte is all output “0”.



(ii) Full-size font character

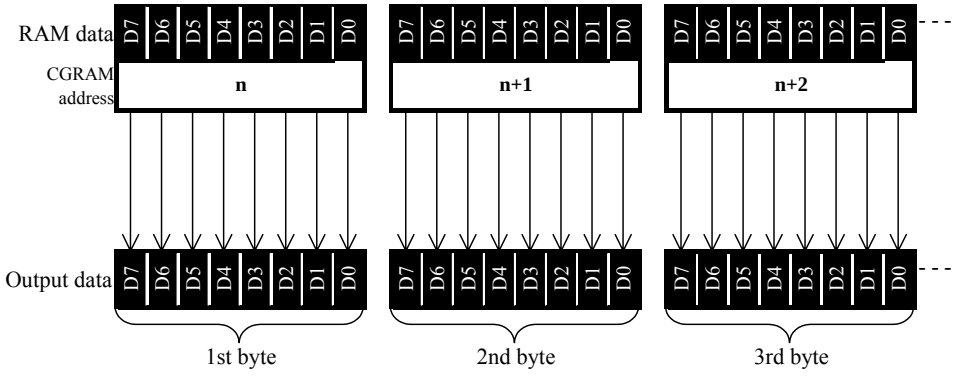
When the content of DDRAM data is full-size character code, the address data of 1-address is read by 1-byte. And after read, the address is incremented according to the entry mode.



(3-8-2) Read Data from CGRAM and MKRAM

The CGRAM and MKRAM read the address data of one address by 1-byte as follows. And after read, the address is incremented according to the entry mode.

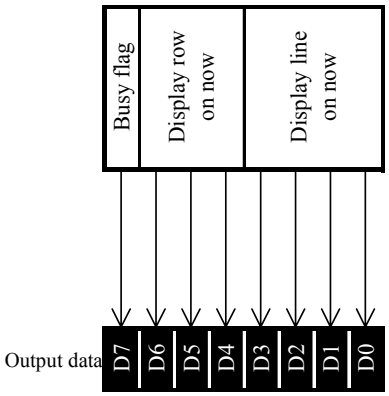
Relation between the interface, RAM data, and RAM address, in the CGRAM and MKRAM data reading



(3-9) Status Read

The status reading is output to the following bits. The dummy reading is not necessary for the status reading. However, the dummy reading is necessary for the status reading at the serial interface.

Status Read



Correspondence Table of Character code and JIS code (ROM version "00")

- 0000 ~ 00FF : Half-size character code (256-character)
- 0100 ~ 015F : CGRAM character code (96-character)
- 10A1 ~ 3A7F : Full-size character code (8064-character)

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000																	
001																	
002		SPACE															
003																	
004																	
005																	
006																	
007																	
008																	
009																	
00A																	
00B																	
00C																	
00D																	
00E																	
00F																	
010																	
011																	
012																	
013																	
014																	
015																	
10A	212		、	。	,	.	・	:	;	?	!	゛	゜	´	`	¨	
10B	213	^	￣	_	ヽ	ヾ	ゝ	ゞ	〃	仝	々	〆	〇	ー	―	‐	／
10C	214	＼	～	∥	｜	…	‥	'	'	"	"	（	）	〔	〕	［	］
10D	215	｛	｝	〈	〉	《	》	「	」	『	』	【	】	＋	－	±	×
10E	216	÷	＝	≠	＜	＞	≦	≧	∞	∴	♂	♀	°	′	″	℃	¥
10F	217	$	¢	£	%	#	&	*	@	§	☆	★	○	●	◎	◇	
112	222		◆	□	■	△	▲	▽	▼	※	〒	→	←	↑	↓	〓	・
113	223	・	・	・	・	・	・	・	・	・	・	∈	∋	⊆	⊇	⊂	⊃
114	224	∪	∩	・	・	・	・	・	・	・	・	∧	∨	¬	⇒	⇔	∀
115	225	∃	・	・	・	・	・	・	・	・	・	・	・	∠	⊥	⌒	∂
116	226	∇	≡	≒	≪	≫	√	∽	∝	∵	∫	∬	・	・	・	・	・
117	227	・	・	Å	‰	#	♭	♪	†	‡	¶	・	・	・	・	○	
11A	232		・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
11B	233	0	1	2	3	4	5	6	7	8	9	・	・	・	・	・	・
11C	234	・	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
11D	235	P	Q	R	S	T	U	V	W	X	Y	Z	・	・	・	・	・
11E	236	・	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
11F	237	p	q	r	s	t	u	v	w	x	y	z	・	・	・	・	
122	242		ぁ	あ	ぃ	い	ぅ	う	ぇ	え	ぉ	お	か	が	き	ぎ	く
123	243	ぐ	け	げ	こ	ご	さ	ざ	し	じ	す	ず	せ	ぜ	そ	ぞ	た
124	244	だ	ち	ぢ	っ	つ	づ	て	で	と	ど	な	に	ぬ	ね	の	は
125	245	ば	ぱ	ひ	び	ぴ	ふ	ぶ	ぷ	へ	べ	ぺ	ほ	ぼ	ぽ	ま	み
126	246	む	め	も	ゃ	や	ゅ	ゆ	ょ	よ	ら	り	る	れ	ろ	ゎ	わ
127	247	ゐ	ゑ	を	ん	・	・	・	・	・	・	・	・	・	・	・	
12A	252		ァ	ア	ィ	イ	ゥ	ウ	ェ	エ	ォ	オ	カ	ガ	キ	ギ	ク
12B	253	グ	ケ	ゲ	コ	ゴ	サ	ザ	シ	ジ	ス	ズ	セ	ゼ	ソ	ゾ	タ
12C	254	ダ	チ	ヂ	ッ	ツ	ヅ	テ	デ	ト	ド	ナ	ニ	ヌ	ネ	ノ	ハ
12D	255	バ	パ	ヒ	ビ	ピ	フ	ブ	プ	ヘ	ベ	ペ	ホ	ボ	ポ	マ	ミ
12E	256	ム	メ	モ	ャ	ヤ	ュ	ユ	ョ	ヨ	ラ	リ	ル	レ	ロ	ヮ	ワ
12F	257	ヰ	ヱ	ヲ	ン	ヴ	ヵ	ヶ	・	・	・	・	・	・	・	・	

Half-size character

CGRAM character code

Note) Refer to "Correspondence Table of Half-size character code and Character pattern" for the half-size character.

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
132	262		Α	Β	Γ	Δ	Ε	Ζ	Η	Θ	Ι	Κ	Λ	Μ	Ν	Ξ	Ο
133	263	Π	Ρ	Σ	Τ	Υ	Φ	Χ	Ψ	Ω	·	·	·	·	·	·	·
134	264	·	α	β	γ	δ	ε	ζ	η	θ	ι	κ	λ	μ	ν	ξ	ο
135	265	π	ρ	σ	τ	υ	φ	χ	ψ	ω	·	·	·	·	·	·	·
136	266	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
137	267	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	
13A	272		А	Б	В	Г	Д	Е	Ё	Ж	З	И	Й	К	Л	М	Н
13B	273	О	П	Р	С	Т	У	Ф	Х	Ц	Ч	Ш	Щ	Ъ	Ы	Ь	Э
13C	274	Ю	Я	·	·	·	·	·	·	·	·	·	·	·	·	·	·
13D	275	·	а	б	в	г	д	е	ё	ж	з	и	й	к	л	м	н
13E	276	о	п	р	с	т	у	ф	х	ц	ч	ш	щ	ъ	ы	ь	э
13F	277	ю	я	·	·	·	·	·	·	·	·	·	·	·	·	·	
142	282		─	│	┌	┐	┘	└	├	┬	┤	┴	┼	━	┃	┏	┓
143	283	┛	┗	┣	┳	┫	┻	╋	┠	┯	┨	┷	┿	┝	┰	┥	┸
144	284	╂	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
145	285	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
146	286	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
147	287	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	
14A	292		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
14B	293	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
14C	294	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
14D	295	P	Q	R	S	T	U	V	W	X	Y	Z	[	¥	]	^	_
14E	296	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
14F	297	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	
152	2A2		。	「	」	、	・	ヲ	ァ	ィ	ゥ	ェ	ォ	ャ	ュ	ョ	ッ
153	2A3	ー	ア	イ	ウ	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ
154	2A4	タ	チ	ツ	テ	ト	ナ	ニ	ヌ	ネ	ノ	ハ	ヒ	フ	ヘ	ホ	マ
155	2A5	ミ	ム	メ	モ	ヤ	ユ	ヨ	ラ	リ	ル	レ	ロ	ワ	ン	゛	゜
156	2A6	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
157	2A7	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	
15A	2B2		·	゛	゜	'	˙	·	·	·	·	·	·	·	·	·	·
15B	2B3	·		‖	·	·	·	·	·	·	·	·	·	ˈ	ˌ	ˈ	·
15C	2B4	·	·	≀	═	─	⋮	:	·	·	·	·	⁀	‿	⁀	‿	‾
15D	2B5	⌐	^	ˇ	≍	≭	¬	⌙	⌑	⌐	⌐	⌙	·	ˈ	·	·	·
15E	2B6	‖	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
15F	2B7	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	
162	2C2		↓	↑	→	←	∎	∣	―	┐	┘	└	┌	┬	┤	┴	├
163	2C3	┼	┃	━	┓	┛	┗	┏	┳	┫	┻	┣	╋	┳	┫	┻	┣
164	2C4	╋	┳	┫	┻	┣	╋	·	·	·	·	·	·	·	·	·	·
165	2C5	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
166	2C6	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
167	2C7	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	
16A	2D2		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮
16B	2D3	⑯	⑰	⑱	⑲	⑳	Ⅰ	Ⅱ	Ⅲ	Ⅳ	Ⅴ	Ⅵ	Ⅶ	Ⅷ	Ⅸ	Ⅹ	·
16C	2D4	ミリ	キロ	センチ	メートル	グラム	トン	アール	ヘクタール	リットル	ワット	カロリー	ドル	セント	パーセント	ミリバール	ページ
16D	2D5	mm	cm	km	mg	kg	cc	m²	·	·	·	·	·	·	·	·	平成
16E	2D6	〃	〃	No.	K.K.	Tel.	㊤	㊥	㊦	㊧	㊨	㊫	㊬	㊭	㊮	㊯	㊰
16F	2D7	≒	≡	∫	∮	Σ	√	⊥	∠	∟	⊿	∵	∩	∪	·	亜	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
172	2E2		あ	・	い	・	う	・	え	・	お	・	・	・	・	・	・
173	2E3	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
174	2E4	・	・	・	ぅ	・	・	ﾘﾐ	ﾛｷ	ﾁｾ	ﾄﾒﾙ	ﾑｸﾗ	ﾝﾄ	ﾙｱｰ	ﾀﾝｸ	ﾄﾘﾙｼﾞ	ﾄﾜｼ
175	2E5	ﾘｶﾛ	ﾙﾄﾞ	ﾄｾﾝ	ｼﾍﾟｲ	ﾍﾐﾙﾘ	ｼﾍﾟｰ	・	・	・	・	・	・	・	・	・	・
176	2E6	・	・	・	ゃ	・	ゆ	・	よ	・	・	・	・	・	・	わ	・
177	2E7	・	・	・	・	・	か	け	・	・	・	・	・	・	・	雛祭	
17A	2F2		ア	・	イ	・	ウ	・	エ	・	オ	・	・	・	・	・	・
17B	2F3	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
17C	2F4	・		・	ッ	・	・	・	・	・	・	・	・	・	・	・	・
17D	2F5	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
17E	2F6	・	・	・	ヤ	・	ユ	・	ヨ	・	・	・	・	・	・	ワ	・
17F	2F7	・	・	・	・	・	カ	ケ	・	・	・	・	・	・	・	・	
182	302		亜	唖	娃	阿	哀	愛	挨	姶	逢	葵	茜	穐	悪	握	渥
183	303	旭	葦	芦	鯵	梓	圧	斡	扱	宛	姐	虻	飴	絢	綾	鮎	或
184	304	粟	袷	安	庵	按	暗	案	闇	鞍	杏	以	伊	位	依	偉	囲
185	305	夷	委	威	尉	惟	意	慰	易	椅	為	畏	異	移	維	緯	胃
186	306	萎	衣	謂	違	遺	医	井	亥	域	育	郁	磯	一	壱	溢	逸
187	307	稲	茨	芋	鰯	允	印	咽	員	因	姻	引	飲	淫	胤	蔭	
18A	312		院	陰	隠	韻	吋	右	宇	烏	羽	迂	雨	卯	鵜	窺	丑
18B	313	碓	臼	渦	嘘	唄	蝿	蔚	鰻	姥	厩	浦	瓜	閏	噂	云	運
18C	314	雲	荏	餌	叡	営	嬰	影	映	曳	栄	永	泳	洩	瑛	盈	穎
18D	315	頴	英	衛	詠	鋭	液	疫	益	駅	悦	謁	越	閲	榎	厭	円
18E	316	園	堰	奄	宴	延	怨	掩	援	沿	演	炎	焔	煙	燕	猿	縁
18F	317	艶	苑	薗	遠	鉛	鴛	塩	於	汚	甥	凹	央	奥	往	応	
192	322		押	旺	横	欧	殴	王	翁	襖	鴬	鴎	黄	岡	沖	荻	億
193	323	屋	憶	臆	桶	牡	乙	俺	卸	恩	温	穏	音	下	化	仮	何
194	324	伽	価	佳	加	可	嘉	夏	嫁	家	寡	科	暇	果	架	歌	河
195	325	火	珂	禍	禾	稼	箇	花	苛	茄	荷	華	菓	蝦	課	嘩	貨
196	326	迦	過	霞	蚊	俄	峨	我	牙	画	臥	芽	蛾	賀	雅	餓	駕
197	327	介	会	解	回	塊	壊	廻	快	怪	悔	恢	懐	戒	拐	改	
19A	332		魁	晦	械	海	灰	界	皆	絵	芥	蟹	開	階	貝	凱	劾
19B	333	外	咳	害	崖	慨	概	涯	碍	蓋	街	該	鎧	骸	浬	馨	蛙
19C	334	垣	柿	蛎	鈎	劃	嚇	各	廓	拡	撹	格	核	殻	獲	確	穫
19D	335	覚	角	赫	較	郭	閣	隔	革	学	岳	楽	額	顎	掛	笠	樫
19E	336	橿	梶	鰍	潟	割	喝	恰	括	活	渇	滑	葛	褐	轄	且	鰹
19F	337	叶	椛	樺	鞄	株	兜	竃	蒲	釜	鎌	噛	鴨	栢	茅	萱	
1A2	342		粥	刈	苅	瓦	乾	侃	冠	寒	刊	勘	勧	巻	喚	堪	姦
1A3	343	完	官	寛	干	幹	患	感	慣	憾	換	敢	柑	桓	棺	款	歓
1A4	344	汗	漢	澗	潅	環	甘	監	看	竿	管	簡	緩	缶	翰	肝	艦
1A5	345	莞	観	諌	貫	還	鑑	間	閑	関	陥	韓	館	舘	丸	含	岸
1A6	346	巌	玩	癌	眼	岩	翫	贋	雁	頑	顔	願	企	伎	危	喜	器
1A7	347	基	奇	嬉	寄	岐	希	幾	忌	揮	机	旗	既	期	棋	棄	
1AA	352		機	帰	毅	気	汽	畿	祈	季	稀	紀	徽	規	記	貴	起
1AB	353	軌	輝	飢	騎	鬼	亀	偽	儀	妓	宜	戯	技	擬	欺	犠	疑
1AC	354	祇	義	蟻	誼	議	掬	菊	鞠	吉	吃	喫	桔	橘	詰	砧	杵
1AD	355	黍	却	客	脚	虐	逆	丘	久	仇	休	及	吸	宮	弓	急	救
1AE	356	朽	求	汲	泣	灸	球	究	窮	笈	級	糾	給	旧	牛	去	居
1AF	357	巨	拒	拠	挙	渠	虚	許	距	鋸	漁	禦	魚	亨	享	京	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1B2	362		供	侠	僑	兇	競	共	凶	協	匡	卿	叫	喬	境	峡	強
1B3	363	彊	怯	恐	恭	挟	教	橋	況	狂	狭	矯	胸	脅	興	蒋	郷
1B4	364	鏡	響	饗	驚	仰	凝	尭	暁	業	局	曲	極	玉	桐	粁	僅
1B5	365	勤	均	巾	錦	斤	欣	欽	琴	禁	禽	筋	緊	芹	菌	衿	襟
1B6	366	謹	近	金	吟	銀	九	倶	句	区	狗	玖	矩	苦	躯	駆	駈
1B7	367	駒	具	愚	虞	喰	空	偶	寓	遇	隅	串	櫛	釧	屑	屈	
1BA	372		掘	窟	沓	靴	轡	窪	熊	隈	粂	栗	繰	桑	鍬	勲	君
1BB	373	薫	訓	群	軍	郡	卦	袈	祁	係	傾	刑	兄	啓	圭	珪	型
1BC	374	契	形	径	恵	慶	慧	憩	掲	携	敬	景	桂	渓	畦	稽	系
1BD	375	経	維	緊	罫	茎	荊	蛍	計	詣	警	軽	頚	鶏	芸	迎	鯨
1BE	376	劇	戟	撃	激	隙	桁	傑	欠	決	潔	穴	結	血	訣	月	件
1BF	377	倹	倦	健	兼	券	剣	喧	圏	堅	嫌	建	憲	懸	拳	捲	
1C2	382		検	権	牽	犬	献	研	県	絹	県	肩	見	謙	賢	軒	遣
1C3	383	鍵	険	顕	験	鹸	元	原	厳	幻	弦	減	源	玄	現	絃	舷
1C4	384	言	諺	限	乎	個	古	呼	固	姑	孤	己	庫	弧	戸	故	枯
1C5	385	湖	狐	糊	袴	股	胡	菰	虎	誇	跨	鈷	雇	顧	鼓	五	互
1C6	386	伍	午	呉	吾	娯	後	御	悟	梧	檎	瑚	碁	語	誤	護	醐
1C7	387	乞	鯉	交	佼	侯	候	倖	光	公	功	効	勾	厚	口	向	
1CA	392		后	喉	坑	垢	好	孔	孝	宏	工	巧	巷	幸	広	庚	康
1CB	393	弘	恒	慌	抗	拘	控	攻	昂	晃	更	杭	校	梗	構	江	洪
1CC	394	浩	港	溝	甲	皇	硬	稿	糠	紅	紘	絞	綱	耕	考	肯	肱
1CD	395	腔	膏	航	荒	行	衡	講	貢	購	郊	酵	鉱	砿	鋼	閤	降
1CE	396	項	香	高	鴻	剛	劫	号	合	壕	拷	濠	豪	轟	麹	克	刻
1CF	397	告	国	穀	酷	鵠	黒	獄	漉	腰	甑	忽	惚	骨	狛	込	
1D2	3A2		此	頃	今	困	坤	墾	婚	恨	懇	昏	昆	根	梱	混	痕
1D3	3A3	紺	艮	魂	些	佐	叉	唆	嵯	左	差	査	沙	瑳	砂	詐	鎖
1D4	3A4	裟	坐	座	挫	債	催	再	最	哉	塞	妻	宰	彩	才	採	栽
1D5	3A5	歳	済	災	采	犀	砕	砦	祭	斎	細	菜	裁	載	際	剤	在
1D6	3A6	材	罪	財	冴	坂	阪	堺	榊	肴	咲	崎	埼	碕	鵠	作	削
1D7	3A7	咋	搾	昨	朔	柵	窄	策	索	錯	桜	鮭	笹	匙	冊	刷	
1DA	3B2		察	拶	撮	擦	札	殺	薩	雑	皐	鯖	捌	錆	鮫	皿	晒
1DB	3B3	三	傘	参	山	惨	撒	散	桟	燦	珊	産	算	纂	蚕	讃	賛
1DC	3B4	酸	餐	斬	暫	残	仕	仔	伺	使	刺	司	史	嗣	四	士	始
1DD	3B5	姉	姿	子	屍	市	師	志	思	指	支	孜	斯	施	旨	枝	止
1DE	3B6	死	氏	獅	祉	私	糸	紙	紫	肢	脂	至	視	詞	詩	試	誌
1DF	3B7	諮	資	賜	雌	飼	歯	事	似	侍	児	字	寺	慈	持	時	
1E2	3C2		次	滋	治	爾	璽	痔	磁	示	而	耳	自	蒔	辞	汐	鹿
1E3	3C3	式	識	鴫	竺	軸	宍	雫	七	叱	執	失	嫉	室	悉	湿	漆
1E4	3C4	疾	質	実	蔀	篠	偲	柴	芝	屡	蕊	縞	舎	写	射	捨	赦
1E5	3C5	斜	煮	社	紗	者	謝	車	遮	蛇	邪	借	勺	尺	杓	灼	爵
1E6	3C6	酌	釈	錫	若	寂	弱	惹	主	取	守	手	朱	殊	狩	珠	種
1E7	3C7	腫	趣	酒	首	儒	受	呪	寿	授	樹	綬	需	囚	収	周	
1EA	3D2		宗	就	州	修	愁	拾	洲	秀	秋	終	繍	習	臭	舟	蒐
1EB	3D3	衆	襲	讐	蹴	輯	週	酋	酬	集	醜	什	住	充	十	従	戎
1EC	3D4	柔	汁	洪	獣	縦	重	銃	叔	夙	宿	淑	祝	縮	粛	塾	熟
1ED	3D5	出	術	述	俊	峻	春	瞬	竣	舜	駿	准	循	旬	楯	殉	淳
1EE	3D6	準	潤	盾	純	巡	遵	醇	順	処	初	所	暑	曙	渚	庶	緒
1EF	3D7	署	書	薯	藷	諸	助	叙	女	序	徐	恕	鋤	除	傷	償	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1F2	3E2		勝	匠	升	召	哨	商	唱	嘗	奨	妾	娼	宵	将	小	少
1F3	3E3	尚	庄	床	廠	彰	承	抄	招	掌	捷	昇	昌	昭	晶	松	梢
1F4	3E4	樟	樵	沼	消	渉	湘	焼	焦	照	症	省	硝	礁	祥	称	章
1F5	3E5	笑	粧	紹	肖	菖	蒋	蕉	衝	裳	訟	証	詔	詳	象	賞	醤
1F6	3E6	鉦	鍾	鐘	障	鞘	上	丈	丞	乗	冗	剰	城	場	壌	嬢	常
1F7	3E7	情	擾	条	杖	浄	状	畳	穣	蒸	譲	醸	錠	嘱	埴	飾	
1FA	3F2		拭	植	殖	燭	織	職	色	触	食	蝕	辱	尻	伸	信	侵
1FB	3F3	唇	娠	寝	審	心	慎	振	新	晋	森	榛	浸	深	申	疹	真
1FC	3F4	神	秦	紳	臣	芯	薪	親	診	身	辛	進	針	震	人	仁	刃
1FD	3F5	塵	壬	尋	甚	尽	腎	訊	迅	陣	靭	笥	諏	須	酢	図	厨
1FE	3F6	逗	吹	垂	帥	推	水	炊	睡	粋	翠	衰	遂	酔	錐	錘	随
1FF	3F7	瑞	髄	崇	嵩	数	枢	趨	雛	据	杉	椙	菅	頗	雀	裾	
202	402		澄	摺	寸	世	瀬	畝	是	凄	制	勢	姓	征	性	成	政
203	403	整	星	晴	棲	栖	正	清	牲	生	盛	精	聖	声	製	西	誠
204	404	誓	請	逝	醒	青	静	斉	税	脆	隻	席	惜	戚	斥	昔	析
205	405	石	積	籍	績	脊	責	赤	跡	蹟	碩	切	拙	接	摂	折	設
206	406	窃	節	説	雪	絶	舌	蝉	仙	先	千	占	宣	専	尖	川	戦
207	407	扇	撰	栓	栴	泉	浅	洗	染	潜	煎	煽	旋	穿	箭	線	
20A	412		繊	羨	腺	舛	船	薦	詮	賤	践	選	遷	銭	銑	閃	鮮
20B	413	前	善	漸	然	全	禅	繕	膳	糎	噌	塑	岨	措	曾	曽	楚
20C	414	狙	疏	踈	礎	祖	租	粗	素	組	蘇	訴	阻	遡	鼠	僧	創
20D	415	双	叢	倉	喪	壮	奏	爽	宋	層	匝	惣	想	捜	掃	挿	掻
20E	416	操	早	曹	巣	槍	槽	漕	燥	争	痩	相	窓	糟	総	綜	聡
20F	417	草	荘	葬	蒼	藻	装	走	送	遭	鎗	霜	騒	像	増	憎	
212	422		臓	蔵	贈	造	促	側	則	即	息	捉	束	測	足	速	俗
213	423	属	賊	族	続	卒	袖	其	揃	存	孫	尊	損	村	遜	他	多
214	424	太	汰	詑	唾	堕	妥	惰	打	柁	舵	楕	陀	駄	騨	体	堆
215	425	対	耐	岱	帯	待	怠	態	戴	替	泰	滞	胎	腿	苔	袋	貸
216	426	退	逮	隊	黛	鯛	代	台	大	第	醍	題	鷹	滝	瀧	卓	啄
217	427	宅	托	択	拓	沢	濯	琢	託	鐸	濁	諾	茸	凧	蛸	只	
21A	432		叩	但	達	辰	奪	脱	巽	竪	辿	棚	谷	狸	鱈	樽	誰
21B	433	丹	単	嘆	坦	担	探	旦	歎	淡	湛	炭	短	端	箪	綻	耽
21C	434	胆	蛋	誕	鍛	団	壇	弾	断	暖	檀	段	男	談	値	知	地
21D	435	弛	恥	智	池	痴	稚	置	致	蜘	遅	馳	築	畜	竹	筑	蓄
21E	436	逐	秩	窒	茶	嫡	着	中	仲	宙	忠	抽	昼	柱	注	虫	衷
21F	437	註	酎	鋳	駐	樗	瀦	猪	苧	著	貯	丁	兆	凋	喋	寵	
222	442		帖	帳	庁	弔	張	彫	徴	懲	挑	暢	朝	潮	牒	町	眺
223	443	聴	脹	腸	蝶	調	諜	超	跳	銚	長	頂	鳥	勅	捗	直	朕
224	444	沈	珍	賃	鎮	陳	津	墜	椎	槌	追	鎚	痛	通	塚	栂	掴
225	445	槻	佃	漬	柘	辻	蔦	綴	鍔	椿	潰	坪	壷	嬬	紬	爪	吊
226	446	釣	鶴	亭	低	停	偵	剃	貞	呈	堤	定	帝	底	庭	廷	弟
227	447	悌	抵	挺	提	梯	汀	碇	禎	程	締	艇	訂	諦	蹄	逓	
22A	452		邸	鄭	釘	鼎	泥	摘	擢	敵	滴	的	笛	適	鏑	溺	哲
22B	453	徹	撤	轍	迭	鉄	典	填	天	展	店	添	纏	甜	貼	転	顛
22C	454	点	伝	殿	澱	田	電	兎	吐	堵	塗	妬	屠	徒	斗	杜	渡
22D	455	登	菟	賭	途	都	鍍	砥	砺	努	度	土	奴	怒	倒	党	冬
22E	456	凍	刀	唐	塔	塘	套	宕	島	嶋	悼	投	搭	東	桃	梼	棟
22F	457	盗	淘	湯	涛	灯	燈	当	痘	祷	等	答	筒	糖	統	到	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
232	462		葷	蕩	藏	討	謄	豆	踏	逃	透	鐙	陶	頭	騰	闘	働
233	463	動	同	堂	導	憧	撞	洞	瞳	童	胴	萄	道	銅	峠	鴇	匿
234	464	得	徳	涜	特	督	禿	篤	毒	独	読	栃	橡	凸	突	椴	届
235	465	豚	吶	寅	酉	瀞	噸	屯	惇	敦	沌	豚	遁	頓	呑	曇	鈍
236	466	奈	那	内	乍	凪	薙	謎	灘	捺	鍋	楢	馴	縄	暖	南	楠
237	467	軟	難	汝	二	尼	弐	迩	匂	賑	肉	虹	廿	日	乳	入	
23A	472		如	尿	韮	任	妊	忍	認	濡	禰	祢	寧	葱	猫	熱	年
23B	473	念	捻	撚	燃	粘	乃	廼	之	埜	嚢	悩	濃	納	能	脳	膿
23C	474	農	覗	蚤	巴	把	播	覇	杷	波	派	琶	破	婆	罵	芭	馬
23D	475	俳	廃	拝	排	敗	杯	盃	牌	背	肺	輩	配	倍	培	媒	梅
23E	476	楳	煤	狽	買	売	賠	陪	這	蝿	秤	矧	萩	伯	剥	博	拍
23F	477	柏	泊	白	箔	粕	舶	薄	迫	曝	漠	爆	縛	莫	駁	麦	
242	482		函	箱	硲	箸	肇	筈	櫨	幡	肌	畑	畠	八	鉢	溌	発
243	483	醗	髪	伐	罰	抜	筏	閥	鳩	噺	塙	蛤	隼	伴	判	半	反
244	484	叛	帆	搬	斑	板	氾	汎	版	犯	班	畔	繁	般	藩	販	範
245	485	采	煩	頒	飯	挽	晩	番	盤	磐	蕃	蛮	匪	卑	否	妃	庇
246	486	彼	悲	扉	批	披	斐	比	泌	疲	皮	碑	秘	緋	罷	肥	被
247	487	誹	費	避	非	飛	樋	簸	備	尾	微	枇	毘	琵	眉	美	
24A	492		鼻	柊	稗	匹	疋	髭	彦	膝	菱	肘	弼	必	畢	筆	逼
24B	493	桧	姫	媛	紐	百	謬	俵	彪	標	氷	漂	瓢	票	表	評	豹
24C	494	廟	描	病	秒	苗	錨	鋲	蒜	蛭	鰭	品	彬	斌	浜	瀕	貧
24D	495	賓	頻	敏	瓶	不	付	埠	夫	婦	富	冨	布	府	怖	扶	敷
24E	496	斧	普	浮	父	符	腐	膚	芙	譜	負	賦	赴	阜	附	侮	撫
24F	497	武	舞	葡	無	部	封	楓	風	葺	蕗	伏	副	復	幅	服	
252	4A2		福	腹	複	覆	淵	弗	払	沸	仏	物	鮒	分	吻	噴	墳
253	4A3	憤	扮	焚	奮	粉	糞	紛	雰	文	聞	丙	併	兵	塀	幣	平
254	4A4	弊	柄	並	蔽	閉	陛	米	頁	僻	壁	癖	碧	別	瞥	蔑	箆
255	4A5	偏	変	片	篇	編	辺	返	遍	便	勉	娩	弁	鞭	保	舗	鋪
256	4A6	圃	捕	歩	甫	補	輔	穂	募	墓	慕	戊	暮	母	簿	菩	倣
257	4A7	俸	包	呆	報	奉	宝	峰	峯	崩	庖	抱	捧	放	方	朋	
25A	4B2		法	泡	烹	砲	縫	胞	芳	萌	蓬	蜂	褒	訪	豊	邦	鋒
25B	4B3	飽	鳳	鵬	乏	亡	傍	剖	坊	妨	帽	忘	忙	房	暴	望	某
25C	4B4	棒	冒	紡	肪	膨	謀	貌	貿	鉾	防	吠	頬	北	僕	卜	墨
25D	4B5	撲	朴	牧	睦	穆	釦	勃	没	殆	堀	幌	奔	本	翻	凡	盆
25E	4B6	摩	磨	魔	麻	埋	妹	昧	枚	毎	哩	槙	幕	膜	枕	鮪	柾
25F	4B7	鱒	桝	亦	俣	又	抹	末	沫	迄	侭	繭	麿	万	慢	満	
262	4C2		漫	蔓	味	未	魅	巳	箕	岬	密	蜜	湊	蓑	稔	脈	妙
263	4C3	粍	民	眠	務	夢	無	牟	矛	霧	鵡	椋	婿	娘	冥	名	命
264	4C4	明	盟	迷	銘	鳴	姪	牝	滅	免	棉	綿	緬	面	麺	摸	模
265	4C5	茂	妄	孟	毛	猛	盲	網	耗	蒙	儲	木	黙	目	杢	勿	餅
266	4C6	尤	戻	籾	貰	問	悶	紋	門	匁	也	冶	夜	爺	耶	野	弥
267	4C7	矢	厄	役	約	薬	訳	躍	靖	柳	薮	鑓	愉	愈	油	癒	
26A	4D2		諭	輸	唯	佑	優	勇	友	宥	幽	悠	憂	揖	有	柚	湧
26B	4D3	涌	猶	猷	由	祐	裕	誘	遊	邑	郵	雄	融	夕	予	余	与
26C	4D4	誉	輿	預	傭	幼	妖	容	庸	揚	揺	擁	曜	楊	様	洋	溶
26D	4D5	熔	用	窯	羊	耀	葉	蓉	要	謡	踊	遙	陽	養	慾	抑	欲
26E	4D6	沃	浴	翌	翼	淀	羅	螺	裸	来	莱	頼	雷	洛	絡	落	酪
26F	4D7	乱	卵	嵐	欄	濫	藍	蘭	覧	利	吏	履	李	梨	理	璃	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
272	4E2		痢	裏	裡	里	離	陸	律	率	立	葎	掠	略	劉	流	溜
273	4E3	琉	留	硫	粒	隆	竜	龍	侶	慮	旅	虜	了	亮	僚	両	凌
274	4E4	寮	料	梁	涼	猟	療	瞭	稜	糧	良	諒	遼	量	陵	領	力
275	4E5	緑	倫	厘	林	淋	燐	琳	臨	輪	隣	鱗	麟	瑠	塁	涙	累
276	4E6	類	令	伶	例	冷	励	嶺	怜	玲	礼	苓	鈴	隷	零	霊	麗
277	4E7	齢	暦	歴	列	劣	烈	裂	廉	恋	憐	漣	煉	簾	練	聯	
27A	4F2		蓮	連	錬	呂	魯	櫓	炉	賂	路	露	労	婁	廊	弄	朗
27B	4F3	楼	榔	浪	漏	牢	狼	篭	老	聾	蝋	郎	六	麓	禄	肋	録
27C	4F4	論	倭	和	話	歪	賄	脇	惑	枠	鷲	亙	亘	鰐	詫	藁	蕨
27D	4F5	椀	湾	碗	腕	・	・	・	・	・	・	・	・	・	・	・	・
27E	4F6	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
27F	4F7	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	
282	502		弌	丐	丕	个	丱	丶	丼	丿	乂	乖	乘	亂	亅	豫	亊
283	503	舒	弍	于	亞	亟	亠	亢	亰	亳	亶	从	仍	仄	仆	仂	仗
284	504	仞	仭	仟	价	伉	佚	估	佛	佝	佗	佇	佶	侈	侏	侘	佻
285	505	佩	佰	侑	佯	來	侖	儘	俔	俟	俎	俘	俛	俑	俚	俐	俤
286	506	俥	倚	倨	倔	倪	倥	倅	伜	俶	倡	倩	倬	俾	俯	們	倆
287	507	偃	假	會	偕	偐	偈	做	偖	偬	偸	傀	傚	傅	傴	傲	
28A	512		僉	僊	傳	僂	僖	僞	僥	僭	僣	僮	價	僵	儉	儁	儂
28B	513	儖	儕	儔	儚	儡	儺	儷	儼	儻	儿	兀	兒	兌	兔	兢	竸
28C	514	兩	兪	兮	冀	冂	囘	册	冉	冏	冑	冓	冕	冖	冤	冦	冢
28D	515	冩	冪	冫	决	冱	冲	冰	况	冽	凅	凉	凛	几	處	凩	凭
28E	516	凰	凵	凾	刄	刋	刔	刎	刧	刪	刮	刳	刹	剏	剄	剋	剌
28F	517	剞	剔	剪	剴	剩	剳	剿	剽	劍	劔	劒	剱	劈	劑	辨	
292	522		辧	劬	劭	劼	劵	勁	勍	勗	勞	勣	勦	飭	勠	勳	勵
293	523	勸	勹	匆	匈	甸	匍	匐	匏	匕	匚	匣	匯	匱	匳	匸	區
294	524	卆	卅	丗	卉	卍	凖	卞	卩	卮	夘	卻	卷	厂	厖	厠	厦
295	525	厥	厮	厰	厶	參	簒	雙	叟	曼	燮	叮	叨	叭	叺	吁	吽
296	526	呀	听	吭	吼	吮	吶	吩	吝	呎	咏	呵	咎	呟	呱	呷	呰
297	527	咒	呻	咀	呶	咄	咐	咆	哇	咢	咸	咥	咬	哄	哈	咨	
29A	532		咫	哂	咤	咾	咼	哘	哥	哦	唏	唔	哽	哮	哭	哺	哢
29B	533	唹	啀	啣	啌	售	啜	啅	啖	啗	唸	唳	啝	喙	喀	咯	喊
29C	534	喟	啻	啾	喘	喞	單	啼	喃	喩	喇	喨	嗚	嗅	嗟	嗄	嗜
29D	535	嗤	嗔	嘔	嗷	嘖	嗾	嗽	嘛	嗹	噎	噐	營	嘴	嘶	嘲	嘸
29E	536	噫	噤	嘯	噬	噪	嚆	嚀	嚊	嚠	嚔	嚏	嚥	嚮	嚶	嚴	囂
29F	537	嚼	囁	囃	囀	囈	囎	囑	囓	囗	囮	囹	圀	囿	圄	圉	
2A2	542		圈	國	圍	圓	團	圖	嗇	圜	圦	圷	圸	坎	圻	址	坏
2A3	543	坩	埀	垈	坡	坿	垉	垓	垠	垳	垤	垪	垰	埃	埆	埔	埒
2A4	544	埓	堊	埖	埣	堋	堙	堝	塲	堡	塢	塋	塰	毀	塒	堽	塹
2A5	545	墅	墹	墟	墫	墺	壞	墻	墸	墮	壅	壓	壑	壗	壙	壘	壥
2A6	546	壜	壤	壟	壯	壺	壹	壻	壼	壽	夂	夊	夐	夛	梦	夥	夬
2A7	547	夭	夲	夸	夾	竒	奕	奐	奎	奚	奘	奢	奠	奧	奬	奩	
2AA	552		奸	妁	妝	佞	侫	妣	妲	姆	姨	姜	妍	姙	姚	娥	娟
2AB	553	娑	娜	娉	娚	婀	婬	婉	娵	娶	婢	婪	媚	媼	媾	嫋	嫂
2AC	554	媽	嫣	嫗	嫦	嫩	嫖	嫺	嫻	嬌	嬋	嬖	嬲	嫐	嬪	嬶	嬾
2AD	555	孃	孅	孀	孑	孕	孚	孛	孥	孩	孰	孳	孵	學	斈	孺	宀
2AE	556	它	宦	宸	寃	寇	寉	寔	寐	寤	實	寢	寞	寥	寫	寰	寶
2AF	557	寳	尅	將	專	對	尓	尠	尢	尨	尸	尹	屁	屆	屎	屓	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2B2	562		屐	屏	孱	屬	屮	乢	屶	屹	岌	岑	岔	妛	岫	岻	岶
2B3	563	岼	岷	峅	岾	峇	峙	峩	峽	峺	峭	嶌	峪	崋	崕	崗	嵜
2B4	564	崟	崛	崑	崔	崢	崚	崙	崘	嵌	嵒	嵎	嵋	嵬	嵳	嵶	嶇
2B5	565	嶄	嶂	嶢	嶝	嶬	嶮	嶽	嶐	嶷	嶼	巉	巍	巓	巒	巖	巛
2B6	566	巫	已	巵	帋	帚	帙	帑	帛	帶	帷	幄	幃	幀	幎	幗	幔
2B7	567	幟	幢	幤	幇	幵	并	幺	麼	广	庠	廁	廂	廈	廐	廏	
2BA	572		廖	廣	廝	廚	廛	廢	廡	廨	廩	廬	廱	廳	廰	廴	廸
2BB	573	廾	弃	弉	彝	彜	弋	弑	弖	弩	弭	弸	彁	彈	彌	彎	弯
2BC	574	彑	彖	彗	彙	彡	彭	彳	彷	徃	徂	彿	徊	很	徑	徇	從
2BD	575	徙	徘	徠	徨	徭	徼	忖	忻	忤	忸	忱	忝	悳	忿	怡	恠
2BE	576	怙	怐	怩	怎	怱	怛	怕	怫	怦	怏	怺	恚	恁	恪	恷	恟
2BF	577	恊	恆	恍	恣	恃	恤	恂	恬	恫	恙	悁	悍	惧	悃	悚	
2C2	582		悄	悛	悖	悗	悒	悧	悋	惡	悸	惠	惓	悴	忰	悽	惆
2C3	583	悵	惘	慍	愕	愆	惶	惷	愀	惴	惺	愃	愡	惻	惱	愍	愎
2C4	584	慇	愾	愨	愧	慊	愿	愼	愬	愴	愽	慂	慄	慳	慷	慘	慙
2C5	585	慚	慫	慴	慯	慥	慱	慟	慝	慓	慵	憙	憖	憇	憬	憔	憚
2C6	586	憊	憑	憫	憮	懌	懊	應	懷	懈	懃	懆	憺	懋	罹	懍	懦
2C7	587	懣	懶	懺	懴	懿	懽	懼	懾	戀	戈	戉	戍	戌	戔	戛	
2CA	592		戞	戡	截	戮	戰	戲	戳	扁	扎	扞	扣	扛	扠	扨	扼
2CB	593	抂	抉	找	抒	抓	抖	拔	抃	抔	拗	拑	抻	拏	拿	拆	擔
2CC	594	拈	拜	拌	拊	拂	拇	抛	拉	挌	拮	拱	挧	挂	挈	拯	拵
2CD	595	捐	挾	捍	搜	捏	掖	掎	掀	掫	捶	掣	掏	掉	掟	掵	捫
2CE	596	捩	掾	揩	揀	揆	揣	揉	插	揶	揄	搖	搴	搆	搓	搦	搶
2CF	597	攝	搗	搨	搏	摧	摯	摶	摎	攪	撕	撓	撥	撩	撈	撼	
2D2	5A2		據	擒	擅	擇	撻	擘	擂	擱	擧	舉	擠	擡	抬	擣	擯
2D3	5A3	攬	擶	擴	擲	擺	攀	擽	攘	攜	攅	攤	攣	攫	攴	攵	攷
2D4	5A4	收	攸	畋	效	敖	敕	敍	敘	敞	敝	敲	數	斂	斃	變	斛
2D5	5A5	斟	斫	斷	旃	旆	旁	旄	旌	旒	旛	旙	无	旡	旱	杲	昊
2D6	5A6	昃	旻	杳	昵	昶	昴	昜	晏	晄	晉	晁	晞	晝	晤	晧	晨
2D7	5A7	晟	晢	晰	暃	暈	暎	暉	暄	暘	暝	曁	暹	曉	暾	暼	
2DA	5B2		曄	暸	曖	曚	曠	昿	曦	曩	曰	曵	曷	朏	朖	朞	朦
2DB	5B3	朧	霸	朮	朿	朶	杁	朸	朷	杆	杞	杠	杙	杣	杤	枉	杰
2DC	5B4	枩	杼	杪	枌	枋	枦	枡	枅	枷	柯	枴	柬	枳	柩	枸	柤
2DD	5B5	柞	柝	柢	柮	枹	柎	柆	柧	檜	栞	框	栩	桀	桍	栲	桎
2DE	5B6	梳	栫	桙	档	桷	桿	梟	梏	梭	梔	條	梛	梃	檮	梹	桴
2DF	5B7	梵	梠	梺	椏	梍	桾	椁	棊	椈	棘	椢	椦	棡	椌	棍	
2E2	5C2		棔	棧	棕	椶	椒	椄	棗	棣	椥	棹	棠	棯	椨	椪	椚
2E3	5C3	椣	椡	棆	楹	楷	楜	楸	楫	楔	楾	楮	椹	楴	椽	楙	椰
2E4	5C4	楡	楞	楝	榁	楪	榲	榮	槐	榿	槁	槓	榾	槎	寨	槊	槝
2E5	5C5	榻	槃	榧	樮	榑	榠	榜	榕	榴	槞	槨	樂	樛	槿	權	槹
2E6	5C6	槲	槧	樅	榱	樞	槭	樔	槫	樊	樒	櫁	樣	樓	橄	樌	橲
2E7	5C7	樶	橸	橇	橢	橙	橦	橈	樸	樢	檐	檍	檠	檄	檢	檣	
2EA	5D2		檗	蘗	檻	櫃	櫂	檸	檳	檬	櫞	櫑	櫟	檪	櫚	櫪	櫻
2EB	5D3	欅	蘖	櫺	欒	欖	鬱	欟	欸	欷	盜	欹	飮	歇	歃	歉	歐
2EC	5D4	歙	歔	歛	歟	歡	歸	歹	歿	殀	殄	殃	殍	殘	殕	殞	殤
2ED	5D5	殪	殫	殯	殲	殱	殳	殷	殼	毆	毋	毓	毟	毬	毫	毳	毯
2EE	5D6	麾	氈	氓	气	氛	氤	氣	汞	汕	汢	汪	沂	沍	沚	沁	沛
2EF	5D7	汾	汨	汳	沒	沐	泄	泱	泓	沽	泗	泅	泝	沮	沱	沾	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2F2	5E2		洄	泛	泯	泙	泪	洟	衍	洶	洫	洽	洸	洙	洵	洳	洒
2F3	5E3	洌	浣	涓	浤	浚	浹	浙	涎	涕	濤	涅	淹	渕	渊	涵	淇
2F4	5E4	淦	涸	淆	淬	淞	淌	淨	淒	淅	淺	淙	淤	淕	淪	淮	渭
2F5	5E5	湮	渮	渙	湲	湟	渾	渣	湫	渫	湶	湍	渟	湃	渺	湎	渤
2F6	5E6	滿	渝	游	溂	溪	溘	滉	溷	滓	溽	溯	滄	溲	滔	滕	溏
2F7	5E7	溥	滂	溟	潁	漑	灌	滬	滸	滾	漿	滲	漱	滯	漲	滌	
2FA	5F2		漾	漓	滷	澆	潺	潸	澁	澀	潯	潛	濳	潭	澂	潼	潘
2FB	5F3	澎	澑	濂	潦	澳	澣	澡	澤	澹	濆	澪	濟	濕	濬	濔	濘
2FC	5F4	濱	濮	濛	瀉	瀋	濺	瀑	瀁	瀏	濾	瀛	瀚	潴	瀝	瀘	瀟
2FD	5F5	瀰	瀾	瀲	灑	灣	炙	炒	炯	烱	炬	炸	炳	炮	烟	烋	烝
2FE	5F6	烙	焉	烽	焜	焙	煥	煕	熈	煦	煢	煌	煖	煬	熏	燻	熄
2FF	5F7	熕	熨	熬	燗	熹	熾	燒	燉	燔	燎	燠	燬	燧	燵	燼	
302	602		燹	燿	爍	爐	爛	爨	爭	爬	爰	爲	爻	爼	爿	牀	牆
303	603	牋	牘	牴	牾	犂	犁	犇	犒	犖	犢	犧	犹	犲	狃	狆	狄
304	604	狎	狒	狢	狠	狡	狹	狷	倏	猗	猊	猜	猖	猝	猴	猯	猩
305	605	猥	猾	獎	獏	默	獗	獪	獨	獰	獸	獵	獻	獺	珈	玳	珎
306	606	玻	珀	珥	珮	珞	璢	琅	瑯	琥	珸	琲	琺	瑕	琿	瑟	瑙
307	607	瑁	瑜	瑩	瑰	瑣	瑪	瑶	瑾	璋	璞	璧	瓊	瓏	瓔	珱	
30A	612		瓠	瓣	瓧	瓩	瓮	瓲	瓰	瓱	瓸	瓷	甄	甃	甅	甌	甎
30B	613	甍	甕	甓	甞	甦	甬	甼	畄	畍	畊	畉	畛	畆	畚	畩	畤
30C	614	畧	畫	畭	畸	當	疆	疇	畴	疊	疉	疂	疔	疚	疝	疥	疣
30D	615	痂	疳	痃	疵	疽	疸	疼	疱	痍	痊	痒	痙	痣	痞	痾	痿
30E	616	痼	瘁	痰	痺	痲	痳	瘋	瘍	瘉	瘟	瘧	瘠	瘡	瘢	瘤	瘴
30F	617	瘰	瘻	癇	癈	癆	癜	癘	癡	癢	癨	癩	癪	癧	癬	癰	
312	622		癲	癶	癸	發	皀	皃	皈	皋	皎	皖	皓	皙	皚	皰	皴
313	623	皸	皹	皺	盂	盍	盖	盒	盞	盡	盥	盧	盪	蘯	盻	眈	眇
314	624	眄	眩	眤	眞	眥	眦	眛	眷	眸	睇	睚	睨	睫	睛	睥	睿
315	625	睾	睹	瞎	瞋	瞑	瞠	瞞	瞰	瞶	瞹	瞿	瞼	瞽	瞻	矇	矍
316	626	矗	矚	矜	矣	矮	矼	砌	砒	礦	砠	礪	硅	碎	硴	碆	硼
317	627	碚	碌	碣	碵	碪	碯	磑	磆	磋	磔	碾	碼	磅	磊	磬	
31A	632		磧	磚	磽	磴	礇	礒	礑	礙	礬	礫	祀	祠	祗	祟	祚
31B	633	祕	祓	祺	祿	禊	禝	禧	齋	禪	禮	禳	禹	禺	秉	秕	秧
31C	634	秬	秡	秣	稈	稍	稘	稙	稠	稟	禀	稱	稻	稾	稷	穃	穗
31D	635	穉	穡	穢	穩	龝	穰	穹	穽	窈	窗	窕	窘	窖	窩	竈	窰
31E	636	窶	竅	竄	窿	邃	竇	竊	竍	竏	竕	竓	站	竚	竝	竡	竢
31F	637	竦	竭	竰	笂	笏	笊	笆	笳	笘	笙	笞	笵	笨	笶	筐	
322	642		筺	笄	筍	笋	筌	筅	筵	筥	筴	筧	筰	筱	筬	筮	箝
323	643	箘	箟	箍	箜	箚	箋	箒	箏	筝	箙	篋	篁	篌	篏	箴	篆
324	644	篝	篩	簑	簔	篦	篥	籠	簀	簇	簓	篳	篷	簗	簍	篶	簣
325	645	簧	簪	簟	簷	簫	簽	籌	籃	籔	籏	籀	籐	籘	籟	籤	籖
326	646	籥	籬	籵	粃	粐	粤	粭	粢	粫	粡	粨	粳	粲	粱	粮	粹
327	647	粽	糀	糅	糂	糘	糒	糜	糢	鬻	糯	糲	糴	糶	糺	紆	
32A	652		紂	紜	紕	紊	絅	絋	紮	紲	紿	紵	絆	絳	絖	絎	絲
32B	653	絨	絮	絏	絣	經	綉	絛	綏	絽	綛	綺	綮	綣	綵	緇	綽
32C	654	綫	總	綢	綯	緜	綸	綟	綰	緘	緝	緤	緞	緻	緲	緡	縅
32D	655	縊	縣	縡	縒	縱	縟	縉	縋	縢	繆	繦	縻	縵	縹	繃	縷
32E	656	縲	縺	繧	繝	繖	繞	繙	繚	繹	繪	繩	繼	繻	纃	緕	繽
32F	657	辮	繿	纈	纉	續	纒	纐	纓	纔	纖	纎	纛	纜	缸	缺	

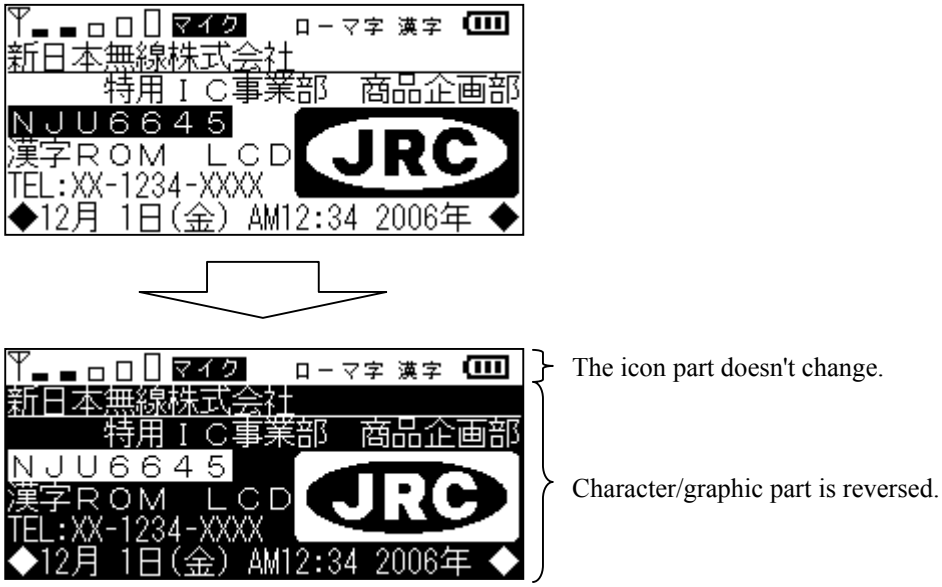
Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
332	662		罅	罌	罍	罎	罐	网	罕	罔	罘	罟	罠	罨	罩	罧	罸
333	663	羂	羆	羃	羈	羇	羌	羔	羞	羝	羚	羣	羯	羲	羹	羮	羶
334	664	羸	譱	翅	翆	翊	翕	翔	翡	翦	翩	翳	翹	飜	耆	耄	耋
335	665	耒	耘	耙	耜	耡	耨	耿	耻	聊	聆	聒	聘	聚	聟	聢	聨
336	666	聳	聲	聰	聶	聹	聽	聿	肄	肆	肅	肛	肓	肚	肭	冐	肬
337	667	胛	胥	胙	胝	胄	胚	胖	脉	胯	胱	脛	脩	脣	脯	腋	
33A	672		隋	腆	脾	腓	腑	胼	腱	腮	腥	腦	腴	膃	膈	膊	膀
33B	673	膂	膠	膕	膤	膣	腟	膓	膩	膰	膵	膾	膸	膽	臀	臂	膺
33C	674	臉	臍	臑	臙	臘	臈	臚	臟	臠	臧	臺	臻	臾	舁	舂	舅
33D	675	與	舊	舍	舐	舖	舩	舫	舸	舳	艀	艙	艘	艝	艚	艟	艤
33E	676	艢	艨	艪	艫	舮	艱	艷	艸	艾	芍	芒	芫	芟	芻	芬	苡
33F	677	苣	苟	苒	苴	苳	苺	莓	范	苻	苹	苞	茆	苜	茉	苙	
342	682		茵	茴	茖	茲	茱	荀	茹	荐	荅	茯	茫	茗	茘	莅	莚
343	683	莪	莟	莢	莖	茣	莎	莇	莊	荼	莵	荳	荵	莠	莉	莨	菴
344	684	萓	菫	菎	菽	萃	菘	萋	菁	菷	萇	菠	菲	萍	萢	萠	莽
345	685	萸	蔆	菻	葭	萪	萼	蕚	蒄	葷	葫	蒭	葮	蒂	葩	葆	萬
346	686	葯	葹	萵	蓊	葢	蒹	蒿	蒟	蓙	蓍	蒻	蓚	蓐	蓁	蓆	蓖
347	687	蒡	蔡	蓿	蓴	蔗	蔘	蔬	蔟	蔕	蔔	蓼	蕀	蕣	蕘	蕈	
34A	692		蕁	蘂	蕋	蕕	薀	薤	薈	薑	薊	薨	蕭	薔	薛	藪	薇
34B	693	薜	蕷	蕾	薐	藉	薺	藏	薹	藐	藕	藝	藥	藜	藹	蘊	蘓
34C	694	蘋	藾	藺	蘆	蘢	蘚	蘰	蘿	虍	乕	虔	號	虧	虱	蚓	蚣
34D	695	蚩	蚪	蚋	蚌	蚶	蚯	蛄	蛆	蚰	蛉	蠣	蚫	蛔	蛞	蛩	蛬
34E	696	蛟	蛛	蛯	蜒	蜆	蜈	蜀	蜃	蛻	蜑	蜉	蜍	蛹	蜊	蜴	蜿
34F	697	蜷	蜻	蜥	蜩	蜚	蝠	蝟	蝸	蝌	蝎	蝴	蝗	蝨	蝮	蝙	
352	6A2		蝓	蝣	蝪	蠅	螢	螟	螂	螯	蟋	螽	蟀	蟐	雖	螫	蟄
353	6A3	螳	蟇	蟆	螻	蟯	蟲	蟠	蠏	蠍	蟾	蟶	蟷	蠎	蟒	蠑	蠖
354	6A4	蠕	蠢	蠡	蠱	蠶	蠹	蠧	蠻	衄	衂	衒	衙	衞	衢	衫	袁
355	6A5	衾	袞	衵	衽	袵	衲	袂	袗	袒	袮	袙	袢	袍	袤	袰	袿
356	6A6	袱	裃	裄	裔	裘	裙	裝	裹	褂	裼	裴	裨	裲	褄	褌	褊
357	6A7	褓	襃	褞	褥	褪	褫	襁	襄	褻	褶	褸	襌	褝	襠	襞	
35A	6B2		襦	襤	襭	襪	襯	襴	襷	襾	覃	覈	覊	覓	覘	覡	覩
35B	6B3	覦	覬	覯	覲	覺	覽	覿	觀	觚	觜	觝	觧	觴	觸	訃	訖
35C	6B4	訐	訌	訛	訝	訥	訶	詁	詛	詒	詆	詈	詼	詭	詬	詢	誅
35D	6B5	誂	誄	誨	誡	誑	誥	誦	誚	誣	諄	諍	諂	諚	諫	諳	諧
35E	6B6	諤	諱	謔	諠	諢	諷	諞	諛	謌	謇	謚	諡	謖	謐	謗	謠
35F	6B7	謳	鞫	謦	謫	謾	謨	譁	譌	譏	譎	證	譖	譛	譚	譫	
362	6C2		譟	譬	譯	譴	譽	讀	讌	讎	讒	讓	讖	讙	讚	谺	豁
363	6C3	谿	豈	豌	豎	豐	豕	豢	豬	豸	豺	貂	貉	貅	貊	貍	貎
364	6C4	貔	豼	貘	戝	貭	貪	貽	貲	貳	貮	貶	賈	賁	賤	賣	賚
365	6C5	賽	賺	賻	贄	贅	贊	贇	贏	贍	贐	齎	贓	賍	贔	贖	赧
366	6C6	赭	赱	赳	趁	趙	跂	趾	趺	跏	跚	跖	跌	跛	跋	跪	跫
367	6C7	跟	跣	跼	踈	踉	跿	踝	踞	踐	踟	蹂	踵	踰	踴	蹊	
36A	6D2		蹇	蹉	蹌	蹐	蹈	蹙	蹤	蹠	踪	蹣	蹕	蹶	蹲	蹼	躁
36B	6D3	躇	躅	躄	躋	躊	躓	躑	躔	躙	躪	躡	躬	躰	軆	躱	躾
36C	6D4	軅	軈	軋	軛	軣	軼	軻	軫	軾	輊	輅	輕	輒	輙	輓	輜
36D	6D5	輟	輛	輌	輦	輳	輻	輹	轅	轂	輾	轌	轉	轆	轎	轗	轜
36E	6D6	轢	轣	轤	辜	辟	辣	辭	辯	辷	迚	迥	迢	迪	迯	邇	迴
36F	6D7	逅	迹	迺	逑	逕	逡	逍	逞	逖	逋	逧	逶	逵	逹	迸	

Upper BIT		Lower BIT															
Chara. code	JIS code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
372	6E2		遏	遐	遑	遒	逎	遉	逾	遖	遘	遞	遨	遯	遶	隨	遲
373	6E3	邂	遽	邁	邀	邊	邉	邏	邨	邯	邱	邵	郢	郤	扈	郛	鄂
374	6E4	鄒	鄙	鄲	鄰	酊	酖	酘	酣	酥	酩	酳	酲	醋	醉	醂	醢
375	6E5	醫	醯	醪	醵	醴	醺	釀	釁	釉	釋	釐	釖	釟	釡	釛	釼
376	6E6	釵	釶	鈞	釿	鈔	鈬	鈕	鈑	鉞	鉗	鉅	鉉	鉤	鉈	銕	鈿
377	6E7	鉋	鉐	銜	銖	銓	銛	鉚	鋏	銹	銷	鋩	錏	鋺	鍄	錮	
37A	6F2		錙	錢	錚	錣	錺	錵	錻	鍜	鍠	鍼	鍮	鍖	鎰	鎬	鎭
37B	6F3	鎔	鎹	鏖	鏗	鏨	鏥	鏘	鏃	鏝	鏐	鏈	鏤	鐚	鐔	鐓	鐃
37C	6F4	鐇	鐐	鐶	鐫	鐵	鐡	鐺	鑁	鑒	鑄	鑛	鑠	鑢	鑞	鑪	鈩
37D	6F5	鑰	鑵	鑷	鑽	鑚	鑼	鑾	钁	鑿	閂	閇	閊	閔	閖	閘	閙
37E	6F6	閠	閨	閧	閭	閼	閻	閹	閾	闊	濶	闃	闍	闌	闕	闔	闖
37F	6F7	關	闡	闥	闢	阡	阨	阮	阯	陂	陌	陏	陋	陷	陜	陞	
382	702		陝	陟	陦	陲	陬	隍	隘	隕	隗	險	隧	隱	隲	隰	隴
383	703	隶	隸	隹	雎	雋	雉	雍	襍	雜	霍	雕	雹	霄	霆	霈	霓
384	704	霎	霑	霏	霖	霙	霤	霪	霰	霹	霽	霾	靄	靆	靈	靂	靉
385	705	靜	靠	靤	靦	靨	勒	靫	靱	靹	鞅	靼	鞁	靺	鞆	鞋	鞏
386	706	鞐	鞜	鞨	鞦	鞣	鞳	鞴	韃	韆	韈	韋	韜	韭	齏	韲	竟
387	707	韶	韵	頏	頌	頸	頤	頡	頷	頽	顆	顏	顋	顫	顯	顰	
38A	712		顱	顴	顳	颪	颯	颱	颶	飄	飃	飆	飩	飫	餃	餉	餒
38B	713	餔	餘	餡	餝	餞	餤	餠	餬	餮	餽	餾	饂	饉	饅	饐	饋
38C	714	饑	饒	饌	饕	馗	馘	馥	馭	馮	馼	駟	駛	駝	駘	駑	駭
38D	715	駮	駱	駲	駻	駸	騁	騏	騅	駢	騙	騫	騷	驅	驂	驀	驃
38E	716	騾	驕	驍	驛	驗	驟	驢	驥	驤	驩	驫	驪	骭	骰	骼	髀
38F	717	髏	髑	髓	體	髞	髟	髢	髣	髦	髯	髫	髮	髴	髱	髷	
392	722		髻	鬆	鬘	鬚	鬟	鬢	鬣	鬥	鬧	鬨	鬩	鬪	鬮	鬯	鬲
393	723	魄	魃	魏	魍	魎	魑	魘	魴	鮓	鮃	鮑	鮖	鮗	鮟	鮠	鮨
394	724	鮴	鯀	鯊	鮹	鯆	鯏	鯑	鯒	鯣	鯢	鯤	鯔	鯡	鰺	鯲	鯱
395	725	鯰	鰕	鰔	鰉	鰓	鰌	鰆	鰈	鰒	鰊	鰄	鰮	鰛	鰥	鰤	鰡
396	726	鰰	鱇	鰲	鱆	鰾	鱚	鱠	鱧	鱶	鱸	鳧	鳬	鳰	鴉	鴈	鳫
397	727	鴃	鴆	鴪	鴦	鶯	鴣	鴟	鵄	鴕	鴒	鵁	鴿	鴾	鵆	鵈	
39A	732		鵝	鵞	鵤	鵑	鵐	鵙	鵲	鶉	鶇	鶫	鵯	鵺	鶚	鶤	鶩
39B	733	鶲	鷄	鷁	鶻	鶸	鶺	鷆	鷏	鷂	鷙	鷓	鷸	鷦	鷭	鷯	鷽
39C	734	鸚	鸛	鸞	鹵	鹹	鹽	麁	麈	麋	麌	麒	麕	麑	麝	麥	麩
39D	735	麸	麪	麭	靡	黌	黎	黏	黐	黔	黜	點	黝	黠	黥	黨	黯
39E	736	黴	黶	黷	黹	黻	黼	黽	鼇	鼈	皷	鼕	鼡	鼬	鼾	齊	齒
39F	737	齔	齣	齟	齠	齡	齦	齧	齬	齪	齷	齲	齶	龕	龜	龠	
3A2	742		堯	槇	遙	瑤	凜	熙	·	·	·	·	·	·	·	·	·
3A3	743	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
3A4	744	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
3A5	745	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
3A6	746	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
3A7	747	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	

Correspondence Table of Half-size character code and Character pattern (ROM version “00”)

(4) FULL SCREEN REVERSE DISPLAY FUNCTION

This function reverses the full character and graphic display part except the icon display part. It is possible to reverse display easily without the RAM rewriting by this function. The cursor and the attribute display part are reversed too.



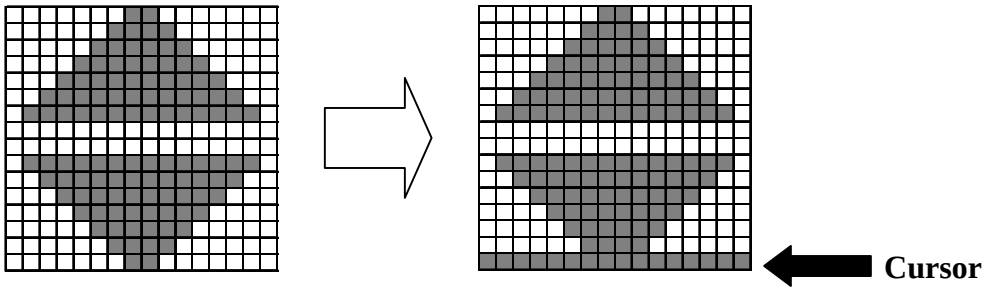
(5) CURSOR CONTROL

The method of displaying the cursor has 3-kind that are the reversing blink (BW="1") and the underline blinks of 16th row (C="1") and the black blink (B="1"). The "LC" register is possible to switch the cursor display of 1-character corresponding to the DDRAM address set in the address counter and the cursor display of the entire line including the setting address.

(5-1) Character Cursor

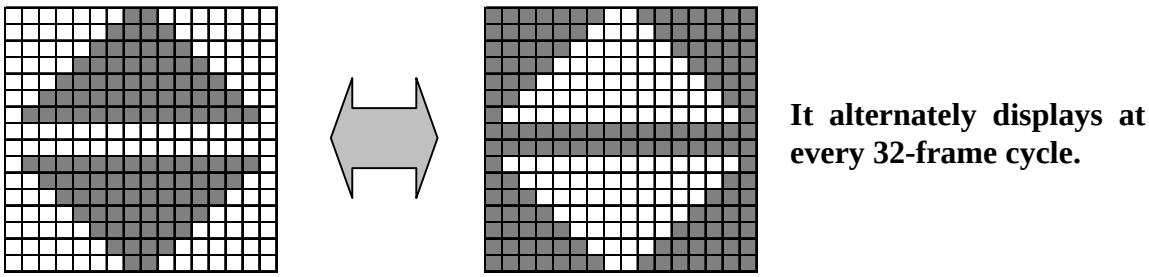
(5-1-1) Underline <C="1", LC="0", B="0", BW="0">

The underline is displayed to the 16th row. When there is ON data in the 16th row, the data displays the logical add with original data.



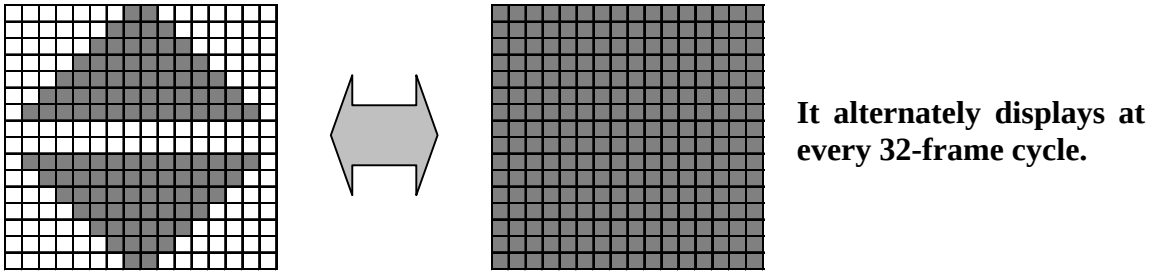
(5-1-2) Reverse Blink <C="1", LC="0", B="0", BW="1">

The character at the cursor position is blinking with the reversing display. And then, the reversing switches at every 32-frame cycle.



(5-1-3) Black Blink <C="1", LC="0", B="1", BW="0">

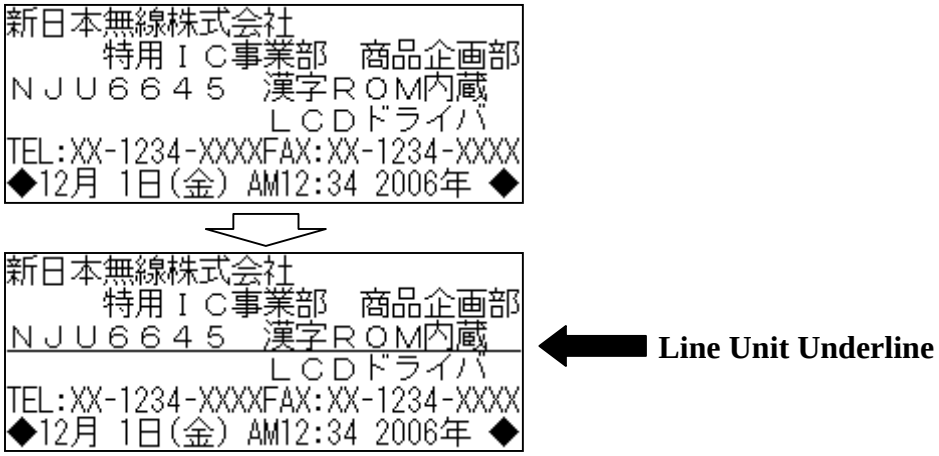
The character at the cursor position is blinking with the black pattern display. The blinking switches the all black pattern and the character pattern at every 32-frame cycle.



(5-2) Line Cursor

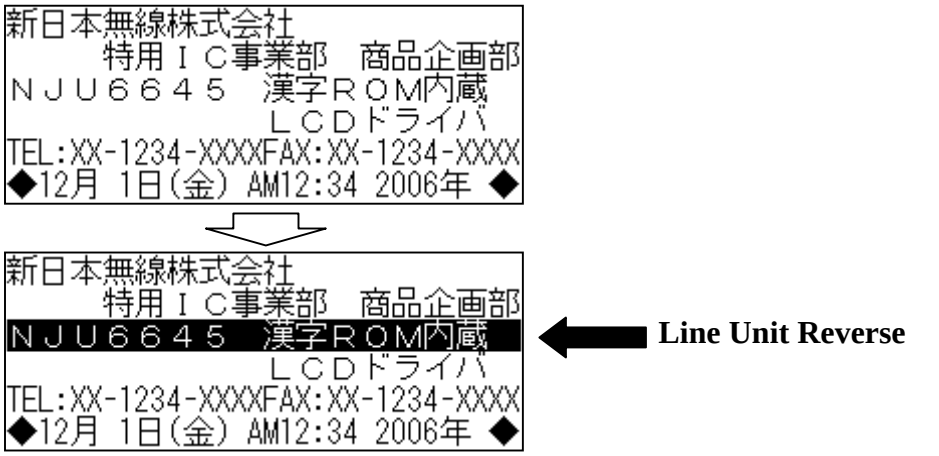
(5-2-1) Line Unit Underline <C="1", LC="1", B="0", BW="0">

The 16th row of the line including the DDRAM address setting in the address counter is all ON. When there is character data, the data displays the logical add.



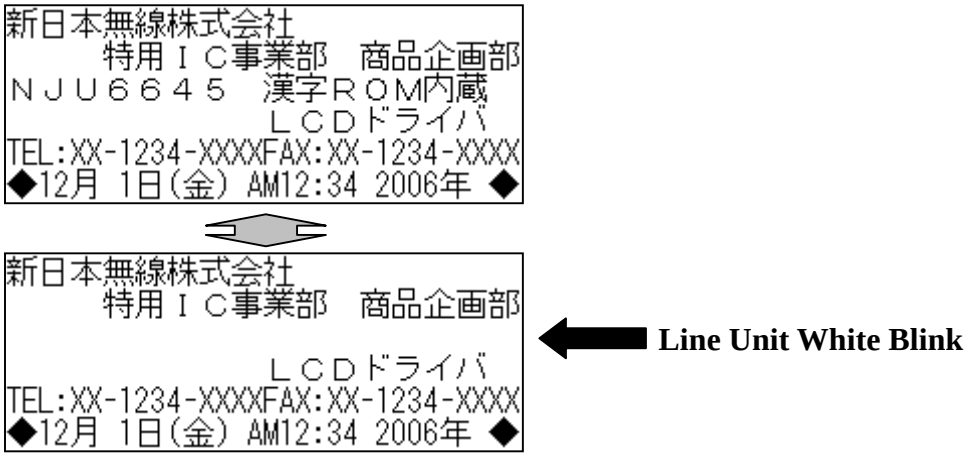
(5-2-2) Line Unit Reverse <C="1", LC="1", B="0", BW="1">

The line including the DDRAM address setting in the address counter is reversed display.



(5-2-3) Line Unit White Blink <C="1", LC="1", B="1", BW="0">

The line including the DDRAM address setting in the address counter is blinking with the white pattern display. The blinking switches the all white pattern and the character data at every 32-frame cycle.



(6) DISPLAY ATTRIBUTE SETTING

NJU6645 is set the Reverse Display, the White Blink Display and the Reverse Blink Display by the display attribute code of each character in 2-bit. This display is applied in matrix unit of the 16 x 16 dots in the full-size data and the 8 x 16 dots in the half-size data. The White Blink Display and the Reverse Blink Display are switching at every 32-frame cycle.

< Relation between the input data at the data writing to DDRAM and the bit >

The attribute code of full-size / half-size character is allocated the 1st bit and 2nd bit in the 1st byte. When the DDRAM data is written, it is necessary to select the attribute code of this bit and to input the attribute of each character.

[Full-size character data]

1st byte								2nd byte							
D7	**D6**	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Attribute 1	Attribute 0	Full-size character code 14bit													
P1	P0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

[Half-size character data]

1st byte								2nd byte							
D7	**D6**	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Attribute 1	Attribute 0	Half-size attribute code						Half-size character code 8bit							
P1	P0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

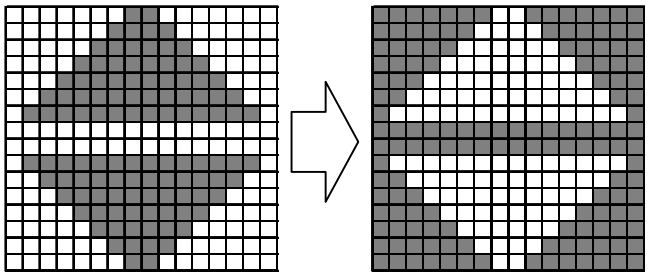
< Correspondence of the attribute code and the display status >

The display status changes according to the following tables.

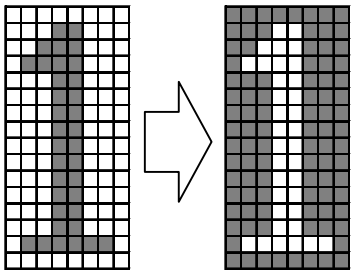
P1	P0	Display Status
0	0	Normal
0	1	Reverse
1	0	White blink
1	1	Reverse blink

< Example of display when the display attribute is selected >

(i) Reverse

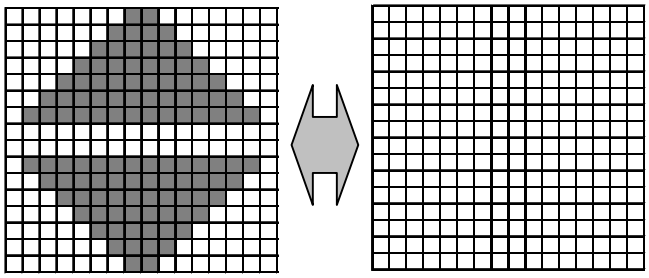


<Full-size character display>



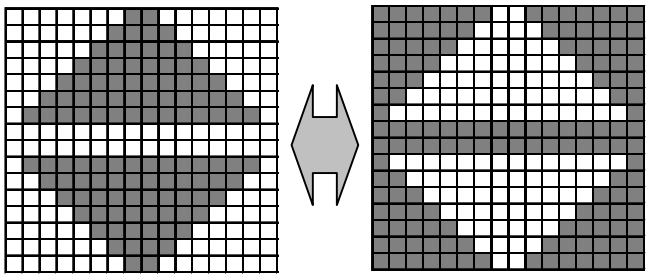
<Half-size character display>

(ii) White blink



It alternately displays at every 32-frame cycle.

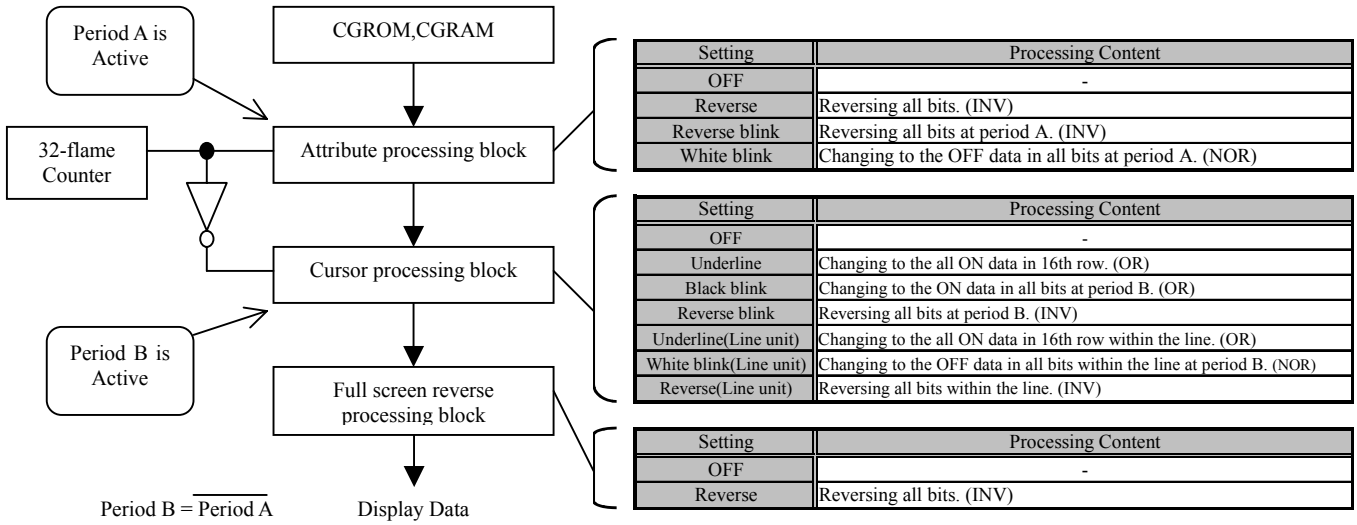
(iii) Reverse blink



It alternately displays at every 32-frame cycle.

(7) RELATION BETWEEN ATTRIBUTE, BLINK and FULL SCREEN REVERSE DISPLAY

The attribute display, the cursor display, and full screen reverse display are sequentially processed as shown in the following figures. The period that the data of various blinks is converted is reversed in the attribute display processing block and the cursor display processing block. Therefore, when the part where the attribute of the blink was selected and the cursor position of the blink overlap, the attribute display and the cursor display are alternately displayed. The full screen reverse display reverses the data after the attribute display processing and the cursor display processing are done.



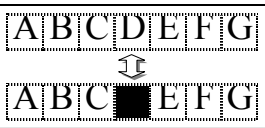
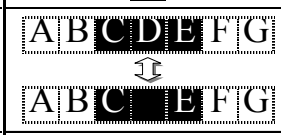
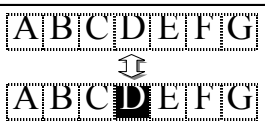
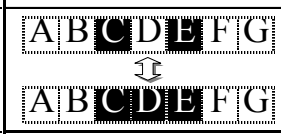
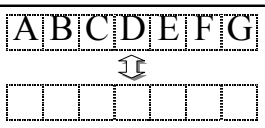
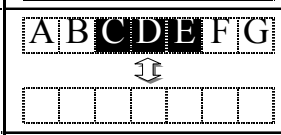
Setting	Processing Content
OFF	-
Reverse	Reversing all bits. (INV)
Reverse blink	Reversing all bits at period A. (INV)
White blink	Changing to the OFF data in all bits at period A. (NOR)

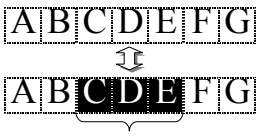
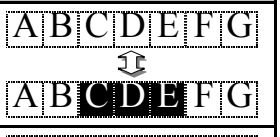
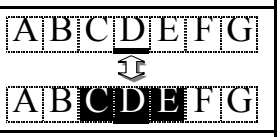
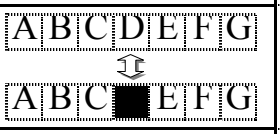
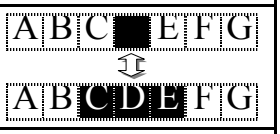
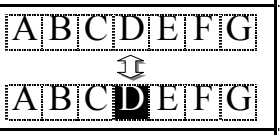
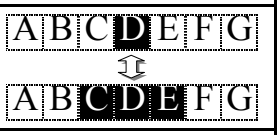
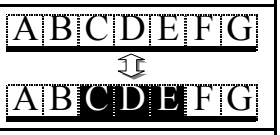
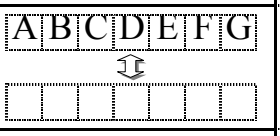
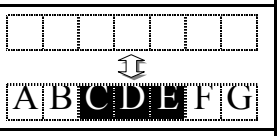
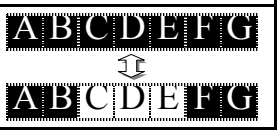
Setting	Processing Content
OFF	-
Underline	Changing to the all ON data in 16th row. (OR)
Black blink	Changing to the ON data in all bits at period B. (OR)
Reverse blink	Reversing all bits at period B. (INV)
Underline(Line unit)	Changing to the all ON data in 16th row within the line. (OR)
White blink(Line unit)	Changing to the OFF data in all bits within the line at period B. (NOR)
Reverse(Line unit)	Reversing all bits within the line. (INV)

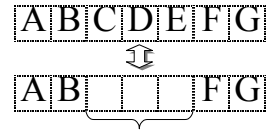
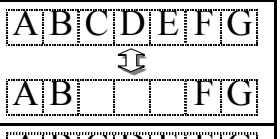
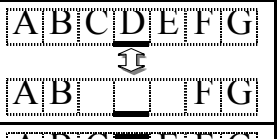
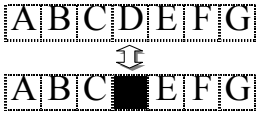
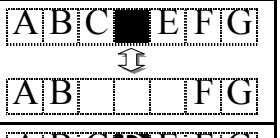
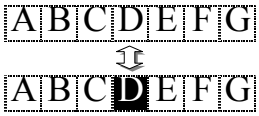
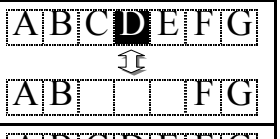
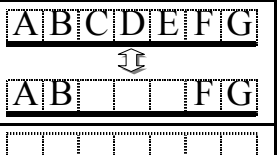
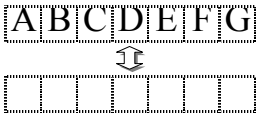
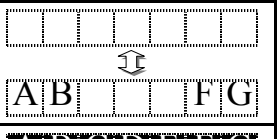
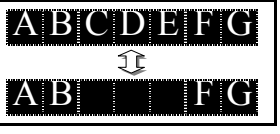
Setting	Processing Content
OFF	-
Reverse	Reversing all bits. (INV)

< Method of display when attribute selection overlaps with cursor display >

Attribute			Cursol			Attribute + Cursol display
Nomal	A B C D E F G	+	OFF	A B C D E F G	=	A B C D E F G
			Underline	A B C D E F G	=	A B C D E F G
			Black blink	A B C D E F G ⇕ A B C ■ E F G	=	A B C D E F G ⇕ A B C ■ E F G
			Reverse blink	A B C D E F G ⇕ A B C **D** E F G	=	A B C D E F G ⇕ A B C **D** E F G
			Underline (Line unit)	A B C D E F G	=	A B C D E F G
			White blink (Line unit)	A B C D E F G ⇕	=	A B C D E F G ⇕
			Reverse (Line unit)	**A B C D E F G**	=	**A B C D E F G**

Attribute			Cursol			Attribute + Cursol display
Reverse	 Reverse attribute selection part	+	OFF		=	
			Underline		=	
			Black blink		=	
			Reverse blink		=	
			Underline (Line unit)		=	
			White blink (Line unit)		=	
			Reverse (Line unit)		=	

Attribute			Cursol			Attribute + Cursol display
Reverse blink	 Reverse blink attribute selection part	+	OFF		=	
			Underline		=	
			Black blink		=	
			Reverse blink		=	
			Underline (Line unit)		=	
			White blink (Line unit)		=	
			Reverse (Line)		=	

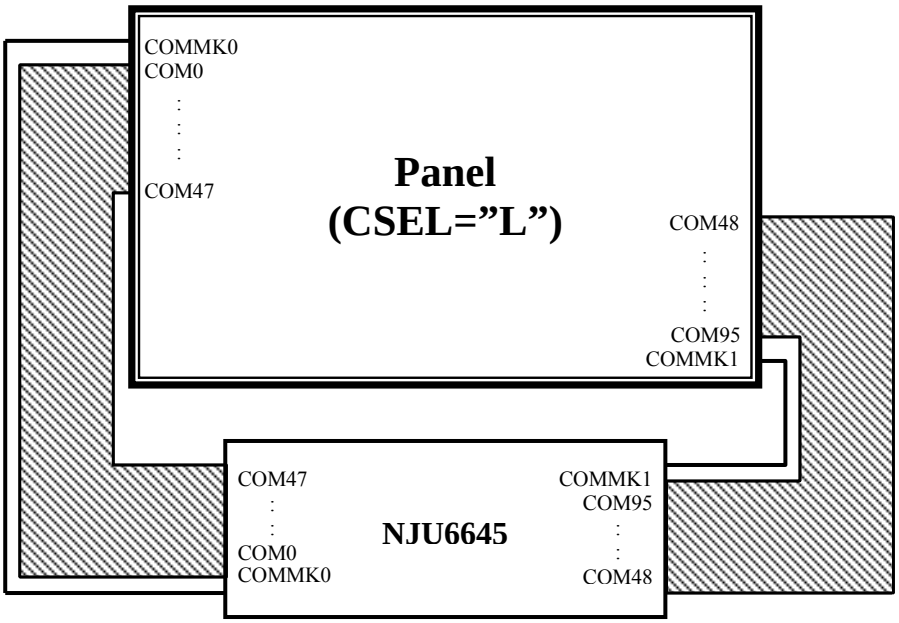
Attribute			Cursol			Attribute + Cursol display
White blink	 White blink attribute selection part	+	OFF		=	
			Underline		=	
			Black blink		=	
			Reverse blink		=	
			Underline (Line unit)		=	
			White blink (Line unit)		=	
			Reverse (Line)		=	

(8) COMMON DRIVER OUTPUT SWITCHING

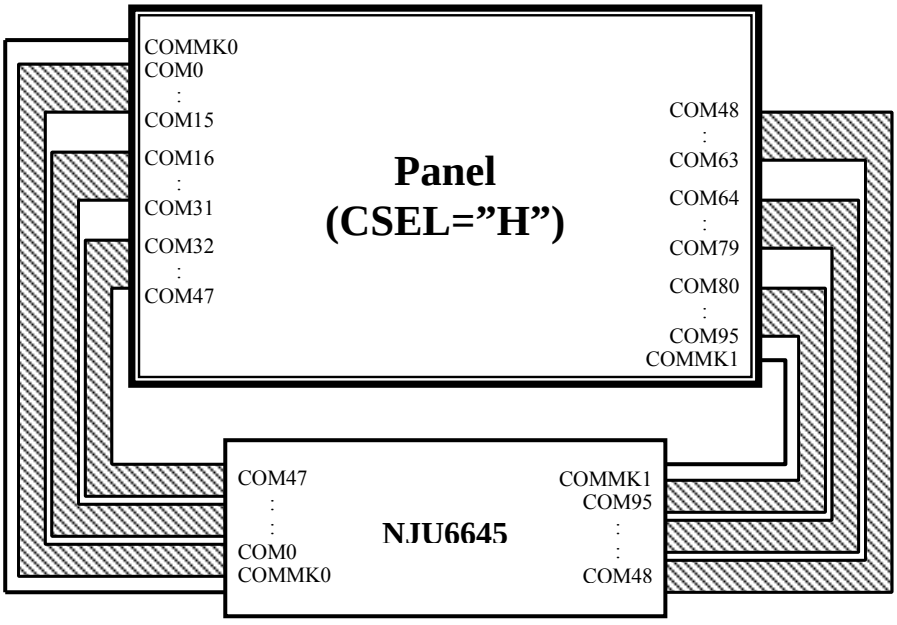
The common output order of NJU6645 is selected by CSEL terminal (Both sides wiring or Comb wiring). When the CSEL="L", the COM0 to 47 connects on the upper half of the panel and the COM48 to 95 connects on the lower half. When the CSEL="H", the COM is divided by 16, that is connected to the panel by the comb pattern.

< Wiring image >

(i) CSEL=”L” Both sides wiring mode



(ii) CSEL=”H” Comb wiring mode

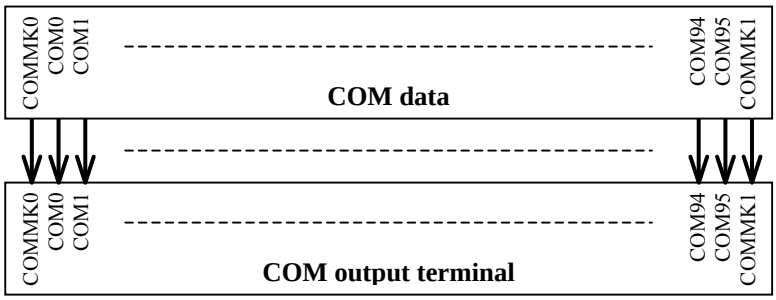


(9) COMMON SHIFT DIRECTION / SEGMENT OUTPUT DIRECTION

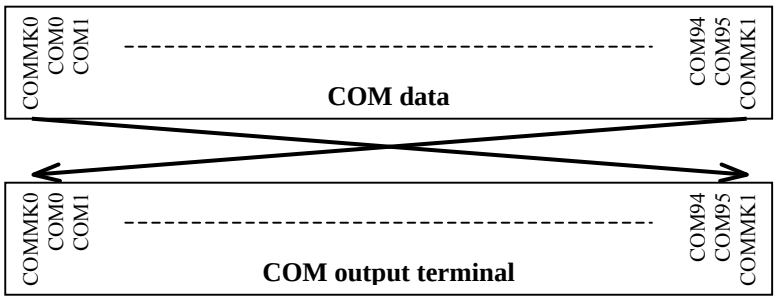
The direction of COM scan and SEG output of the dot matrix part and icon part is changed by "Driver Output Control" instruction (SEL1, SEL2). The output data of SEG and COM changes as follows.

COM output direction switching

< SEL1="0" >

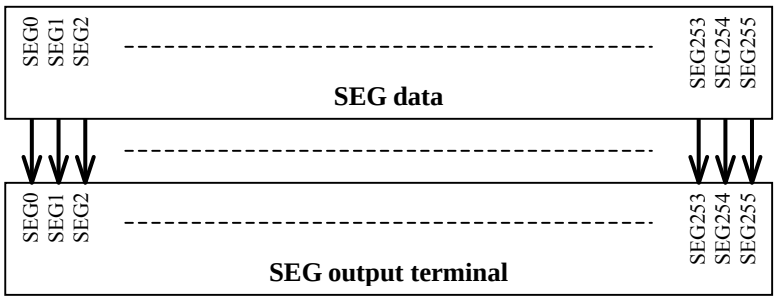


< SEL1="1" >

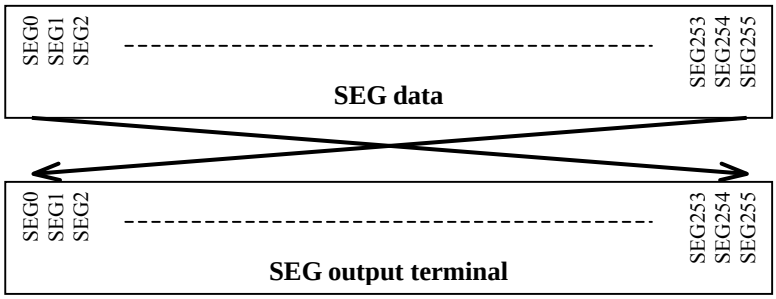


SEG output direction switching

< SEL2="0" >



< SEL2="1" >

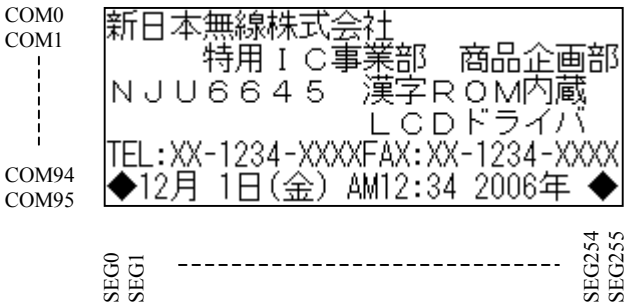


The correspondence of the display position on the panel and the DDRAM address is changed as follows.

SEL1=”0”, SEL2=”0"

The correspondence of the display position on the panel and the DDRAM address (SEL1=”0", SEL2=”0")

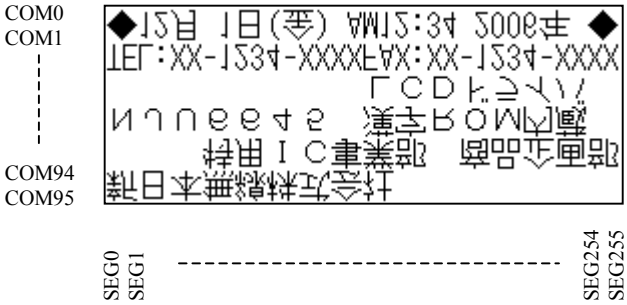
	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F
2-line	020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F	030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F
3-line	040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F	050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F
4-line	060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F	070	071	072	073	074	075	076	077	078	079	07A	07B	07C	07D	07E	07F
5-line	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
6-line	0A0	0A1	0A2	0A3	0A4	0A5	0A6	0A7	0A8	0A9	0AA	0AB	0AC	0AD	0AE	0AF	0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF



SEL1=”1”, SEL2=”0"

The correspondence of the display position on the panel and the DDRAM address (SEL1=”1", SEL2=”0")

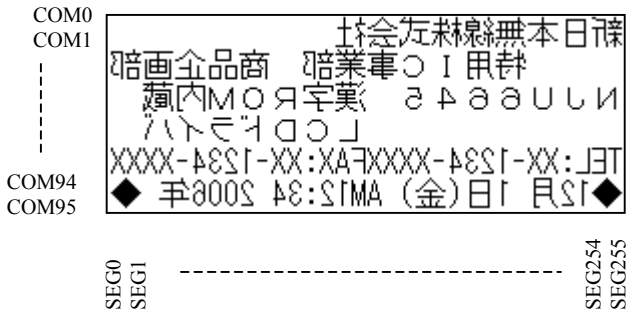
	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	0A0	0A1	0A2	0A3	0A4	0A5	0A6	0A7	0A8	0A9	0AA	0AB	0AC	0AD	0AE	0AF	0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF
2-line	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
3-line	060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F	070	071	072	073	074	075	076	077	078	079	07A	07B	07C	07D	07E	07F
4-line	040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F	050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F
5-line	020	021	022	023	024	025	026	027	028	029	02A	02B	02C	02D	02E	02F	030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F
6-line	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F



SEL1=”0”, SEL2=”1"

The correspondence of the display position on the panel and the DDRAM address (SEL1=”0", SEL2=”1")

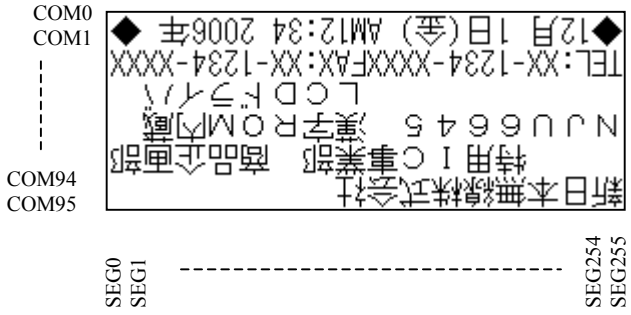
	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	01F	01E	01D	01C	01B	01A	019	018	017	016	015	014	013	012	011	010	00F	00E	00D	00C	00B	00A	009	008	007	006	005	004	003	002	001	000
2-line	03F	03E	03D	03C	03B	03A	039	038	037	036	035	034	033	032	031	030	02F	02E	02D	02C	02B	02A	029	028	027	026	025	024	023	022	021	020
3-line	05F	05E	05D	05C	05B	05A	059	058	057	056	055	054	053	052	051	050	04F	04E	04D	04C	04B	04A	049	048	047	046	045	044	043	042	041	040
4-line	07F	07E	07D	07C	07B	07A	079	078	077	076	075	074	073	072	071	070	06F	06E	06D	06C	06B	06A	069	068	067	066	065	064	063	062	061	060
5-line	09F	09E	09D	09C	09B	09A	099	098	097	096	095	094	093	092	091	090	08F	08E	08D	08C	08B	08A	089	088	087	086	085	084	083	082	081	080
6-line	0BF	0BE	0BD	0BC	0BB	0BA	0B9	0B8	0B7	0B6	0B5	0B4	0B3	0B2	0B1	0B0	0AF	0AE	0AD	0AC	0AB	0AA	0A9	0A8	0A7	0A6	0A5	0A4	0A3	0A2	0A1	0A0



SEL1=”1”, SEL2=”1"

The correspondence of the display position on the panel and the DDRAM address (SEL1=”1", SEL2=”1")

	1-digit		2-digit		3-digit		4-digit		5-digit		6-digit		7-digit		8-digit		9-digit		10-digit		11-digit		12-digit		13-digit		14-digit		15-digit		16-digit	
1-line	0BF	0BE	0BD	0BC	0BB	0BA	0B9	0B8	0B7	0B6	0B5	0B4	0B3	0B2	0B1	0B0	0AF	0AE	0AD	0AC	0AB	0AA	0A9	0A8	0A7	0A6	0A5	0A4	0A3	0A2	0A1	0A0
2-line	09F	09E	09D	09C	09B	09A	099	098	097	096	095	094	093	092	091	090	08F	08E	08D	08C	08B	08A	089	088	087	086	085	084	083	082	081	080
3-line	07F	07E	07D	07C	07B	07A	079	078	077	076	075	074	073	072	071	070	06F	06E	06D	06C	06B	06A	069	068	067	066	065	064	063	062	061	060
4-line	05F	05E	05D	05C	05B	05A	059	058	057	056	055	054	053	052	051	050	04F	04E	04D	04C	04B	04A	049	048	047	046	045	044	043	042	041	040
5-line	03F	03E	03D	03C	03B	03A	039	038	037	036	035	034	033	032	031	030	02F	02E	02D	02C	02B	02A	029	028	027	026	025	024	023	022	021	020
6-line	01F	01E	01D	01C	01B	01A	019	018	017	016	015	014	013	012	011	010	00F	00E	00D	00C	00B	00A	009	008	007	006	005	004	003	002	001	000



The correspondence of the SEG/COM terminals and the MKRAM address is changed as follows.

The correspondence of the SEG/COM terminals and MKRAM address (SEL1="0", SEL2="0")

	SEG																															
	0 : 7	8 : 15	16 : 23	24 : 31	32 : 39	40 : 47	48 : 55	56 : 63	64 : 71	72 : 79	80 : 87	88 : 95	96 : 103	104 : 111	112 : 119	120 : 127	128 : 135	136 : 143	144 : 151	152 : 159	160 : 167	168 : 175	176 : 183	184 : 191	192 : 199	200 : 207	208 : 215	216 : 223	224 : 231	232 : 239	240 : 247	248 : 255
MK COM0	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
MK COM1	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F

The correspondence of the SEG/COM terminals and MKRAM address (SEL1="1", SEL2="0")

	SEG																															
	0 : 7	8 : 15	16 : 23	24 : 31	32 : 39	40 : 47	48 : 55	56 : 63	64 : 71	72 : 79	80 : 87	88 : 95	96 : 103	104 : 111	112 : 119	120 : 127	128 : 135	136 : 143	144 : 151	152 : 159	160 : 167	168 : 175	176 : 183	184 : 191	192 : 199	200 : 207	208 : 215	216 : 223	224 : 231	232 : 239	240 : 247	248 : 255
MK COM0	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
MK COM1	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F

The correspondence of the SEG/COM terminals and MKRAM address (SEL1="0", SEL2="1")

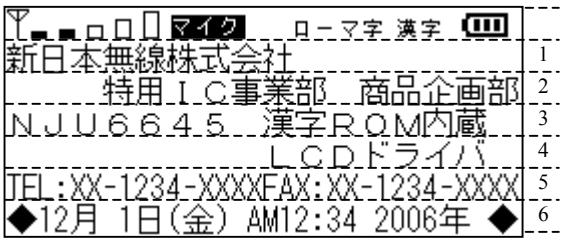
	SEG																															
	0 : 7	8 : 15	16 : 23	24 : 31	32 : 39	40 : 47	48 : 55	56 : 63	64 : 71	72 : 79	80 : 87	88 : 95	96 : 103	104 : 111	112 : 119	120 : 127	128 : 135	136 : 143	144 : 151	152 : 159	160 : 167	168 : 175	176 : 183	184 : 191	192 : 199	200 : 207	208 : 215	216 : 223	224 : 231	232 : 239	240 : 247	248 : 255
MK COM0	11F	11E	11D	11C	11B	11A	119	118	117	116	115	114	113	112	111	110	10F	10E	10D	10C	10B	10A	109	108	107	106	105	104	103	102	101	100
MK COM1	13F	13E	13D	13C	13B	13A	139	138	137	136	135	134	133	132	131	130	12F	12E	12D	12C	12B	12A	129	128	127	126	125	124	123	122	121	120

The correspondence of the SEG/COM terminals and MKRAM address (SEL1="1", SEL2="1")

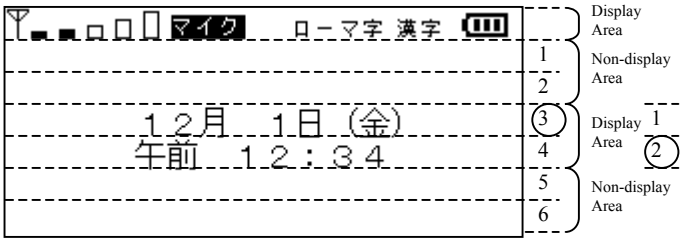
	SEG																															
	0 : 7	8 : 15	16 : 23	24 : 31	32 : 39	40 : 47	48 : 55	56 : 63	64 : 71	72 : 79	80 : 87	88 : 95	96 : 103	104 : 111	112 : 119	120 : 127	128 : 135	136 : 143	144 : 151	152 : 159	160 : 167	168 : 175	176 : 183	184 : 191	192 : 199	200 : 207	208 : 215	216 : 223	224 : 231	232 : 239	240 : 247	248 : 255
MK COM0	13F	13E	13D	13C	13B	13A	139	138	137	136	135	134	133	132	131	130	12F	12E	12D	12C	12B	12A	129	128	127	126	125	124	123	122	121	120
MK COM1	11F	11E	11D	11C	11B	11A	119	118	117	116	115	114	113	112	111	110	10F	10E	10D	10C	10B	10A	109	108	107	106	105	104	103	102	101	100

(10) PARTIAL DISPLAY

The partial display is executed by combining the Display Duty Ratio instruction "DN2, 1, 0" with the Display Start Position instruction "DST2, 1, 0". This function reduces the LCD driving voltage and the power consumption when the duty set low like the clock display of stand-by.



Display Duty Ratio = 6th line



Display Duty Ratio = 2nd line
Display Start Position = 3rd line

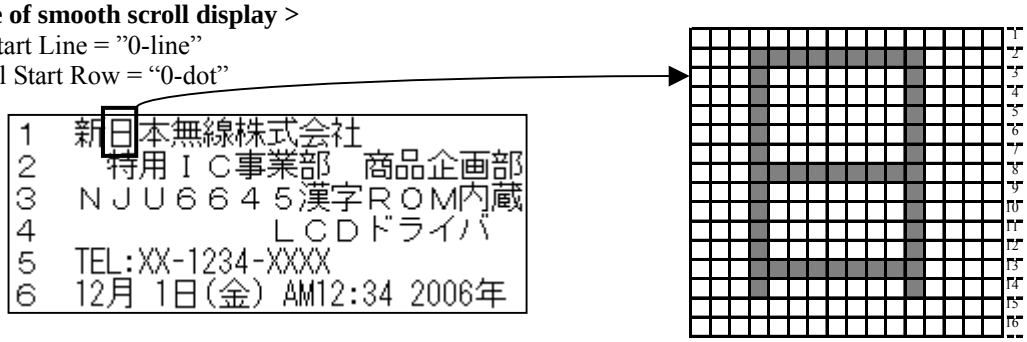
When the Display Start Position is set to the 3rd line, the character data of the first line of the DDRAM address is displayed from the 3rd line (33 to 48 rows). When the Display Duty Ratio is set to the 2nd line, the duty corresponds to 2-line (16 rows x 2 + 2 rows of icon part).

(11) VERTICAL SMOOTH SCROLL

NJU6645 is executed to the vertical smooth scroll display of 1-dot unit by combining the Scroll Start Row with the Scroll Start Line. The display scroll is set by the "Scroll Start Line" instruction (0,1,2,3,4, and 5-line scroll) at the unit of line (16-dot units). The display scroll is set by the "Scroll Start Row" instruction (0,1,2, --- 14, and 15-dot scroll) at the 1 dot unit. The display shifts to the upside only the amount of "Scroll Start Line" + "Scroll Start Row". When it is made to scroll by Display Duty Ratio = 6-line, the display that pushed outside the screen appears from the other side.

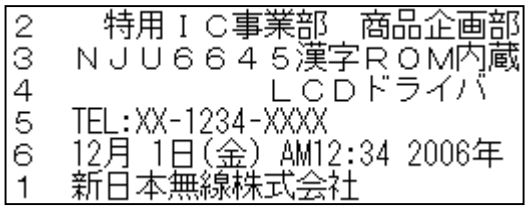
< Example of smooth scroll display >

(i) Scroll Start Line = "0-line"
Scroll Start Row = "0-dot"



(ii) Scroll Start Line = "0-line"
Scroll Start Row = "8-dot"

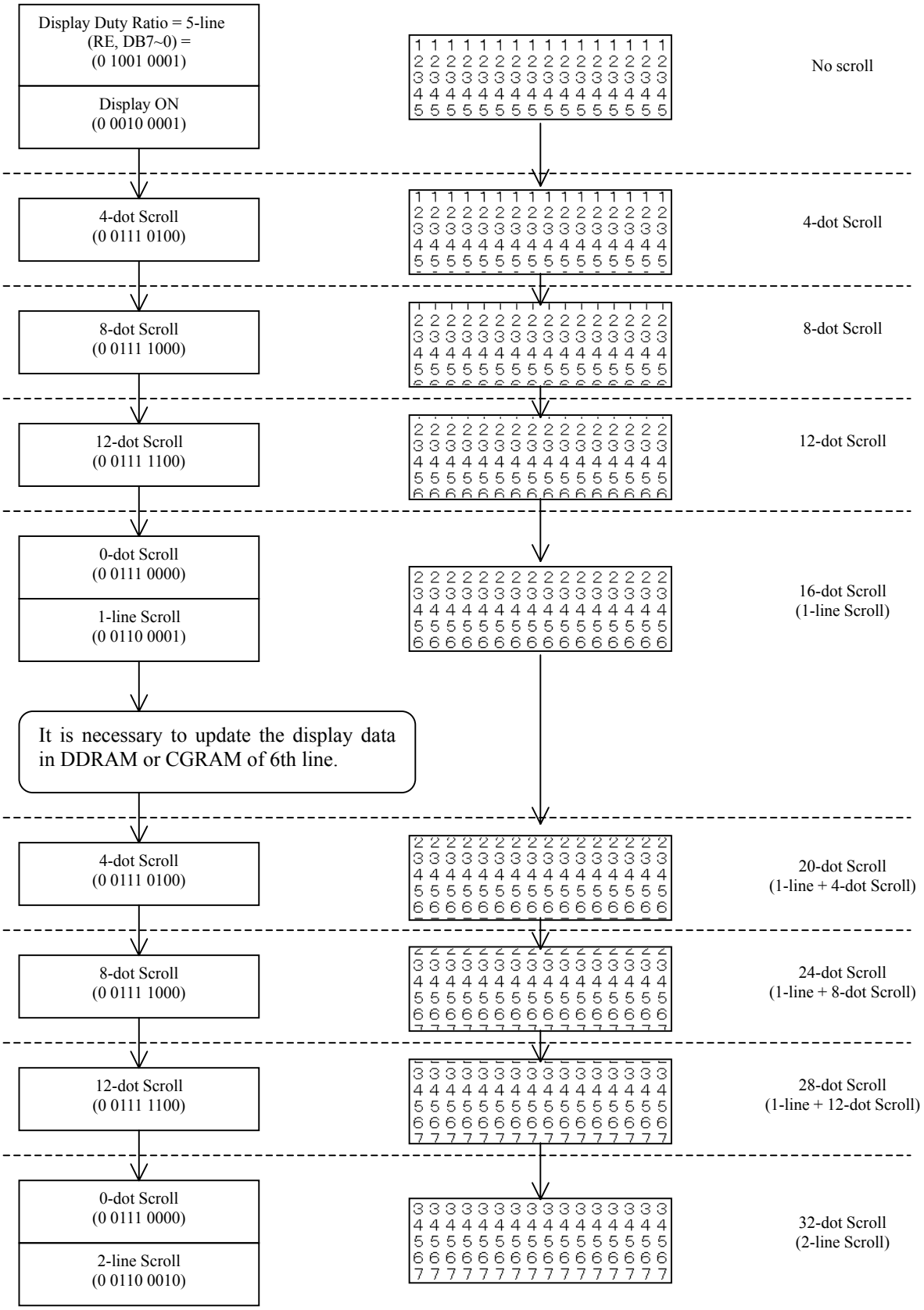
(iii) Scroll Start Line = "1-line"
Scroll Start Row = "0-dot"



(iv) Scroll Start Line = "2-line"
Scroll Start Row = "8-dot"

< Example of 4-dot smooth scroll display >

When the scroll operation to above by 4-dot of the 5-line display, the sequence and the panel image are shown below.

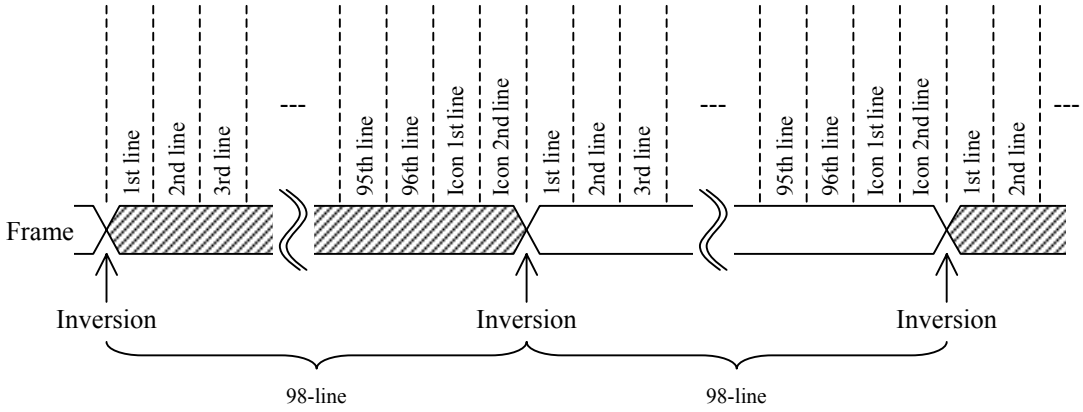


(12) N-LINE INVERSION

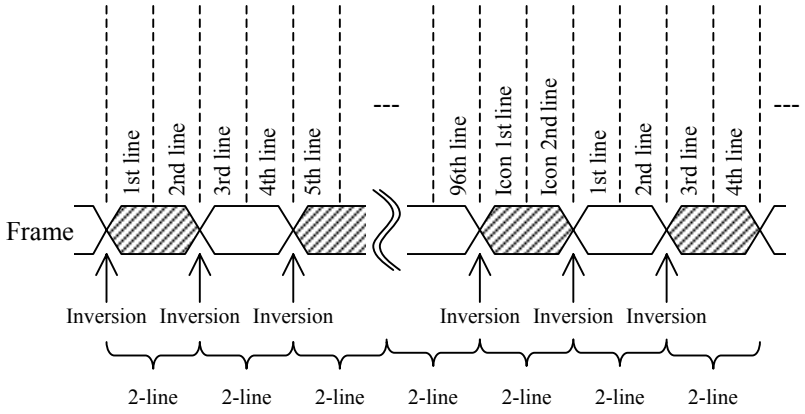
NJU6645 sets the number of inversion line of the alternating signal for LCD to the optional values from 2 ~ 98.

< Setting example >

- N-line inversion = 98-line



- N-line inversion = 2-line



(13) DISPLAY MODE

NJU6645 sets the 3 kinds display mode by the SPR and GR instructions.

(13-1)Character Mode (SPR="0", GR="0")

In the character mode, the font pattern that uses the CGROM and CGRAM is displayed. The font pattern is displayed at the position that corresponds to the DDRAM address by the character code written in DDRAM.

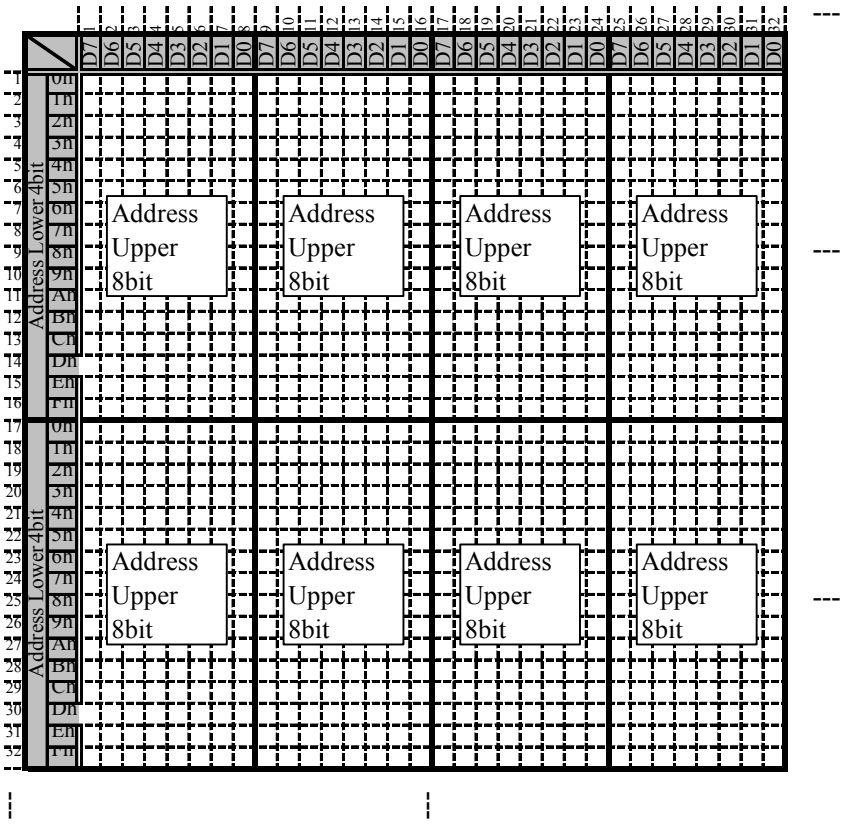
(13-2)Graphics Mode (SPR="0", GR="1")

In the graphics mode, the graphics of maximum 256x96 dots is displayed by using only CGRAM. At this time, the relation between the CGRAM address and the position of display is shown in the following tables. Because all CGRAM is used for graphics, it is not possible to use it as a user font.

Besides, the setting of "Scroll Start Line" and "Scroll Start Row" instructions is not reflected in the graphics mode.

Correspondence of display position on panel and CGRAM address. (In the graphics mode)

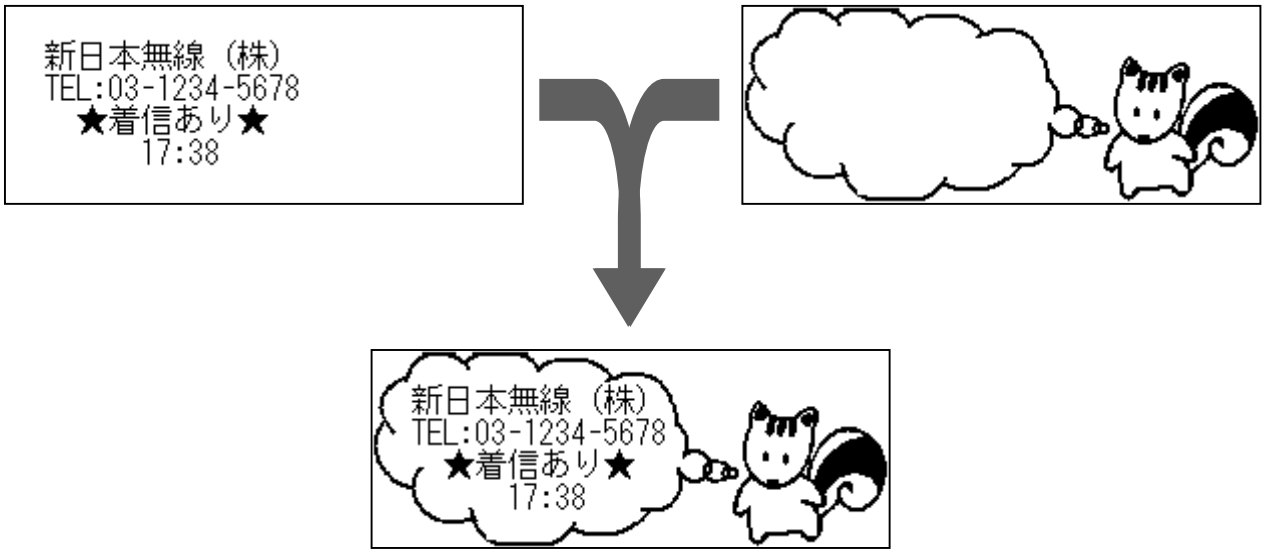
200 ~ 20F	210 ~ 21F	220 ~ 22F	230 ~ 23F	240 ~ 24F	250 ~ 25F	260 ~ 26F	270 ~ 27F	280 ~ 28F	290 ~ 29F	2A0 ~ 2AF	2B0 ~ 2BF	2C0 ~ 2CF	2D0 ~ 2DF	2E0 ~ 2EF	2F0 ~ 2FF	300 ~ 30F	310 ~ 31F	320 ~ 32F	330 ~ 33F	340 ~ 34F	350 ~ 35F	360 ~ 36F	370 ~ 37F	380 ~ 38F	390 ~ 39F	3A0 ~ 3AF	3B0 ~ 3BF	3C0 ~ 3CF	3D0 ~ 3DF	3E0 ~ 3EF	3F0 ~ 3FF
400 ~ 40F	410 ~ 41F	420 ~ 42F	430 ~ 43F	440 ~ 44F	450 ~ 45F	460 ~ 46F	470 ~ 47F	480 ~ 48F	490 ~ 49F	4A0 ~ 4AF	4B0 ~ 4BF	4C0 ~ 4CF	4D0 ~ 4DF	4E0 ~ 4EF	4F0 ~ 4FF	500 ~ 50F	510 ~ 51F	520 ~ 52F	530 ~ 53F	540 ~ 54F	550 ~ 55F	560 ~ 56F	570 ~ 57F	580 ~ 58F	590 ~ 59F	5A0 ~ 5AF	5B0 ~ 5BF	5C0 ~ 5CF	5D0 ~ 5DF	5E0 ~ 5EF	5F0 ~ 5FF
600 ~ 60F	610 ~ 61F	620 ~ 62F	630 ~ 63F	640 ~ 64F	650 ~ 65F	660 ~ 66F	670 ~ 67F	680 ~ 68F	690 ~ 69F	6A0 ~ 6AF	6B0 ~ 6BF	6C0 ~ 6CF	6D0 ~ 6DF	6E0 ~ 6EF	6F0 ~ 6FF	700 ~ 70F	710 ~ 71F	720 ~ 72F	730 ~ 73F	740 ~ 74F	750 ~ 75F	760 ~ 76F	770 ~ 77F	780 ~ 78F	790 ~ 79F	7A0 ~ 7AF	7B0 ~ 7BF	7C0 ~ 7CF	7D0 ~ 7DF	7E0 ~ 7EF	7F0 ~ 7FF
800 ~ 80F	810 ~ 81F	820 ~ 82F	830 ~ 83F	840 ~ 84F	850 ~ 85F	860 ~ 86F	870 ~ 87F	880 ~ 88F	890 ~ 89F	8A0 ~ 8AF	8B0 ~ 8BF	8C0 ~ 8CF	8D0 ~ 8DF	8E0 ~ 8EF	8F0 ~ 8FF	900 ~ 90F	910 ~ 91F	920 ~ 92F	930 ~ 93F	940 ~ 94F	950 ~ 95F	960 ~ 96F	970 ~ 97F	980 ~ 98F	990 ~ 99F	9A0 ~ 9AF	9B0 ~ 9BF	9C0 ~ 9CF	9D0 ~ 9DF	9E0 ~ 9EF	9F0 ~ 9FF
A00 ~ A0F	A10 ~ A1F	A20 ~ A2F	A30 ~ A3F	A40 ~ A4F	A50 ~ A5F	A60 ~ A6F	A70 ~ A7F	A80 ~ A8F	A90 ~ A9F	AA0 ~ AAF	AB0 ~ ABF	AC0 ~ ACF	AD0 ~ ADF	AE0 ~ AEF	AF0 ~ AFF	B00 ~ B0F	B10 ~ B1F	B20 ~ B2F	B30 ~ B3F	B40 ~ B4F	B50 ~ B5F	B60 ~ B6F	B70 ~ B7F	B80 ~ B8F	B90 ~ B9F	BA0 ~ BAF	BB0 ~ BBF	BC0 ~ BCF	BD0 ~ BDF	BE0 ~ BEF	BF0 ~ BFF
C00 ~ C0F	C10 ~ C1F	C20 ~ C2F	C30 ~ C3F	C40 ~ C4F	C50 ~ C5F	C60 ~ C6F	C70 ~ C7F	C80 ~ C8F	C90 ~ C9F	CA0 ~ CAF	CB0 ~ CBF	CC0 ~ CCF	CD0 ~ CDF	CE0 ~ CEF	CF0 ~ CFF	D00 ~ D0F	D10 ~ D1F	D20 ~ D2F	D30 ~ D3F	D40 ~ D4F	D50 ~ D5F	D60 ~ D6F	D70 ~ D7F	D80 ~ D8F	D90 ~ D9F	DA0 ~ DAF	DB0 ~ DBF	DC0 ~ DCF	DD0 ~ DDF	DE0 ~ DEF	DF0 ~ DFF



(13-3)Superimpose mode (SPR="1", GR="*")

The superimpose mode overlaps and displays the character mode and the graphics mode. The displayed data is a logical addition of the character mode data and the graphics mode data. Because all CGRAM is used for graphics, it is not possible to use it as a user font.

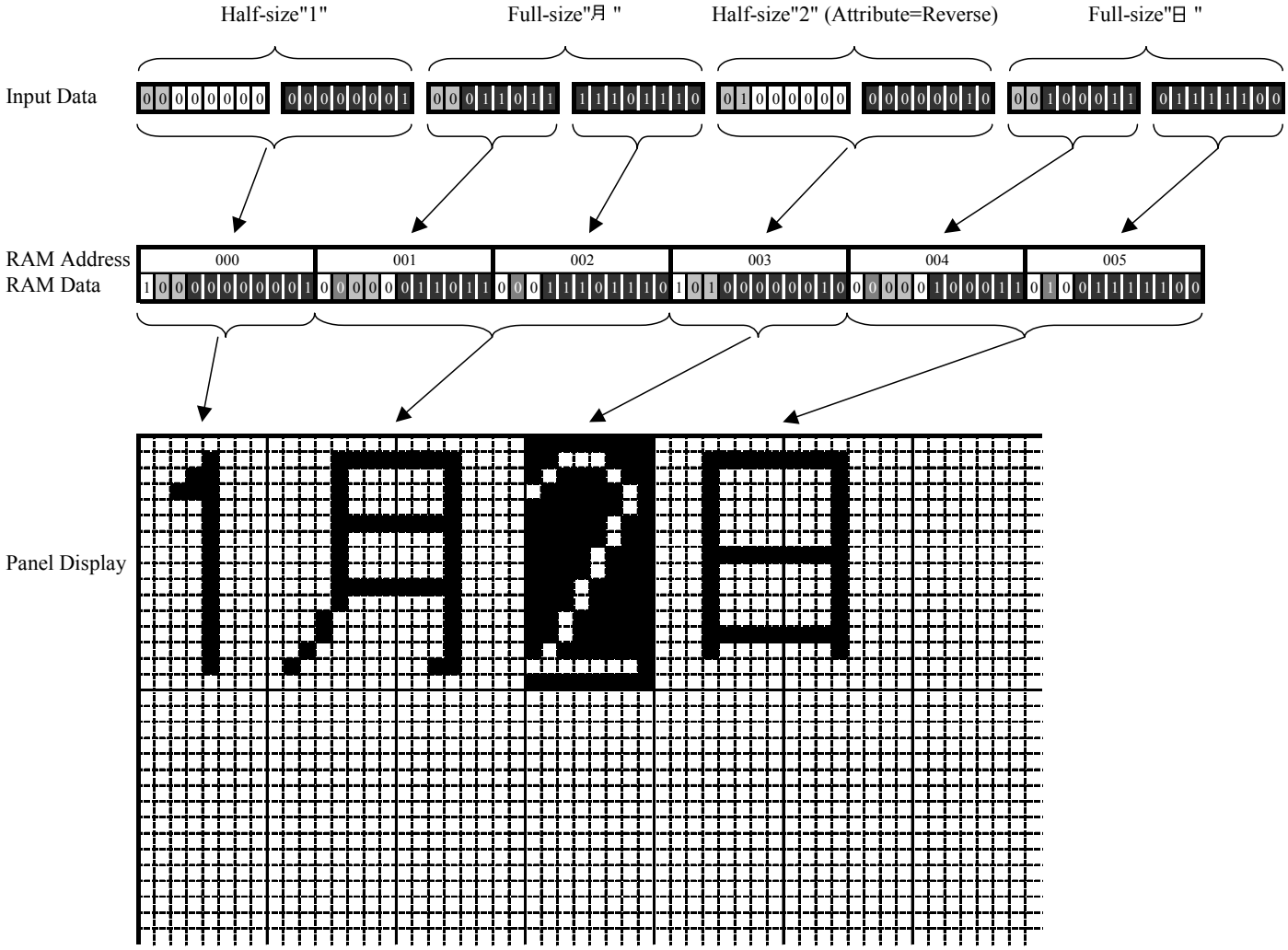
Besides, the setting of "Scroll Start Line" and "Scroll Start Row" instructions is reflected only in the character part, and not reflected in the graphics part.



(14) FULL-SIZE and HALF-SIZE MIXED DISPLAY

NJU6645 displays from the left end of the screen with mixing the full-size character (16 x 16 dots) and the half-size character (8 x 16 dots). The distinction between full-size and half-size is decided by 1st bit of DDRAM data writing of the 2-byte format. In case of the "0", it is the full-size character. In case of the "1", it is the half-size character. 1-character of the full-size character is composed of two DDRAM addresses, and 1-character of the half-size character is composed of one DDRAM address.

The corresponding example of that input data, DDRAM data, and display are shown below.



Note) When the Full-size character is written to the half-size address of the end of line, the character is displayed unexpected. The number of writing characters must become just 32-character at half-size by 1-line.

(15) RESET FUNCTION

The reset function initializes the LSI by setting the RSTb terminal to "L". The reset operation is always required after the power supply is turned on.

The reset status is as follows.

Item	Register	Initial Value
RE Flag : 1st page	RE	0
Address Counter : DDRAM left end of the 1st line	AC	000h
Dot Matrix Display : OFF	D	0
Icon Display : OFF	M	0
Full Screen Reverse Display : OFF	REV	0
Standby mode : OFF	HALT	0
Cursor Display : OFF	C	0
Line Cursor Setting : OFF	LC	0
Blink Setting : OFF	B	0
Reverse Cursor Setting : OFF	BW	0
Display Mode : Character Mode	SPR / GR	0 / 0
Read Modify Write Mode : OFF	RDM	0
Scroll Start Line : 1st line	SSN2,1,0	0,0,0
Scroll Start Row : 1st row	SSL3,2,1,0	0,0,0,0
Display Start Line : 1st line	DST2,1,0	0,0,0
Display Duty Ratio : 6-line	DN2,1,0	0,0,0
N-line Inversion : 98	NL6,5,4,3,2,1,0	1,1,0,0,0,0,1
Driver Output Control : Forward Direction	SEL1,SEL2	0,0
Internal Oscillation / External Clock : Internal OSC	INTCK	0
Internal Capacitance Adjust : Reference Value	OC2,1,0	0,0,0
Discharge : OFF	DIS	0
Voltage Boost Circuit : OFF	DCON	0
Internal Power Circuit : OFF	AMPON	0
Boost Level : No Boost	VU2,1,0	0,0,0
Bias Ratio: 1/11 Bias	BS3,2,1,0	0,0,0,0
Electrical Volume : Low (Minimum value)	EV6,5,4,3,2,1,0	0,0,0,0,0,0,0

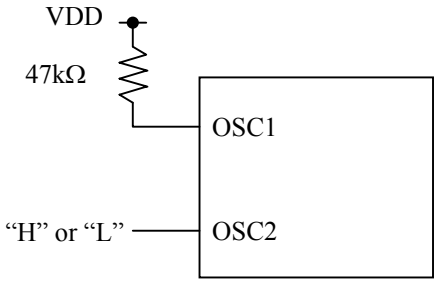
Note) After the resetting, the DDRAM, CGRAM, and MKRAM are not initialized. After the data is written, it is necessary to turn on the display.

(16) OSCILLATION CIRCUIT

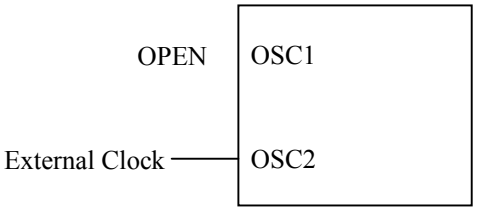
NJU6645 is equipped with the CR oscillation circuit with the external resistor used, and generates internal clocks used for the display timing. The generating method of the clock selects by the internal oscillation or external clock. When the internal oscillation circuit is used, connect OSC1 and VDD with an external resistor. At this time, it is necessary to fix the OSC2 to "H" or "L". The internal capacity value of the internal oscillation circuit is set by the instruction (0.7/0.8/0.9/1/1.1/1.2/1/3 times.). The oscillation frequency is adjusted by setting the internal capacity value.

When the external clock is used, INTCK="1" and the external clock is supplied from the OSC2. At this time, the OSC1 opens.

< Using Internal Oscillation >



< Using External Clock >



(17) POWER SUPPLY CIRCUIT

(17-1)LCD power supply

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator.

If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

The configuration of the LCD power supply is arranged by setting the D1 (AMPON) and D0 (DCON) bits of the "Power Control" instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown below.

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	Note
0	0	Inactive	Inactive	VOUT, VLCD, V1, V2, V3, V4	*1, 3
0	1	Inactive	Active	VOUT	*2, 3
1	1	Active	Active	VDCOUT is supplied to VOUT.	-

Note 1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C1+, C1-, C2+, C2-, C3+, C3-, C4+, C4-, C5+, C5-, VREF, VREG and VEE are open.

Note 2) Only the voltage converter is used. The VOUT is externally supplied, and the C1+, C1-, C2+, C2-, C3+, C3-, C4+, C4-, C5+, C5- and VEE are open. The reference voltage is supplied on the VREF.

Note 3) The following relation among each LCD bias voltages must be maintained.

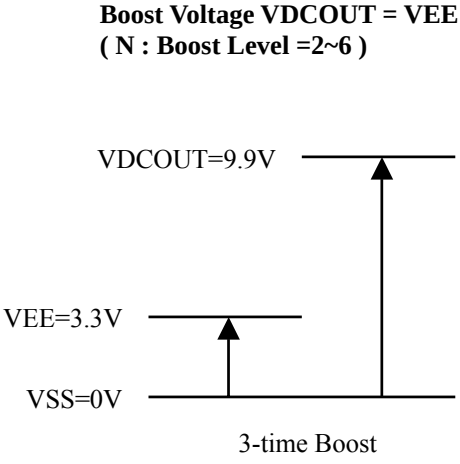
$VOUT \geq VLCD \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$

(17-2) Voltage booster

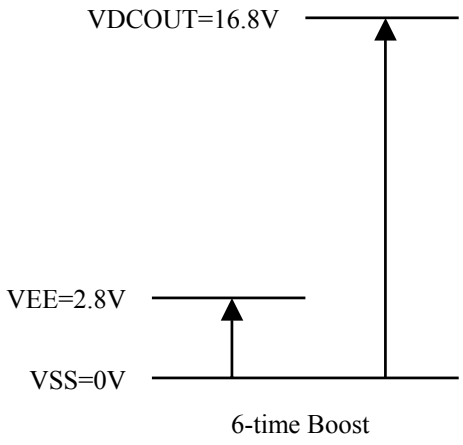
The internal voltage booster generates up to 6xVEE voltage. The boost level is selected from 2x, 3x, 4x, 5x or 6x by setting the D2 to D0 (VU2 to VU0) bits of the "Boost Level" instruction. VDCOUT terminal and VOUT terminal are connected on the outside and used.

The boost voltage VDCOUT must not exceed 17.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

Boost Voltage VDCOUT = VEE x N [V]
(N : Boost Level =2~6)



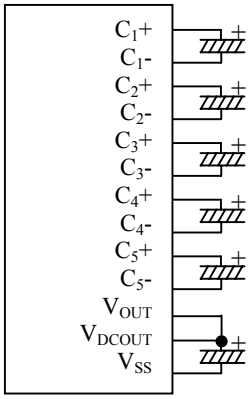
3-time Boost



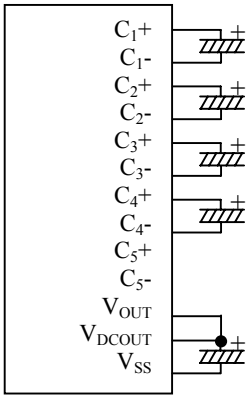
6-time Boost

- External Capacitor Connection of Voltage Booster

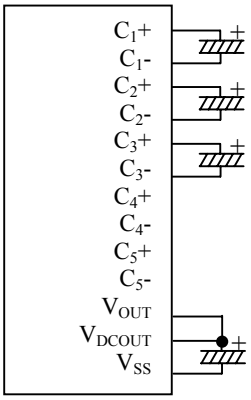
6-time Boost



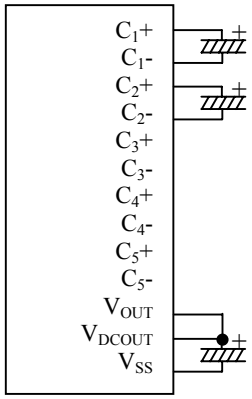
5-time Boost



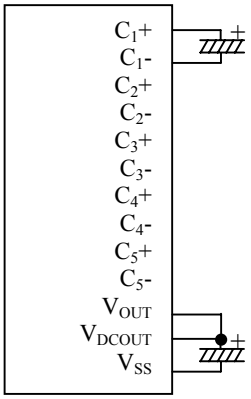
4-time Boost



3-time Boost



2-time Boost



(17-3) Reference voltage generator

The reference voltage generator produces the reference voltage.

Reference Voltage : VBA = 0.75 x VEE

When using the internal LCD power supply, connect the VBA and the VREF, or supply 0.75xVEE or lower voltage on the VREF. When using an external LCD power supply, the VBA should be open.

(17-4) Voltage regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The VREF voltage is multiplied to obtain the VREG voltage, and its multiple (boost level) is set by the D2 to D0 (VU2 to VU0) bits of the "Boost Level" instruction. The formula is shown below.

VREG = VREF x N [V]
(N : Boost Level = 2~6)

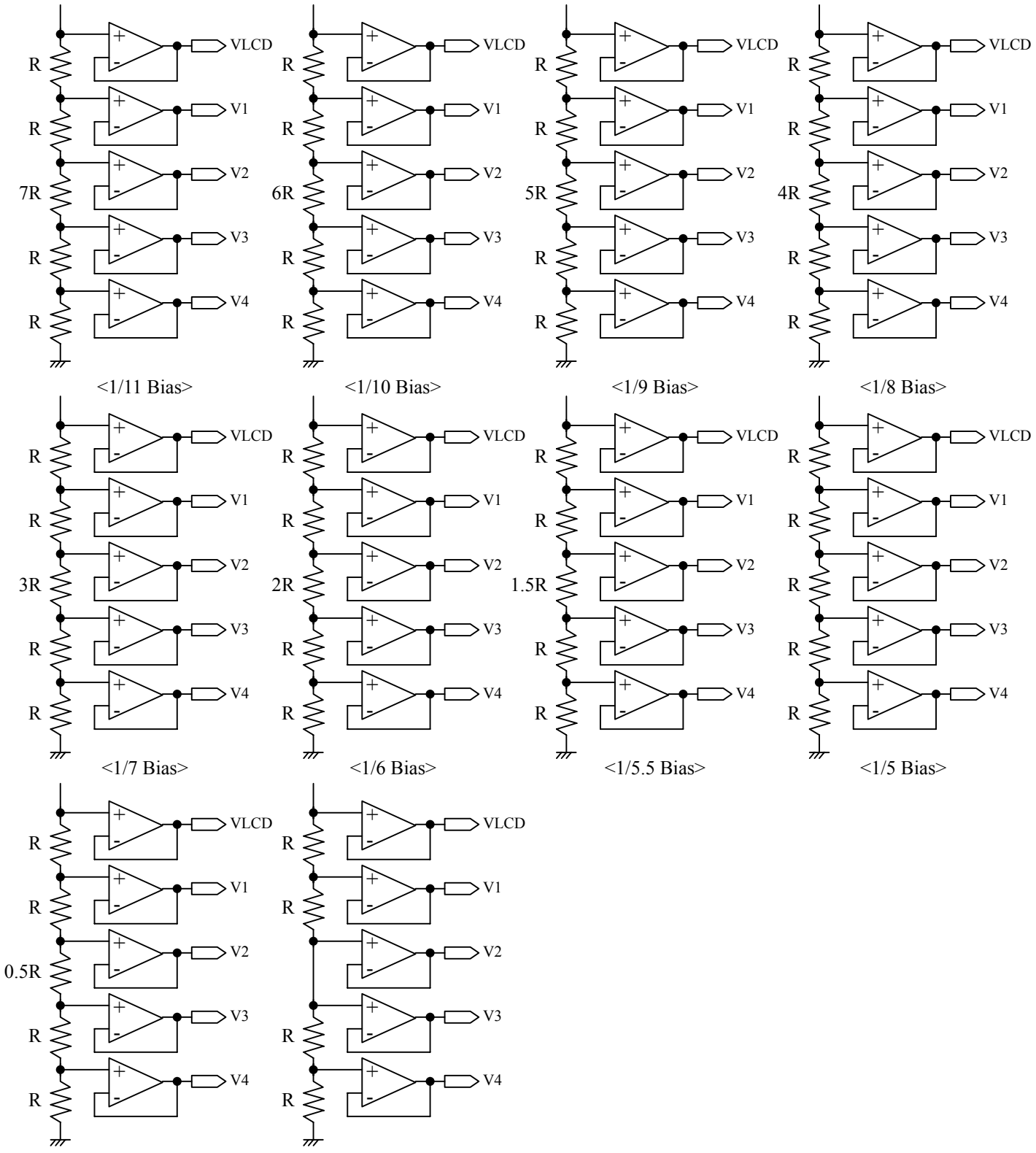
(17-5) Electrical variable Resistor (EVR)

The EVR is used to fine-tune the V LCD voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the D3 to D0 (DV6 to DV0) bits of the "EVR Control" instruction. The formula is shown below.

VLCD = 0.5 x VREG + M(VREG –0.5VREG) / 127 [V]
(M : EVR Value = 0 to 127)

(17-6)LCD bias circuit

The suitable bias is set by the bias register (BS3 to 0) according to the display duty. When the VLCD voltage is close to minimum (nearly equal: 4.5V), it is recommended not to use it because there is a possibility of not operating in 1/11 bias setting.



<1/11 Bias> <1/10 Bias> <1/9 Bias> <1/8 Bias>

<1/7 Bias> <1/6 Bias> <1/5.5 Bias> <1/5 Bias>

<1/4.5 Bias> <1/4 Bias>

Note) R = Reference resistor

LCD Bias Circuit

(17-7)Discharge circuit

The LSI incorporates a discharge circuit for the VLCD and V1 to V4 and for the VOUT. The VLCD and V1 to V4 are discharged by setting "1" at the D0 (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. Be sure to turned off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to “(r) Discharge ON/OFF”.

(17-8)Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to “(21) TYPICAL INSTRUCTION SEQUENCES”.

(i) Power ON/OFF in using external LCD supply

-Power ON

First “VDD and VEE ON”, next “Reset by RSTb”, then “External LCD power supply ON”. When using only external VOUT, first “VDD ON”, next “Reset by RSTb”, then “External VOUT ON”, as well.

-Power OFF

First “Reset by RSTb or “HALT” instruction” to isolate external LCD bias voltage, next “VDD OFF”. For more safety, placing a resistor in series on the VLCD line (or the VOUT line in using only the external VOUT) is recommended. That resistance is usually between 50Ω and 100Ω.

(ii) Power ON/OFF in using internal LCD supply

-Power ON

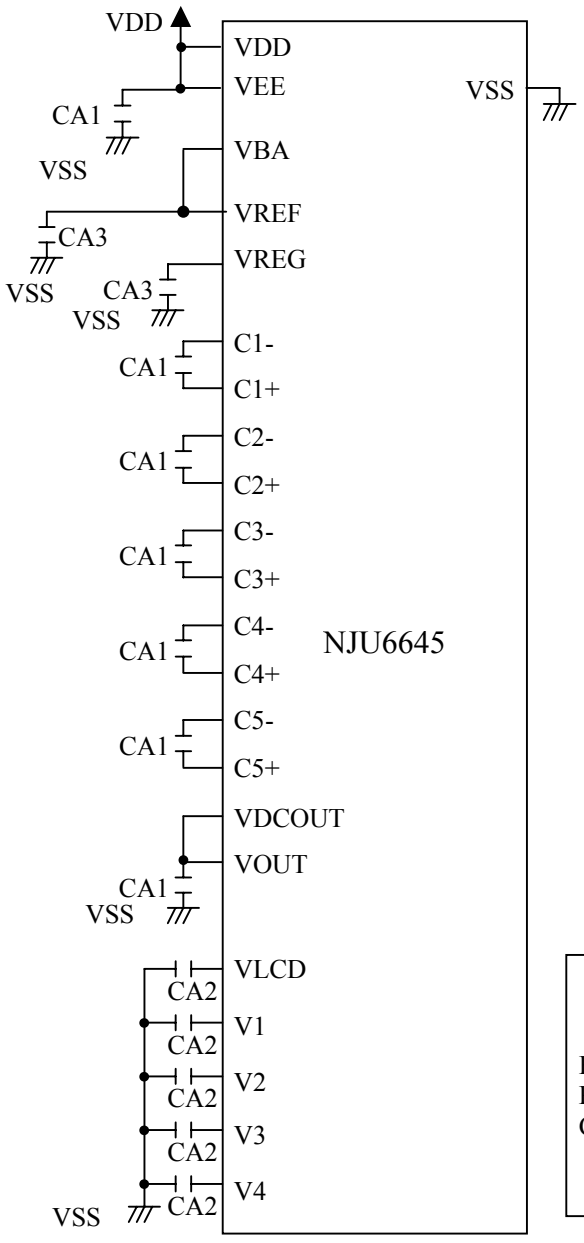
First “VDD and VEE ON”, next “Reset by RSTb”, then “Internal LCD power supply ON”. Be sure to execute the “Display ON” instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

-Power OFF

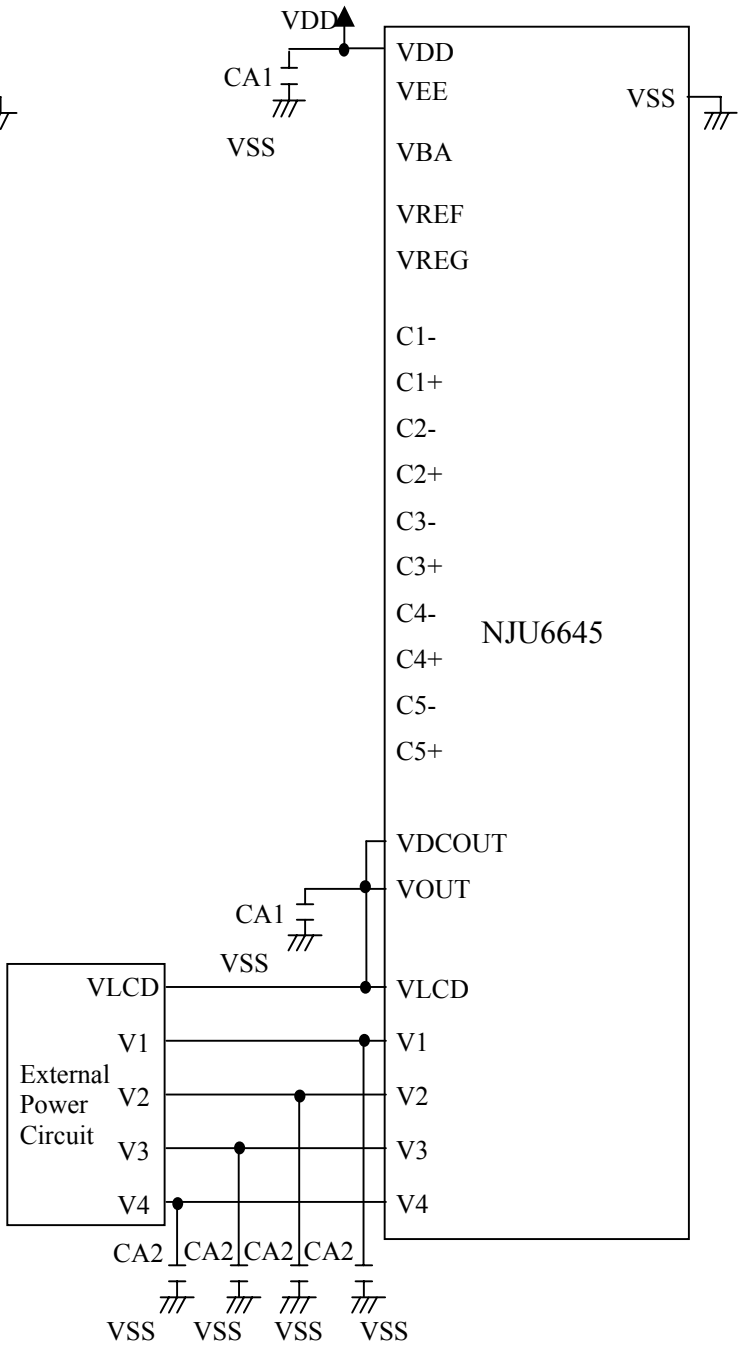
First “Reset by RSTb or “HALT” instruction”, next “VDD and VEE OFF”. If using different power sources for the VDD and the VEE individually, the VEE must be turned off after the reset or the “HALT”. After that, the VDD can be turned off, waiting until the LCD bias voltages (VLCD, V1, V2, V3 and V4) drop below the threshold level of LCD pixels.

- External Components for LCD Power Supply

Using Only Internal LCD Power Supply (6x boost)



Using Only External LCD Power Supply



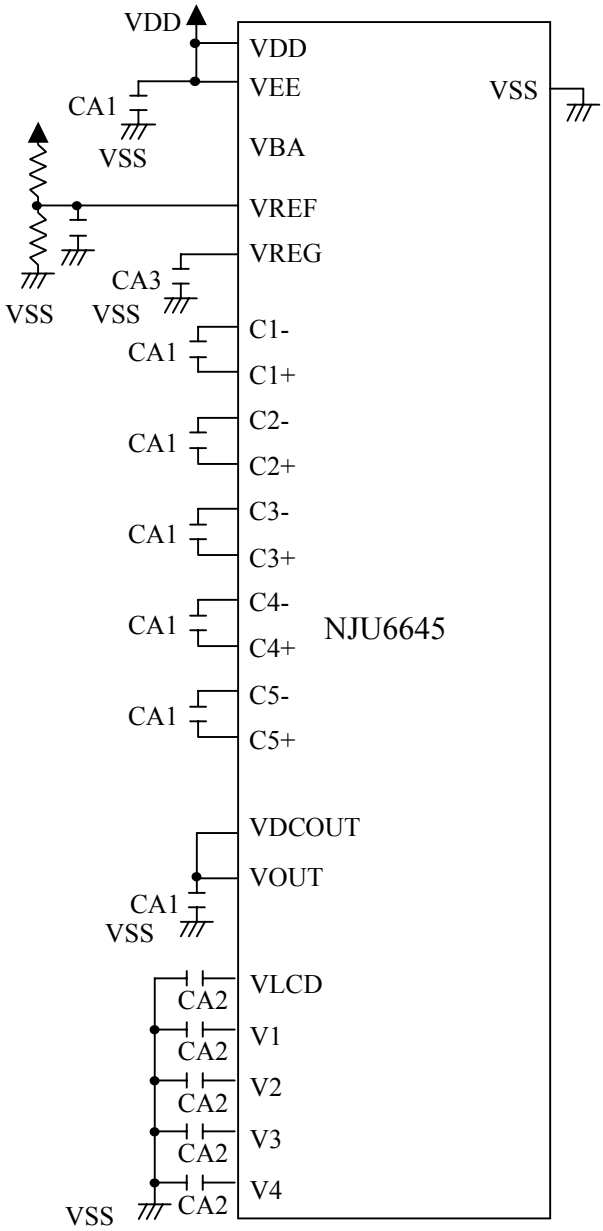
Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

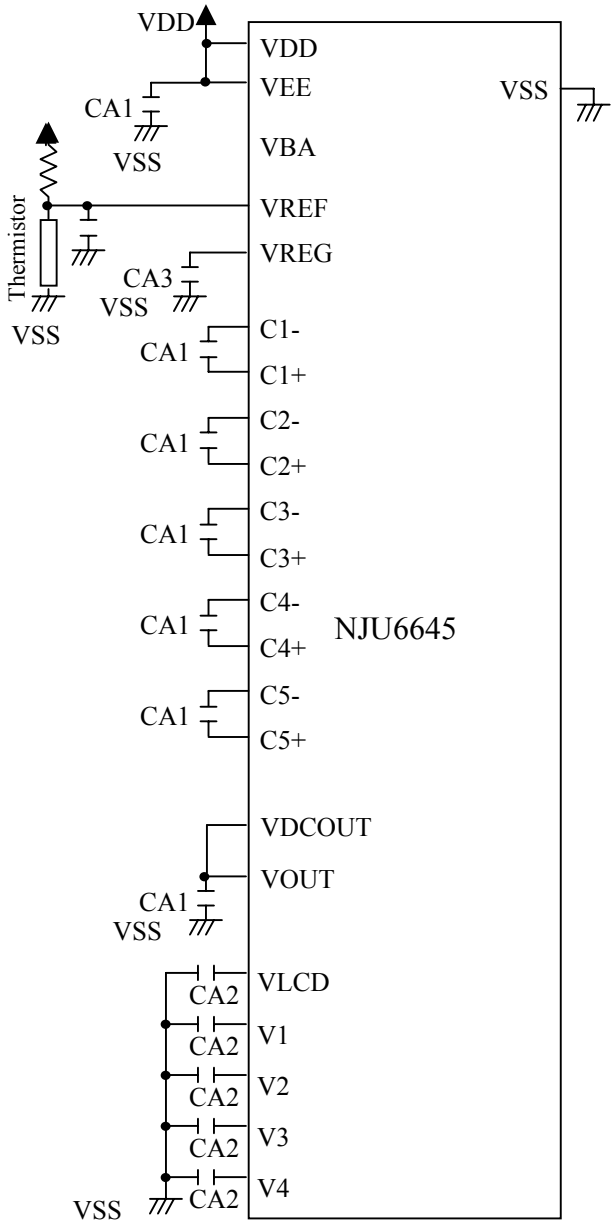
Note 1) B grade capacitor is recommended for CA1 to CA3. Make sure what is the best capacitor value in the particular application.

Note 2) Parasitic resistance on the power supply lines (VDD, VSS, VEE, VOUT, VLCD, V1, V2, V3 and V4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply Without Reference Voltage Generator (1)
(6x boost)



Using Internal LCD Power Supply Without Reference Voltage Generator (2)
(6x boost)



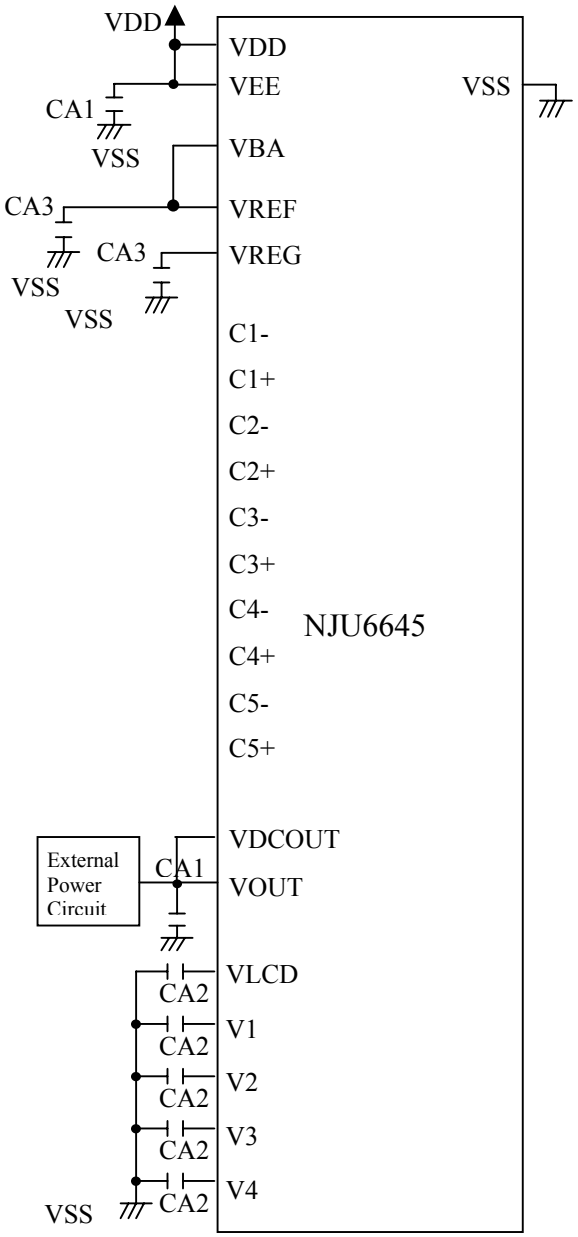
Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

Note 1) B grade capacitor is recommended for CA1 to CA3. Make sure what is the best capacitor value in the particular application.

Note 2) Parasitic resistance on the power supply lines (VDD, VSS, VEE, VOUT, VLCD, V1, V2, V3 and V4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply Without Voltage Booster



Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

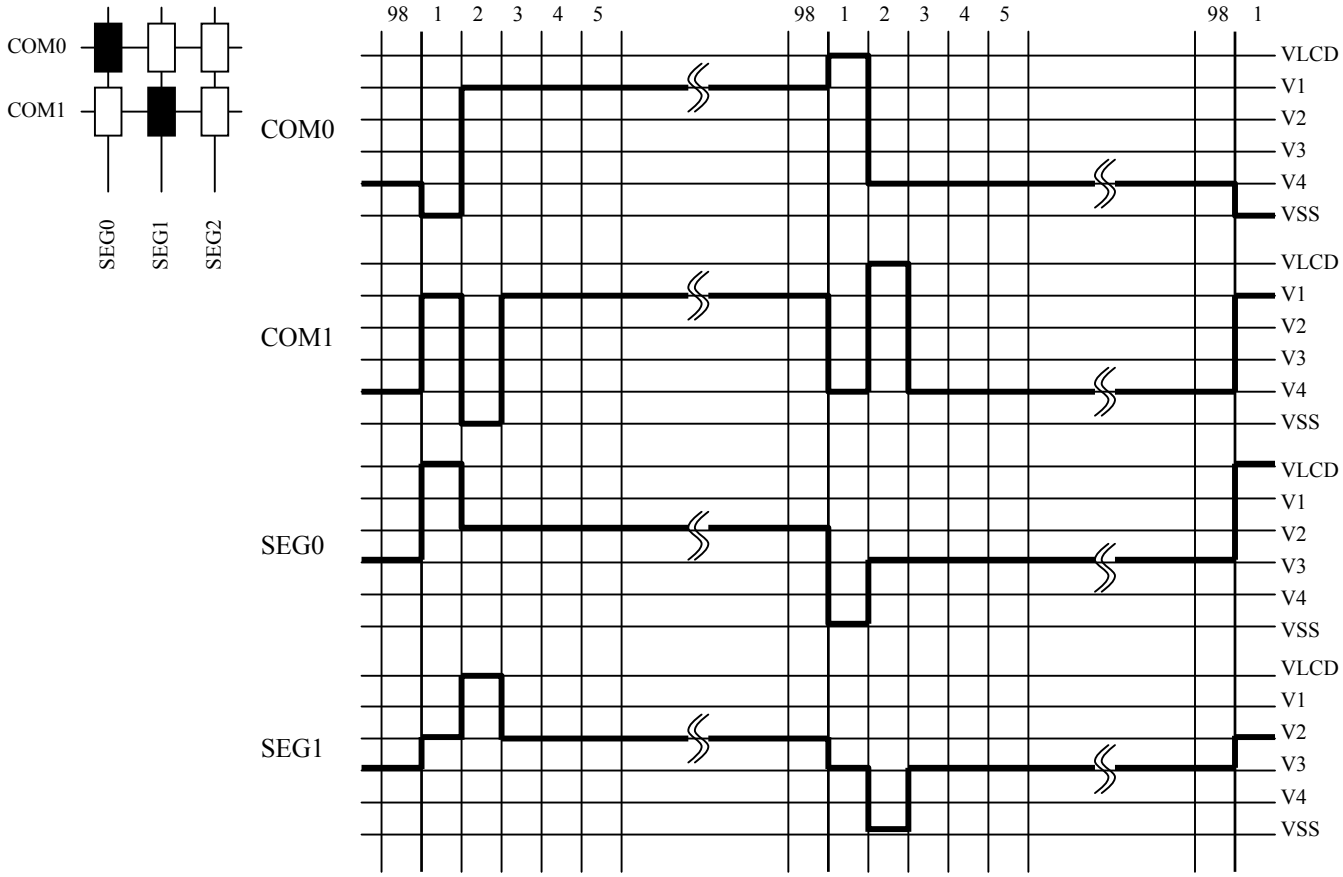
Note 1) B grade capacitor is recommended for CA1 to CA3. Make sure what is the best capacitor value in the particular application.

Note 2) Parasitic resistance on the power supply lines (VDD, VSS, VEE, VOUT, VLCD, V1, V2, V3 and V4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(18) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 256-segment drivers and 98-common drivers. 2 out of 98-common drivers are assigned to the COMMK0 and COMMK1 for an icon display. The common drivers generates LCD driving waveforms formed on the VLCD, V1, V4 and VSS levels. The segment drivers generates waveforms formed on the VLCD, V2, V3 and VSS levels.

(19) LCD DRIVING WAVEFORMS



(20) INSTRUCTION
Instruction Tables (1/2)

	Instruction	RE	RS	RW	Code D7	D6	D5	D4	D3	D2	D1	D0	Default	Description
a	RAM Data Write	*	1	0	DDRAM, CGRAM, MKRAM Data								-	
b	RAM Data Read	*	1	1	DDRAM, CGRAM, MKRAM Data								-	
c	Status Read	*	0	1	BF	NF2	NF1	NF0	LF3	LF2	LF1	LF0	-	BF: Busy Flag NF: Display Line at present LF: Display Row at present

* : Don't care

	Instruction	RE	RS	RW	Code D7	D6	D5	D4	D3	D2	D1	D0	Default	Description
d	Display Clear (Note)	0	0	0	0	0	0	0	0	0	0	1	-	Writing the half-size space code "0020h" into all DDRAM. Setting the DDRAM address "000h" into address counter. Execution time is required.
e	Cursor Home	0	0	0	0	0	0	1	0	0	0	1	-	Setting the DDRAM address "000h" into address counter. Initialization the Scroll Start Line and the Scroll Start Row.
f	Display Control	0	0	0	0	0	1	0	ALL ON	REV	M	D	000	ALLON: All pixels ON/OFF REV: Full Screen Reverse Display ON/OFF M: Icon Display ON/OFF D: Dot Matrix Display ON/OFF
g	Standby	0	0	0	0	0	1	1	*	*	*	HALT	0	
h	Cursor Display	0	0	0	0	1	0	0	BW	B	LC	C	0000	BW: Reverse Cursor B: Blink LC: Line Cursor C: Cursor
i	Display / Entry Mode	0	0	0	0	1	0	1	*	SPR	GR	RDM	000	SPR: Superimpose Mode GR: Graphics Mode RDM: Read Modify Write
j	Scroll Start Line	0	0	0	0	1	1	0	*	SSN2	SSN1	SSN0	000	
k	Scroll Start Row	0	0	0	0	1	1	1	SSL3	SSL2	SSL1	SSL0	0000	
l	Display Start Line	0	0	0	1	0	0	0	*	DST2	DST1	DST0	000	
m	Display Duty Ratio	0	0	0	1	0	0	1	*	DN2	DN1	DN0	000	
n	N-line Inversion (Upper)	0	0	0	1	0	1	0	*	NL6	NL5	NL4	110	
	N-line Inversion (Lower)	0	0	0	1	0	1	1	NL3	NL2	NL1	NL0	0001	
o	Driver Output Control	0	0	0	1	1	0	0	*	*	SEL1	SEL2	00	SEL1: COM Shift Direction Set SEL2: SEG Output Direction Set
p	Oscillation Control	0	0	0	1	1	0	1	INT CK	OC2	OC1	OC0	0000	INTCK: Internal OSC / External Clock OC2,1,0: Internal Capacitance Adjust
q	RE Flag	*	0	0	1	1	1	1	*	*	*	RE	0	RE Flag Set

* : Don't care

Note) The Execution time of "Display Clear" can't be neglected. (Please refer to p.80 "Status Read" and p.81 "Display Clear" execution time.

Instruction Tables (2/2)

Instruction					Code								Default	Description
		RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0		
r	Discharge	1	0	0	0	0	0	0	*	*	*	DIS	0	
s	Boost Level	1	0	0	0	0	0	1	*	VU2	VU1	VU0	000	VU2,1,0: Boost Level
t	Bias Ratio	1	0	0	0	0	1	0	BS3	BS2	BS1	BS0	0000	
u	Electrical Volume (Upper)	1	0	0	0	0	1	1	*	EV6	EV5	EV4	000	
	Electrical Volume (Lower)	1	0	0	0	1	0	0	EV3	EV2	EV1	EV0	0000	
v	Power Control	1	0	0	0	1	0	1	*	*	AMP ON	DC ON	00	AMPON: Internal Operational Amplifier ON/OFF DCON: Voltage Boost Circuit ON/OFF
w	RAM Address Set 1	1	0	0	0	1	1	0	AD3	AD2	AD1	AD0	0000	RAM Address 4bit (AD3 to AD0)
	RAM Address Set 2	1	0	0	0	1	1	1	AD7	AD6	AD5	AD4	0000	RAM Address 4bit (AD7 to AD4)
	RAM Address Set 3	1	0	0	1	0	0	0	AD11	AD10	AD9	AD8	0000	RAM Address 4bit (AD11 to AD8)
x	Address Shift	1	0	0	1	0	0	1	*	*	*	ARL	-	ARL="0" Address -1 ARL="1" Address +1
y	Maker Test 1	1	0	0	1	0	1	0	TS3	TS2	TS1	TS0	-	Maker Test Instruction (Not used usually.)
	Maker Test 2	1	0	0	1	0	1	1	TS7	TS6	TS5	TS4	-	
	Maker Test 3	1	0	0	1	1	0	0	TS11	TS10	TS9	TS8	-	
	Maker Test 4	1	0	0	1	1	0	1	*	*	TS13	TS12	-	
	Maker Test 5	1	0	0	1	1	1	0	TSM3	TSM2	TSM1	TSM0	-	
q	RE Flag	*	0	0	1	1	1	1	*	*	*	RE	0	RE Flag Set

* : Don't care

< Instruction Descriptions >

(a) RAM Data Write

The "RAM Data Write" instruction writes display data on a specified address. The address is incremented automatically by "Display / Entry Mode" instruction.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
*	1	0	WRITE DATA							

(b) RAM Data Read

The "RAM Data Read" instruction reads out display data from a specified address. The address is incremented automatically by "Display / Entry Mode" instruction.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
*	1	1	READ DATA							

(c) Status Read

The "Status Read" instruction reads out Busy Flag(BF) , Display Line (NF[2:0]) and Display Row(LF[3:0]) numbers that are selected on the display scanning at this moment. When the BF is "1", it indicates the NJU6645 is executing a instruction internally, and no instruction except "Status Read" will be accepted. Any instruction except "Status Read" should be input when the BF is "0" or after the last instruction has been comoleted. However any instruction except "Display Clear" could be input without checking BF nor considering instruction execution time if the system cycle time satisfies the AC charactristic specification.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
*	0	1	BF	NF2	NF1	NF0	LF3	LF2	LF1	LF0

- Busy Flag Read

BF	Internal Operation
0	Instruction is enable
1	Operating (Instruction is disabled)

- Display Line Read

NF	Display Line
000	1st line
001	2nd line
010	3rd line
011	4th lint
100	5th line
101	6th line
110	-
111	-

- Display Row Read

LF	Display Row
0000	1st row
0001	2nd row
0010	3rd row
0011	4th row
0100	5th row
0101	6th row
0110	7th row
0111	8th row
1000	9th row
1001	10th row
1010	11th row
1011	12th row
1100	13th row
1101	14th row
1110	15th row
1111	16th row

(d) Display Clear

When the "Display Clear" instruction is executed, the Half-size space code "0020h" is written into every DD RAM address, the DD RAM address "000h" is set into the address counter. The MK RAM / CG RAM data is unchanged.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	1

・ Display Clear execute time.

The Execution time is required at “Display Clear” instruction as shown in below.
When the internal circuits are in the operation mode, the busy flag (BF) = “1”, and any instruction reading is inhibited by status read.

Display Line	Clock Count	Execute Time	Execute. Time @1MHz
1 Line	5766*FOSC	5766*(1/FOSC)	5.766ms
2 Line	2883*FOSC	2883*(1/FOSC)	2.883ms
3 Line	1922*FOSC	1922*(1/FOSC)	1.922ms
4 to 6 Line	961*FOSC	961*(1/FOSC)	0.961ms

(e) Cursor Home

When the "Cursor Home" instruction is executed, the DD RAM address "000h" is set into the address counter. The Scroll Start Line and the Scroll Start Row are set to default. The DD RAM contents are unchanged.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	0	0	1

(f) Display Control

The "Display Control" instruction controls the Dot Matrix Display ON/OFF, the Icon Display ON/OFF, the Full Screen Reverse Display ON/OFF and All Pixels ON/OFF. The Icon Display ON/OFF and the Dot Matrix Display ON/OFF are controlled separately. When the M=”0” and D=”0”, common / segment drivers are turning OFF and output VSS level.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	ALLON	REV	M	D

- All Pixels ON/OFF

ALLON	Display
0	Normal display
1	All ON display (Both dot matrix and Icon display)

- Full Screen Reverse Display ON/OFF

REV	Display
0	Normal display
1	Full screen reverse display

- Icon Display ON/OFF

M	Icon Display
0	OFF
1	ON

- Dot Matrix Display ON/OFF

D	Dot Matrix Display
0	OFF
1	ON

(g) Standby

The "Standby" instruction controls the Standby mode ON/OFF.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	*	*	*	HALT

HALT	Function
0	OFF (Normal mode)
1	ON (Standby mode)

During the standby ON, operating current is down to the standby level. The internal state of the LSI in the standby mode is listed below.

- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at VSS level.
- External clock to the OSC2 cannot be accepted.
- Voltage booster is halted.
- Display data in the DDRAM and data in the instruction registers are being maintained.
- VLCD, V1, V2, V3 and V4 are in high impedance.

In the standby ON sequence, execute the "Display OFF" prior to the "Standby ON". In the standby OFF sequence, execute the "Standby OFF" prior to the "Display ON". If the "Standby ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

(h) Cursor Display

The "Cursor Display" instruction controls the Cursor ON/OFF, the Line Cursor ON/OFF and display method.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	BW	B	LC	C

BW	B	LC	C	Display State
*	*	*	0	Cursor OFF
0	0	0	1	Underline cursor (Character unit)
0	1	0	1	Black blink cursor (Character unit)
1	0	0	1	Reverse blink cursor (Character unit)
1	1	0	1	Inhibited
0	0	1	1	Underline cursor (Line unit)
0	1	1	1	White blink cursor (Line unit)
1	0	1	1	Reverse cursor (Line unit)
1	1	1	1	Inhibited

(i) Display Mode / Entry Mode

The "Display Mode / Entry Mode" instruction controls the Display Mode and Entry Mode.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	*	SPR	GR	RDM

- Display Mode

SPR	GR	Display state
0	0	Character Mode
0	1	Graphics Mode
1	*	Superimpose Mode

- Read Modify Write Mode

RDM	Function
0	OFF (Auto increment in writing and reading display data)
1	ON (Auto increment in writing display data only)

(j) Scroll Start Line

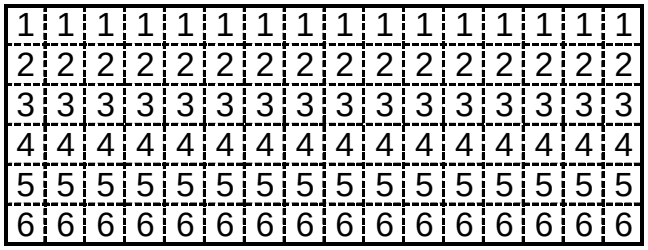
The "Scroll Start Line" instruction controls the Display Line from COM0 output.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	*	SSN2	SSN1	SSN0

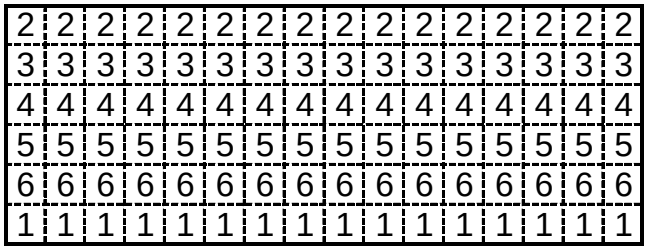
SSN2	SSN1	SSN0	Scroll Start Line
0	0	0	1st line
0	0	1	2nd line
0	1	0	3rd line
0	1	1	4th line
1	0	0	5th line
1	0	1	6th line
1	1	*	Inhibited

- Example of Display

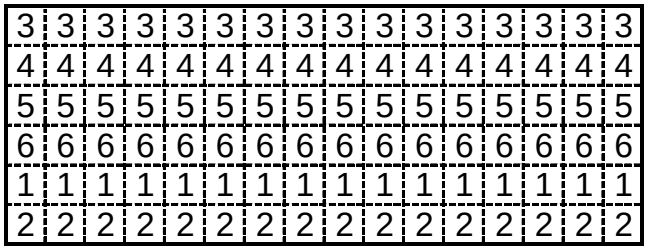
SSN="000" (Default)



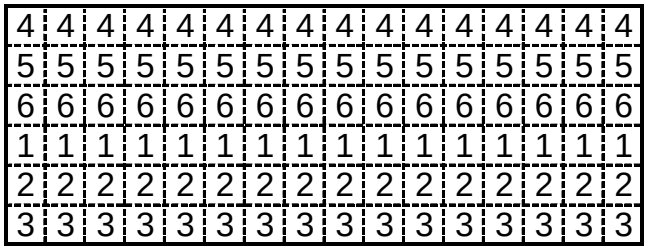
SSN="001"



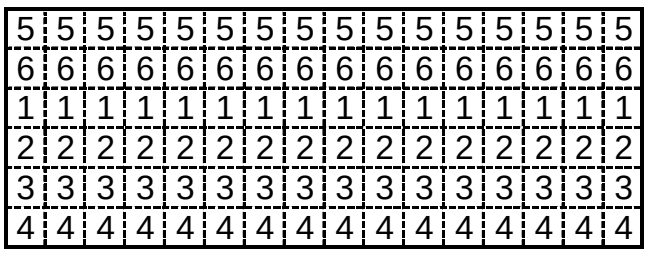
SSN="010"



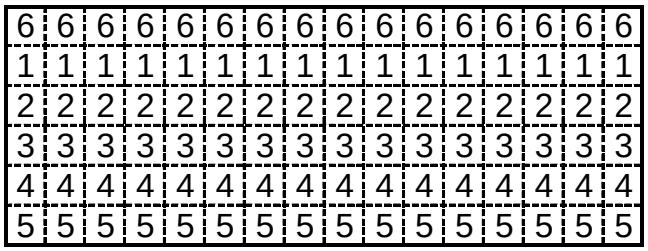
SSN="011"



SSN="100"



SSN="101"



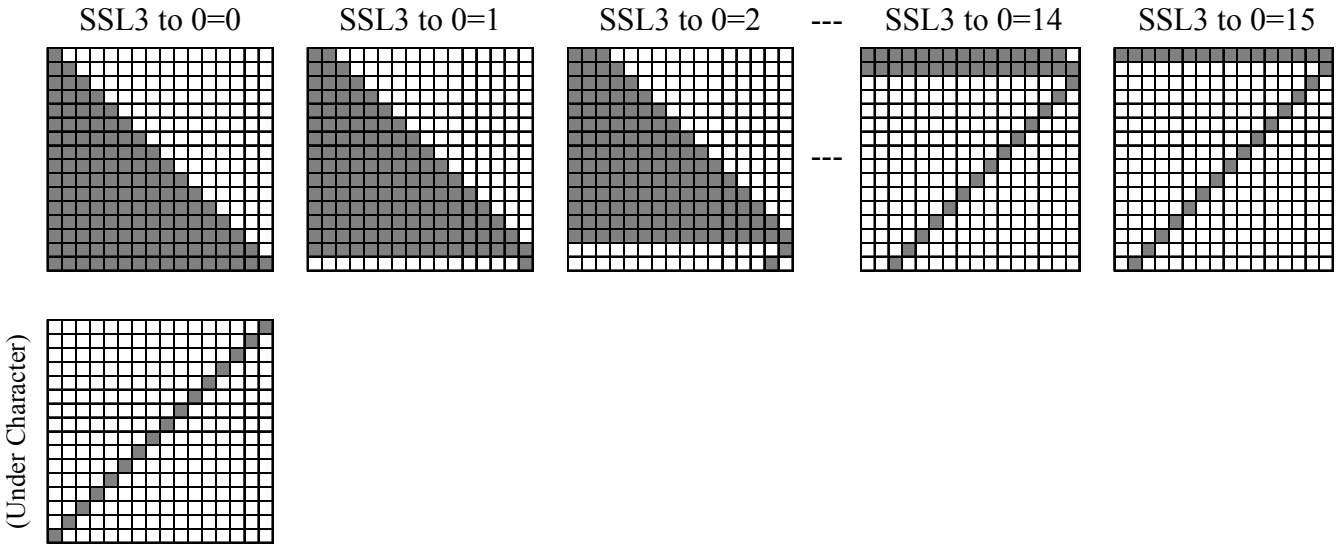
(k) Scroll Start Row

The "Scroll Start Row" instruction controls number of the Scroll Start Row.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	SSL3	SSL2	SSL1	SSL0

SSL3	SSL2	SSL1	SSL0	Scroll Start Row
0	0	0	0	1st row
0	0	0	1	2nd row
0	0	1	0	3rd row
0	0	1	1	4th row
		:		:
1	1	1	1	16th row

- Example of Display



(l) Display Start Line

The "Display Start Line" instruction controls the Display Start Line. The displayed data of the 1st line shifts to the setting line.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	*	DST2	DST1	DST0

DST2	DST1	DST0	Display Start Line
0	0	0	1st line
0	0	1	2nd line
0	1	0	3rd line
0	1	1	4th line
1	0	0	5th line
1	0	1	6th line
1	1	*	Inhibited

- Example of Display

DST=”000”
(Default)

1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6

DST=”001”

6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5

DST=”010”

5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4

DST=”011”

4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3

DST=”100”

3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2

DST=”101”

2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(m) Display Duty Ratio

The "Display Duty Ratio" instruction controls the number of display line, and is used to carry out the partial display.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	*	DN2	DN1	DN0

DN2	DN1	DN0	Display Line (Duty)
0	0	0	6-line (1/98 Duty)
0	0	1	5-line (1/82 Duty)
0	1	0	4-line (1/66 Duty)
0	1	1	3-line (1/50 Duty)
1	0	0	2-line (1/34 Duty)
1	0	1	1-line (1/18 Duty)
1	1	*	Inhibited

(n) N-line Inversion

The "N-line Inversion" instruction controls the number of inversion line. The setting range are 2 to 98 lines, and is alternated by setting (N+1).

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	*	NL6	NL5	NL4

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	NL3	NL2	NL1	NL0

NL6	NL5	NL4	NL3	NL2	NL1	NL0	Inversion Line
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
0	0	0	0	0	1	1	4
:							:
1	1	0	0	0	0	0	97
1	1	0	0	0	0	1	98
:							Inhibited
1	1	1	1	1	1	1	

(o) Driver Output Control

The "Driver Output Control" instruction controls the SEG / COM driver output direction.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	*	*	SEL1	SEL2

SEL1	Function
0	COM scan forward direction
1	COM scan backward direction

SEL2	Function
0	SEG output forward direction
1	SEG output backward direction

(p) Oscillation Control

The "Oscillation Control" instruction controls the system clock type and the internal capacitance of internal oscillation circuits. The frame frequency is adjusted by internal capacitance setting. When the frame frequency is set by this instruction, make sure what is the best setting in the particular application.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	1	INTCK	OC2	OC1	OC0

INTCK	Function
0	Internal oscillation circuit
1	External oscillation input

OC2	OC1	OC0	Internal Capacitance
0	0	0	Reference capacitance
0	0	1	0.7 x Reference capacitance
0	1	0	0.8 x Reference capacitance
0	1	1	0.9 x Reference capacitance
1	0	0	1.1 x Reference capacitance
1	0	1	1.2 x Reference capacitance
1	1	0	1.3 x Reference capacitance
1	1	1	Inhibited

(q) RE Flag Set

The "RE Flag Set" instruction controls the access to the expanded register. When it accesses each instruction, it is necessary to set the RE flag in advance.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
*	0	0	1	1	1	1	*	*	*	RE

(r) Discharge

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the VLCD, V1, V2, V3, V4 and VSS. This instruction prevents the unknown display at the power supply off.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	*	*	*	DIS

DIS	Function
0	Discharge OFF
1	Discharge ON

(s) Boost Level

The "Boost Level" instruction controls the level of Voltage Boost Circuit..

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	*	VU2	VU1	VU0

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	6 times
1	1	0	Inhibited
1	1	1	

(t) Bias Ratio

The "Bias Ratio" instruction controls the Bias Ratio.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	BS3	BS2	BS1	BS0

BS3	BS2	BS1	BS0	Bias Ratio
0	0	0	0	1/11
0	0	0	1	1/10
0	0	1	0	1/9
0	0	1	1	1/8
0	1	0	0	1/7
0	1	0	1	1/6
0	1	1	0	1/5.5
0	1	1	1	1/5
1	0	0	0	1/4.5
1	0	0	1	1/4
1	0	1	0	Inhibited
:				
1	1	1	1	

(u) Electrical Volume

The "Electrical Volume" instruction adjusts VLCD to optimize display contrast. The voltage divided into 127 is set. The setting order requires upper byte first.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	1	*	EV6	EV5	EV4

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	EV3	EV2	EV1	EV0

EV6	EV5	EV4	EV3	EV2	EV1	EV0	Output Voltage
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
:							:
1	1	1	1	1	1	0	
1	1	1	1	1	1	1	High

This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high VLCD. The setting order is upper byte first, then lower byte.

Note) When the electrical volume setting is changed to wide range at keeping display on, there is possibility that the unknown display appears. In this case, add waiting time and change the electrical volume value gradually.

< Example of the changing from EV=80 to EV=110 at keeping display on >
EV=80 → Wait (~ms) → EV=90 → Wait (~ms) → EV=100 → Wait (~ms) → EV=110

* The wait time and electrical volume setting range is different depending on the capacitance value of V1 to V4 and the panel size. Please make sure what is the best setting in the particular application.

(v) Power Control

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	*	*	AMPON	DCON

AMPON : This instruction controls ON/OFF of the operational amplifier parts of the internal power supply circuits (Voltage regulator, electrical variable resistor, and voltage converter).

AMPON	Function
0	Internal operational amplifier OFF
1	Internal operational amplifier ON

DCON : This instruction controls Internal Voltage Booster ON/OFF,

DCON	Function
0	Voltage booster OFF
1	Voltage booster ON

(w) RAM Address Set

The "RAM Address Set" instruction specifies the DDRAM, CGRAM, and MKRAM address.
The RAM address should set lower 4-bit (AD3 to AD0) at first. This instruction is finally effective when upper 4-bit (AD11 to AD8) are transmitted.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	AD3	AD2	AD1	AD0

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	1	AD7	AD6	AD5	AD4

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	AD11	AD10	AD9	AD8

(x) Address Shift

The "Address Shift" instruction controls increment (+1) or decrement (-1) of the address. The address moves whenever this instruction is executed.

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	*	*	*	ARL

ARL	Function
0	Address –1
1	Address +1

(y) Maker Test

This instruction is using for device testing mode. Please do not use this instruction usually.

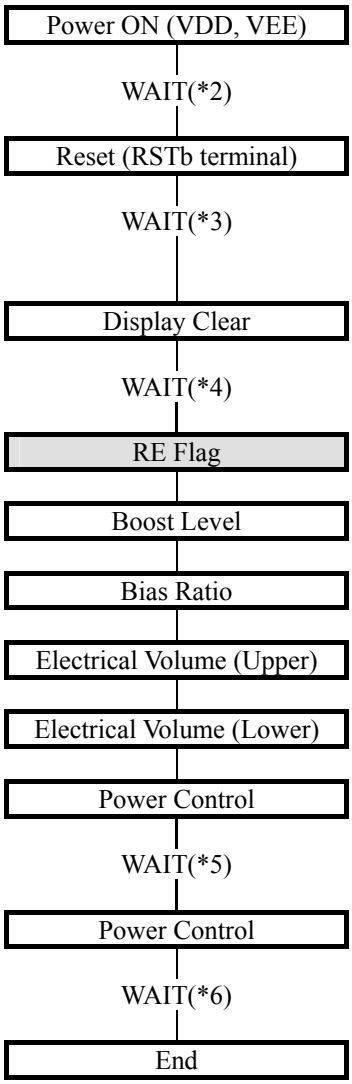
RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	*	*	*	*

≀

RE	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	1	0	*	*	*	*

(21) TYPICAL INSTRUCTION SEQUENCE

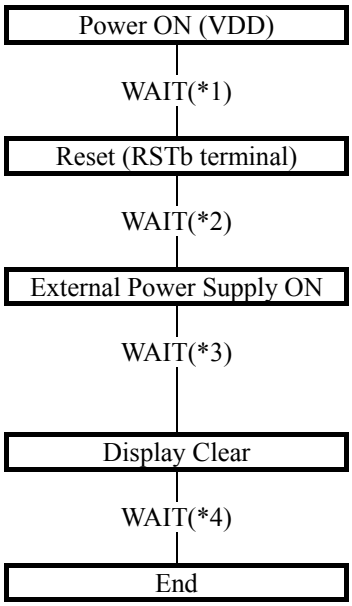
(21-1)Initialization Sequence in Using Internal LCD Power Supply



	Instruction Code								Setting Example
	D7	D6	D5	D4	D3	D2	D1	D0	
Display Clear	0	0	0	0	0	0	0	1	Display clear
RE Flag	1	1	1	1	*	*	*	1	RE="1"
Boost Level	0	0	0	1	*	1	0	1	6 times boost
Bias Ratio	0	0	1	0	0	0	0	0	1/11 bias
Electrical Volume (Upper)	0	0	1	1	*	1	0	0	EV="1,0,0,0,0,0,0"
Electrical Volume (Lower)	0	1	0	0	0	0	0	0	
Power Control	0	1	0	1	*	*	0	1	Voltage booster "ON"
Power Control	0	1	0	1	*	*	1	1	Internal operational amplifier "ON"

*1 If different power sources are applied to the VDD and the VEE, turn ON the VDD first.
*2 Wait until the VDD and VEE are stabilized.
*3 Wait 1.5ms or more.
*4 Wait until the finishes execution of "Display Clear" or When the BF is "0".
*5 Wait until the VDCOUT (VOUT) is stabilized.
*6 Wait until the VLCD and V1 to V4 are stabilized.

(21-2)Initialization Sequence in Using External LCD Power Supply



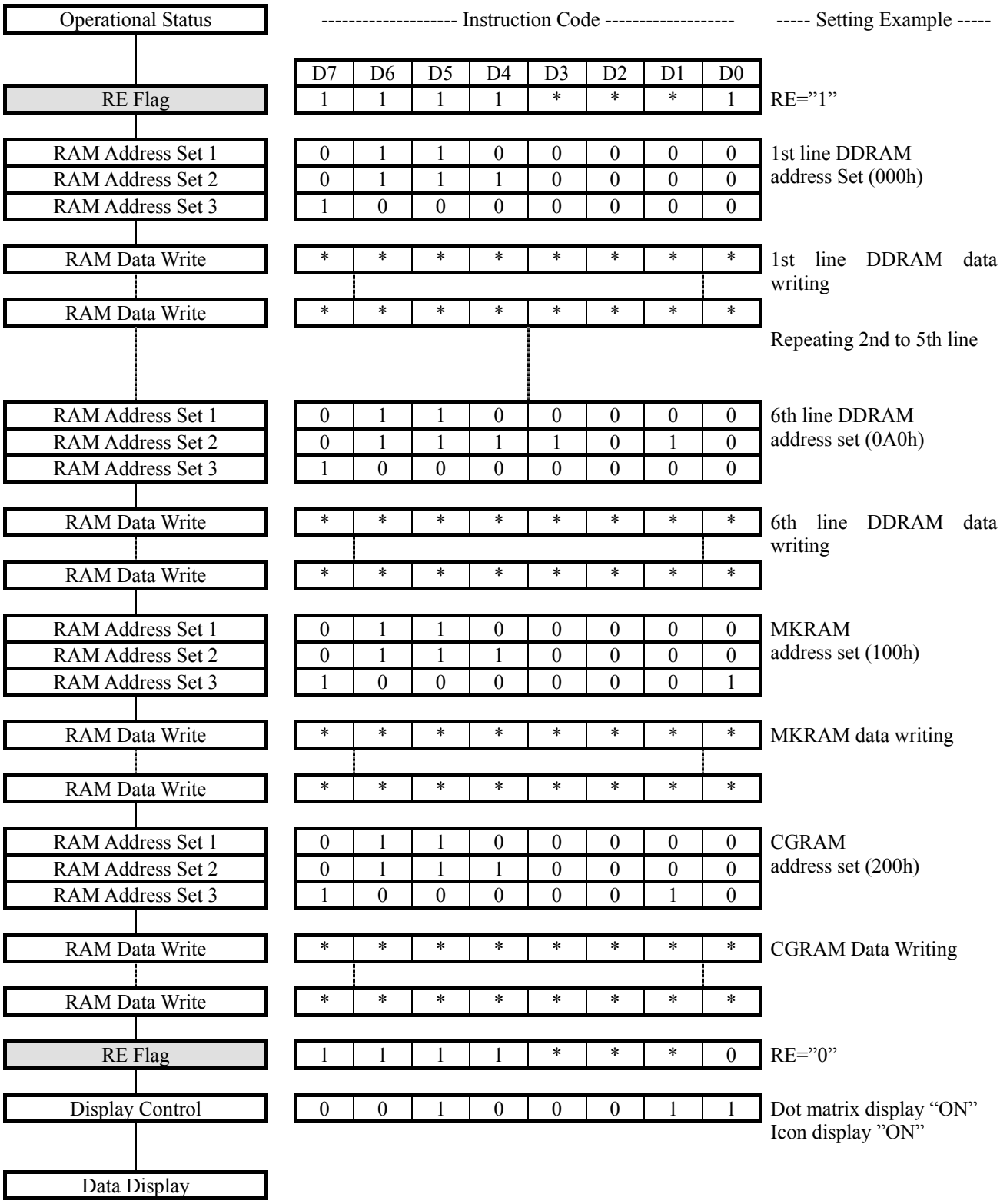
Refer to (15)RESET FUNCTION

---------- Instruction Code ---------- ----- Setting Example -----

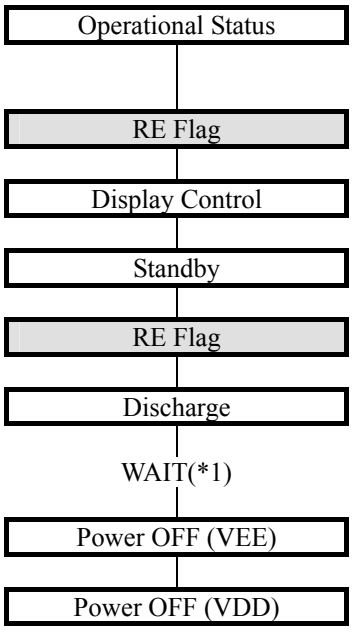
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	1	Display clear

*1 Wait until the VDD is stabilized.
*2 Wait 1.5ms or more.
*3 Wait until the external LCD power supply (VOUT, VLCD, V1 to V4) are stabilized.
*4 Wait until the finishes execution of “Display Clear” or When the BF=”0”

(21-3)Display Data Write Sequence



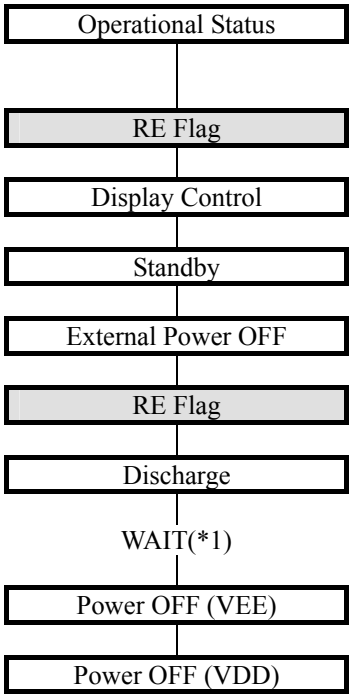
(21-4)Power OFF Sequence in Using Internal LCD Power Supply



	D7	D6	D5	D4	D3	D2	D1	D0	
RE Flag	1	1	1	1	*	*	*	0	RE=”0”
Display Control	0	0	1	0	0	0	0	0	Display ”OFF"
Standby	0	0	1	1	*	*	*	1	Standby ”ON”
RE Flag	1	1	1	1	*	*	*	1	RE=”1”
Discharge	0	0	0	0	*	*	*	1	Discharge ”ON”

*1 Wait until the discharge is completed.

(21-5)Power OFF Sequence in Using External LCD Power Supply



	D7	D6	D5	D4	D3	D2	D1	D0	
RE Flag	1	1	1	1	*	*	*	0	RE=”0”
Display Control	0	0	1	0	0	0	0	0	Display ”OFF"
Standby	0	0	1	1	*	*	*	1	Standby ”ON”
RE Flag	1	1	1	1	*	*	*	1	RE=”1”
Discharge	0	0	0	0	*	*	*	1	Discharge ”ON”

*1 Wait until the discharge is completed.

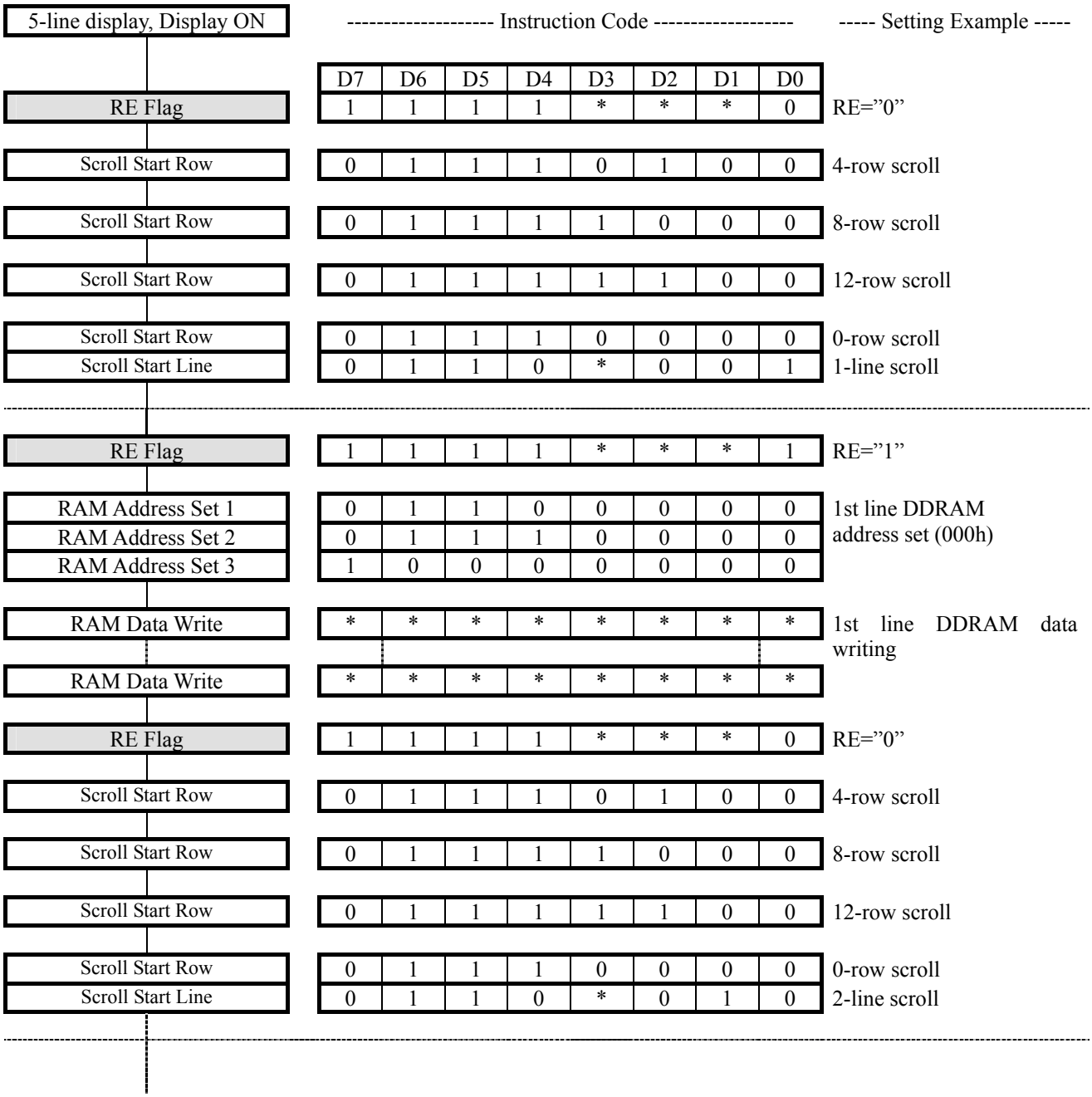
(21-6)Partial Display Sequence [Example : Display Duty Ratio = 2-line (1/34 Duty), Display Start Line = 3rd line]

Operational Status	D7	D6	D5	D4	D3	D2	D1	D0	----- Setting Example -----
	---------- Instruction Code ----------								
RE Flag	1	1	1	1	*	*	*	0	RE="0"
Display Control	0	0	1	0	0	0	0	0	Display "OFF"
RE Flag	1	1	1	1	*	*	*	1	RE="1"
Power Control	0	1	0	1	*	*	0	0	Voltage booster "OFF" Internal operational amplifier "OFF"
WAIT(*1)									
Boost Level	0	0	0	1	*	0	1	0	3 times boost
Bias Ratio	0	0	1	0	0	1	0	1	1/6 bias
Electrical Volume (Upper)	0	0	1	1	*	1	0	0	EV="1,0,0,0,0,0,0"
Electrical Volume (Lower)	0	1	0	0	0	0	0	0	
Power Control	0	1	0	1	*	*	0	1	Voltage booster "ON"
WAIT(*2)									
Power Control	0	1	0	1	*	*	1	1	Internal operational amplifier "ON"
WAIT(*3)									
RE Flag	1	1	1	1	*	*	*	0	RE="0"
Display Start line	1	0	0	0	*	0	1	0	3rd line
Display Duty Ratio	1	0	0	1	*	1	0	0	2-line (1/34Duty)
Display Control	0	0	1	0	0	0	1	1	Dot matrix display "ON" Icon display "ON"
Partial Display									

*1 Wait until the discharge is completed.
*2 Wait until the VDCOUT (VOUT) is stabilized.
*3 Wait until the external LCD power supply (VOUT, VLCD, V1 to V4) are stabilized.

Refer to (10) PARTIAL DISPLAY .

(21-7)Smooth Scroll Display Sequence [Example : 5-line display, 4-dot scroll]



Refer to (11) VERTICAL SMOOTH S SCROLL.

(21-8)Superimpose Mode Display Sequence [Example : Character display on 2nd ~ 5th line]

Operational Status	D7	D6	D5	D4	D3	D2	D1	D0	----- Setting Example -----
	---------- Instruction Code ----------								
RE Flag	1	1	1	1	*	*	*	0	RE="0"
Display / Entry Mode	0	1	0	1	*	1	0	0	Superimpose mode
RE Flag	1	1	1	1	*	*	*	1	RE="1"
RAM Address Set 1	0	1	1	0	0	0	0	0	2nd line DDRAM address set (020h)
RAM Address Set 2	0	1	1	1	0	0	1	0	
RAM Address Set 3	1	0	0	0	0	0	0	0	
RAM Data Write	*	*	*	*	*	*	*	*	2nd line DDRAM data writing
RAM Data Write	*	*	*	*	*	*	*	*	Repeating 3rd to 4th line
RAM Address Set 1	0	1	1	0	0	0	0	0	5th line DDRAM address set (080h)
RAM Address Set 2	0	1	1	1	1	0	0	0	
RAM Address Set 3	1	0	0	0	0	0	0	0	
RAM Data Write	*	*	*	*	*	*	*	*	5th line DDRAM data writing
RAM Data Write	*	*	*	*	*	*	*	*	
RAM Address Set 1	0	1	1	0	0	0	0	0	CGRAM address set (200h)
RAM Address Set 2	0	1	1	1	0	0	0	0	
RAM Address Set 3	1	0	0	0	0	0	1	0	
RAM Data Write	*	*	*	*	*	*	*	*	CGRAM data writing
RAM Data Write	*	*	*	*	*	*	*	*	
RE Flag	1	1	1	1	*	*	*	0	RE="0"
Display Control	0	0	1	0	0	0	1	1	Dot matrix display "ON" Icon display "ON"
Data Display									

Refer to (13-3) Superimpose Mode.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	VDD	VSS=0V Common Ta=+25°C	VDD	-0.3 to +4.0	V
Supply Voltage (2)	VEE		VEE	-0.3 to +4.0	V
Supply Voltage (3)	VOUT, VDCOUT		VOUT, VDCOUT	-0.3 to +19.0	V
Supply Voltage (4)	VREG		VREG	-0.3 to +19.0	V
Supply Voltage (5)	VLCD		VLCD	-0.3 to +19.0	V
Supply Voltage (6)	V1, V2, V3, V4		V1, V2, V3, V4	-0.3 to VLCD+0.3	V
Input Voltage (1)	VI			-0.3 to VDD+0.3	V
Operating Temperature	Topr			-40 to +85	°C
Storage Temperature	Tstg	Bump Chip		-55 to +125	°C

*1 If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

*2 The order of turning on the power supply should turn on VDD earlier than other power supplies. When the power supply is turned off, that requires turning off VDD at the last.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	VDD1	VDD	2.4	-	3.6	V	*1
	VDD2		2.4	-	3.6	V	*2
	VEE	VEE	2.4	-	3.6	V	*3
Operating Voltage	VLCD	VLCD	4.5	-	17.0	V	*4
	VOUT	VOUT	-	-	17.0	V	
	VDCOUT	VDCOUT	-	-	17.0	V	
	VREG	VREG	-	-	VOUTx0.9	V	*5
	VREF	VREF	1.8	-	3.6	V	*6

*1 Applied to the condition when the reference voltage generator (VBA) is not used. (VSS common)

*2 Applied to the condition when the reference voltage generator (VBA) is used. (VSS common)

*3 Applied to the condition when the voltage booster is used.

*4 The following relation among the LCD bias voltages must be maintained.

$VSS<V4<V3<V2<V1<VLCD \leq VOUT$

*5 When the voltage booster is used, there is possibility that the VDCOUT is changing by the ITO resistance and the panel load. The setting of the VREG voltage is recommended to become a voltage that is lower than the lowest value of the changing VOUT.

*6 Relation : VREF < VEE must be maintained.

*7 To stabilize the LSI operation, place decoupling capacitors between VDD and VSS, between VEE and VSS, between VBA and VSS, between VREF and VSS, between VREG and VSS, between VLCD and VSS, and between V1 to V4 and VSS.

■ DC CHARACTERISTICS

VDD=+2.4 to 3.6V, VSS=0V, Ta=-40 to +85°C

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
"H" Level Input Voltage	VIH		0.8VDD	-	VDD	V	*1
"L" Level Input Voltage	VIL		VSS	-	0.2VDD	V	*1
"H" Level Output Voltage	VOH	IOH=-0.1mA	VDD-0.2	-	-	V	*2
"L" Level Output Voltage	VOL	IOL= 0.1mA	-	-	0.2	V	*2
Input Leakage Current	ILI	VI=VSS or VDD	-1	-	1	µA	*3
Output Leakage Current	ILO	VI=VSS or VDD	-1	-	1	µA	*4
Driver ON-resistance	RON1	|ΔVON|=0.5V, VLCD=10V	-	1	2	kΩ	*5
	RON2	|ΔVON|=0.5V, VLCD=6V	-	2	4	kΩ	
Oscillation Frequency	fOSC	VDD=3V, Ta=25°C, Rf=47kΩ	0.82	1	1.18	MHz	*6
Voltage Booster Output Voltage	VOUT	N-time boost (N=2 to 6) RL=500kΩ (VDCOUT-VSS)	NxVEE x0.95	-	-	V	*7
Operating Current (1)	IDD1	Ta=25°C, 6-time boost, All pixels ON, VEE=2.4V, VREF=1.8V	-	1.5	3.6	mA	*8
Operating Current (2)	IDD2	Ta=25°C, 5-time boost, All pixels ON, VEE=3.0V, VREF=2.25V	-	1.5	3.6	mA	
Operating Current (3)	IDD3	Ta=25°C, 4-time boost, All pixels ON, VEE=3.6V, VREF=2.7V	-	1.5	3.6	mA	
Operating Current (4)	ISTB	Ta=25°C, CSb=VDD, HALT="1"	-	-	10	µA	*9
VBA Output Voltage	VBA	VEE=2.4 to 3.6V	(0.75VEE)x 0.98	0.75VEE	(0.75VEE)x 1.02	V	*10
VREG Output Voltage	VREG	VEE=2.4 to 3.6V N-time boost (N=2 to 6)	(VREFxN)x 0.95	(VREFxN)	(VREFxN)x 1.05	V	*11
LCD Bias Voltages	VLCD	VEE=3.0V, VREF=2.25V, VOUT=15V, Bias=1/4 to 1/11, Electrical Volume=MAX., DCON="0", Display OFF, No-load, AMPON="1", Boost Level=5-time	-0.1	-	+0.1	V	
	V1		-0.1	-	+0.1	V	
	V2		-0.1	-	+0.1	V	
	V3		-0.1	-	+0.1	V	
	V4		-0.1	-	+0.1	V	

*1 D7 to D0, CSb, RS, WRb, RDb, SEL68, PS, CSEL, and RSTb terminals.
*2 D7 to D0 terminals.
*3 D7 to D0, CSb, RS, WRb, RDb, SEL68, PS, CSEL, RSTb, and OSC2 terminals.
*4 D7 to D0 in high impedance.
*5 SEG0 to SEG255, COM0 to COM95, and COMMK0 to COMMK1 terminals.
This parameter defines the resistance between each COM/SEG and each LCD bias (VLCD, V1, V2, V3, V4).
0.5V difference / 1/11 LCD bias
*6 Oscillation frequency of using the internal oscillation circuit.
(OS2, OS1, OS0) = "0, 0, 0"
*7 VDCOUT terminal.
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used. N-time boost (N=2 to 6).
VEE=2.4V to 3.6V / Electrical Volume : Max = "1, 1, 1, 1, 1, 1, 1" / 1/11 LCD Bias / 1/98 Duty / No-load on COM/SEG / RL=500kΩ between VDCOUT and VSS / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"
*8 VSS terminal.
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used, and the no accessing from MPU.
Electrical Volume : Max = "1, 1, 1, 1, 1, 1, 1" / All pixels ON or Checker Flag Display / No-load on COM/SEG / VDD=VEE / VREF=0.75VEE / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NL6 to 0="1, 1, 0, 0, 0, 0, 1" (98-line) / 1/98 Duty / Ta=25°C
*9 VDD terminal.
Internal oscillator is halted. / CSb=VDD (No active) / No-load

*10 VBA terminal.
VBA=VREF / Boost Level (N)="1" / DCON="0" / VOUT=13.5V

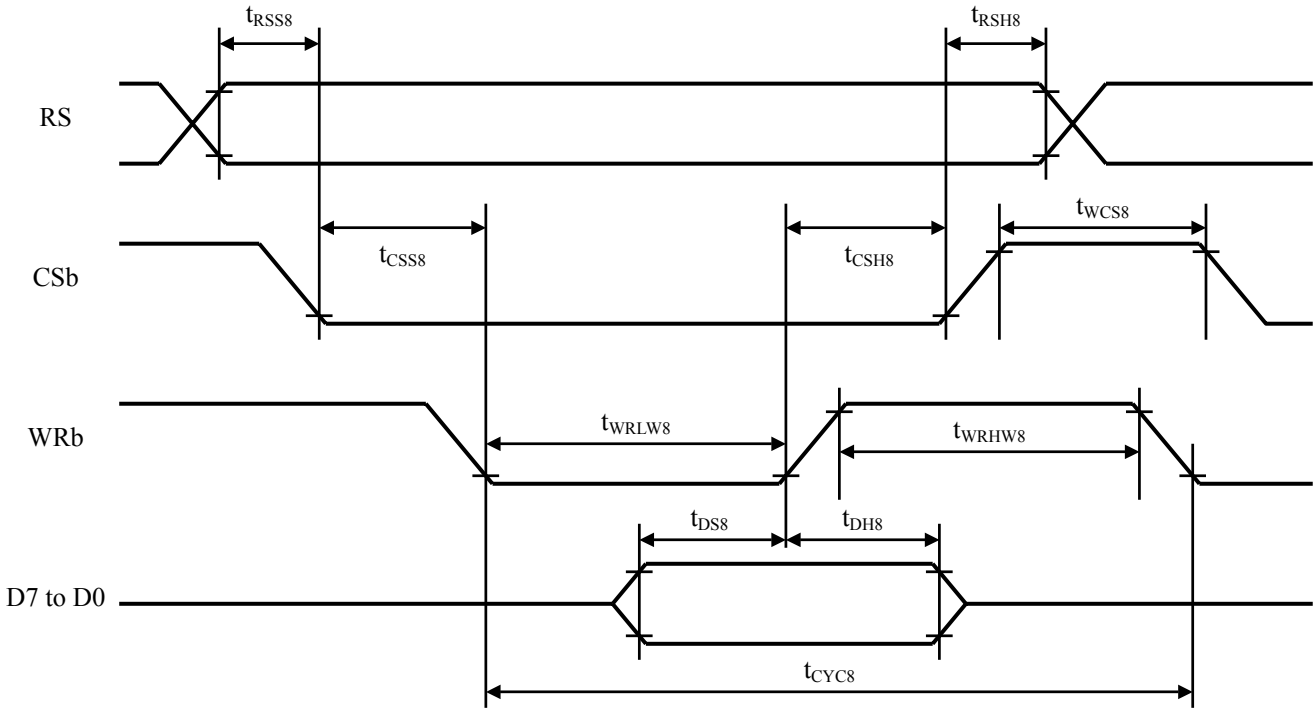
*11 VREG terminal.
VEE=2.4V to 3.6V / VOUT=17V / 1/11 LCD Bias / 1/98 Duty / Electrical Volume : Max = "1, 1, 1, 1, 1, 1, 1" / Checker Flag Display / No-load on COM/SEG / Boost Level (N)="2 to 6" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1" / NL6 to 0="1, 1, 0, 0, 0, 0, 1" (98-line)

■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

OSCILLATOR /EXTERNAL CLOCK	DISPLAY DUTY (1/D)					
	98	82	66	50	34	18
Using Internal Oscillator	(f_{OSC}/(128xD))	(f_{OSC}/(128xD))	(f_{OSC}/(128xD))	(f_{OSC}/(128xD))/2	(f_{OSC}/(128xD))/3	(f_{OSC}/(128xD))/6
Using External Clock	(f_{CK}/(128xD))	(f_{CK}/(128xD))	(f_{CK}/(128xD))	(f_{CK}/(128xD))/2	(f_{CK}/(128xD))/3	(f_{CK}/(128xD))/6

■ AC CHARACTERISTICS

(1) Write Operation (Parallel Interface / 80-series MPU)

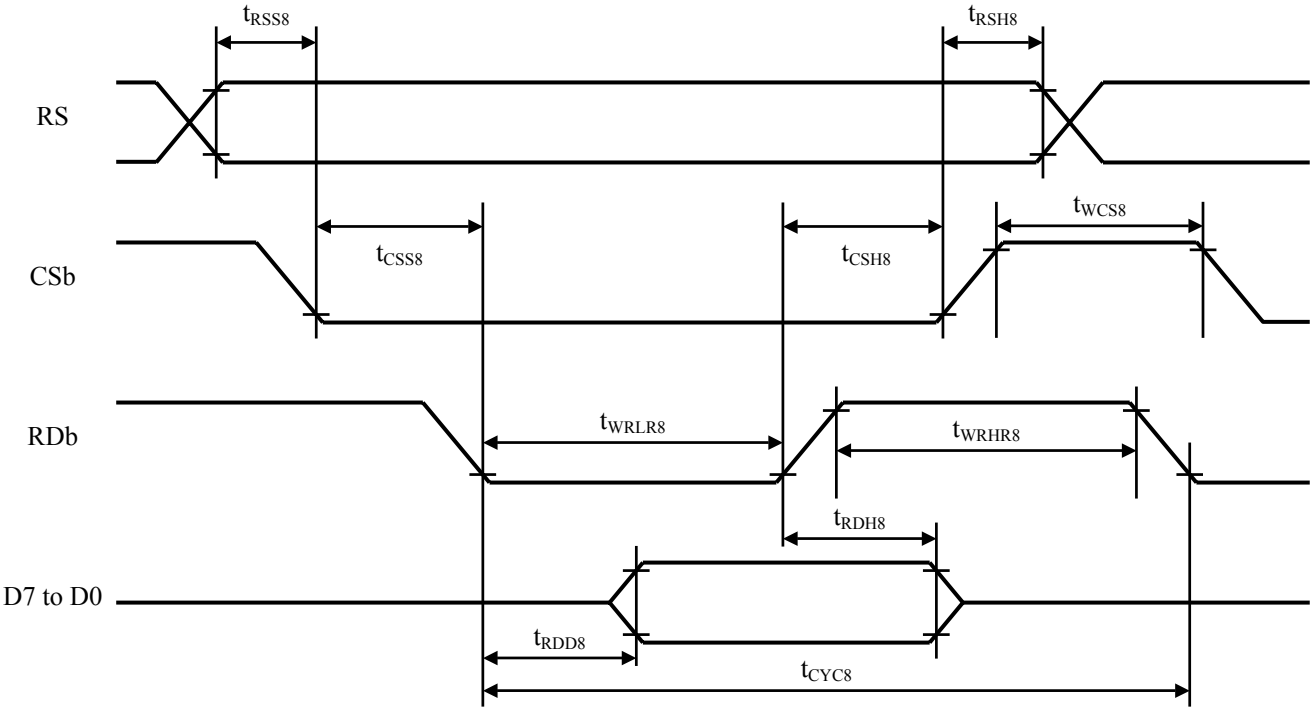


(VDD=2.4 to 3.6V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
RS Hold Time	t_{RSH8}		30	-	ns	RS
RS Setup Time	t_{RSS8}		30		ns	
CSb Hold Time	t_{CSH8}		30	-	ns	CSb
CSb Setup Time	t_{CSS8}		30		ns	
CSb "H" Level Pulse Width	t_{WCS8}		180		ns	
System Cycle Time	t_{CYC8}		180	-	ns	WRb
Enable "L" Level Pulse Time	t_{WRLW8}		80		ns	
Enable "H" Level Pulse Time	t_{WRHW8}		80		ns	
Data Setup Time	t_{DS8}		70	-	ns	D7 to D0
Data Hold Time	t_{DH8}		40		ns	

Note) Each timing is specified based on 20% and 80% of VDD.

(2) Read Operation (Parallel Interface / 80-series MPU)

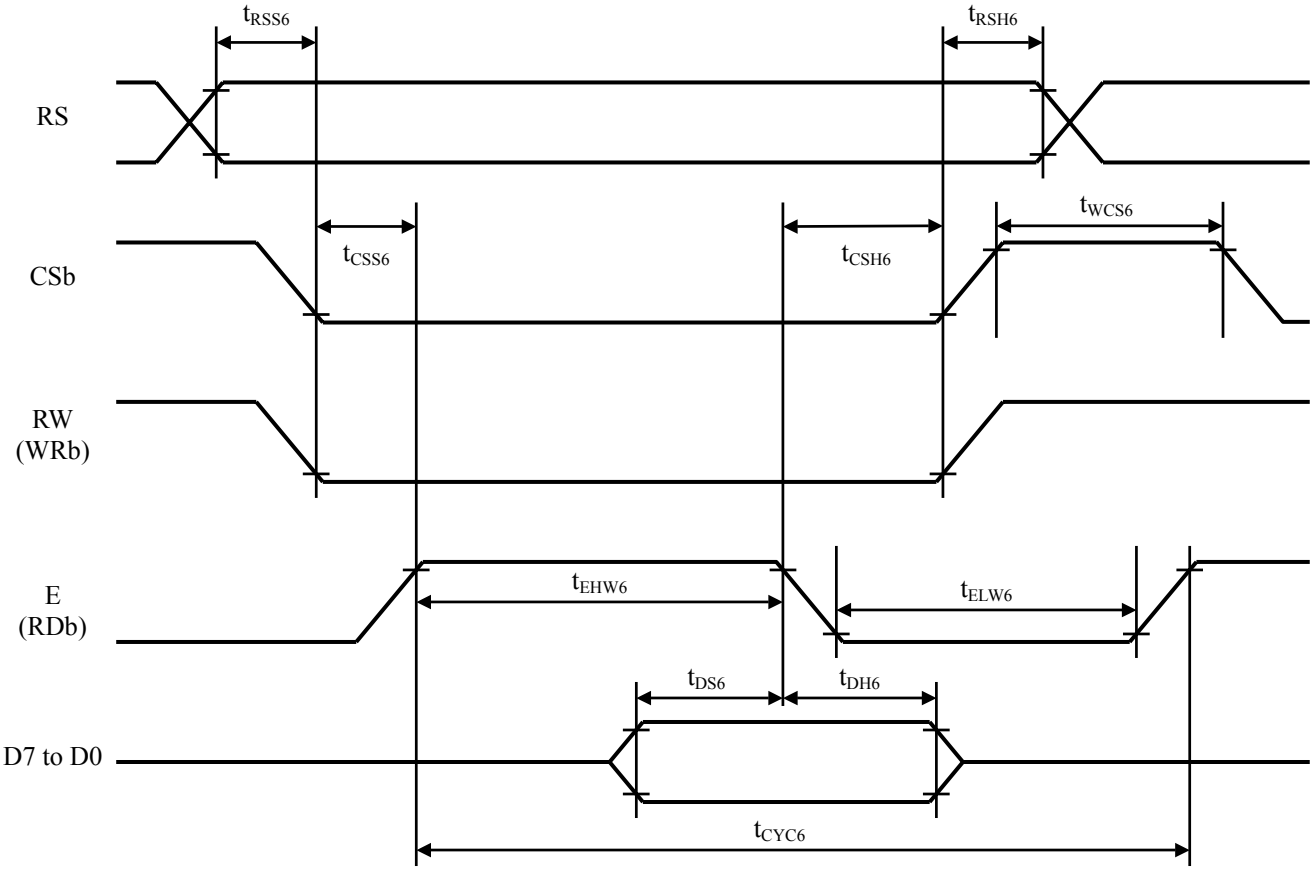


(VDD=2.4 to 3.6V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
RS Hold Time	t_{RSH8}		40	-	ns	RS
RS Setup Time	t_{RSS8}		40		ns	
CSb Hold Time	t_{CSH8}		40		ns	CSb
CSb Setup Time	t_{CSS8}		40	-	ns	
CSb "H" Level Pulse Width	t_{WCS8}		140		ns	
System Cycle Time	t_{CYC8}		250		ns	RDb
Enable "L" Level Pulse Time	t_{WRLR8}		120	-	ns	
Enable "H" Level Pulse Time	t_{WRHR8}		120		ns	
Read Data Delay Time	t_{RDD8}	CL=15pF		110	ns	D7 to D0
Read Data Hold Time	t_{RDH8}		0		ns	

Note) Each timing is specified based on 20% and 80% of VDD.

(3) Write Operation (Parallel Interface / 68-series MPU)

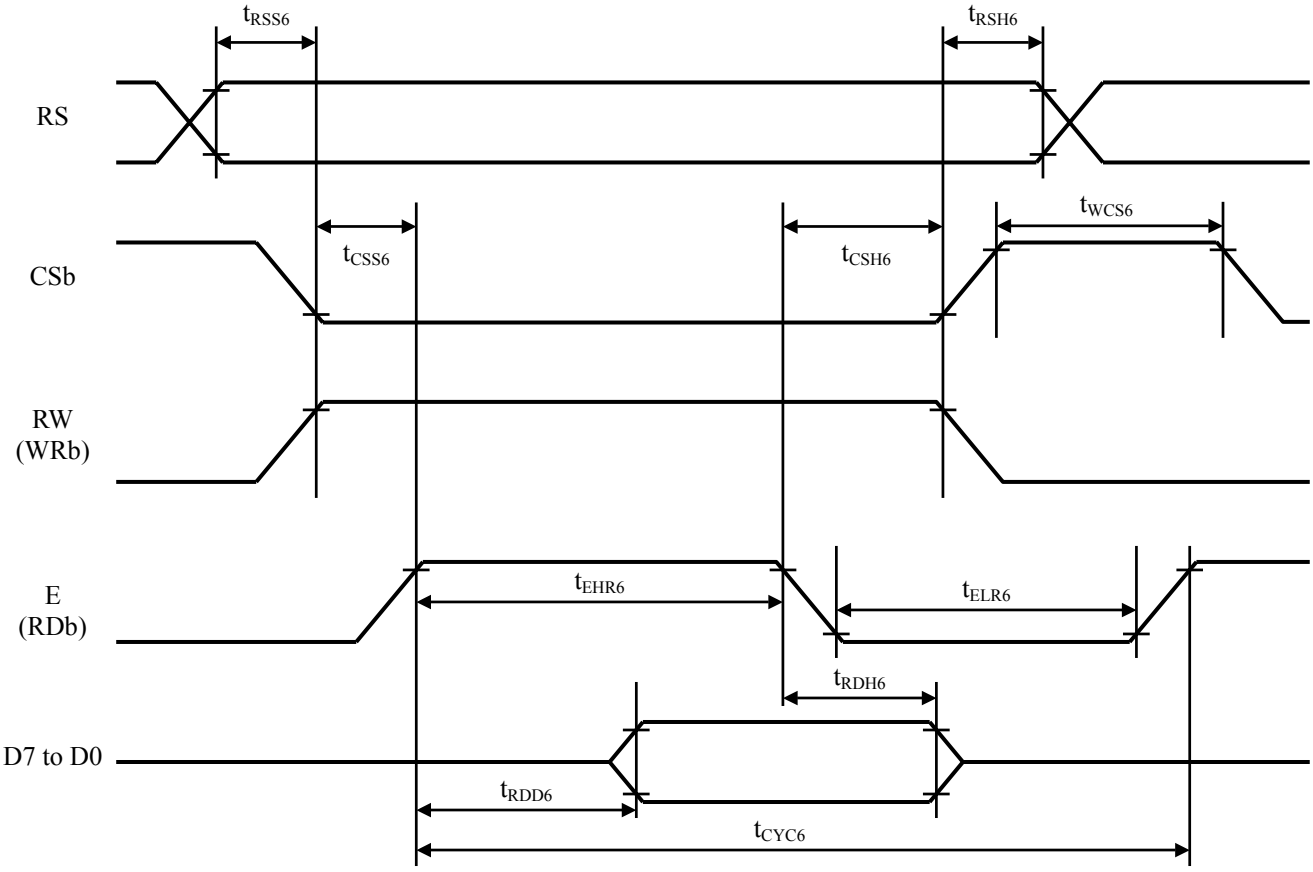


(VDD=2.4 to 3.6V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
RS Hold Time	t_{RSH6}		30	-	ns	RS
RS Setup Time	t_{RSS6}		30		ns	
CSb Hold Time	t_{CSH6}		30	-	ns	CSb
CSb Setup Time	t_{CSS6}		30		ns	
CSb "H" Level Pulse Width	t_{WCS6}		180		ns	
System Cycle Time	t_{CYC6}		180	-	ns	E
Enable "L" Level Pulse Time	t_{ELW6}		80		ns	
Enable "H" Level Pulse Time	t_{EHW6}		80		ns	
Data Setup Time	t_{DS6}		70	-	ns	D7 to D0
Data Hold Time	t_{DH6}		40		ns	

Note) Each timing is specified based on 20% and 80% of VDD.

(4) Read Operation (Parallel Interface / 68-series MPU)

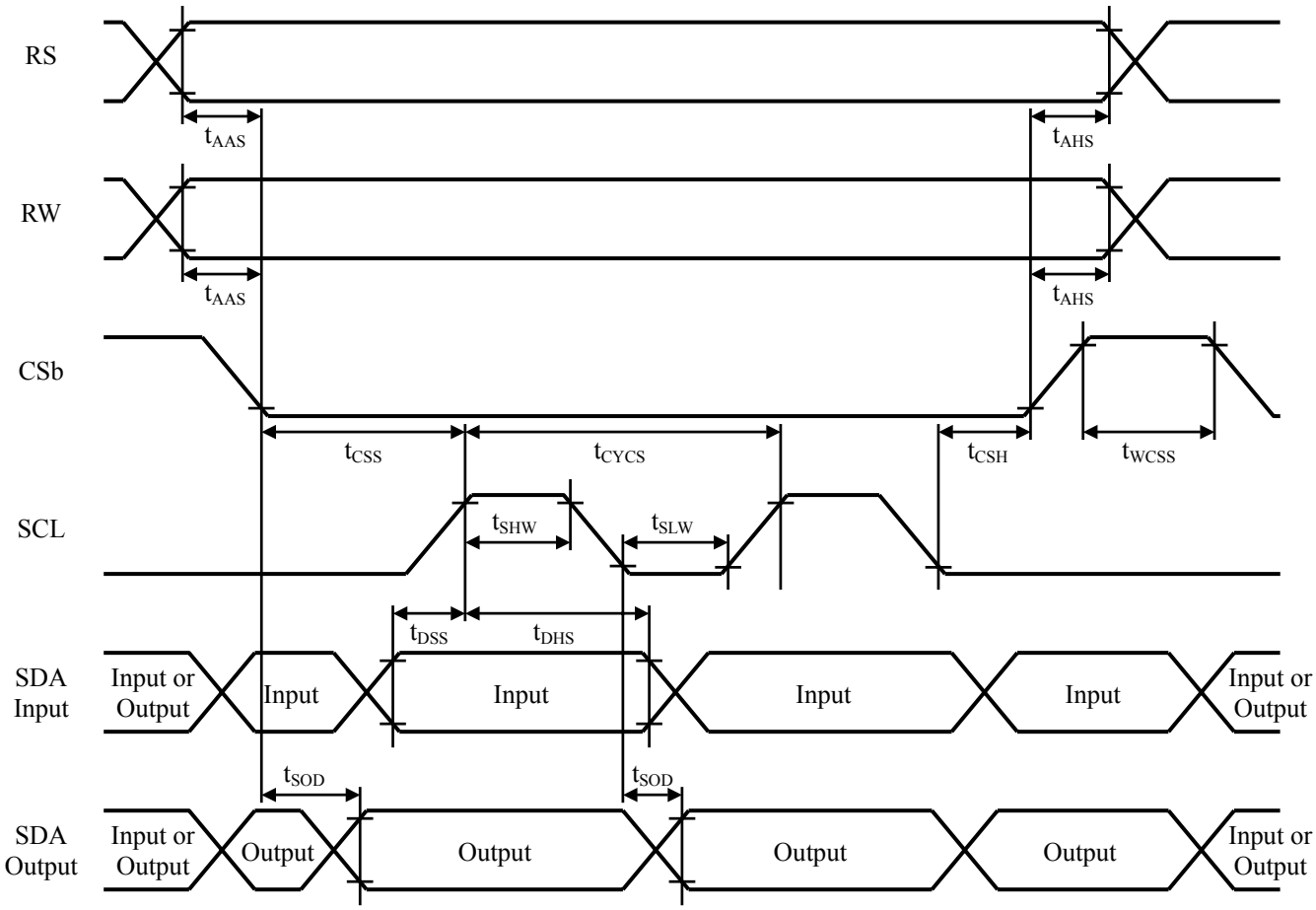


(VDD=2.4 to 3.6V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
RS Hold Time	t_{RSH6}		40	-	ns	RS
RS Setup Time	t_{RSS6}		40		ns	
CSb Hold Time	t_{CSH6}		40	-	ns	CSb
CSb Setup Time	t_{CSS6}		40		ns	
CSb "H" Level Pulse Width	t_{WCS6}		140		ns	
System Cycle Time	t_{CYC6}		250	-	ns	E
Enable "L" Level Pulse Time	t_{ELR6}		120		ns	
Enable "H" Level Pulse Time	t_{EHR6}		120		ns	
Read Data Delay Time	t_{RDD6}	CL=15pF		110	ns	D7 to D0
Read Data Hold Time	t_{RDH6}		0		ns	

Note) Each timing is specified based on 20% and 80% of VDD.

(5) Serial Interface

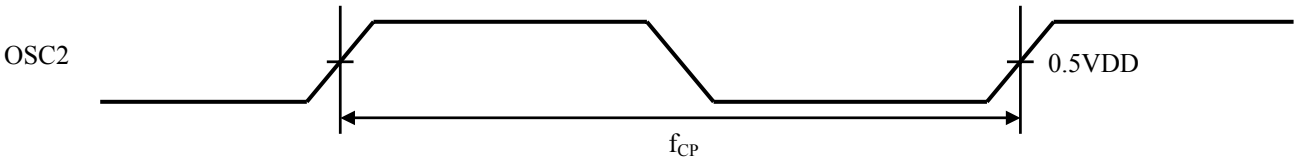


(VDD=2.4 to 3.6V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial Clock Cycle	t_{CYCS}		160		ns	SCL
SCL "H" Level Pulse Width	t_{SHW}		75	-	ns	
SCL "L" Level Pulse Width	t_{SLW}		75		ns	
Address Setup Time	t_{ASS}		35	-	ns	RS / RW
Address Hold Time	t_{AHS}		35		ns	
Data Setup Time	t_{DSS}		35	-	ns	SDA
Data Hold Time	t_{DHS}		35		ns	
Serial Data Delay Time	t_{SOD}		-	40	ns	SDA
CSb – SCL Time	t_{CSS}		35		ns	CSb
CSb Hold Time	t_{CSH}		35	-	ns	
CSb "H" Level Pulse Width	t_{WCSS}		75		ns	

Note) Each timing is specified based on 20% and 80% of VDD.

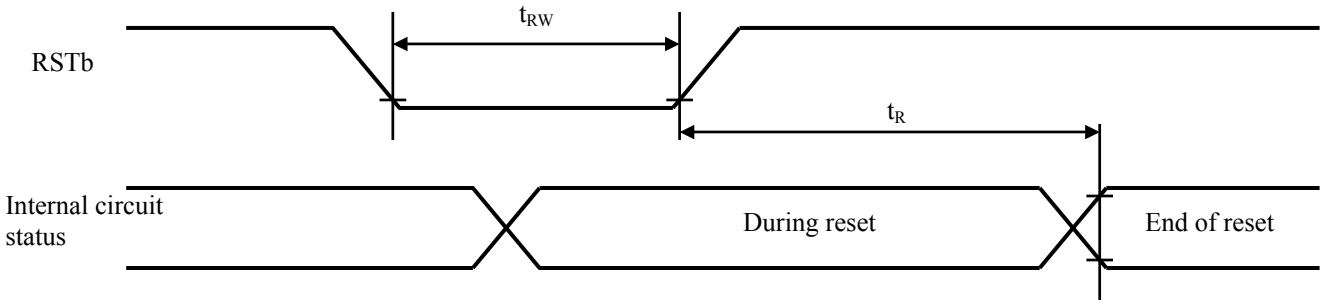
■ External Clock Input Timing



(VDD=2.4 to 3.6V, VSS=0V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	MIN.	MAX.	CONDITION	UNIT
External Clock Operating Frequency	f_{CP}	-	1.18	OSC2	MHz
External Clock Duty	duty	35	65		%

■ Reset Input Timing



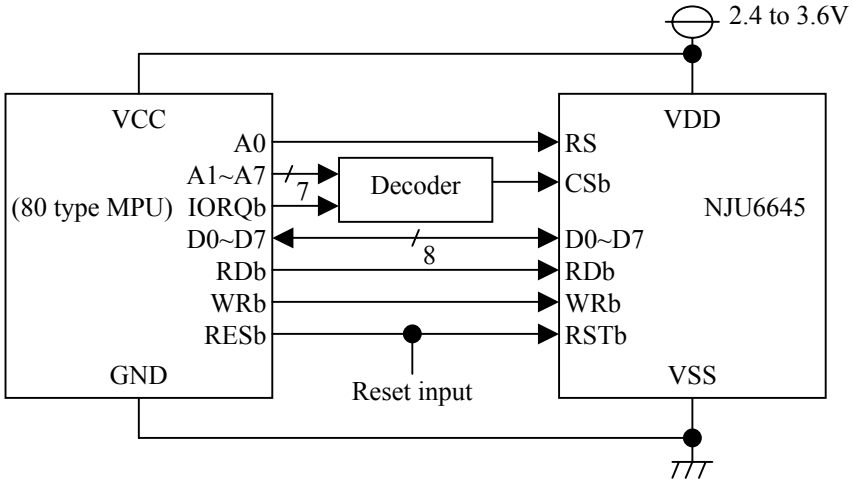
(VDD=2.4 to 3.6V, VSS=0V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	MIN.	MAX.	CONDITION	UNIT
Reset Time	t_R	-	0.5		μs
RSTb "L" Level Pulse Width	t_{RW}	1.5	-		ms

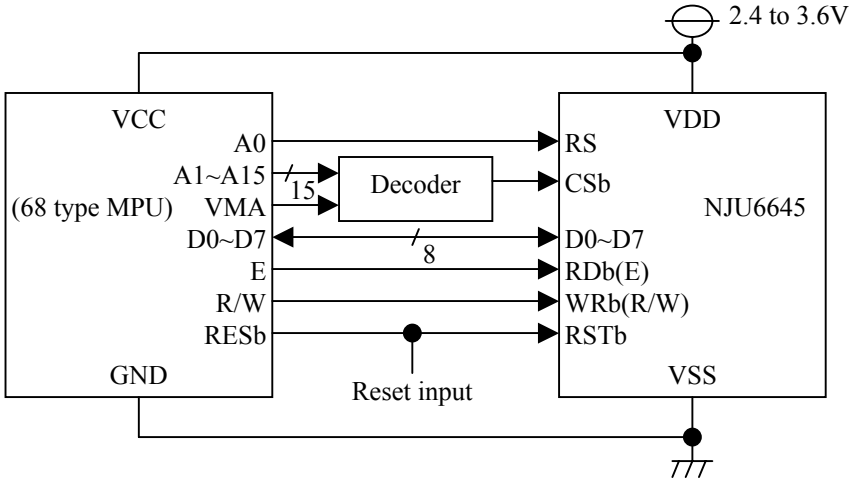
■ APPLICATION CIRCUIT

(1) Microprocessor Interface Example

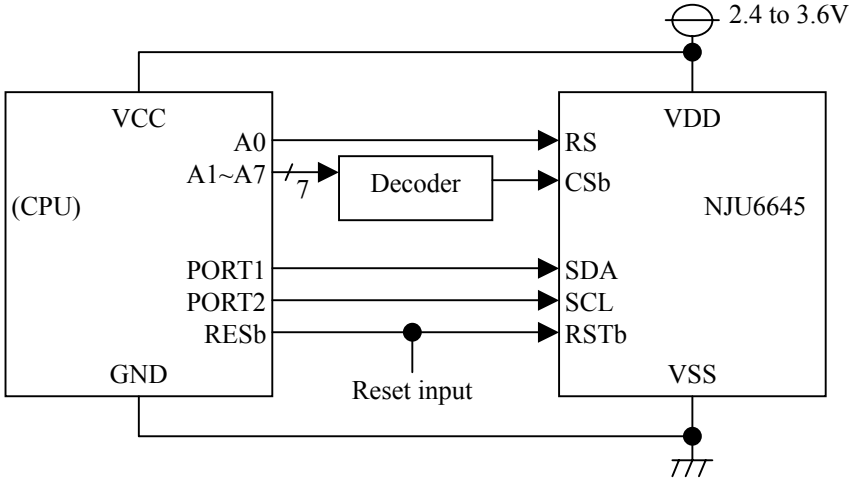
(i) 80 type MPU



(ii) 68 type MPU

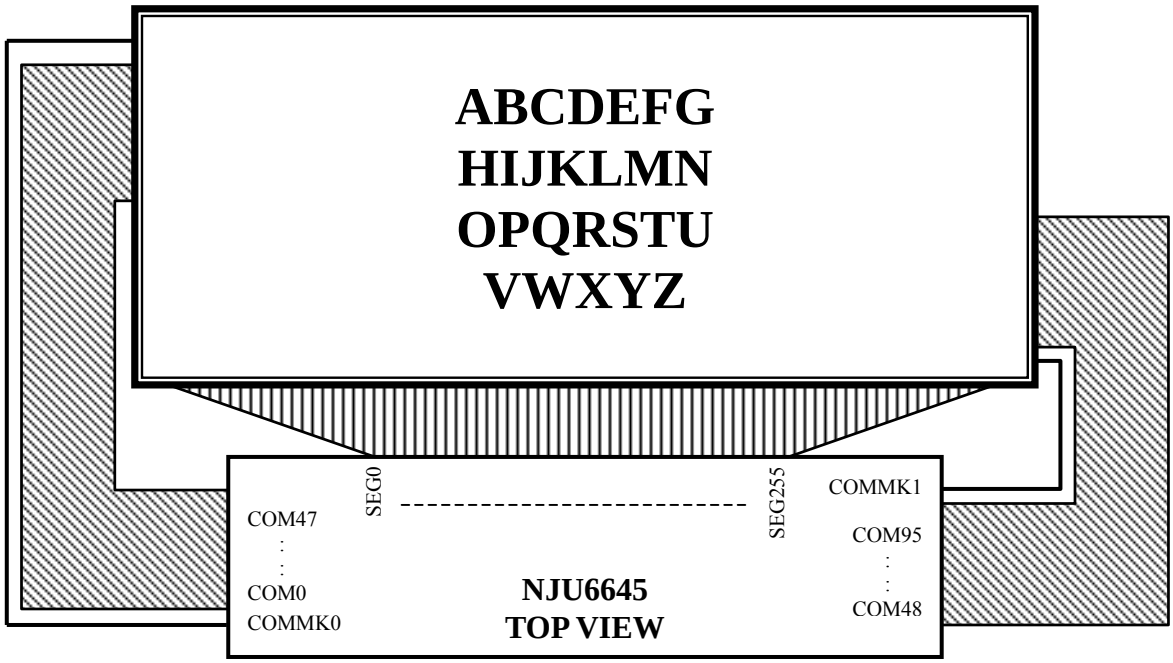


(iii) Serial Interface

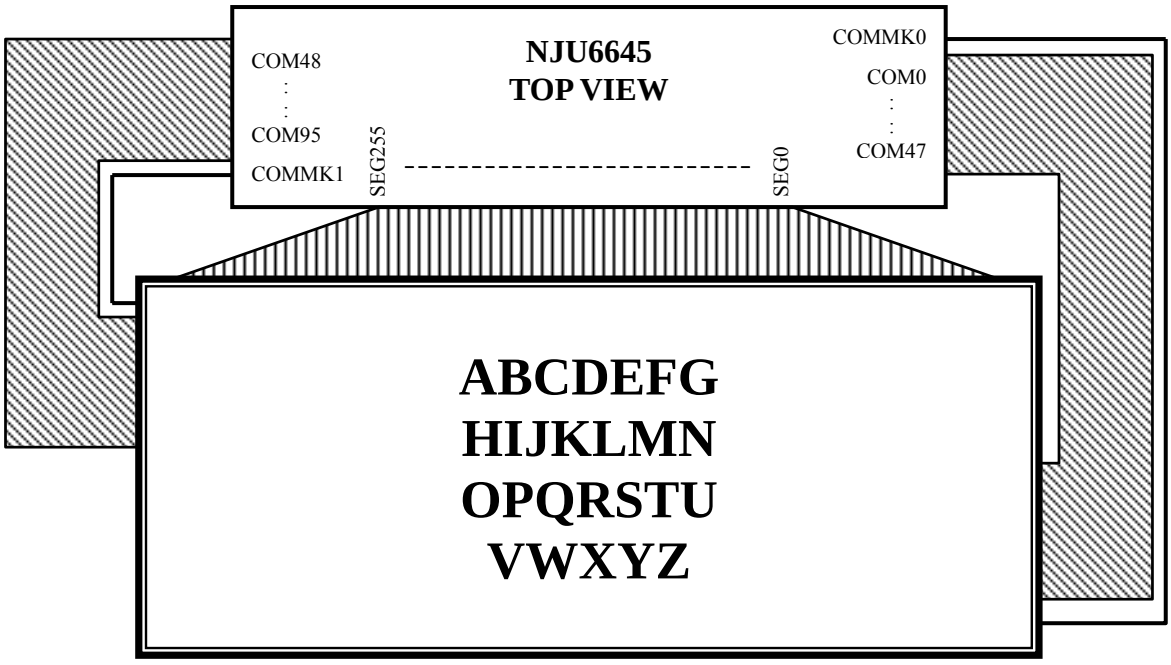


(2) Connection with Panel Display

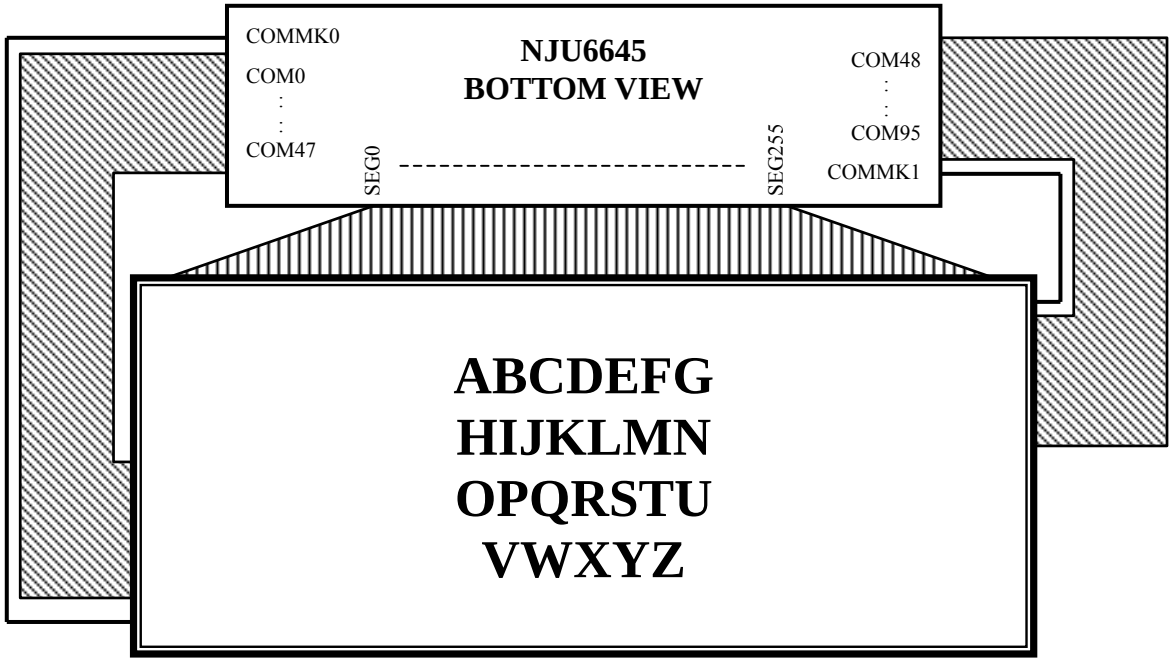
(i) SEL1="0", SEL2="0"



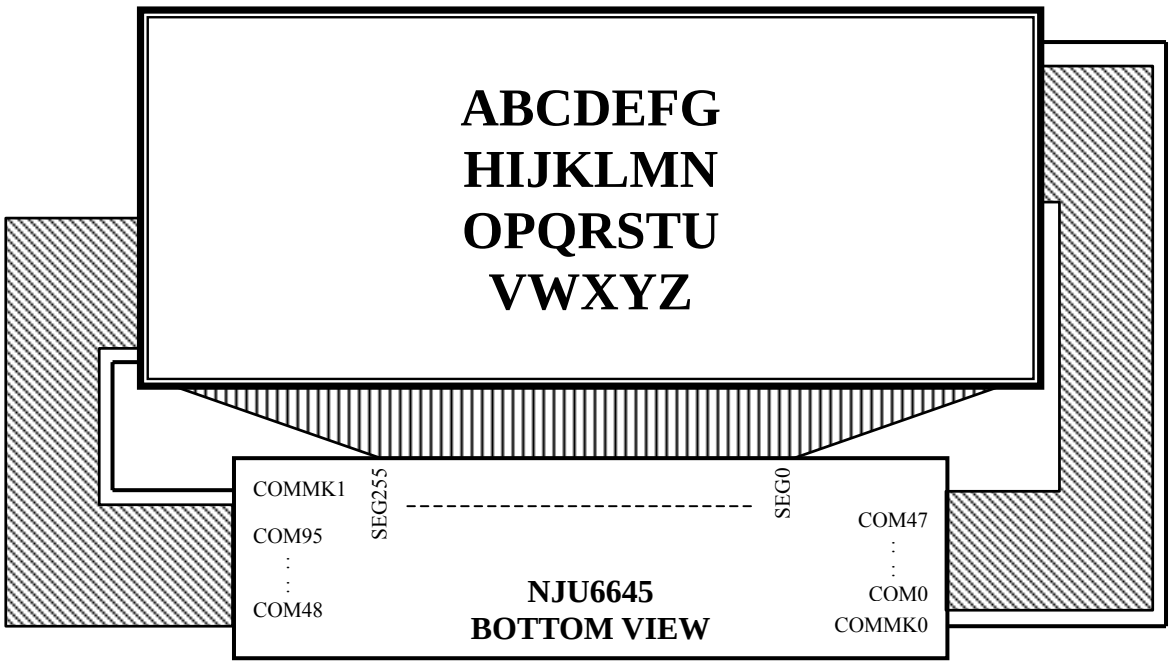
(ii) SEL1="1", SEL2="1"



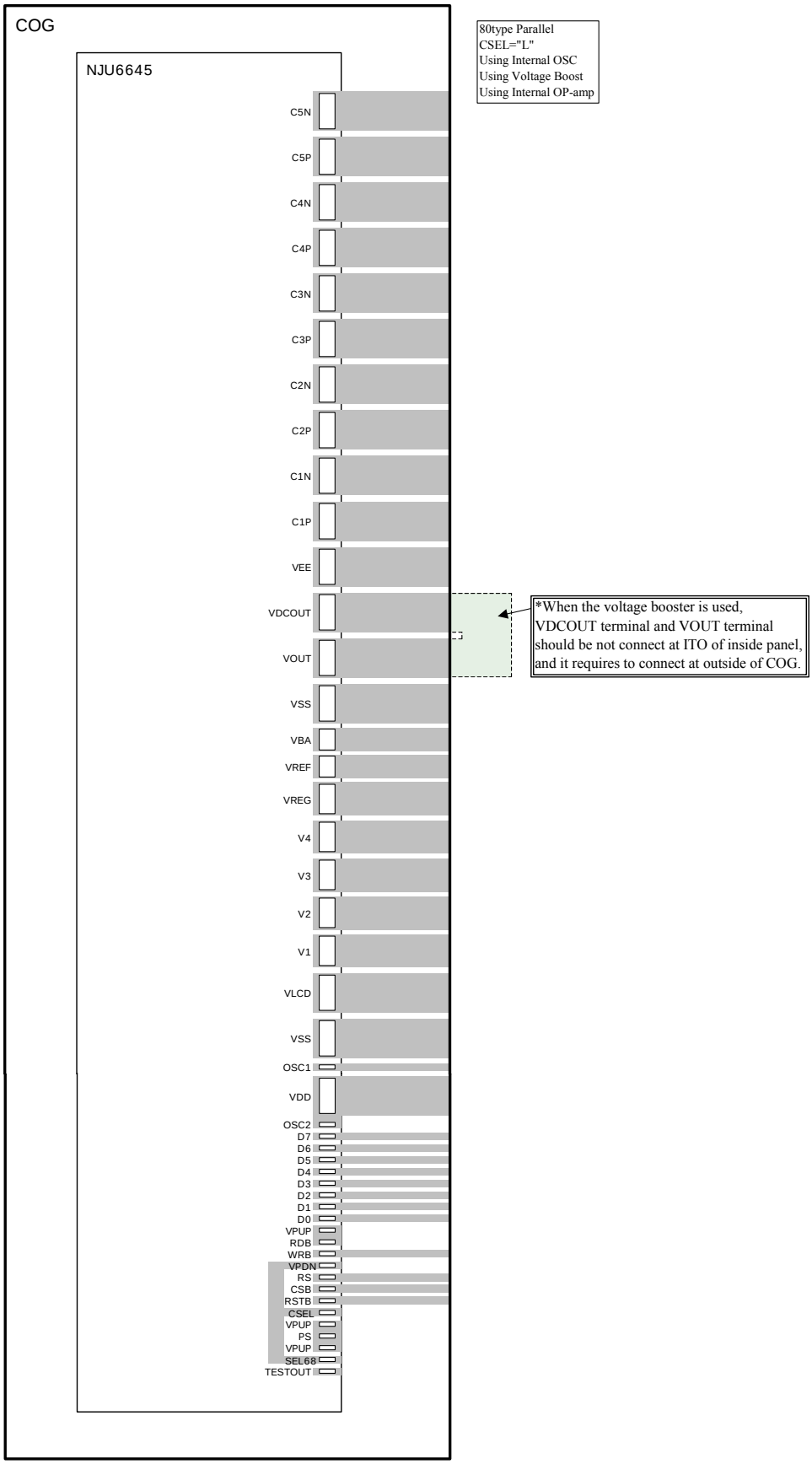
(iii) SEL1="1", SEL2="0"



(iv) SEL1="0", SEL2="1"



■ COG WIRING EXAMPLE



[CAUTION]
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