10-CHARACTER 3-LINE DOT MATRIX LCD CONTROLLER DRIVER with KEYSCAN FUNCTION

■ GENERAL DESCRIPTION

The **NJU6627** is a Dot Matrix LCD controller driver for 10-character 3-line with icon display in single chip.
It contains voltage converter and regulator bleeder resistance, Keyscan circuit, CR oscillator, microprocessor interface circuit, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers, and others.
The character generator ROM consisting of 7,840bits stores 224 kinds of character font, Each 1,120 bits CG RAM and Icon display RAM can store 32 kind of special character displayed on the dot matrix display area or 100 kinds of Icon display area.
The 23-common(21 for character, 2 for Icon) and 50-segment drivers operate 10-character 3-line with 100 Icon LCD display.
The 16th display contrast control function is incorporated. Therefore, only simple power supply circuit on chip operates the contrast adjustment easily.
The complete CR oscillator requires external capacitor and resistor.
The serial interface which operates by 1MHz, communicates with external MCU.

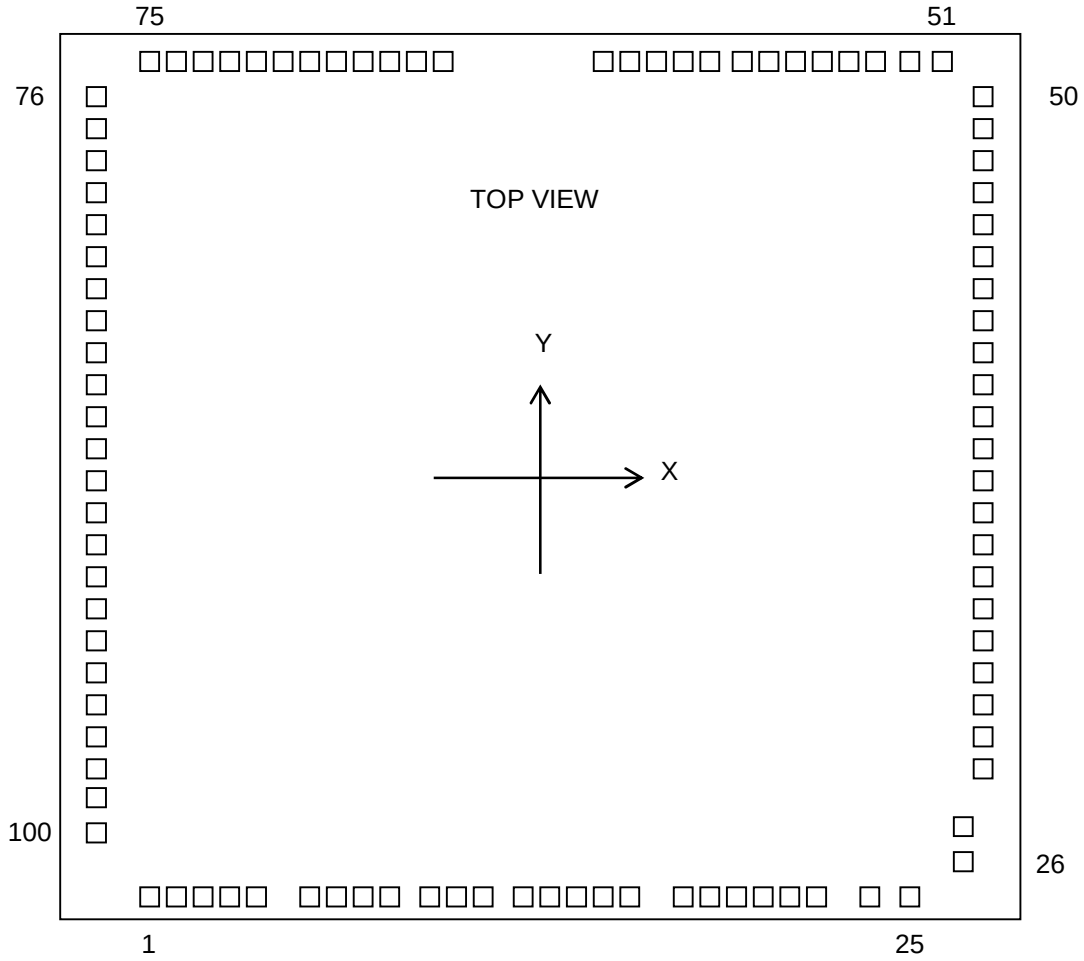
■ PACKAGE OUTLINE

NJU6627C

■ FEATURES

- 10-character 3-line Dot Matrix LCD Controller Driver
- Maximum 100 Icon Display
- Serial Direct Interface with Microprocessor
- Display Data RAM 30 x 8 bits :Maximum 10-character 3-line Display
- Character Generator ROM 7,840bits :224 Characters for 5 x 7 Dots
- Character Generator RAM 1,120bits :32 Patterns (5 x 7 Dots)
- Icon Display RAM Maximum 100-Icons
- High voltage LCD Driver 23-common / 50-segment
- Duty and Bias Ratio 1/23, 1/16 duty, 1/5 bias
- Useful Instruction set Clear Display, Address Home, Display ON/OFF, Display blink, Address shift, Character Shift, Keyscan ON/OFF cont. e.t.c.
- 24-Key input(4x6 Keyscan)
- Power on Initialization / Hardware Reset
- Bleeder resistance on chip
- Software contrast control(16-step)
- Voltage Booster Circuits (2-time)
- Oscillation Circuit on-chip (External CR)
- Operating Voltage 4.5 to 5.5V
- Package Outline Bare Chip
- C-MOS Technology

■ PAD LOCATION



Chip Center	: X=0μm, Y=0μm
Chip Size	: X= 4.50 mm, Y= 4.61 mm
Chip Thickness	: 400μm ± 25 μm
PAD Size	: 90.0 μm x 90.0 μm
PAD Pitch	: 134μm (Min.)
Sub Striate	: P

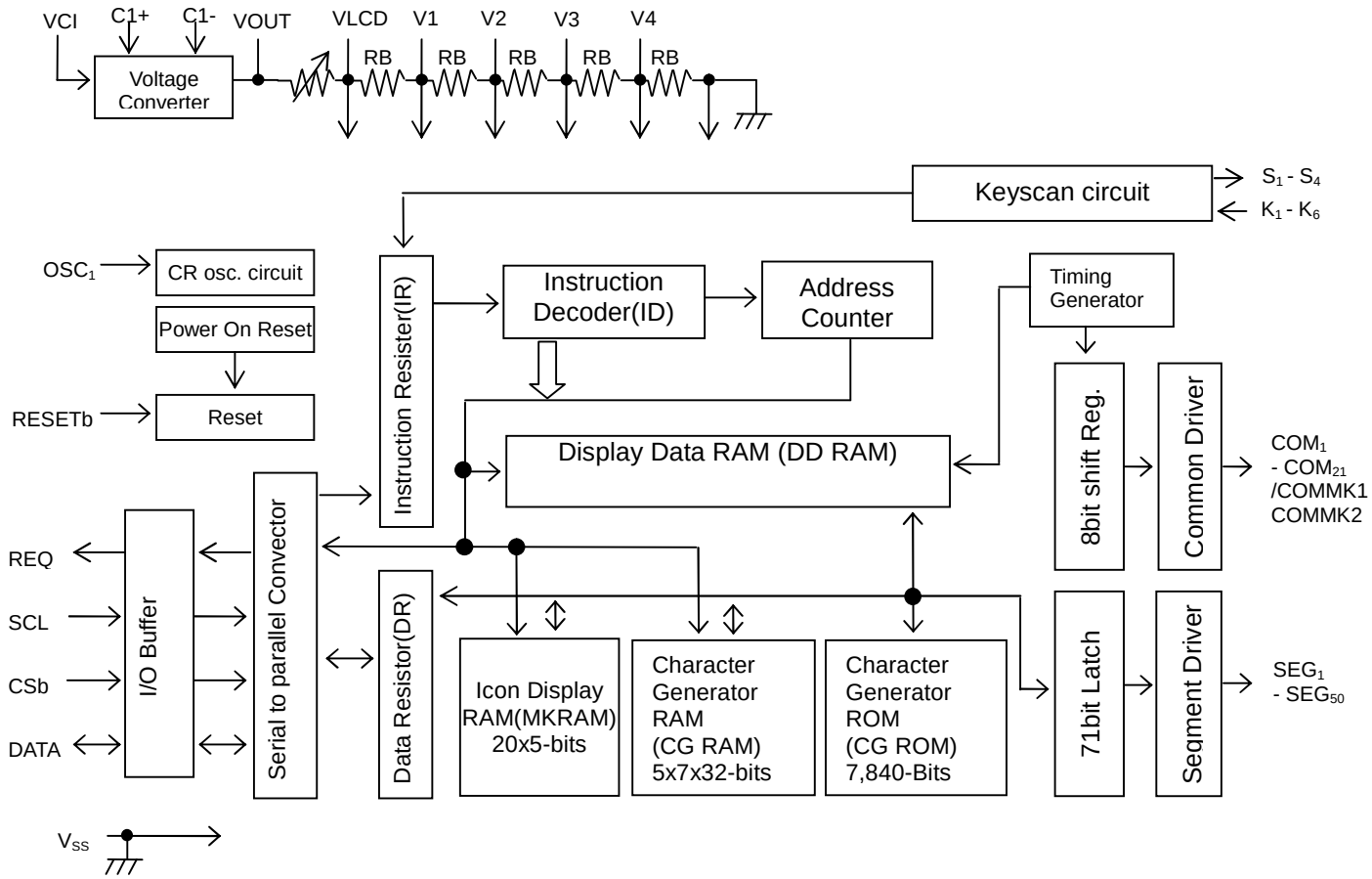
■ PAD COODINATES

Chip Size 4.50 x 4.61 mm(Chip Center X=0μm, Y=0μm)

PAD No.	PAD NAME	X= μm	Y= μm
1	V4	-2007.3	-2038.5
2	V3	-1862.5	-2038.5
3	V2	-1717.7	-2038.5
4	V1	-1572.9	-2038.5
5	VLCD	-1428.1	-2038.5
6	VOUT	-1158.4	-2038.5
7	C1+	-1018.4	-2038.5
8	C1-	-878.4	-2038.5
9	VCI	-738.4	-2038.5
10	VDD	-497.6	-2038.5
11	OSC1	-345.8	-2038.5
12	REQ	-204.0	-2038.5
13	DATA	-17.2	-2038.5
14	SCL	142.6	-2038.5
15	CSb	286.6	-2038.5
16	RESETb	430.6	-2038.5
17	VSS	596.8	-2038.5
18	K1	817.4	-2038.5
19	K2	951.4	-2038.5
20	K3	1098.6	-2038.5
21	K4	1232.6	-2038.5
22	K5	1379.8	-2038.5
23	K6	1513.8	-2038.5
24	S1	1743.2	-2038.5
25	S2	1923.2	-2038.5
26	S3	1978.6	-1656.2
27	S4	1978.6	-1476.2
28	COMMK1	2088.0	-1205.0
29	COM8	2088.0	-1060.0
30	COM9	2088.0	-915.0
31	COM10	2088.0	-770.0
32	COM11	2088.0	-625.0
33	COM12	2088.0	-480.0
34	COM13	2088.0	-335.0
35	COM14	2088.0	-191.0
36	SEG1	2088.0	-45.0
37	SEG2	2088.0	100.0
38	SEG3	2088.0	245.0
39	SEG4	2088.0	390.0
40	SEG5	2088.0	535.0
41	SEG6	2088.0	680.0
42	SEG7	2088.0	825.0
43	SEG8	2088.0	970.0
44	SEG9	2088.0	1115.0
45	SEG10	2088.0	1260.0
46	SEG11	2088.0	1405.0
47	SEG12	2088.0	1550.0
48	SEG13	2088.0	1695.0
49	SEG14	2088.0	1840.0
50	SEG15	2088.0	1985.0

PAD No.	PAD NAME	X= μm	Y= μm
51	SEG16	1930.0	2143.0
52	SEG17	1785.0	2143.0
53	SEG18	1640.0	2143.0
54	SEG19	1495.0	2143.0
55	SEG20	1350.0	2143.0
56	SEG21	1205.0	2143.0
57	SEG22	1060.0	2143.0
58	SEG23	915.0	2143.0
59	SEG24	770.0	2143.0
60	SEG25	625.0	2143.0
61	SEG26	480.0	2143.0
62	SEG27	335.0	2143.0
63	SEG28	190.0	2143.0
64	SEG29	-335.0	2143.0
65	SEG30	-480.0	2143.0
66	SEG31	-625.0	2143.0
67	SEG32	-770.0	2143.0
68	SEG33	-915.0	2143.0
69	SEG34	-1060.0	2143.0
70	SEG35	-1205.0	2143.0
71	SEG36	-1350.0	2143.0
72	SEG37	-1495.0	2143.0
73	SEG38	-1640.0	2143.0
74	SEG39	-1785.0	2143.0
75	SEG40	-1930.0	2143.0
76	SEG41	-2088.0	1999.0
77	SEG42	-2088.0	1854.0
78	SEG43	-2088.0	1709.0
79	SEG44	-2088.0	1564.0
80	SEG45	-2088.0	1419.0
81	SEG46	-2088.0	1274.0
82	SEG47	-2088.0	1129.0
83	SEG48	-2088.0	984.0
84	SEG49	-2088.0	839.0
85	SEG50	-2088.0	694.0
86	COMMK2	-2088.0	549.0
87	COM21	-2088.0	404.0
88	COM20	-2088.0	259.0
89	COM19	-2088.0	114.0
90	COM18	-2088.0	-31.0
91	COM17	-2088.0	-176.0
92	COM16	-2088.0	-321.0
93	COM15	-2088.0	-466.0
94	COM7	-2088.0	-611.0
95	COM6	-2088.0	-756.0
96	COM5	-2088.0	-901.0
97	COM4	-2088.0	-1046.0
98	COM3	-2088.0	-1191.0
99	COM2	-2088.0	-1336.0
100	COM1	-2088.0	-1481.0

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	F U N C T I O N
10 17	V_{DD} V_{SS}	-	Power Source :V_{DD}=+5V, GND :V_{SS}=0V
9	VCI	I	Input terminal for voltage doubler
6	VOUT	O	Voltage doubler output terminal.
5 4 3 2 1	V_{LCD} V_1 V_2 V_3 V_4	I	LCD driving voltage stabilization capacitor terminals. Connect the capacitor between VSS. typ. : 0.1uF
7 8	C1+ C1-		Boosted capacitor connecting terminals used for voltage booster.
11	OSC_1	I	Resistor connection terminal for oscillation / External clock input terminal
15	CSb	I	Chip select signal input of serial I/F.
14	SCL	I	Shift clock input of serial I/F.
13	DATA	I/O	Serial data input of serial I/F.
16	RESETb	I	Reset terminal When the "L" level is input over than 900us to this terminal, the system will be reset (at f_{OSC} 200KHz).
12	REQ	O	Key request signal output terminal.
18-23	K_1-K_6	I	Key scanning input terminals.
24-27	S_1-S_4	O	Key scanning output terminals.
36-85	SEG_1-SEG_{50}	O	LCD segment driving signal output terminals.
94-100 29-35 87-93	COM_1-COM_{21}	O	LCD common driving signal output terminals.
96	COMMK1 COMMK2	O	LCD Icon common driving signal output terminals.

■ FUNCTIOAL DESCRIPTION

(1-1) Register

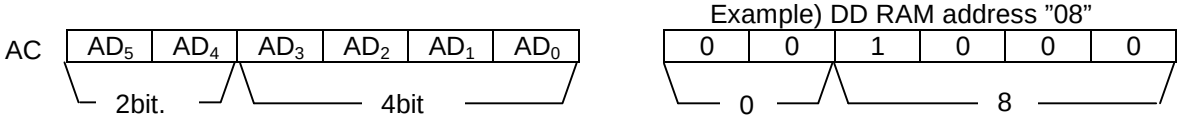
The **NJU6627** incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register (IR) stores instruction codes such as “Clear Display” and “Cursor Shift” or address data for Display Data RAM (DDRAM), Character Generator ROM (CGRAM) and Icon Display RAM (MKRAM).
The Register (DR) is a temporary register, the data in the Register (DR) is written into the DDRAM, CGRAM or MK RAM.
The data in the Register (DR) written by the MPU is transferred automatically to the DDRAM, CGRAM or MKRAM by internal operation.
These two registers are selected by the selection signal RS as shown below.

(1-2) Address Counter (AC)

The address counter (AC) addresses the DDRAM, CGRAM or MKRAM.
When the address setting instruction is written into the Register (IR), the address information is transferred from Register (IR) to the Counter (AC). The selection of either the DDRAM, CGRAM or MKRAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DDRAM, CGRAM or MKRAM, the Counter (AC) increments (or decrements) automatically.

(1-3) Display Data RAM(DD RAM)

The Display Data RAM (DD RAM) consist of 30 x 8 bits stores up to 30-character display data represented in 8-bit code.
The DDRAM address data set in the address counter (AC) is represented in Hexadecimal.



The relation between DDRAM address and display position on the LCD is shown below.

1	2	3	4	5	6	7	8	9	10	←Display Position
00	01	02	03	04	05	06	07	08	09	←DD RAM address(Hex.)
10	11	12	13	14	15	16	17	18	19	
20	21	22	23	24	25	26	27	28	29	

When the display shift is performed, the DDRAM address changes as follows:

(Left Shift Display)

(00) ←	01	02	03	04	05	06	07	08	09	00
(10) ←	11	12	13	14	15	16	17	18	19	10
(20) ←	21	22	23	24	25	26	27	28	29	20

(Right Shift Display)

09	00	01	02	03	04	05	06	07	08	→(09)
19	10	11	12	13	14	15	16	17	18	→(19)
29	20	21	22	23	24	25	26	27	28	→(29)

(1-4) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character code.

The storage capacity is up to 224 kinds of 5 x 7 dots character pattern (available address is $(20)_H$ through $(FF)_H$).

The correspondence between character code and standard character pattern of **NJU6627** is shown in Table 1. User-defined character patterns (Custom Font) are also available by mask option.

Table 1. CG ROM Character Pattern (ROM version -02)

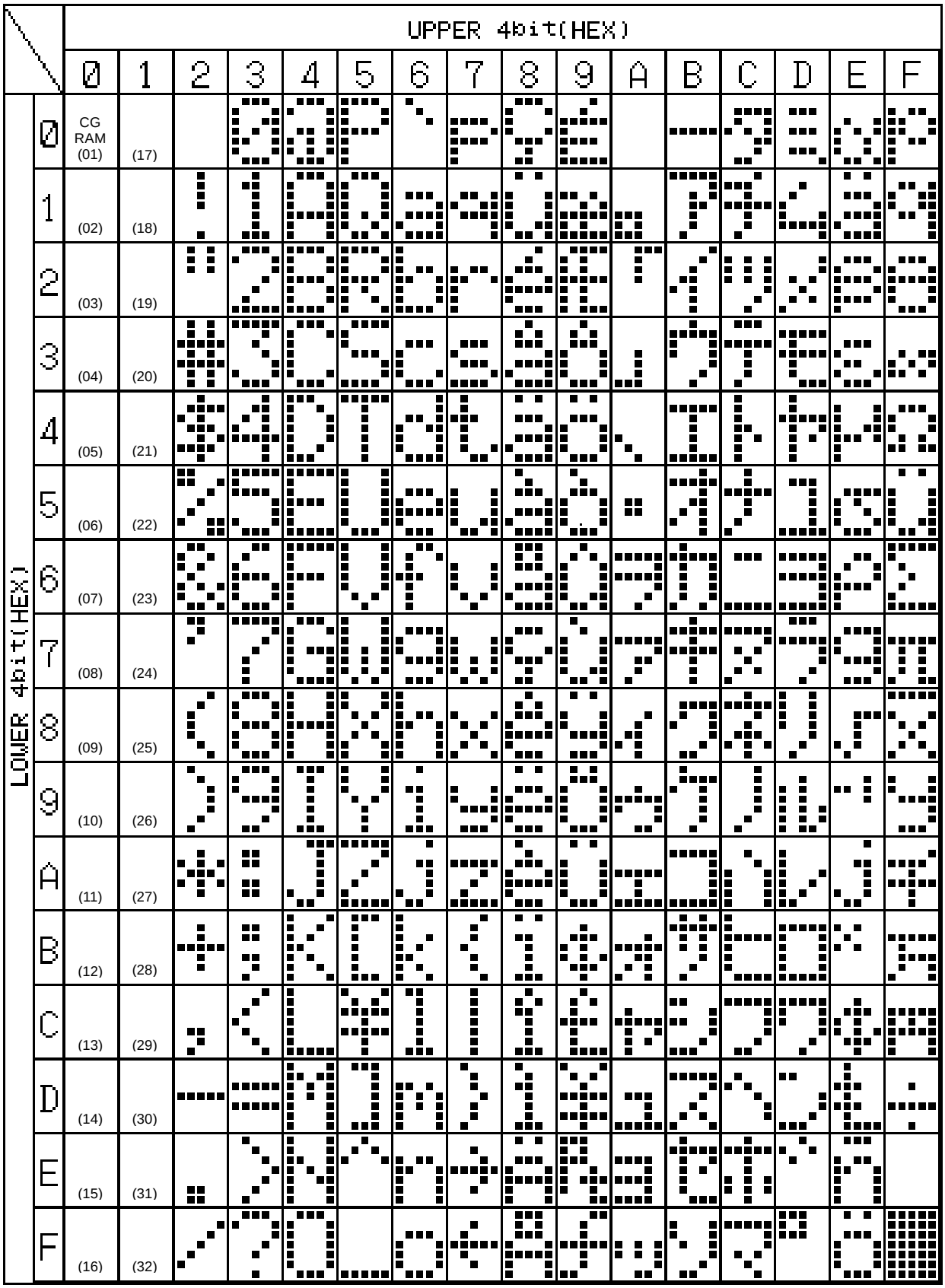
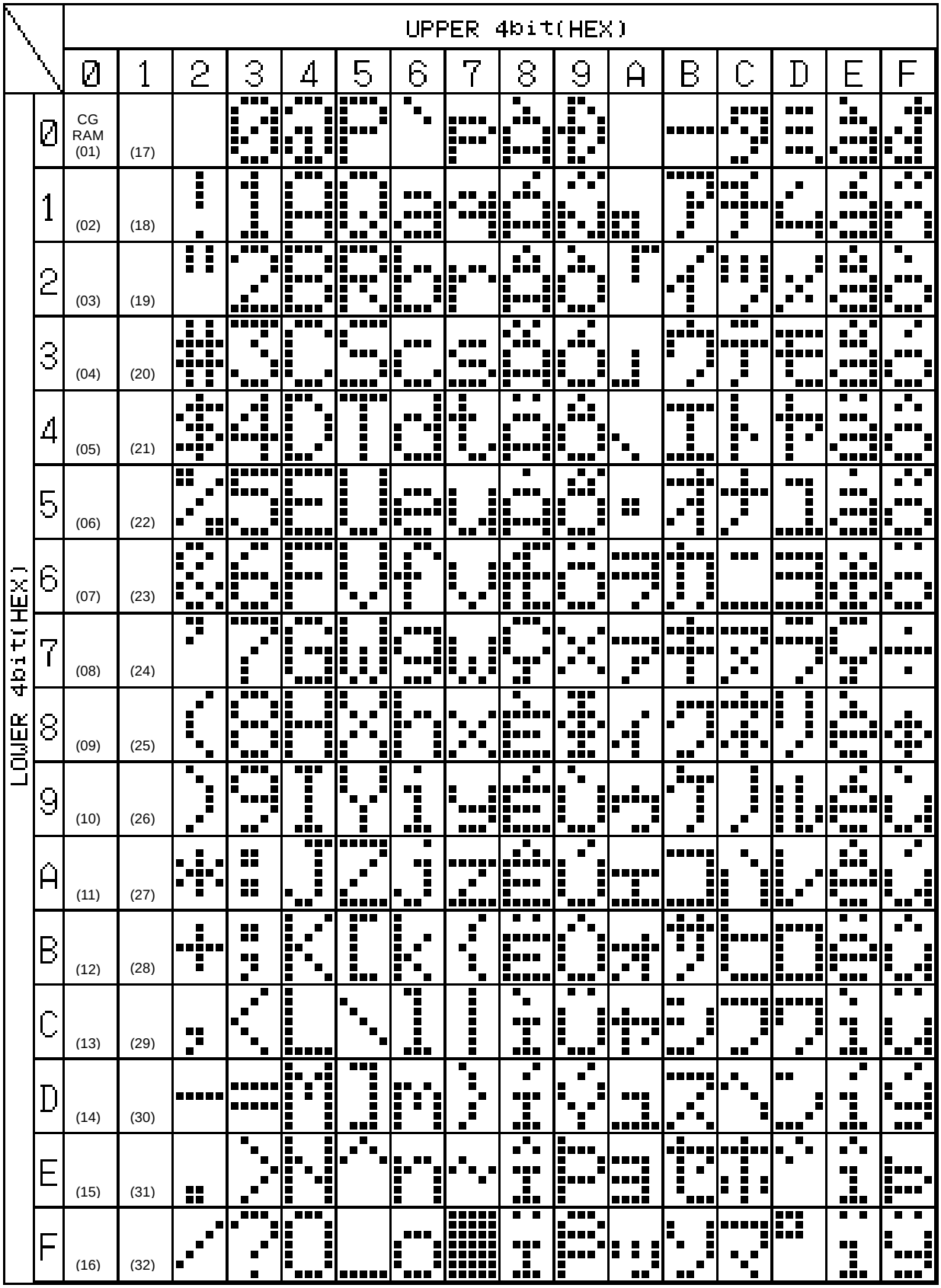


Table 2. CG ROM Character Pattern (ROM version -03)



(1-5) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 32 kind of character in 5 x 7 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$-$(1F)_H$ should be written to the DD RAM as shown in Table 1.

Table 2. shows the correspondence among the character pattern, CG RAM address and Data

Table 2. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots)

Character Code (DD RAM Data)	CG RAM Address			Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 ← → Upper bit Lower bit	7 6 5 4 3 2 1 0 ← → Upper bit Lower bit			4 3 2 1 0 ← → Upper bit Lower bit	
0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * * *	Character Pattern Example (1)
0 0 0 0 0 0 0 1	0 0 0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * * *	Character Pattern Example (2)
		0 0 0 0 0 1			
•	•	•		•	
•	•	•		•	
•	•	•		•	
•	•	•		•	
•	•	•		•	
0 0 0 1 1 1 1 1	1 1 1 1 1	1 0 0 1 0 1 1 1 0 1 1 1			Character Pattern Example (32)

* Don't Care

Note) 1. Character code bit 0 to 4 correspond to the CG RAM address bit 3 to 7 (5bits:32 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is Don't care line. In case of input CG RAM data continuously, invalid address are Cursor position automatically.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code of DD RAM bits 5 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1-6) Icon Display RAM (MK RAM)

The **NJU6627** can display maximum 100 Icons.

The Icon Display can be controlled by writing the Data in MK RAM corresponds to the Icon.

The relation between MK RAM address and Icon Display position is shown below:

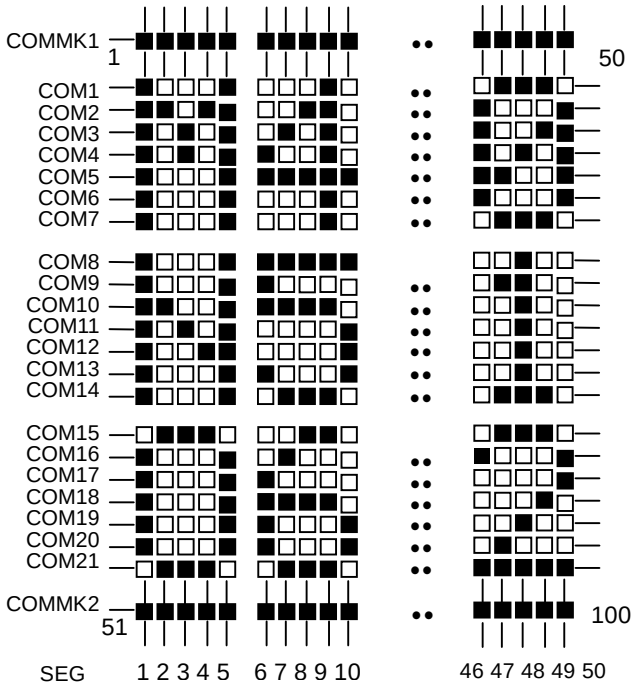


Table 3. Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address (40_H to 53_H)		Bits for Icon Display Position							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
100 0000	40_H	0	0	0	“1”	“2”	“3”	“4”	“5”
100 0001	41_H	0	0	0	“6”	“7”	“8”	“9”	“10”
100 0010	42_H	0	0	0	“11”	“12”	“13”	“14”	“15”
100 0011	43_H	0	0	0	“16”	“17”	“18”	“19”	“20”
:	:	:							
100 0101	53_H	0	0	0	“96”	“97”	“98”	“99”	“100”

Note) After power on or hardware reset, the data of MK RAM can not be initialized. To display Icons, the data of MKRAM need to be written in before display on. The displayed icons can not be shifted by Display Shift instruction.

(1-7) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

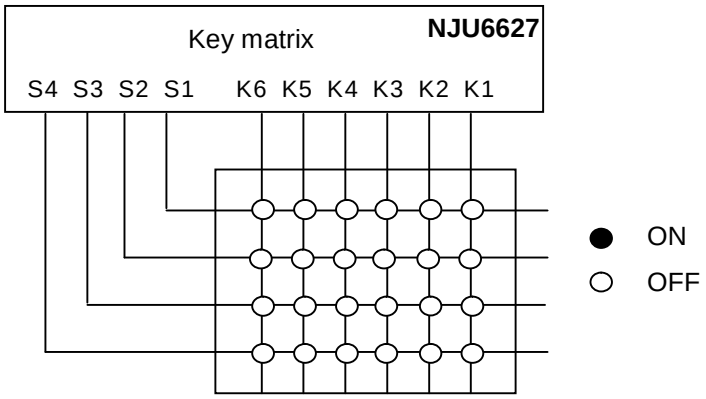
(1-8) LCD Driver

LCD Driver consists of 23-common driver and 50-segment driver.

The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

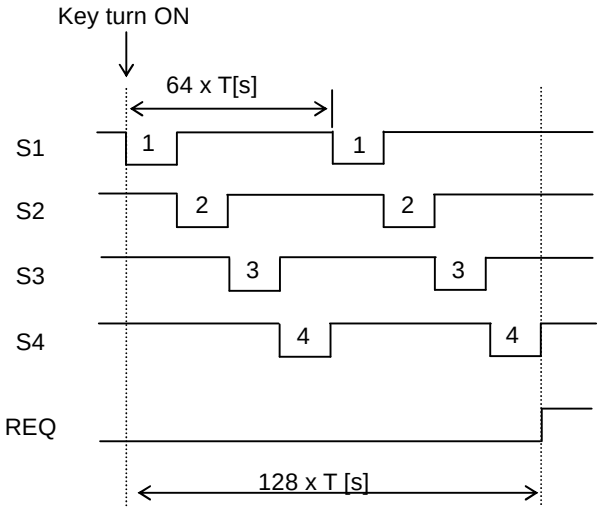
(1-9) Keyscan circuit

The Keyscan circuit consists of a detector block of key pressing and a fetching block of key status. It scans 4x6 key matrix and fetches conditions of 24 keys. Furthermore, it operates correctly against the key roll over input.



(1-10) Timing of Key scan

Key scan cycle is 64 x T[s]. The data of key scan is a result of comparison with a couple of Key scan for correct judge whether Key On or Off. When the result of comparison is correct (accord), the NJU6627 recognizes Key On and outputs “L” level from SO terminal after 128 x T[s] from start of Key scan for a request to read key data out to external CPU. When the REQ terminals outputs “H” signal, the key scan does not operate until end of key data reading by CPU, and scanned key data is kept. When the result of comparison is incorrect (not accord), Key scan operates again if any key is On. Therefore, Key scan may operate incorrectly in case of shorter period of Key on than 128 x T[s]



T=1/ fosc

• Request signal output

When the **NJU6627** detect the key-in to scan start by the key scan circuit, it outputs “H” signal as the request signal from the “REQ” terminal to notice the key pressing information to an application system. The request signal resets to “L” level after Keyscan data read.

• Contents of key register renewal

Contents of key register are no fixed in case of no key operation.

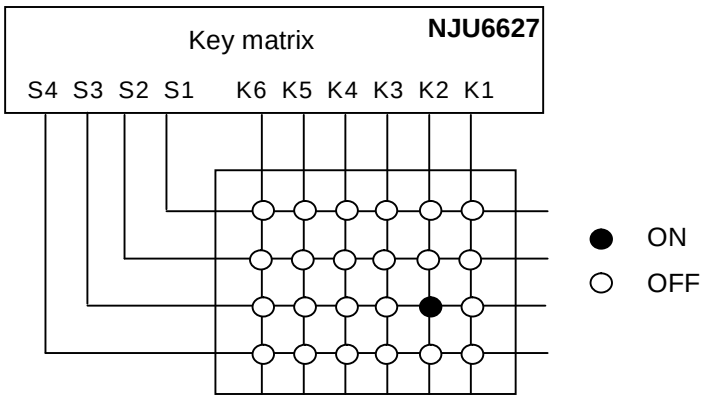
Contents of key register are not changed in busy of key data reading operation.

It stops when a couple of data by continuously twice key scan operations are accorded and fixed as a correct key status. The correct key status data is stored and newly key scan operation does not start until external CPU reads data out after key status is fixed.

When a key on the key matrix is pressed, the bit corresponding to terminals (S1 to S4, K1 to K6) connected the switch goes to “1” and another bits go to “0”.

In case of Example 1, when the switch connecting to K2 and S3 is pressed, bit (D1) corresponding to S3 and K2 go to “1” but another bits go to “0”.

Example 1. One key is pressed



Key register

	D_5	D_4	D_3	D_2	D_1	D_0
S1	K6	K5	K4	K3	K2	K1
S2	K6	K5	K4	K3	K2	K1
S3	K6	K5	K4	K3	K2	K1
S4	K6	K5	K4	K3	K2	K1

•Keyscan data format

Scanned 6-bit data of key are read out through the srial I/F. After the register is chosen, data is read.

D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	0	1	SX1	SX0	*	*	K6	K5	K4	K3	K2	K1

Input Output

SX1	SX0	Keyscan output terminal
0	0	S1
0	1	S2
1	0	S3
1	1	S4

• Keyscan OFF mode

Keyscan operation is turned ON or OFF by the instruction.

After the scanning ends, the key scanning is turned off.

The request signal is output until reading out data even if the turn off command enters while scanning the key. The REQ signal outputs "L" if it reads out data.

Key scan operates shown as follows

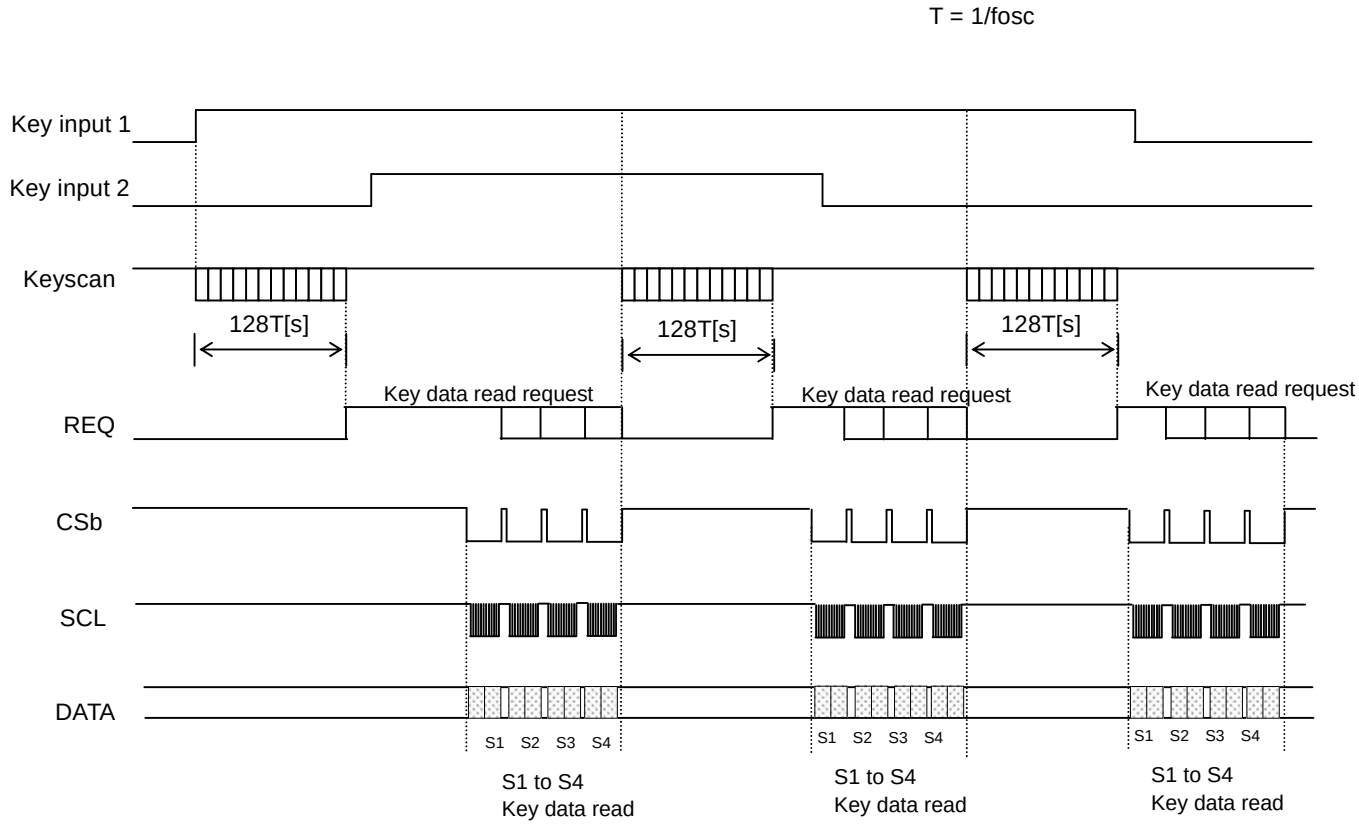
1, Key scan signal output terminals S1 – S4 output “L” signals when key scan does not operate, and output key scan signals after start of key scan operation. The conditions of key scan signal input terminals K1 – K6 are “H” state with internal pull-up resistances, though “L” signal comes in to K1 – K6 corresponding to the turned on keys.

2, The function of key scan starts twice operations when any key is turned on. It stops when a couple of data by continuously twice key scan operations are accorded and fixed as a correct key status. It operates more 2 times when the key status is not fixed and any keys are still turning on. It repeats again and again until key status is fixed. The correct key status data is stored and newly key scan operation does not start until external CPU reads data out after key status is fixed.

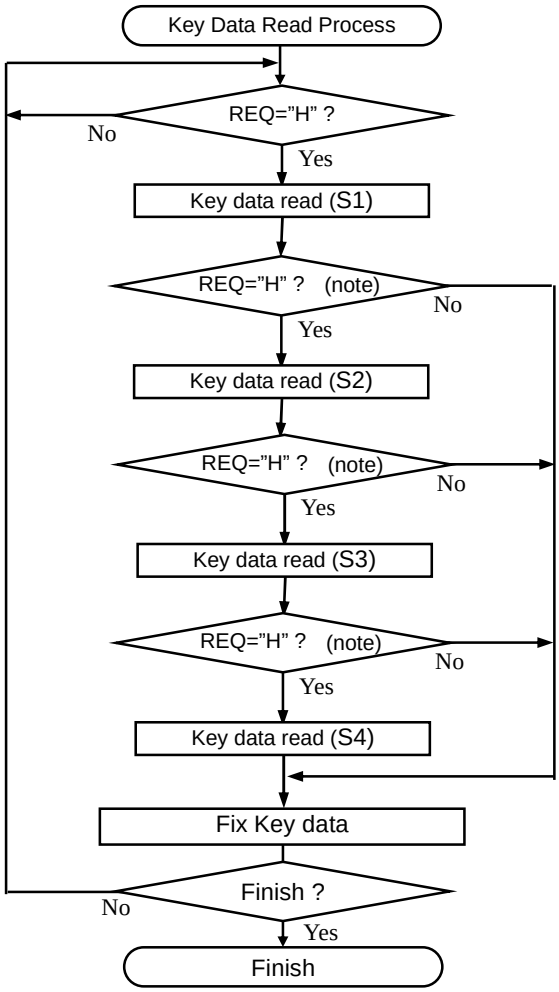
3, When the key status is fixed, REQ terminal outputs “H” signal as Key data read out request to CPU. CPU should read key data out at detection of this “L” signal.

4, The Key data read out request signal is released and REQ terminal outputs “L” signal after finish of CPU key data read out for newly key scan operation. REQ signal shall not be reading between "L".

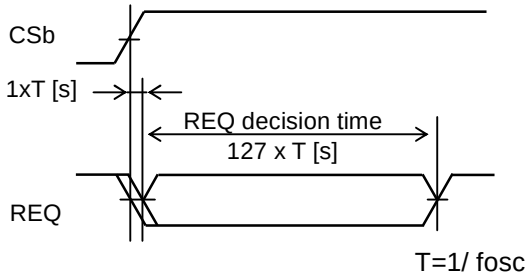
Keyscan example



Key data read flow example



Note)After key data read, please decision REQ signal at the time of REQ decision time of the figure below.



Ex.) Cace of fosc=200KHz
REQ decision time = 127 x 5us = 635us

(1-11) Key More Input

non-pressed key data may change pressed key data in triple or more key Input as shown in Fig. 1 and incorrect key data may be output to external CPU. For prevention of miss-recognition by incorrect key data, diodes should be inserted or control program of CPU should ignore the combination of key data miss-recognition. For example, 4 keys and more ON data should be ignored.

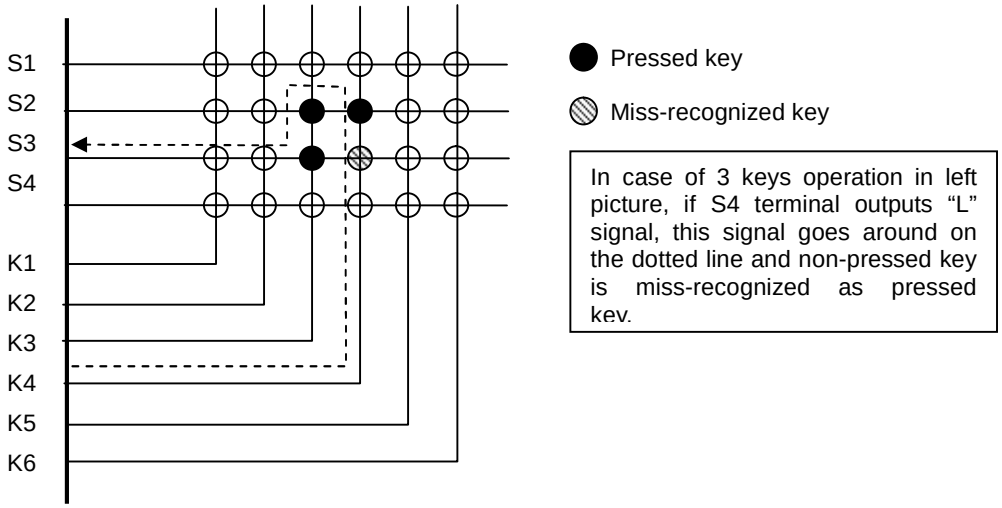
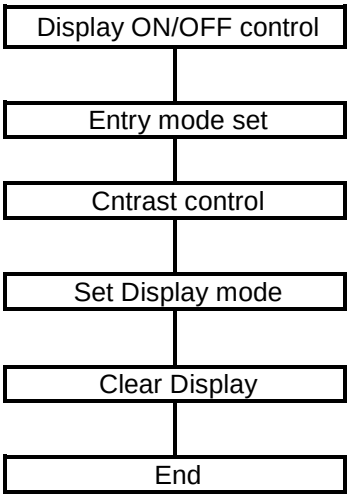


Fig. 1 Miss-recognized example by key more input

(2) Power on Initialization by internal circuits

(2-1) Initialization By Internal Reset Circuits

The **NJU6627** is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, this status is kept 1.45ms (fosc=200kHz) after V_{DD} rises to 4.5V. Initialization flow is shown below:



D=0 Display OFF
M=0 Icon OFF
B=0 Cursor Blink OFF

I/D=1 Increment by 1
S=0 No Shift

E.V.R Value=0000 V_{LCD} Low

V=0 Voltage Booster Circuits OFF
DU=1 Set 1/23Duty (3-line + Icon)
K=1 Keyscan ON
PD=0 Release the power down mode

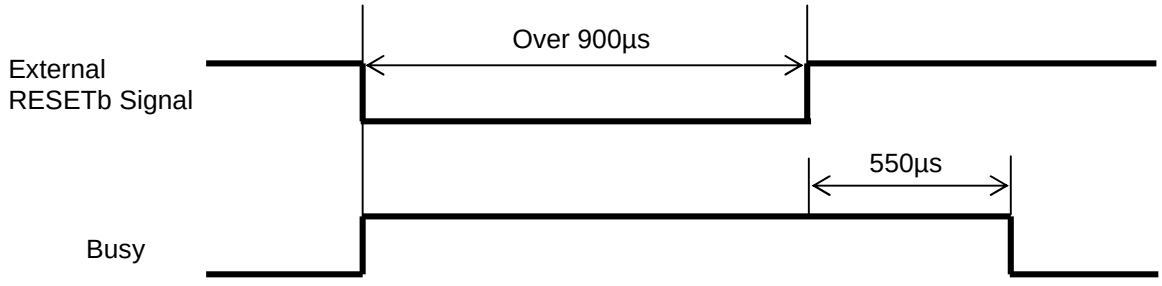
AC=00_H Initialize the address counter to 00H
20_H is written on DD RAM

Note) If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed. In this case the initialization by MPU software is required.

(2-2) Initialization By Hardware

The **NJU6627** incorporates RESETb terminal to initialize the all system. When the "L" level input over 900us to the RESETb terminal, reset sequence is executed. In this time, busy signal output during 550us (fosc=200kHz) after RESETb terminal goes to "H". During this 550us period, any other instruction must not be input to the **NJU6627**.

- Timing Chart



(3) Instructions

The **NJU6627** incorporates two registers, an Instruction Register (IR) and a Data Register (DR).

These two registers store control information temporarily to allow interface between **NJU6627** and MPU or peripheral ICs operating different cycles.

Table 4. Table of Instructions

Instruction		Code																Execute Time *1
		D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(a)	Maker Testing	1	0	0	1	1	1	1	1	Test Data								-
(b)	Clear Display	1	0	0	1	1	0	0	1	*	*	*	*	*	*	*	*	550µs
(c)	Return Home	1	0	0	1	0	0	0	1	*	*	*	*	*	*	*	*	0µs
(d)	Entry Mode Set	1	0	0	0	1	0	0	0	*	*	*	*	*	*	I/D	S	0µs
(e)	Display ON/OFF Control	1	0	0	0	1	0	0	1	*	*	*	*	*	D	M	B	0µs
(f)	Address Shift	1	0	0	1	0	0	1	0	*	*	*	*	*	*	*	ARL	0µs
(g)	Display Shift	1	0	0	0	1	0	1	0	*	*	*	*	*	*	*	DRL	0µs
(h)	Contrast Control	1	0	0	0	1	1	0	0	*	*	*	*	E.V.R Value				0µs
(i)	Set Display Mode	1	0	0	0	1	1	1	0	*	*	*	*	V	DU	K	PD	0µs (PD:35µs)
(j)	Set DD/MK RAM Address	1	0	0	1	0	0	1	1	*	*	*	DD RAM (00 to 29)$_H$					0µs
													MK RAM (40 to 53)$_H$					
(k)	Set CG RAM Address	1	0	0	1	0	0	0	0	CG RAM (00 to FE)$_H$								0µs
(l)	Write DD RAM Data	1	0	0	1	1	0	0	0	Write Data (DD RAM)								35µs
	Write MK RAM Data	1	0	0	1	1	0	0	0	*	*	*	Write Data (MK RAM)					35s
	Write CG RAM Data	1	0	0	1	1	0	0	0	*	*	*	Write Data (CG RAM)					35µs
(m)	Read Keyscan Data	1	0	1	0	0	1	SX		*	*	Key Data						0us

*1 f_{OSC}=200KHz. If the oscillation frequency is changed, the execution time is also changed.

(3-1) Description of each instructions

(a) Maker Test

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	1	1	1	1	*	*	*	*	*	*	*	*

*: Don't care

This code is using for device testing mode (only for maker).
Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".
(Especially please check the output condition of Enable signal when the power turns on.)

(b) Clear Display

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	1	0	0	1	*	*	*	*	*	*	*	*

When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set to increment. The S of entry mode does not change.

Note) The character pattern for character code $(20)_H$ must be blank code in the user-defined character
pattern (Custom font).

(c) Return Home

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	0	0	0	1	*	*	*	*	*	*	*	*

Return home instruction is executed, the DD RAM address $(00)_H$ is set into the address counter. Display is returned its original position if shifted. The DD RAM contents do not change.

(d) Entry Mode Set

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	0	1	0	0	0	*	*	*	*	*	*	I/D	S

Entry mode set instruction which sets the address moving direction and display shift On/Off, is executed when the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the whole display shift in the DD RAM writing.

I/D	Function
1	Address increment : The address of the DD RAM or MK RAM or CG RAM increment(+1) when the write.
0	Address decrement : The address of the DD RAM or MK RAM or CG RAM decrement(-1) when the write.

S	Function
1	Whole display shift. The shift direction is determined by I/D. : Shift to the left at I/D=1 and shift to the right at the I/D=0. The display does not shift when writing into CG RAM, MK RAM
0	The display does not shift.

(e) Display ON/OFF Control

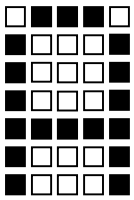
	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	0	1	0	0	1	*	*	*	*	*	D	M	B

Display On/Off control instruction which controls the whole display On/Off and the addressed position character blink, is executed when the codes of (D) and (B) are written into DB_2(D) and DB_0(B), as shown below.

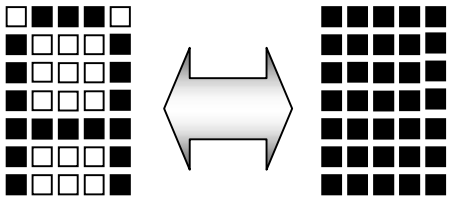
D	Function
1	Display On.
0	Display Off. In the mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

M	Function
1	Icon display ON.
0	Icon display OFF.

B	Function
1	The addressed position character is blinking. Blinking rate is 500ms at f_{OSC}=145kHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots
(1) Cursor display example



Alternating display
(2) Blink display example

When the number of dot-shift is not set “0” in (j) Dot shift instruction, the blink operation will be appeared at the irregular position.

(f) Address Shift

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	0	0	1	0	*	*	*	*	*	*	*	ARL

The Address shift instruction shifts the Address to the right or left without writing or reading display data.

ARL	Function
0	Shift the address position to the left ((AC) is decremented by 1)
1	Shift the address position to the right ((AC) is incremented by 1)

(g) Display Shift

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	0	1	0	1	0	*	*	*	*	*	*	*	DRL

The Display shift instruction shifts the Display to the right or left without writing or reading display data. The contents of address counter (AC) does not change by operation of the display shift only.

DRL	Function
0	Shifts the whole display to the left and the cursor follows it.
1	Shifts the whole display to the right and the cursor follows it.

(h) Contrast Contol

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	0	1	1	0	0	*	*	*	*	C3	C2	C1	C0

Contrast Control instruction which adjusts the contrast of the LCD is executed when the code "1" is written into D_6 and the codes of C3 to C0 are written into D_3 to D_0 as shown below.
The contrast of LCD can be adjusted one of 16 voltage-stages by setting this 4-bit register.
See (4-1) "how to adjust the Contrast of LCD".
Set the binary code "1,1,1,1" when contrast adjustment is unused.

C3	C2	C1	C0	VLCD voltage (Spec)	Ex.) VLCD voltage by VOUT=8.4V
0	0	0	0	VOUT x 80/95	7.074
0	0	0	1	VOUT x 80/94	7.149
0	0	1	0	VOUT x 80/93	7.226
0	0	1	1	VOUT x 80/92	7.304
0	1	0	0	VOUT x 80/91	7.385
0	1	0	1	VOUT x 80/90	7.467
0	1	1	0	VOUT x 80/89	7.551
0	1	1	1	VOUT x 80/88	7.636
1	0	0	0	VOUT x 80/87	7.724
1	0	0	1	VOUT x 80/86	7.814
1	0	1	0	VOUT x 80/85	7.906
1	0	1	1	VOUT x 80/84	8.000
1	1	0	0	VOUT x 80/83	8.096
1	1	0	1	VOUT x 80/82	8.195
1	1	1	0	VOUT x 80/81	8.296
1	1	1	1	VOUT x 80/80	8.400

(i) Set Display Mode

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	0	1	1	1	0	*	*	*	*	V	DU	K	PD

The Set Display Mode instruction control the function of Keyscan and power down mode.

V	Function
1	Voltage Booster Circuits ON.
0	Voltage Booster Circuits OFF. When the internal voltage booster is not used, supply each level of LCD driving voltage from VOUT terminal.

DU	Function
1	1/23Duty (3-line + Icon)
0	1/16Duty (2-line + Icon)

K	Function
1	Keyscan ON
0	Keyscan OFF All of segment terminal (S_1 to S_4) output the voltage of V_{SS}.

PD	Function
1	Power down mode. All common and segment terminal set the voltage level of V_{SS}.
0	Release the power down mode.

In busy of Power down mode, do not input any instructions except for release the power down mode.

The power down mode should be set before power off because any irregular display appearance at power off is prevented.

• The Keyscan operation when switching to the power down mode during Keyscan

When switching to the power down mode during key scan operation, it stops Keyscan operation in the period and after power down mode restart the Keyscan.

After power down mode cancellation, the REQ signal maintains "H" when detects key-in signal before switches to power down mode and REQ signal rises to "H".

However, the key scan operation becomes invalid data even if it reads key-in data because it stopped.

(j) Set DD/MK RAM Address

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	0	0	1	1	*	AD6	AD5	AD4	AD3	AD2	AD1	AD0

The address data (D_4 to D_0) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing is performed into the addressed DD/MK RAM.
The RAM includes DD RAM and MK RAM, and these RAMs are shared by address as shown below.

	RAM Address		
DD RAM 1-line:	$(00)_H$	to	$(09)_H$
DD RAM 2-line:	$(10)_H$	to	$(19)_H$
DD RAM 3-line:	$(20)_H$	to	$(29)_H$
MK RAM :	$(40)_H$	to	$(53)_H$

(k) Set CG RAM Address

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	0	0	0	0	AC7	AC6	AC5	AD4	AD3	AD2	AD1	AD0

The CG RAM address set instruction is executed when the "H" level input to the AC terminal and the address is written into D_7 to D_0 as shown above.
The address data (D_7 to D_0) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing is performed into the addressed RAM.
The RAM includes CG RAM address as shown below.

	RAM Address		
CG RAM :	$(00)_H$	to	$(FE)_H$

(l) Write Data to CG, DD or MK RAM

- Write Data to DD RAM

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	1	0	0	0	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

- Write Data to MK RAM

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	1	0	0	0	*	*	*	DM4	DM3	DM2	DM1	DM0

- Write Data to CG RAM

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	0	1	1	0	0	0	*	*	*	DC4	DC3	DC2	DC1	DC0

By the execution of this instruction, the binary 8-bit data (D_7 to D_0) are written into the DD RAM, and the binary 5-bit data (D_4 to D_0) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment (+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(m) Read Data Key

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Code	1	0	1	0	0	1	SX1	SX0	*	*	K6	K5	K4	K3	K2	K1
	←				Input		→		←			Output			→	

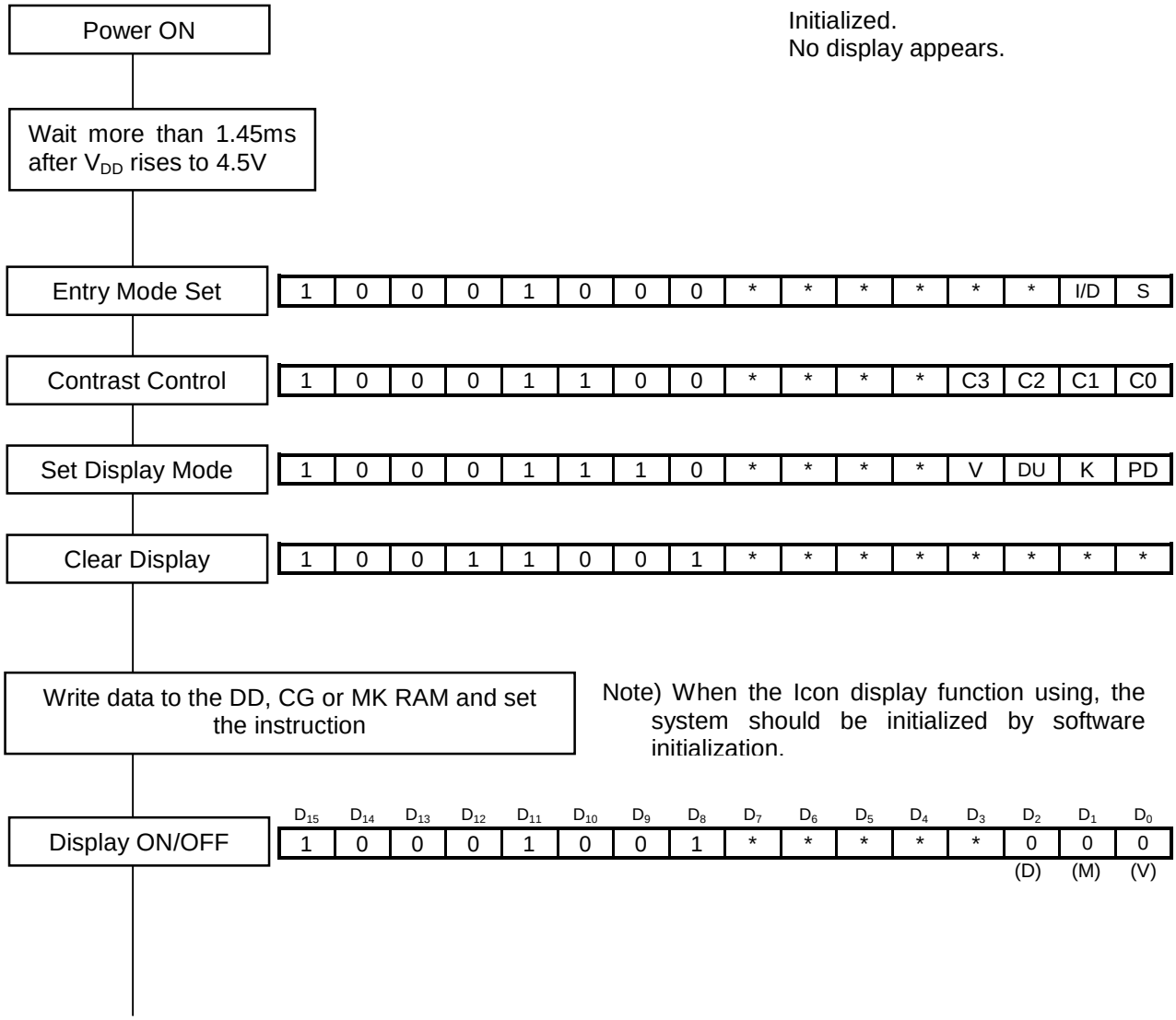
Read data key is a instruction for data reading out of Keyscan.
Select read register.

SX1	SX0	Keyscan output terminal
0	0	S1
0	1	S2
1	0	S3
1	1	S4

However, the bit 8 to 15 are input data. After this 8-bit data were input, the operation change to output from input at the falling edge of 8th SCK clock.

(3-2) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not satisfied, the **NJU6627** must be initialized by the instruction.



(4) Internal power circuits

(4-1) Voltage converter

The doubler power voltage input from the VCI terminal can be turned on and off by setting the instruction.

Set Display Mode instruction D3 = "1" : Voltage Booster Circuits ON

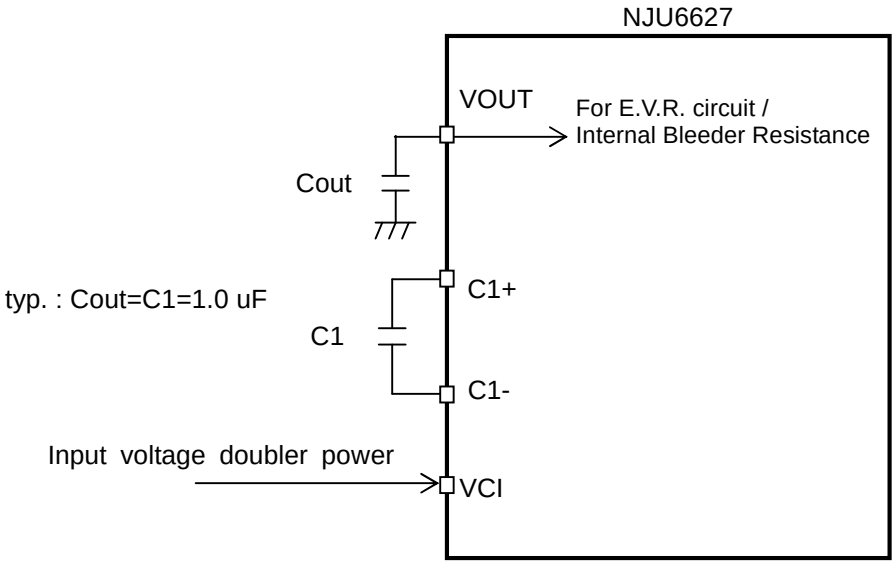
The voltage input to the VCI terminal is boost 2-times. Please set the input so that the output should not exceed 10.5V.

Set Display Mode instruction D3 = "0" : Voltage Booster Circuits OFF

The voltage converter output is turned off.

Irregular data displayed at power supply ON or OFF, and turn off Voltage converter.

When the internal voltage booster is not used, supply each level of LCD driving voltage from VOUT terminal.



Voltage Doubler

(4-2) Bleeder Resistance

Each LCD driving voltage (V_1, V_2, V_3, V_4) is LCD driving high voltage input to the V_{LCD1} terminal, generated by the E.V.R. and high impedance bleeder resistance.

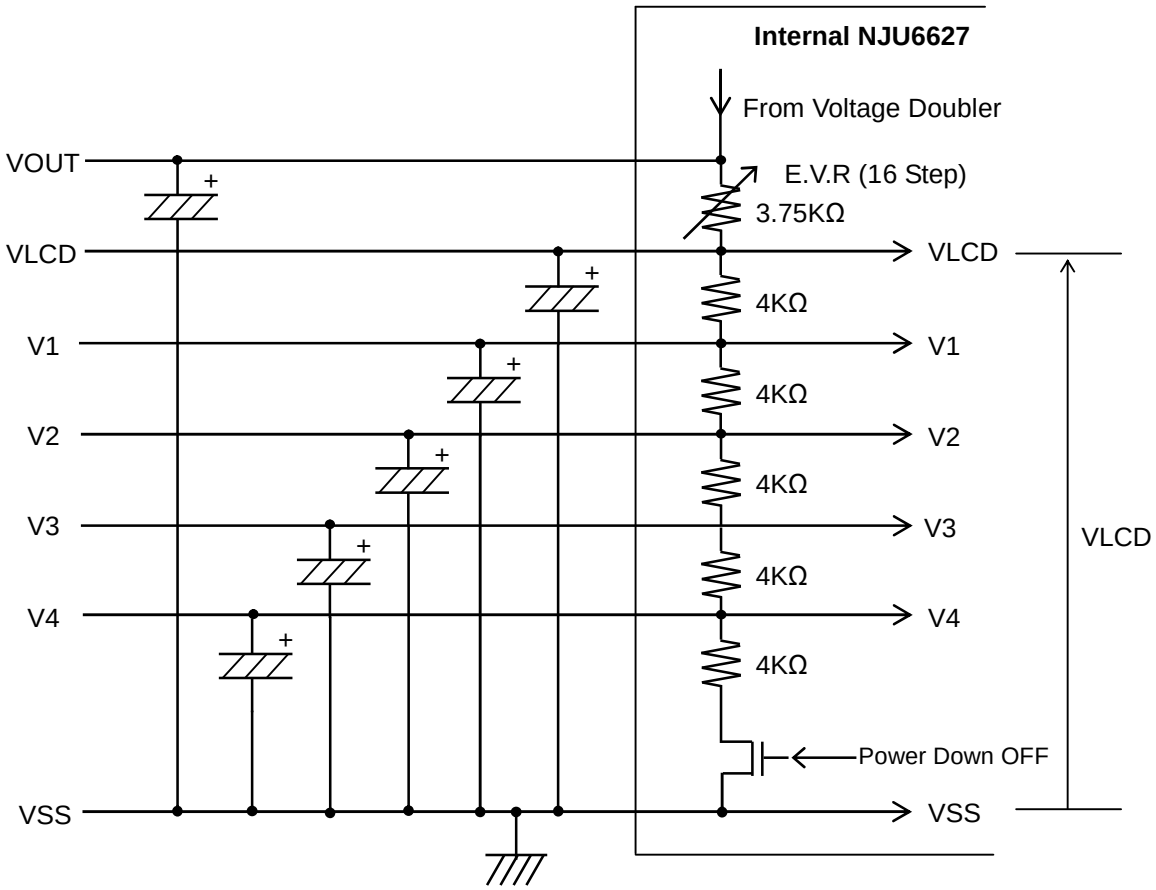
The bleeder resistance is set 1/4 bias suitable for 1/8 duty ratio.

The capacitor connected between V_{LCD2} / V_1/ V_2/ V_4 and V_{SS} is needed for stabilizing V_{LCD}. The determination of the each capacitance requires to operate with the LCD panel actually.

LCD Driving Voltage v.s. Duty Ratio

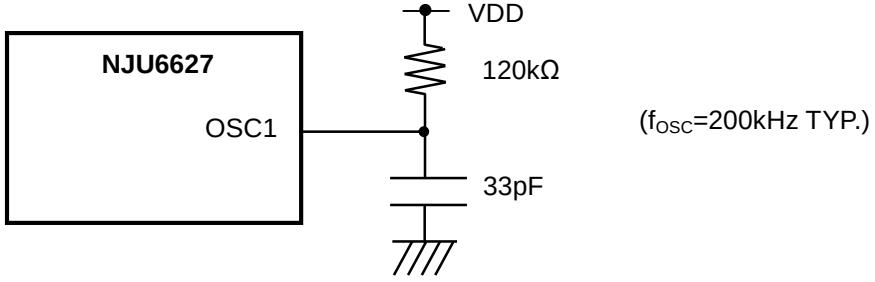
Power supply	Duty Ratio	1/16, 1/23
	Bias	1/5
V_{LCD}		V_{LCD2}- V_{SS}

V_{LCD} is the maximum amplitude for LCD driving voltage.



(4-3) Oscillation Circuit

A resistor and capacitor are connected to OSC_1 pin to configure the oscillation circuit. External clock can also be inputted through the OSC_1 pin.

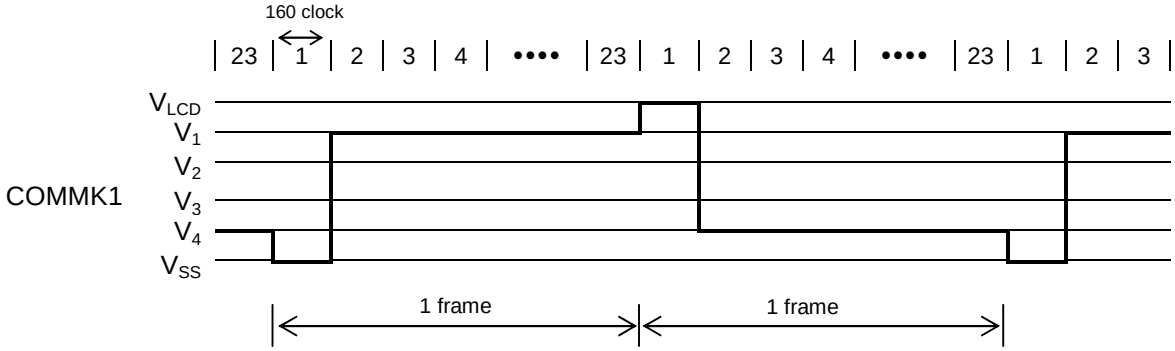


(f_{OSC}=200kHz TYP.)

(4-4) Relation between oscillation frequency and LCD frame frequency

As the **NJU6627** incorporate oscillation capacitor and resistor for CR oscillation, 200kHz oscillation is available without any external components.

The LCD frame frequency example mentioned below is based on 200kHz oscillation.(1clock =5.0us)

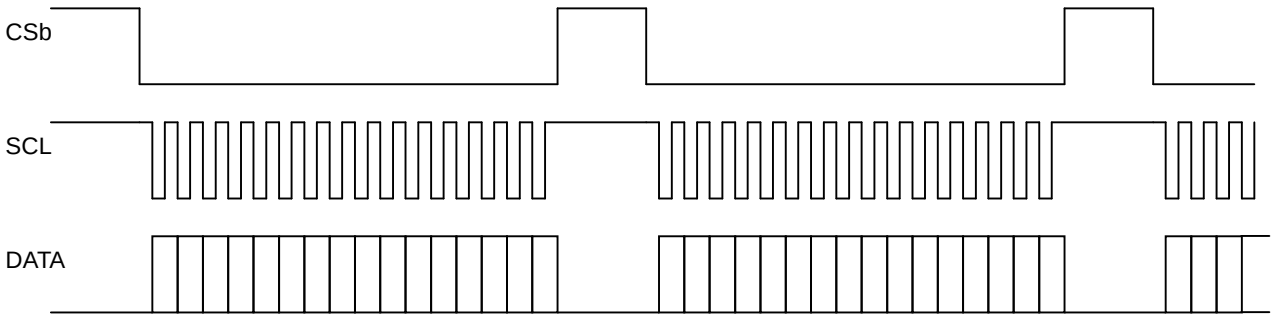


1 frame = 5.0(us) x 160 x 23 = 12.65(ms)
Frame frequency = 1 / 12.65(ms) = 79.0(Hz)

(5) Interface with MPU

The instructions and data are communicated with the serial port which is a clock synchronization type based on 16-bit per word.

The **NJU6627** can be controlled by the serial data as shown below.



The serial interface circuit operates in CSb=L.

A communication unit consists of 16-bit data. The communication period is from the falling edge of CSb terminal to the rising edge. The inputs data and latched at rising edge of shift clock (SCL) and the first 16-bit data are fetched into the **NJU6627** at the rising edge of chip select (CSb). The data over than 16 bits are ignored. If the input data are less than 16 bits, they are ignored at the rising edge of "CSb". Therefore, just 16 bits data should be input for the correct communication. In case of RAM data input, the RAM address is changed automatically as increment or decrement.

The data to input is MSB first. Although the output data is just only key scan, data bits D_8 to D_{15} in the key data read out instruction are input. After these 8-bit instruction is input, this serial data input terminal is changed to the output terminal at the 8th falling edge of SCL clock.

The electrical short between the **NJU6627** and external circuit must be prevented in the application.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage (1)	V_{DD}	-0.3 to +7.0	V	
Supply Voltage (2)	V_{CI}	-0.3 to +7.0	V	V_{CI} Terminal
Supply Voltage (3)	V_{OUT}, $V_{LCD,}$ V_1 to V_4	V_{SS}+0.3 to V_{SS}+10.5	V	V_{OUT}, $V_{LCD,}$ V_1 to V_4 Terminal
Input Voltage	V_t	-0.3 to V_{DD}+0.3	V	OSC1, SCL, DATA, CSb, RESETb, K1-K6 terminals
Operating Temperature	T_{opr}	-40 to +85	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause mal function and poor reliability.

Note 2) Decoupling capacitor should be connected between V_{DD}-V_{SS}, V_{CI}-V_{SS}, V_{OUT}-V_{SS} due to the stabilized operation for the Voltage converter.

Note 3) All voltage values are specified as V_{SS} = 0V
The relation : $V_{OUT} \geq V_{LCD} > V_{DD} > V_{SS}$, V_{SS}=0V must be maintained.

Note 4) in case of internal Voltage Doubler use, $V_{OUT} \geq V_{CI}$ x 2 must be maintained.

■ ELECTRICAL CHARACTERISTICS

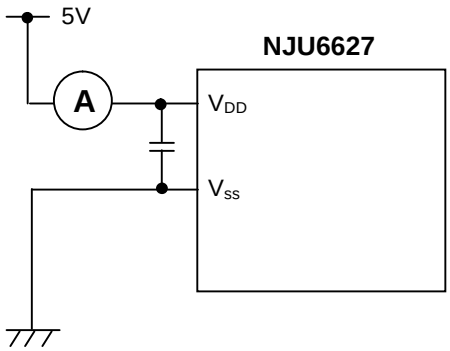
(V_{DD}=4.5V to 5.5V, Ta= -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Power supply (1)	V_{DD}	V_{DD}		4.5	-	5.5	V	
Power supply (2)	V_{CI}	V_{CI}		3.0	-	5.0	V	
Power supply (3)	V_{OUT}	V_{OUT}		V_{DD}	-	10.0	V	4
Input Voltage (1)	V_{IH1}	OSC1,SCL, DATA, CSb, RESETb		$0.8V_{DD}$	-	V_{DD}	V	
	V_{IL1}			V_{SS}	-	$0.2V_{DD}$		
Input Voltage (2)	V_{IH2}	K1-K6		$0.8V_{DD}$	-	V_{DD}	V	
	V_{IL2}			V_{SS}	-	$0.4V_{DD}$		
Output Voltage (1)	V_{OH1}	REQ,DATA	I_{OH1}=-2mA,V_{DD}=5.0V	4.0	-	-	V	
	V_{OL1}		I_{OL1}=1mA,V_{DD}=5.0V	-	-	0.5		
Output Voltage (2)	V_{OH2}	S1-S4	I_{OH}=-20uA ,V_{DD}=5.0V	$0.8V_{DD}$		V_{DD}	V	
	V_{OL2}		I_{OL2}=500uA ,V_{DD}=5.0V	V_{SS}		$0.2V_{DD}$		
Driver On-resist. (COM)	R_{COM}	COM1-COM21 COMMK1, COMMK2	±Id=1uA(COM) V_O=V_{LCD},V_{SS},V_1,V_4	-	-	40	kΩ	5
Driver On-resist. (SEG)	R_{SEG}	SEG1-SEG50	±Id=1uA(SEG) V_O=V_{LCD},V_{SS},V_2,V_3	-	-	40	kΩ	5
Pull-up MOS Current 1	$-I_{p1}$	DATA	V_{DD}=5V, V_{IN} =V_{SS}	5	25	50	uA	
Pull-up MOS Current 2	$-I_{p2}$	K1-K6	V_{DD}=5V, V_{IN} =V_{SS}	10	25	50	uA	
Input Leakage Current	I_{LI}	SCL, CSb, RESETb	V_{IN}=0 to V_{DD}	-1.0	-	1.0	uA	
Operating Current	I_{DD1}	V_{DD}	V_{DD}=5V, f_{OSC}=200 kHz, Display ON, Keyscan ON	-	120	300	uA	6
	I_{DD2}		V_{DD}=5V, Power down mode	-	5	10	uA	6
	I_{CI}	V_{CI}	V_{CI}=5V, f_{OSC}=200 kHz, Voltage Booster Circuits ON E.V.R. value : "1111"		1.1	1.6	mA	
Bleeder resistance circuit — LCD Driving Voltage	V_1	V_1	E.V.R. value : "1111" V_{LCD}= 8.0V	6.2	6.4	6.6	V	
	V_2	V_2		4.6	4.8	5.0		
	V_3	V_3		3.0	3.2	3.4		
	V_4	V_4		1.4	1.6	1.8		
Bleeder resistance circuit — Bleeder resistance RB= (V_{LCD}-V_{SS})/IB	RB	V_{LCD}	E.V.R. value : "1111" V_{OUT}=8.0V, Ta=25°C	14.0	20.0	26.0	KΩ	
Voltage Booster output voltage	V_{out}	V_{OUT}	V_{CI}=5V, f_{OSC}=200 kHz, Voltage Booster Circuits ON Ta=25°C	9.0	9.8		V	
Internal Oscillation Frequency	f_{OSC}	OSC1	V_{DD}=5V, Ta=25°C Rosc=120kΩ, Cosc=33pF	160	200	240	kHz	
External Clock Frequency	f_{CP}	OSC1	Input from OSC_1	280	400	520	kHz	7
External Clock Duty	Duty	OSC1	Input from OSC_1	45	50	55	%	
V_{OUT} Current	I_{OUT}	V_{OUT}	V_{OUT}=8.0V E.V.R. value : ”1111” Ta=25°C	-	0.4	1.0	mA	

Note 4) Apply to the output voltage from each COM and SEG are less than +0.15V against the LCD driving constant voltage (V_{DD}, V_{LCD1}) at no load condition.

Note 5) R_{COM} and R_{COM} are the resistance values between power supply terminals (V_{SS}, V_{LCD} or V_1,V_4) and each common terminal (COM_1 to COM_{21}/COMMK1/COMMK2) and supply voltage (V_{SS}, V_{LCD} or V_2,V_3) and each segment terminal (SEG_1 to SEG_{50}) respectively, and measured when the current Id is flown on every common and segment terminals at a same time.

- Operating Current Measurement Circuit



Note 6) If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

Note 7) External Clock Frequency is 1/2 dividing frequency internally. Therefore, it becomes the same frequency as the internal oscillation circuit.

■ Bus timing characteristics

• Serial Interface Sequence

(V_{DD}=4.5V to 5.5V, Ta=-40 to +85°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT	Note
Serial clock cycle time	t_{CYCE}	1	-	us	
Serial clock width	t_{SC}	300	-	ns	
Chip select pulse width	PW_{CS}	800	-	us	8
Chip select pulse width		50	-	us	9
Chip select pulse width		1	-	us	10
Chip select set up time	t_{CSU}	300	-	ns	
Chip select hold time 1	t_{CH1}	300	-	ns	
Serial input data set up time	t_{SISU}	300	-	ns	
Serial input data hold time	t_{SIH}	300	-	ns	
Key data output delay time	t_{KDD}	-	300	ns	
Data port direction change time from input to output	t_{SRWD}	-	300	ns	
Data port direction change time From output to input	t_{CRWD}	-	300	ns	
Chip select hold time 2	t_{CH2}	1	-	us	
Input Signal Rising Edge	t_R		15	ns	
Input Signal Falling Edge	t_F		15	ns	

Note8) Condition: The clear display command input. (Refer to the Table 4)
Note9) Condition: The Ram writing and power down mode ON. (Refer to the Table 4)
Note10) Condition: The instruction input except Note8 and Note9. (Refer to the Table 4)

Fig.1 Input Data Sequence

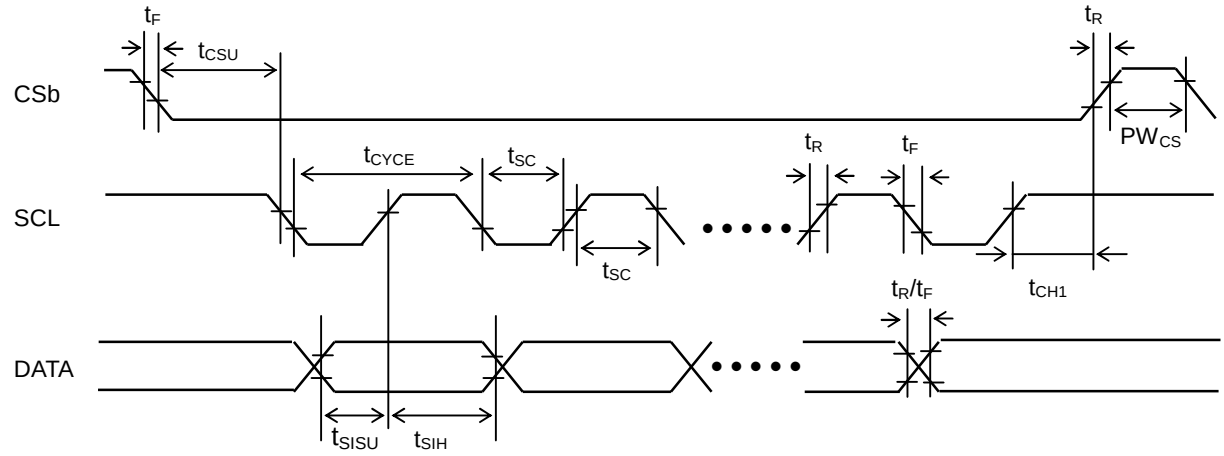
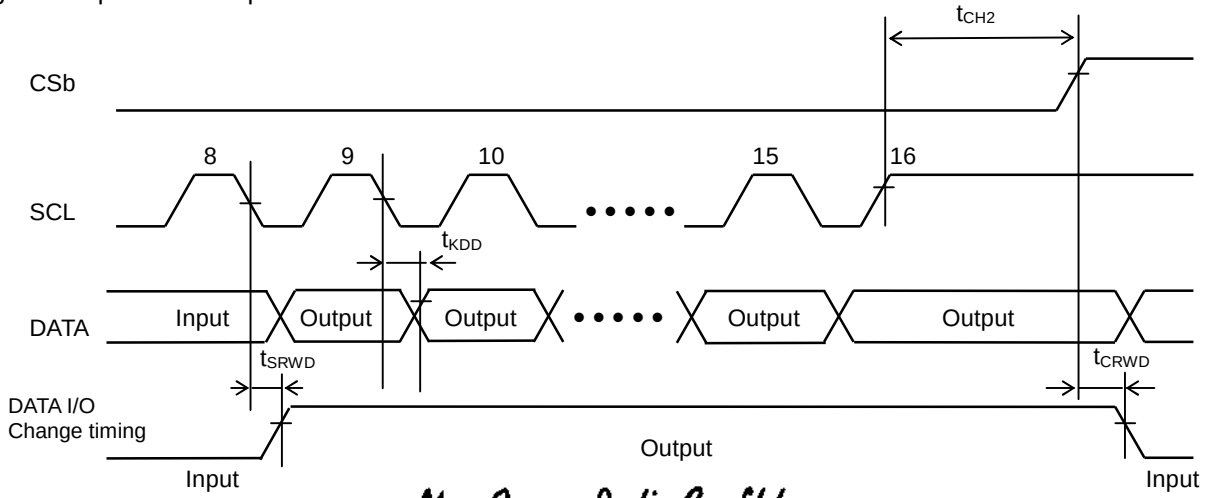


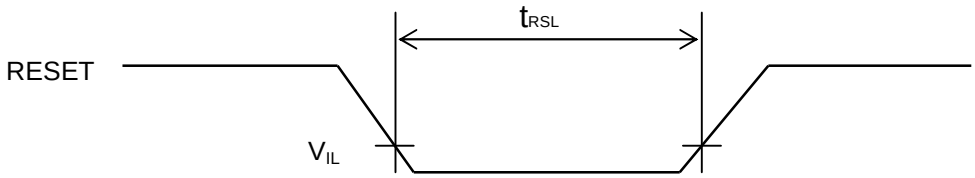
Fig.2 Output Data Sequence



• The Input Condition when using the Hardware Reset Circuit

(Ta=25°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Reset input "L" level width (f_{OSC}=200KHz)	t_{RSL}	900	-	-	µs	

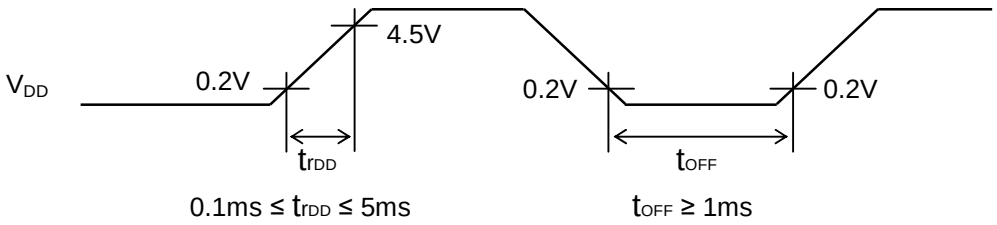


• Power Supply Condition when using the internal initialization circuit

(Ta=25°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Power supply rise time	t_{rDD}	0.1	-	5	ms	
Power supply OFF time	t_{OFF}	1	-	-	ms	

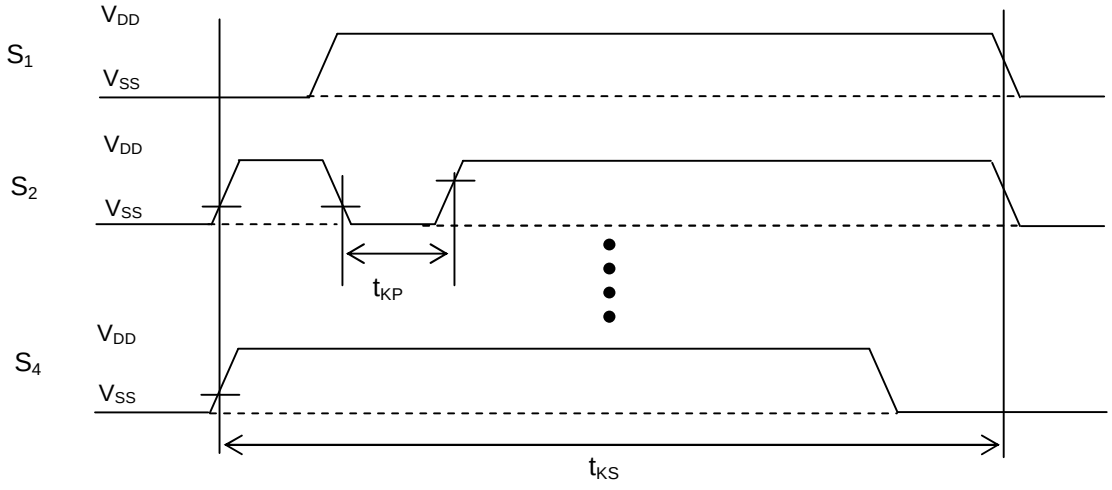
Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction. (Refer to initialization by the instruction)



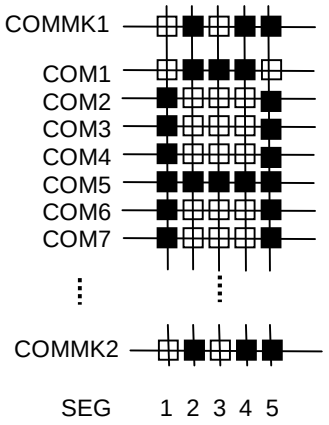
• Key scan timing

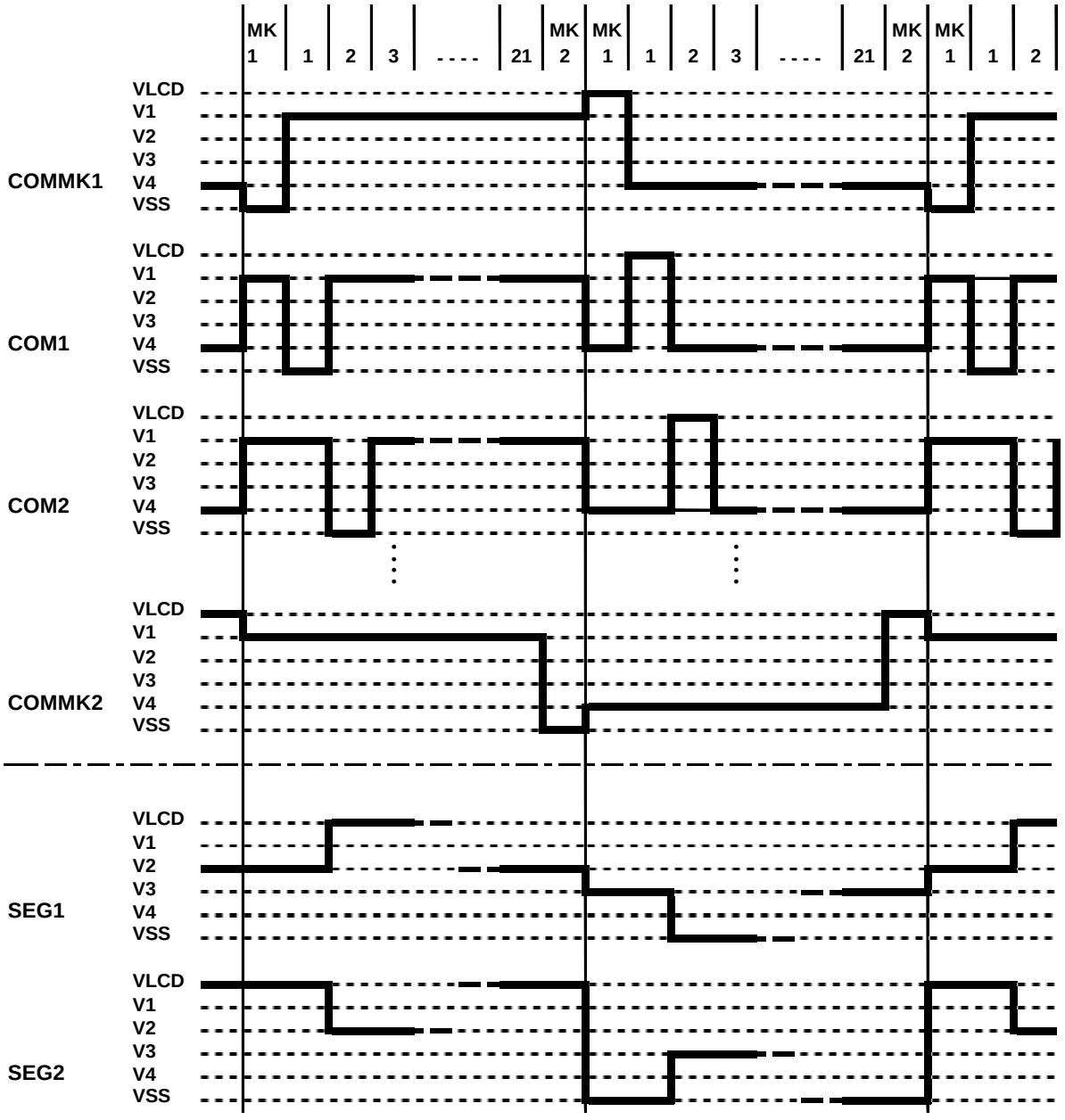
(f_{OSC}=200KHz)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Keyscan time	t_{KS}	-	320	-	us	
Keyscan palse width	t_{KP}	-	80	-	us	

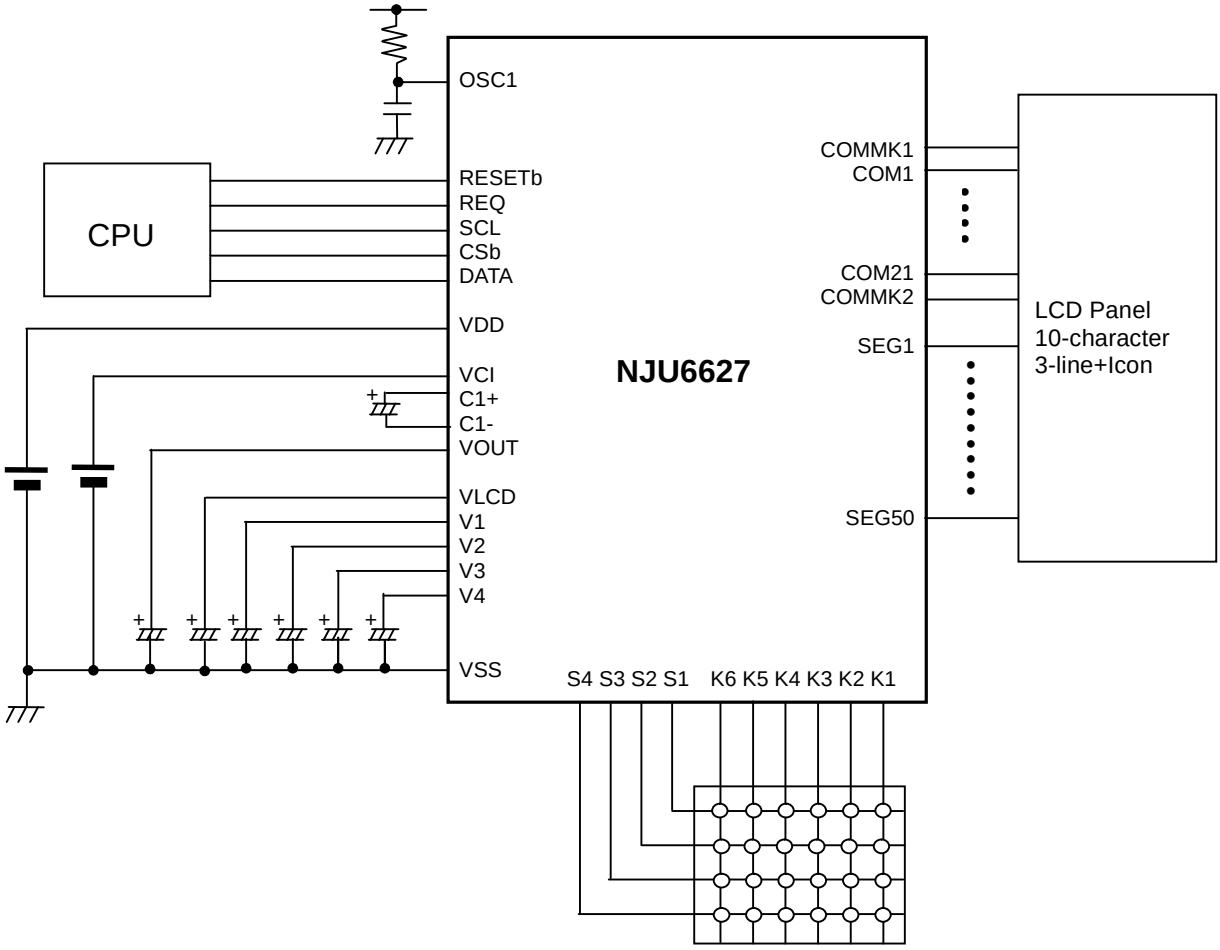


■ LCD DRIVING WAVE FORM





■ APPLICATION CIRCUITS



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