16-CHARACTER 1-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU6460A is a 1 Chip Dot Matrix LCD controller driver for up to 16-character 1-line or 8-character 2-line display.

It contains microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM and common and segment drivers.

The bleeder resistance generates for LCD Bias voltage internally.

The CR oscillator incorporates C and R, therefore no external components for oscillation are required.

The microprocessor interface circuits which operate 2MHz frequency, can be connected directly to 4bit/8bit microprocessor.

The character generator consists of 7,680 bits ROM and 32 x 5 bits RAM. The standard version ROM is coded with 192 characters including capital and small letter fonts.

The 16-common and 40-segment drives up to 16-character 1-line LCD panels which divided two common electrode blocks.

The rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE

NJU6460AC

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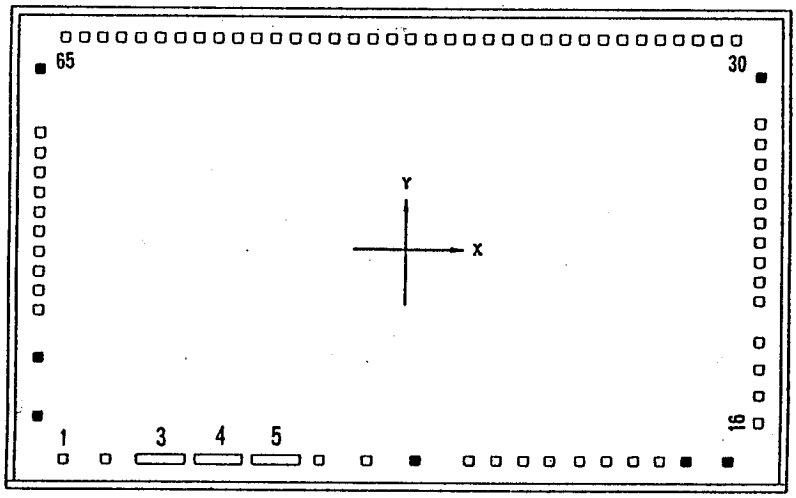
■ FEATURES

- 16-character 1-line Dot Matrix LCD Controller Driver
- 4/8 Bit Microprocessor Direct Interface
- Display Data RAM - 16 x 8 bits ; Maximum 16-character 1-line Display
- Character Generator ROM - 7680 bits ; 192 Characters for 5 x 7 Dots
- Character Generator RAM - 32 x 5 bits ; 4 Patterns(5x7 Dots)
- Microprocessor can access to Display Data RAM and Character Generator RAM
- High Voltage LCD Driver ; 16-common / 40-segment
- Duty Ratio ; 1/16 Duty
- Number of Maximum Display Characters ; 16-Character
- Useful Instruction Set
  Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift,
- Common and Segment driver Location order Select Function
  (Pin configuration mode A / mode B)
- Power On Initialize / Hardware Reset Function
- Bleeder Resistance On-chip
- Oscillation Circuit On-chip
- Low Power Consumption
- Operating Voltage --- +5 V
- Package Outline --- Bumped Chip / TCP
- C-MOS Technology

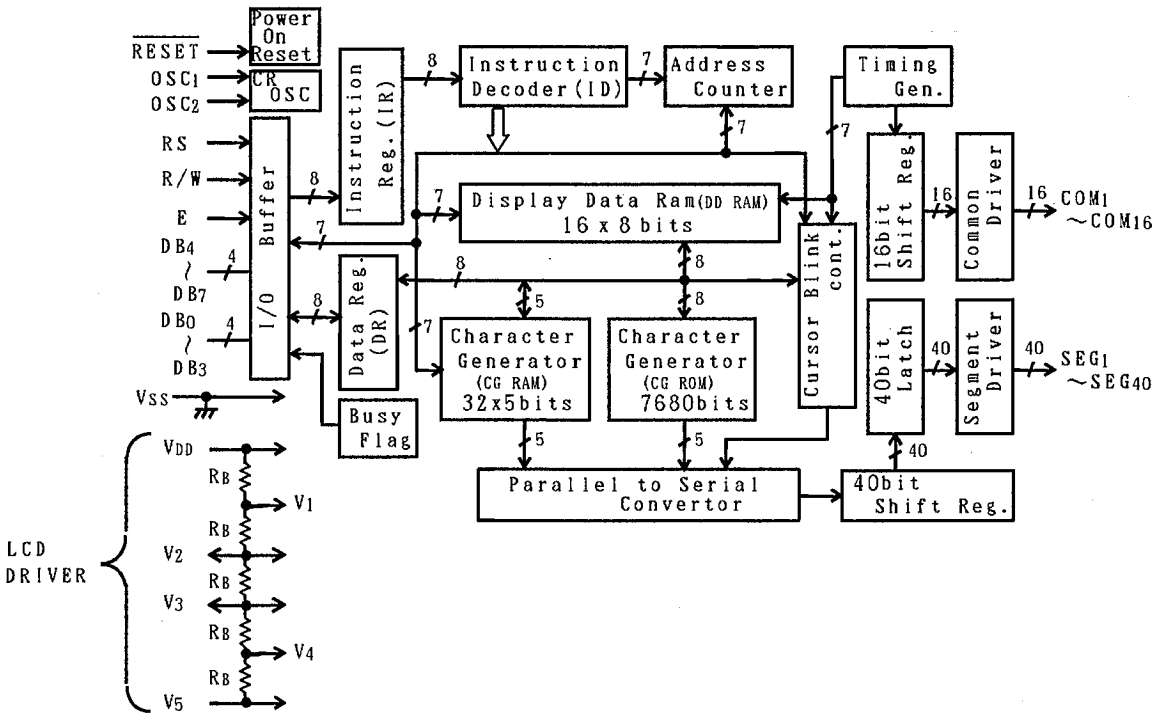
■ PAD LOCATION



Chip Size : X = 4.10mm , Y = 2.50mm
Chip Center : X = 0um , Y = 0um
Pad Size : 50um × 50um
(V_{DD}, V_{SS}, V_5: 250um × 50um)

Bump Size : 60um × 60um
Bump Heigt : 25um Typ.
Bump Material : Au

■ BLOCK DIAGRAM



■ COORDINATES

Pin No.	Pad Name		CENTER	
	Pin configuration		X=(μm)	Y=(μm)
	Mode A	Mode B		
1	OSC_1	OSC_1	-1742	-1078
2	OSC_2	OSC_2	-1514	-1078
3	V_{SS}	V_{SS}	-1231	-1078
4	V_{DD}	V_{DD}	-931	-1078
5	V_5	V_5	-631	-1078
6	V_3	V_3	-408	-1078
7	V_2	V_2	-164	-1078
—	NC1	NC1	93	-1078
8	$\overline{RESET}$	$\overline{RESET}$	368	-1078
9	RS	RS	508	-1078
10	R/W	R/W	649	-1078
11	E	E	786	-1078
12	DB_0	DB_0	945	-1078
13	DB_1	DB_1	1085	-1078
14	DB_2	DB_2	1225	-1078
15	DB_3	DB_3	1365	-1078
—	NC2	NC2	1510	-1078
—	NC3	NC3	1725	-1078
16	DB_4	DB_4	1882	-876
17	DB_5	DB_5	1882	-736
18	DB_6	DB_6	1882	-596
19	DB_7	DB_7	1882	-456
20	COM_1	COM_9	1882	-246
21	COM_2	COM_{10}	1882	-146
22	COM_3	COM_{11}	1882	-46
23	COM_4	COM_{12}	1882	54
24	COM_5	COM_{13}	1882	154
25	COM_6	COM_{14}	1882	254
26	COM_7	COM_{15}	1882	354
27	COM_8	COM_{16}	1882	454
28	SEG_1	SEG_{40}	1882	554
29	SEG_2	SEG_{39}	1882	654
—	NC4	NC4	1882	890
30	SEG_3	SEG_{38}	1750	1079
31	SEG_4	SEG_{37}	1650	1079
32	SEG_5	SEG_{36}	1550	1079
33	SEG_6	SEG_{35}	1450	1079
34	SEG_7	SEG_{34}	1350	1079
35	SEG_8	SEG_{33}	1250	1079
36	SEG_9	SEG_{32}	1150	1079
37	SEG_{10}	SEG_{31}	1050	1079
38	SEG_{11}	SEG_{30}	950	1079
39	SEG_{12}	SEG_{29}	850	1079
40	SEG_{13}	SEG_{28}	750	1079
41	SEG_{14}	SEG_{27}	650	1079
42	SEG_{15}	SEG_{26}	550	1079
43	SEG_{16}	SEG_{25}	450	1079
44	SEG_{17}	SEG_{24}	350	1079
45	SEG_{18}	SEG_{23}	250	1079
46	SEG_{19}	SEG_{22}	150	1079
47	SEG_{20}	SEG_{21}	50	1079
48	SEG_{21}	SEG_{20}	-50	1079
49	SEG_{22}	SEG_{19}	-150	1079
50	SEG_{23}	SEG_{18}	-250	1079
51	SEG_{24}	SEG_{17}	-350	1079
52	SEG_{25}	SEG_{16}	-450	1079
53	SEG_{26}	SEG_{15}	-550	1079
54	SEG_{27}	SEG_{14}	-650	1079
55	SEG_{28}	SEG_{13}	-750	1079
56	SEG_{29}	SEG_{12}	-850	1079
57	SEG_{30}	SEG_{11}	-950	1079
58	SEG_{31}	SEG_{10}	-1050	1079
59	SEG_{32}	SEG_9	-1150	1079
60	SEG_{33}	SEG_8	-1250	1079
61	SEG_{34}	SEG_7	-1350	1079
62	SEG_{35}	SEG_6	-1450	1079
63	SEG_{36}	SEG_5	-1550	1079
64	SEG_{37}	SEG_4	-1650	1079
65	SEG_{38}	SEG_3	-1750	1079
—	NC5	NC5	-1882	918
66	SEG_{39}	SEG_2	-1882	596
67	SEG_{40}	SEG_1	-1882	496
68	COM_{16}	COM_8	-1882	396
69	COM_{15}	COM_7	-1882	296
70	COM_{14}	COM_6	-1882	196
71	COM_{13}	COM_5	-1882	96
72	COM_{12}	COM_4	-1882	-4
73	COM_{11}	COM_3	-1882	-104
74	COM_{10}	COM_2	-1882	-204
75	COM_9	COM_1	-1882	-304
—	NC6	NC6	-1882	-548
—	NC7	NC7	-1882	-856

Note) NC1 to NC7 are Dummy Pad.

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■ TERMINAL DESCRIPTION

PAD NO.		SYMBOL	FUNCTION
Pin Configuration			
Mode A	Mode B		
4	4	V_{DD}	Power Source (+5V)
3	3	V_{SS}	Power Source (0V)
7,6,5	7,6,5	V_2,V_3,V_5	LCD Driving Power Source
1,2	1,2	OSC_1, OSC_2	Oscillation Frequency Adjust Terminals. Normally Open. (Oscillation C and R are incorporated, Osc Freq.=270kHz) For external clock operation, the clock should be input on OSC_1.
9	9	RS	Register selection signal input "0" : Instruction Register (Writing) Busy Flag (Reading) "1" : Data Register (Writing/Reading)
10	10	R/W	Read/Write selection signal input "0" : Write , "1" : Read
11	11	E	Read/Write activation signal input
16~19	16~19	DB_4~DB_7	3-state Data Bus(Upper) to transfer the data between MPU and NJU6460A DB_7 is also used for the Busy Flag reading
12~15	12~15	DB_0~DB_3	3-state Data Bus(Lower) to transfer the data between MPU and NJU6460A These bus are not used in the 4bit operation
20~27 75~68	75~68 20~27	COM_1~COM_8 COM_9~COM_{16}	LCD Common driving signal Terminals Common driver Location order Select as Shown in Table 4 Pin configuration mode A: MO=0 / mode B: MO=1
28~67	67~28	SEG_1~SEG_{40}	LCD Segment driving signal Terminals Segment driver Location order Select as Shown in Table 4 Pin configuration mode A: MO=0 / mode B: MO=1
8	8	$\overline{RESET}$	Reset Terminal. When the "L" level input over than 1.2ms to this terminal the system will be reset. (f_{OSC}=270kHz)

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■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1−1) Register

The NJU6460A incorporates two 8-bit registers, an Instruction Register(IR) and a Data Register(DR).

The Register(IR) stores instruction codes such as "Clear Display" and "Return Home", and address data for Display Data RAM (DD RAM) and Character Generator RAM(CG RAM). The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).

The Register (DR) is a temporary stored register, the data stored in the Register (DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.

The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM or CG RAM by internal operation.

When the address data for the DD RAM or CG RAM is written into the Register(IR), the addressed data in the DD RAM or CG RAM is transferred to the Register(DR). By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.

After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below:

Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter(DB_0～DB_6)
1	0	DR	Write (DR to DD or CG RAM)
1	1		Read (DD or CG RAM to DR)

(1−2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in table 1.

The next instruction should be written after busy flag (BF) goes to "0".

(1−3) Address Counter (AC)

The address Counter(AC) addressing the DD RAM and CG RAM.

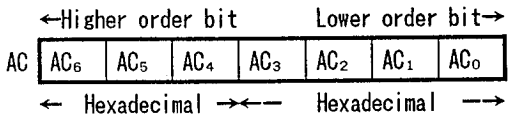
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to counter(AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.

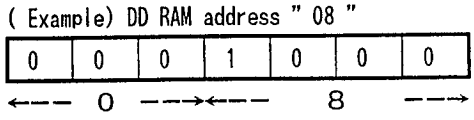
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the Counter (AC) increments (or decrements) automatically.

The address data in the Counter(AC) is output from DB_6～DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1−4) Display Data RAM (DD RAM)

The display data RAM(DD RAM) consists of 16 x 8 bits, stores up to 16-character display data represented in 8-bit code.
The DD RAM address data set in the address Counter(AC) is represented in Hexadecimal.



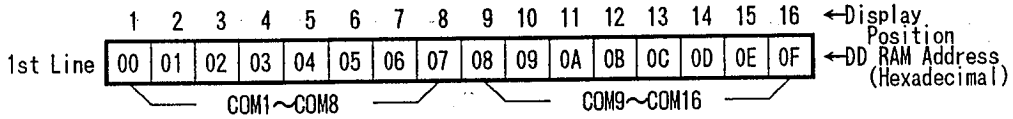


(1−4−1) 16-character 1-line Display

The NJU6460A has two kinds of addressing mode called " Addressing mode 1 " and " Addressing mode 2 " which is determined by the Function Set Instruction (A= 0 and 1).
" Addressing mode 1 " is using consecutive address of $(00)_H$ through $(0F)_H$ for front half 8-character and last half 8-character. " Addressing mode 2 " is not using consecutive address likes as $(00)_H$ through $(07)_H$ and $(40)_H$ through $(47)_H$ for front half 8-character and last half 8-character respectively.
16-character 1-line and 8 character 2-line are also determined by the Function Set Instruction (M1= 0 and 1).

<Addressing mode 1: A=0, M1=0>

• The relation between DD RAM address and display position on the LCD is shown below.



When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

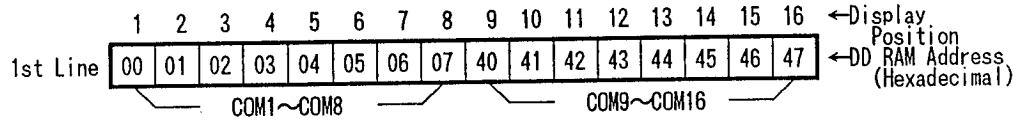
01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00

(Right Shift Display)

0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

<Addressing mode 2: A=1, M1=0>

• The relation between DD RAM address and display position on the LCD is shown below.



When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

01	02	03	04	05	06	07	40	41	42	43	44	45	46	47	00

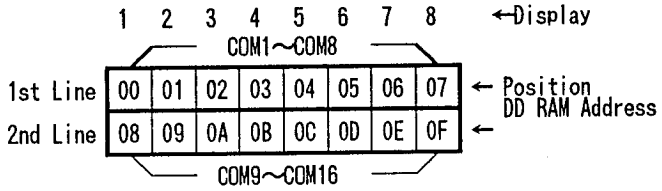
(Right Shift Display)

47	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46

(1−4−2) 8-character 2-line Display

<Addressing mode 1: A=0, M1=1>

• The relation between DD RAM address and display position on the LCD is shown below.



When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

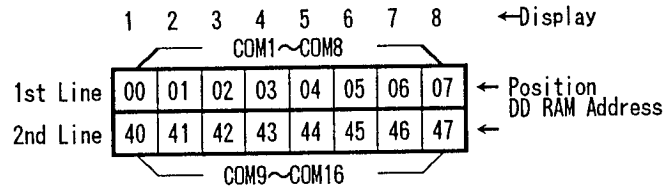
1st Line	01	02	03	04	05	06	07	08
2nd Line	09	0A	0B	0C	0D	0E	0F	00

(Right Shift Display)

1st Line	0F	00	01	02	03	04	05	06
2nd Line	07	08	09	0A	0B	0C	0D	0E

<Addressing mode 2: A=1, M1=1>

• The relation between DD RAM address and display position on the LCD is shown below.



When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

1st Line	01	02	03	04	05	06	07	40
2nd Line	41	42	43	44	45	46	47	00

(Right Shift Display)

1st Line	47	00	01	02	03	04	05	06
2nd Line	07	40	41	42	43	44	45	46

(1−5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character codes.

The storage capacity is up to 192 kinds of 5 x 7 dots character pattern. The correspondence between character code and standard character pattern of NJU6460A is shown in Table 2.

User-defined character pattern (Custom Font) are also available by mask option and the available address for Custom Font is from $(21)_H$ to $(7F)_H$ and from $(A0)_H$ to $(FF)_H$

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Table 2. CG ROM Character Pattern (ROM version -01)

Lower 4-bit (Hexadecimal) \ Upper 4-bit (Hexadecimal)	0	2	3	4	5	6	7	A	B	C	D	E	F
0	CG RAM (01)												
1	(02)												
2	(03)												
3	(04)												
4	(01)												
5	(02)												
6	(03)												
7	(04)												
8	(01)												
9	(02)												
A	(03)												
B	(04)												
C	(01)												
D	(02)												
E	(03)												
F	(04)												

Character code $(1X)_H$, $(8X)_H$, $(9X)_H$ don't exist.

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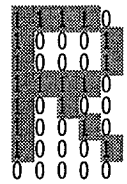
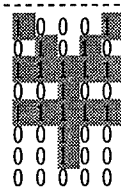
(1－6) Character Generator RAM (CG RAM)

The character generator RAM(CG RAM) can store any kinds of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 4 kinds of character in 5 X 7 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(03)_H$ should be written to the DD RAM as shown in Table 2.

Table 3. shows the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 x 7 dots).

Character Code (DD RAM Data)	CG RAM Address	Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 ←— —→ Upper bit Lower bit	4 3 ←— Upper bit	2 1 0 —→ Lower bit	4 3 2 1 0 ←— —→ Upper bit Lower bit	
0 0 0 0 * * 0 0	0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		Character Pattern Example(1) ←Cursor Position
0 0 0 0 * * 0 1	0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		Character Pattern Example(2) ←Cursor Position
		0 0 0 0 0 1		
0 0 0 0 * * 1 1	1 1	1 0 0 1 0 1 1 1 0 1 1 1		* : Don't Care

Notes : 1. Character code bits 0 to 1 correspond to the CG RAM address 3 and 4 (2 bits : 4 patterns).

2. CG RAM address 0, 1 and 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above. The bits 5 to 7 of the CG RAM do not exist.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and addressed by character code bits 0 and 1. Therefore, the address $(00)_H$, $(04)_H$, $(08)_H$ and $(0C)_H$, select the same character pattern as shown in Table 2 and Table 3.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1−7) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuits operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1−8) LCD Driver

LCD driver consist of 16-common driver and 40-segment driver.

The 40 bits of character pattern data are shifted in the shift-register and latched when the 40 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1−9) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(04)_H$, a cursor position is shown as follows:

AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
0	0	0	0	1	0	0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address (Hexadecimal)

↑ Cursor position

(Note) The cursor or blinks appear when the address counter(AC) selects the CG RAM.
But the displayed the cursor and blink are meaningless.
If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

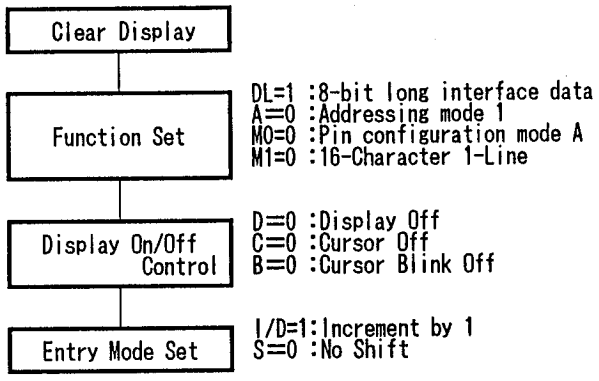
(2) Power on Initialization by internal circuits

(2−1) Initialization By internal Reset circuits

The NJU6460A is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed.

During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 4.5V.

Initialization flow is shown below:



NOTE
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operate and initialization will not be performed.
In this case the initialization by MPU software is required.

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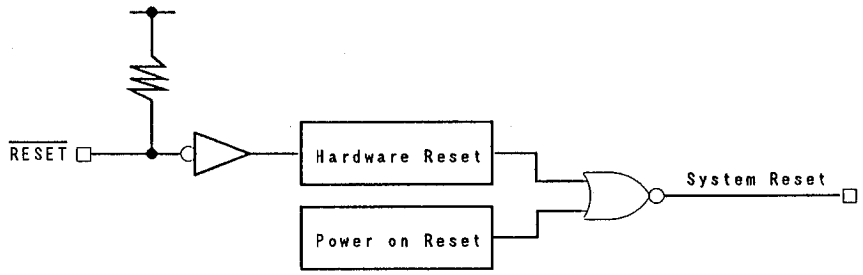
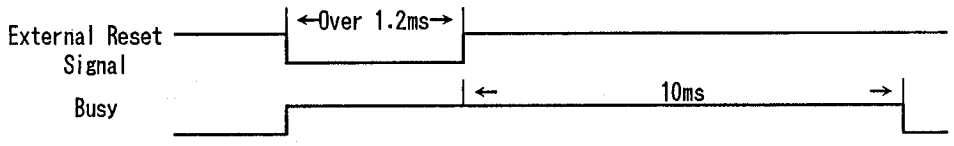
(2-2) Initialization By Hardware

The NJU6460A incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over than 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 10ms after $\overline{\text{RESET}}$ terminal goes to "H".

・Reset Circuit



・Timing Chart



(3) Instructions

The NJU6460A incorporates two registers, an Instruction Register (IR) and a Data Register (DR). These two registers store control information temporarily to allow interface between NJU6460A and MPU or peripheral ICs operating different cycles. The operation of NJU6460A is determined by this control signal from MPU.

The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).

Table 4. shows each instruction and its operating time.

Note) The execution time mentioned in Table 4. based on fcp or fosc=270kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	EXEC TIME
Maker Test	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	—
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged	37us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift	37us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	37us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	56us
Function Set	0	0	0	0	1	DL	A	*	M1	M0	Sets interface data length(DL), Display address mode(A). DL=1 : 8 bits, DL=0 : 4 bits A=0 : Addressing mode 1 A=1 : Addressing mode 2 M1=0: 16-Character 1-Line M1=1: 8-Character 2-Line M0=0: Pin configuration mode A M0=1: Pin configuration mode B	37us
Set CG RAM Address	0	0	0	1	*	←	A_{CG}			→	Sets CG RAM address. After this instruction, the data is transferred on CG RAM.	37us
Set DD RAM Address	0	0	1	←		A_{DD}				→	Sets DD RAM address. After this instruction, the data is transferred on DD RAM.	37us
Read Busy Flag & Address	0	1	BF	←		AC_{DD}				→	Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
	0	1	BF	*	*	←	AC_{CG}			→		
Write Data to CG & DD RAM	1	0	*	*	*	←Write Data(CG)→					Writes data into CG or DD RAMs.	37us
	1	0	←	Write Data(DD)						→		
Read Data from CG or DD RAM	1	1	*	*	*	←Read Data(CG) →					Reads data from CG or DD RAMs.	56us
	1	1	←	Read Data(DD)						→		
Explanation of Abbreviation	DD RAM : Display data RAM , CG RAM : Character generator RAM A_{CG} : CG RAM address, A_{DD} : DD RAM address, Corresponds to cursor address AC : Address counter used for both of DD and CG RAMs											

*=Don't Care

(3−1) Description of each instructions

(a) Maker Test

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker). Therefore, please avoid all "0" input or no meaning Enable signal input at data "0". (Especially please pay attention the output condition of Enable signal when the power turns on.)

All "0" code in 8-bit length is usable for NOP (Not OPerating instruction).

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0. When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set increment. If the cursor or blink are displayed, they are returned to the left end of the LCD.

The S of entry mode does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	*

* = Don't care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD, if the cursor or blink are on the display.

The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

5

(e) Display On/Off Control

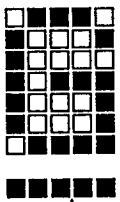
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

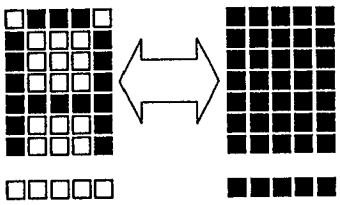
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 455.2ms at or f_{osc}=270kHz. The blink is displayed alternatively with all on (it means all black) and characters display. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* = Don't care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display.

The contents of address counter(AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

5

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	DL	A	*	M1	M0

* = Don't care

Function set instruction which sets the interface data length, the addressing Mode for the DD RAM, 1-line or 2-line display, and Pin configuration mode, is executed when the code "1" is written into DB_5 and the codes of (DL), (A), (M1) and (M0) are written into DB_4(DL), DB_3(A), DB_1(M1) and DB_0(M0), as shown below (character font is fixed 5 X 7 dots).

(DL) sets the interface data length, (A) sets the DD RAM address mode $(00)_H$ through $(0F)_H$ or $(00)_H$ through $(07)_H$ and $(40)_H$ through $(47)_H$, (M1) sets the number of display line either the 1-line or 2-line display, and (M0) sets the Pin configuration for Common and Segment drivers as shown in coordinates.

NOTE

This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length to 8 bits (DB_7 to DB_0)
0	Set the interface data length to 4 bits (DB_7 to DB_4) The data must be sent or received twice.

A	Function
0	Set the Addressing Mode 1 for the DD RAM
1	Set the Addressing Mode 2 for the DD RAM

M1	Function
0	Set the 16-Character 1-Line Display
1	Set the 8-Character 2-Line Display

M0	Function	
0	Set the Pin configuration mode A for Common and Segment Driver	Refer to coordinates
1	Set the Pin configuration mode B for Common and Segment Driver	

(h) Set CG RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	1	*	A	A	A	A	A	* Don't Care
						←Higher order bit			Lower order bit →		

Set CG RAM address instruction is executed when the code "1" is written into DB_6 and the address is written into DB_4 to DB_0 as shown above.

The address data mentioned by binary code "AAAAA" is written into the address counter (AC) together with the CG RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the CG RAM..

(i) Set DD RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A
				←Higher order bit					Lower order bit→	

Set DD RAM address instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data mentioned by binary code "AAAAAAA" is written into the address counter (AC) together with the DD RAM addressing condition. After this instruction, the data writing/reading is performed into/from the DD RAM.

Note : When the "Addressing mode 1" selection, $(00)_H$ through $(0F)_H$ are available but $(10)_H$ through $(7F)_H$ are ignored. When the "Addressing mode 2" selection, $(00)_H$ through $(07)_H$ and $(40)_H$ through $(47)_H$ are available but $(08)_H$ through $(3F)_H$ and $(48)_H$ through $(7F)_H$ are ignored.

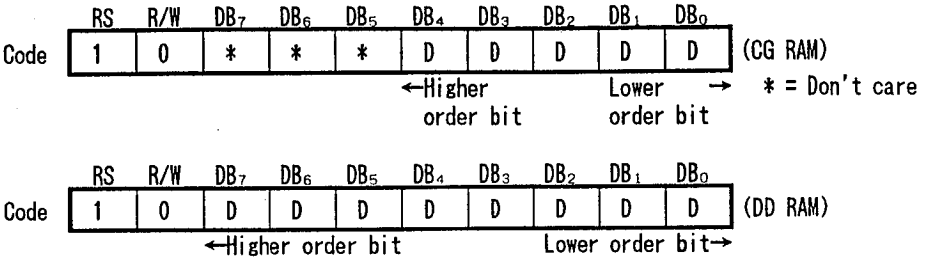
(j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A
				←Higher order bit					Lower order bit→	

This instruction reads out the internal status of the NJU6460A. When this instruction is executed, the busy flag(BF) which indicate internal operation is read out from DB_7 and the address of CG RAM or DD RAM is read out from DB_6 to DB_0 (the address for CG RAM or DD RAM is determined by the previous instruction).

(BF)=1 indicates that internal operation is in progress. The next instruction is inhibited when (BF)=1. Check the (BF) status before the next write operation.

(k) Write Data to CG or DD RAM

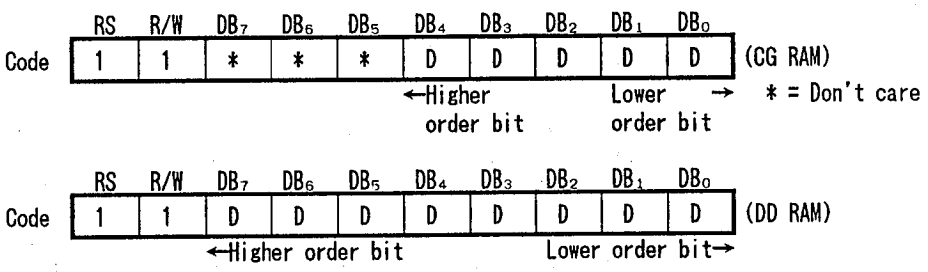


Write Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 5-bit data "DDDDD" are written into the CG RAM, and the binary 8-bit data "DDDDDDDD" are written into the DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

After this instruction execution, the address increment(+1) or decrement(-1) performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(l) Read Data from CG or DD RAM



Read Data from CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 5 bit data "DDDDD" are read out from CG RAM, and the binary 8 bit data "DDDDDDDD" are read out from DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand(only DD RAM reading).

The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

Note: The address counter(AC) is automatically incremented or decremented by 1 after write instructions to either of the CG RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

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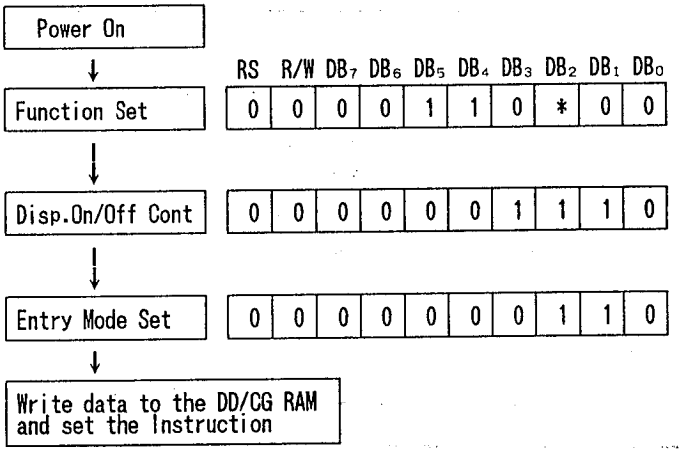
(3−2) Initialization using the internal reset circuits

(a) 16-character 1-line in 8-bit operation Addressing Mode 1 (Using internal reset circuits).

At the 16-character 1-line display, the Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.
Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.



Initialized.
No display appears.

Set the 8-bit operation, 16-Character 1-line display, Pin configuration mode A, Addressing Mode 1.

Turns on display and cursor. Entire display is in space mode by the initialization.

Example for set address increment and cursor right shift when the data write to the DD or CG RAM.

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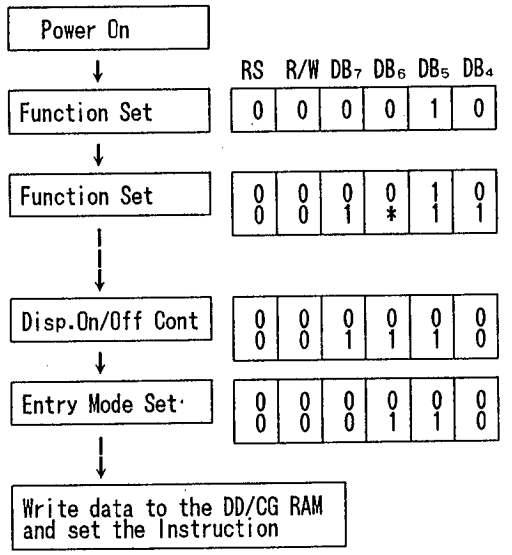
(b) 8-character 2-line in 4-bit operation Addressing Mode 2 (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.
When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full. 8-character 2-line in 4-bit operation is shown as follows:



Initialized.
No display appears.

Set the 4-bit operation.
This step is executed in 8-bit mode set by the initialization.

Set the 4-bit operation / 2-line 8-Character display / Pin configuration mode B / Addressing Mode 2.
The 4-bitoperation starts from this step.

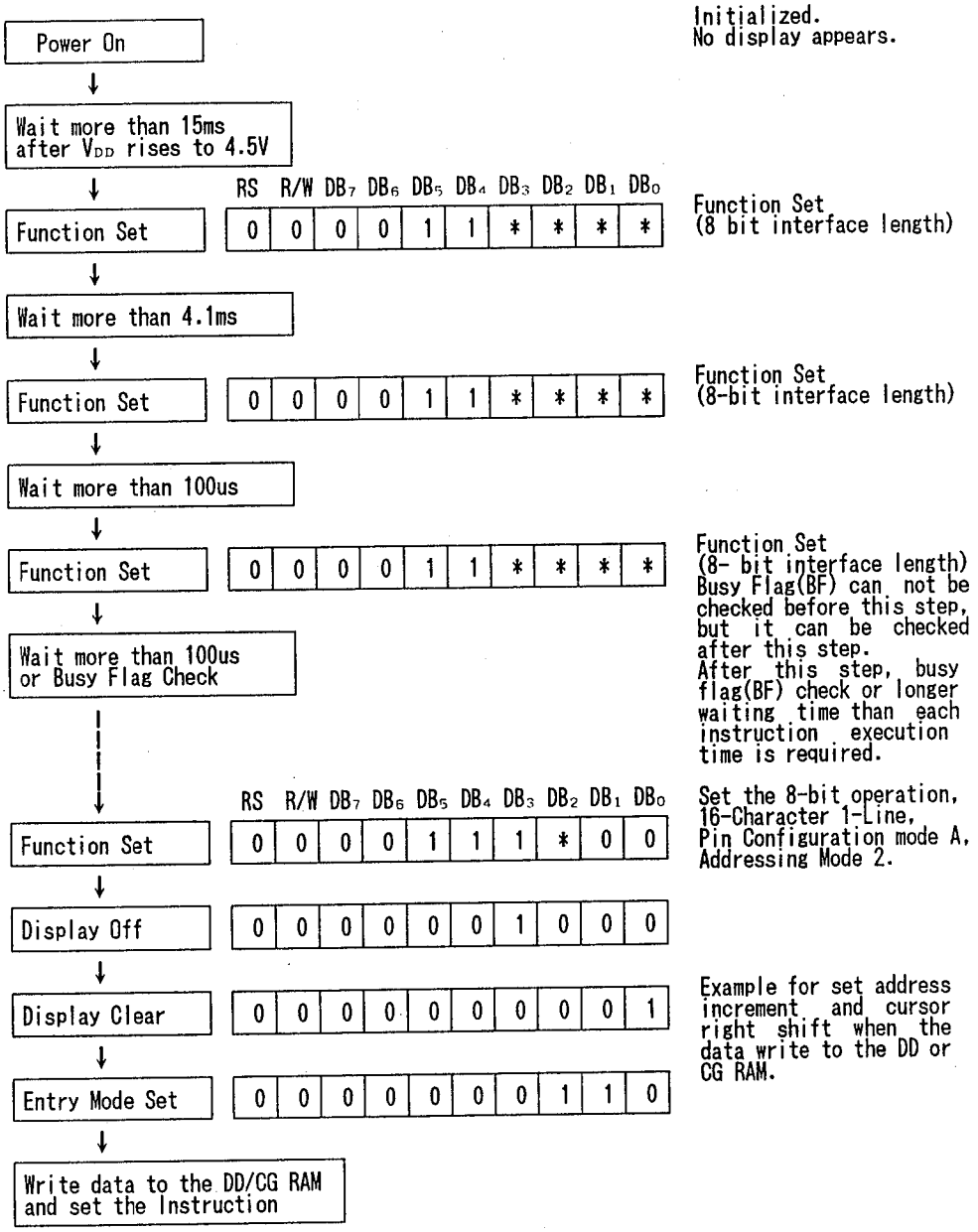
Turn on display and cursor.
Entire display is in space mode by the initialization.

Example for set address increment and cursor right shift when the data write to the DD or CG RAM.

(3−3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6460A must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface



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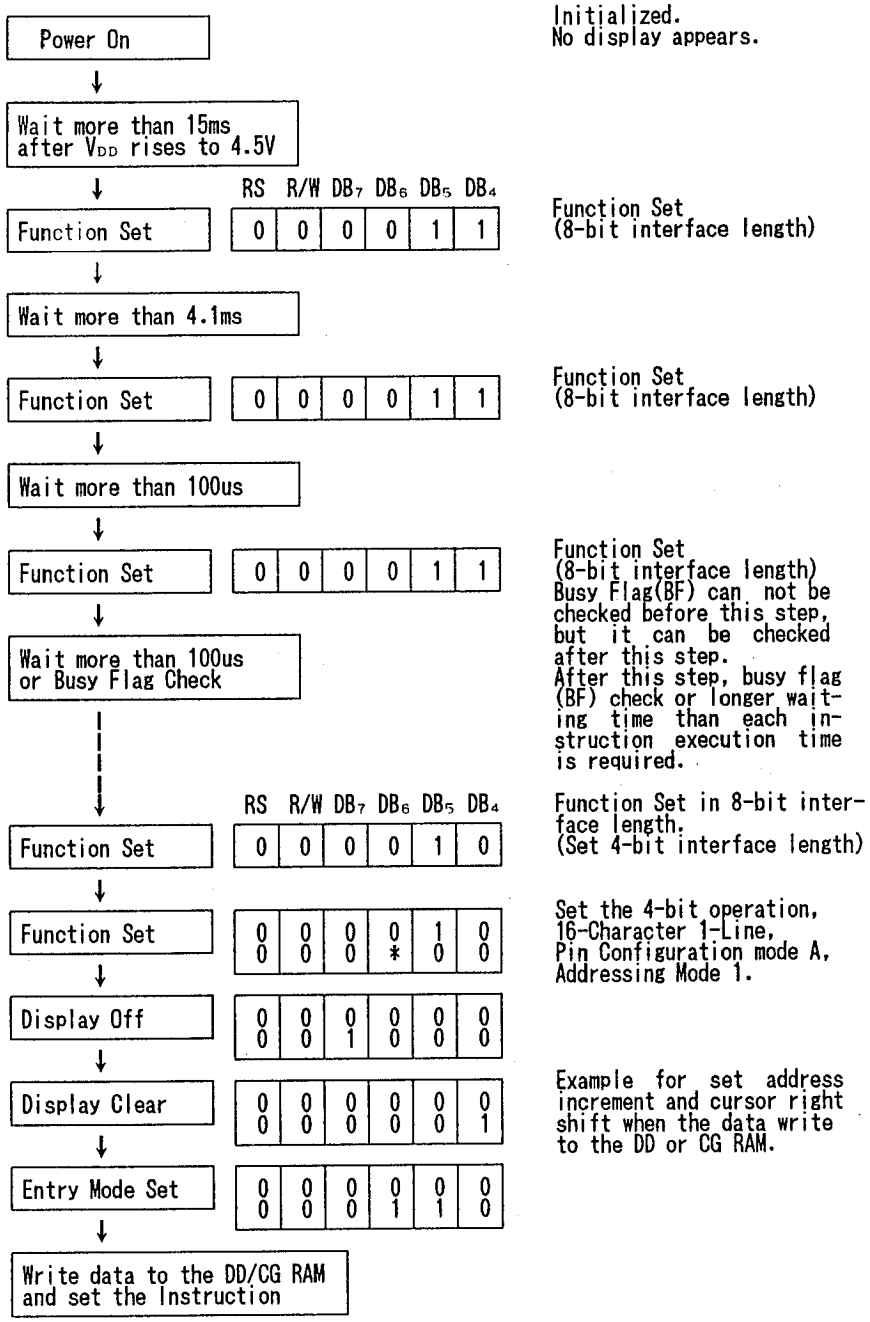
(b) Initialization by Instruction in 4-bit interface



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(4) LCD DISPLAY

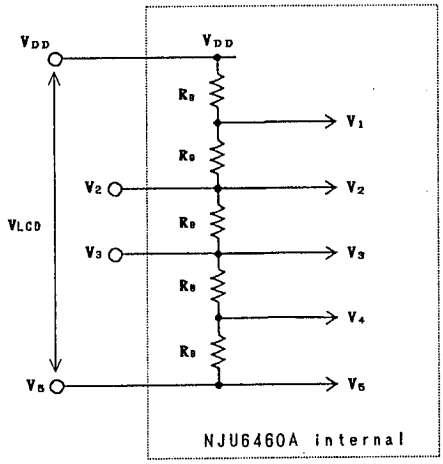
(4−1) Power Supply for LCD Driving

NJU6460A incorporates bleeder resistance to generate the LCD display driving waveform. The bleeder resistance is set 1/5 bias suitable for 1/18 duty ratio and 1.5kΩ per resistance.

Furthermore, the bias level can be changed by connecting external resistance between the V_2, V_3 terminals, if needed.

LCD Driving Voltage vs Duty Ratio

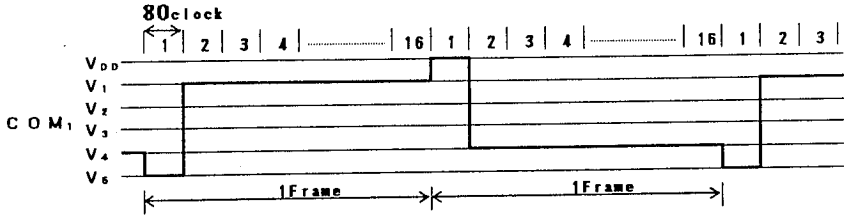
Power Supply	Duty Ratio	1/16
	Bias	1/5
	V_2	$V_{DD}-2/5V_{LCD}$
	V_3	$V_{DD}-3/5V_{LCD}$
	V_5	$V_{DD}-V_{LCD}$



(4−2) Relation between oscillation frequency and LCD frame frequency.

LCD frame frequency example mentioned below is based on 270kHz oscillation.
The clock for the LCD Driving is using 270/2 kHz (1 clock=7.4us).

1/16 duty



1 frame = 7.4(us) x 80 x 16 = 9,472(us) = 9.472(ms)
Frame frequency = 1/9.472(ms) = 105.6(Hz)

(5) Interface with MPU

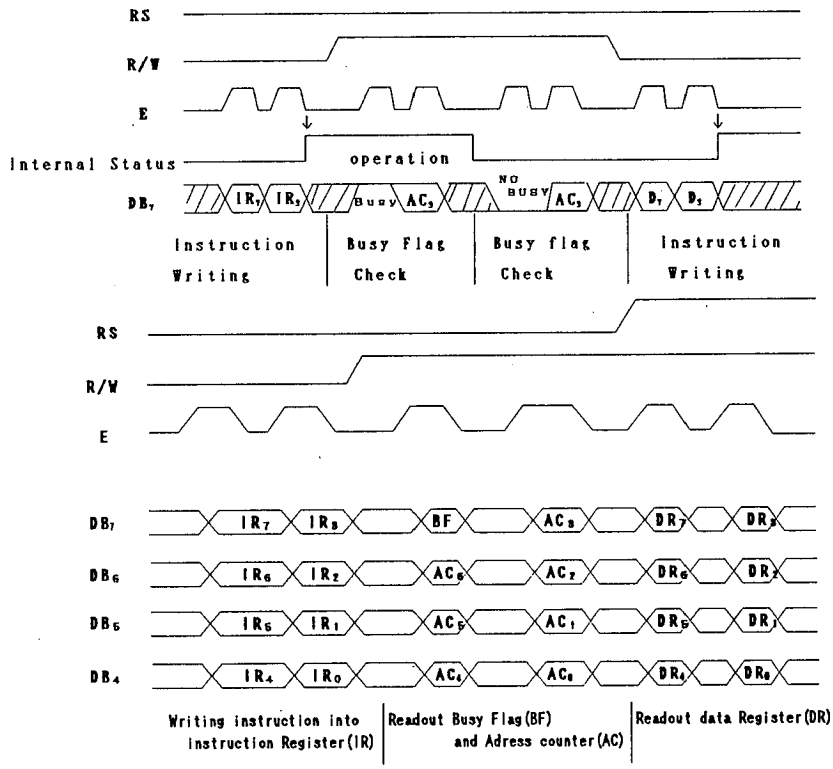
NJU6460A can be interfaced with both of 4/8 bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

(5−1) 4-bit MPU interface

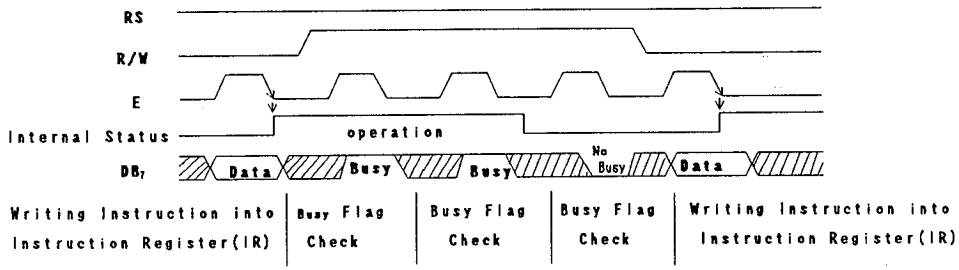
When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).

The busy flag check must be executed after two-time 4-bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.



(5−2) 8-bit MPU interface



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	- 0.3 ～ + 7.0	V
Input Voltage	V_{IN}	- 0.3 ～ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ～ + 80	℃
Storage Temperature	Tstg	- 55 ～ + 125	℃

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 2) All voltage values are specified as V_{SS} = 0 V
Note 3) The relation : $V_{DD}>V_5 \geqq V_{5OUT}$, V_{SS}=0V must be maintained.
Turn on V_{DD} first then turn on V5 must be required.
Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the LSI.

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20 ～ +75℃)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage		V_{DD}		4.5	5.0	5.5	V	
Input Voltage	1	V_{IH1}	All Input/Output Terminals except OSC and E Terminals	2.3		V_{DD}	V	5
		V_{IL1}				0.8		
	2	V_{IH2}	Only OSC Terminal	V_{DD}-1		V_{DD}		
		V_{IL2}				1.0		
	3	V_{IH3}	Only E Terminal	0.8V_{DD}		V_{DD}		
		V_{IL3}				0.2V_{DD}		
Output Voltage		V_{OH}	-I_{OH}=0.205mA	2.4			V	6
		V_{OL}	I_{OL}=1.6mA			0.4		
Driver On-resist.(COM)		R_{COM}	I_D=±50uA(All com.term.)			20	kΩ	9
Driver On-resist.(SEG)		R_{SEG}	I_D=±50uA(All seg.term.)			30		
Input Leakage Current		I_{LI}	V_{IN}=0 ～ V_{DD}	- 1		1	uA	7
Pull-up Resist Current		-I_P	V_{DD}=5V	50	125	250		
Operating Current		I_{DD}	CR Oscillation V_{DD}=5V, f_{OSC}=270kHz		1.0	1.8	mA	8
LCD Driving Voltage		V_2	Ta=25℃, V_{DD}=5V, V_5=0V Measurement Terminal is SEG.	2.7	3.0	3.3	V	
		V_3		1.7	2.0	2.3		
Bleeder Resistance		R_B	V_{DD}-V_5=5V Ta=25℃	3.7	7.5	11.3	kΩ	
Oscillation Frequency		fosc		190	270	350	kHz	
LCD Driving Voltage		V_{LCD}	V_5 Terminal, V_{DD}=5V	V_{DD}-3		V_{DD}-5	V	10

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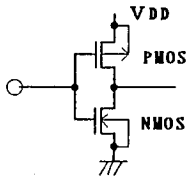
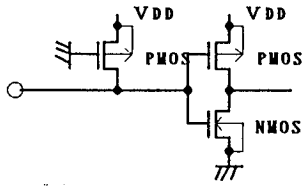
Note 5) Input/Output structure except LCD driver are shown below:

Input Terminal Structure

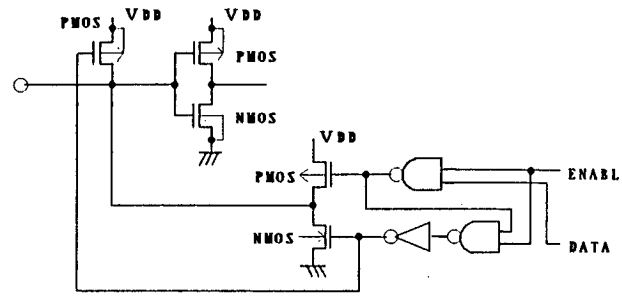


E Terminal



RS, R/W and $\overline{\text{RESET}}$ Terminals

Input/Output Terminal Structure



DB_0 to DB_7 Terminals

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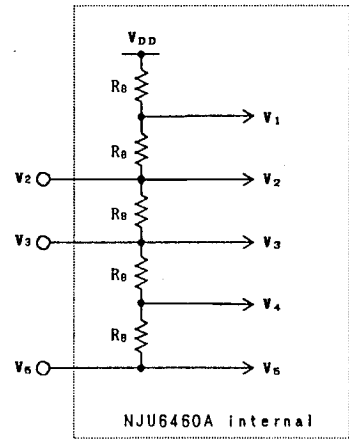
Note 6) Apply to the Input/Output Terminal.
Note 7) Except pull-up resistance current and output driver current.
Note 8) Except Input/output current but including the current flow on bleeder resistance.
Note 9) R_{COM} and R_{SEG} are the resistance values between power supply terminals(V_{DD}, V_2, V_3, V_5) and each common terminal (COM_1 to COM_{16}), and supply voltage (V_{DD}, V_2, V_3, V_5) and each segment terminal(SEG_1 to SEG_{40}) respectively, and measured when the current Id is flown on every common and segment terminals at a same time.
Note 10) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage(V_{DD}, V_5) at no load condition.

・ Bleeder resistance



- **Bus timing characteristics (V_{DD} = 5.0V±10%, VSS = 0V, Ta = -20 ~ +75℃)**

Write operation sequence (Write from MPU to NJU6460A)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	500		fig.1	ns
Enable Pulse Width	"High" level	PW_{EH}	220			
	"Low" level	PW_{EL}	280			
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W-E	t_{AS}	40			
Address Hold Time		t_{AH}	10			
Data Set up Time		t_{DSW}	60			
Data Hold Time		t_H	10			

Timing Characteristics (Write operation)

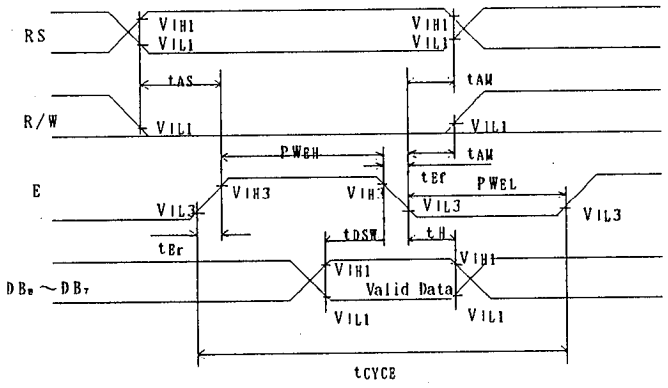


fig. 1 The timing characteristics of the bus write operating sequence. (Write from MPU to NJU6460A)

Read operation sequence (Read from NJU6460A to MPU)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	500		fig.2	ns
Enable Pulse Width	"High" level	PW_{EH}	220			
	"Low" level	PW_{EL}	280			
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W-E	t_{AS}	40			
Address Hold Time		t_{AH}	10			
Data Delay Time		t_{DDR}		240		
Data Hold Time		t_{DHR}	20			

DB0~DB7 Load Condition : C_L=100pF

Timing Characteristics (Read operation)

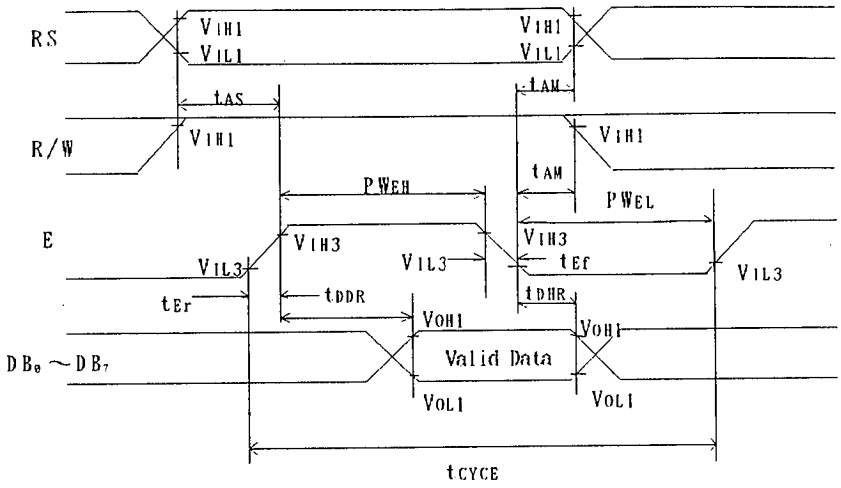


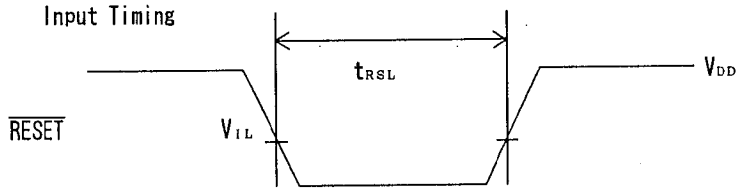
fig. 2 The timing characteristics of the bus read operating sequence.
(Read from NJU6460A to MPU)

5

• The Input Condition when using the Hardware Reset Circuit

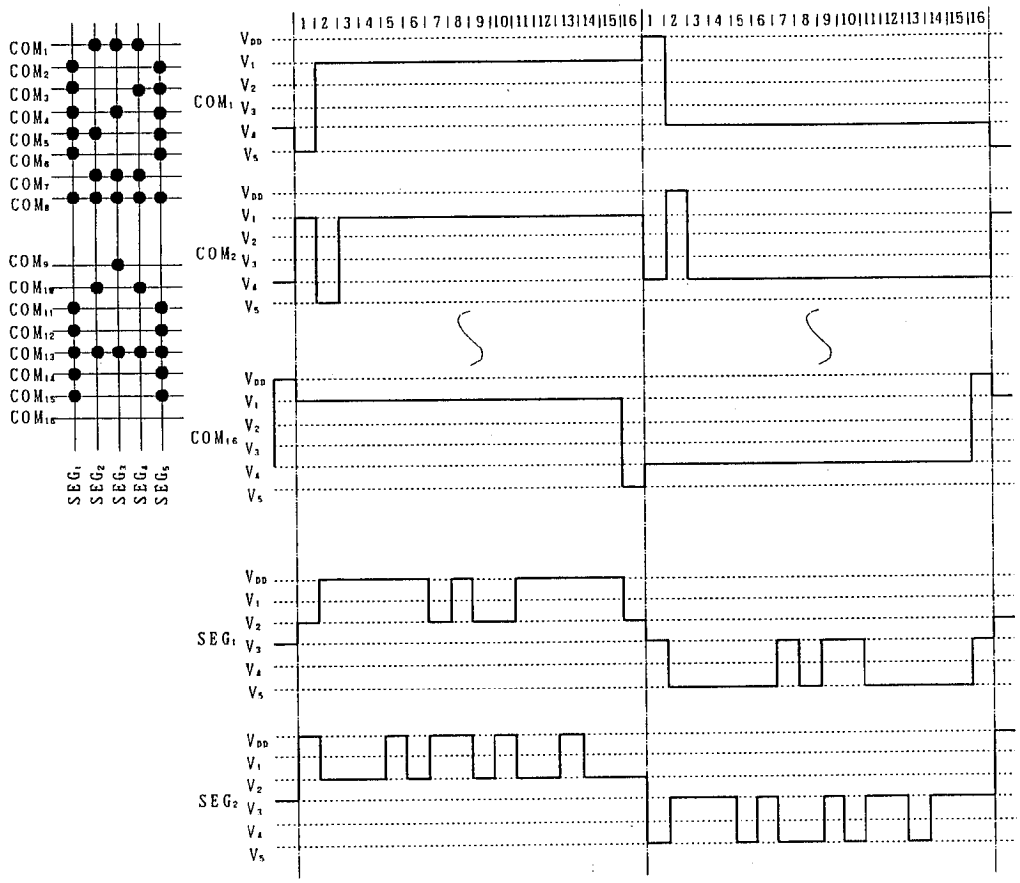
PARAMETER	SYMBOL	MIN	MAX	CONDITION	UNIT
Reset Input "L" Level Width	t_{RSL}	1.2		f_{OSC}=80kHz	ms

Input Timing



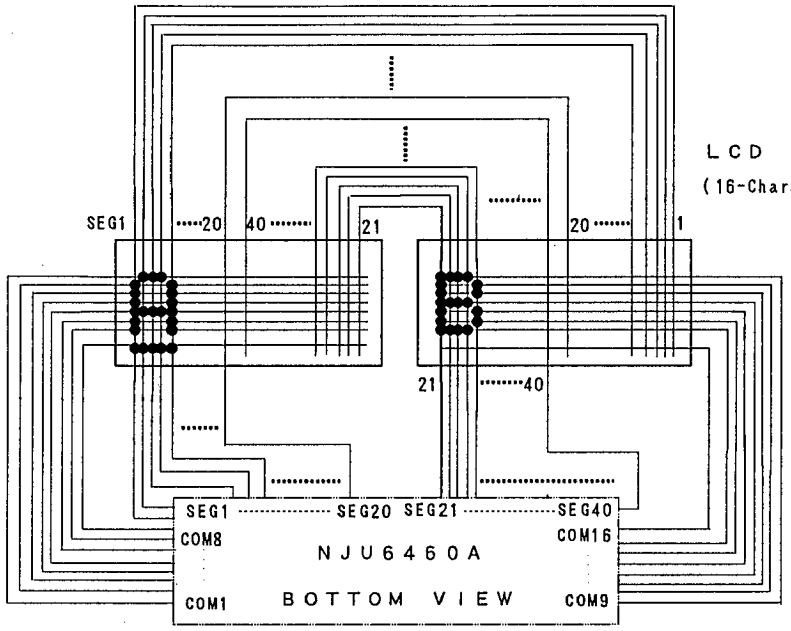
■ LCD DRIVING WAVEFORM

1/16 Duty Driving

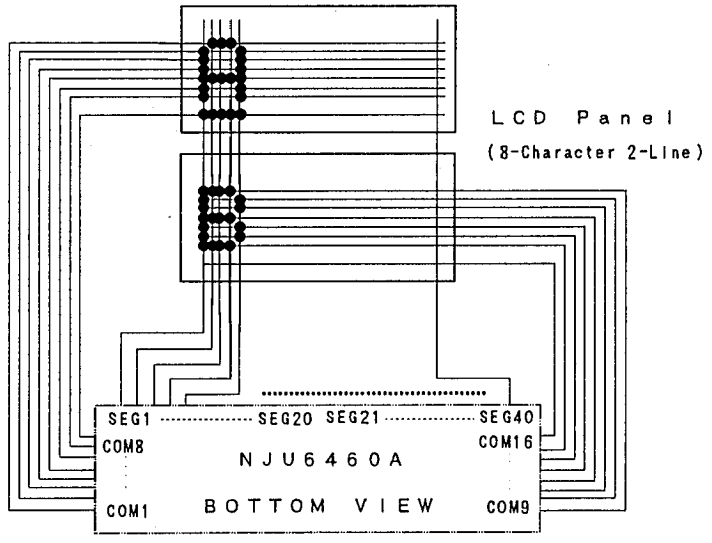


■ APPLICATION CIRCUITS

(1) LCD display interface Pin configuration mode A (BOTTOM VIEW)

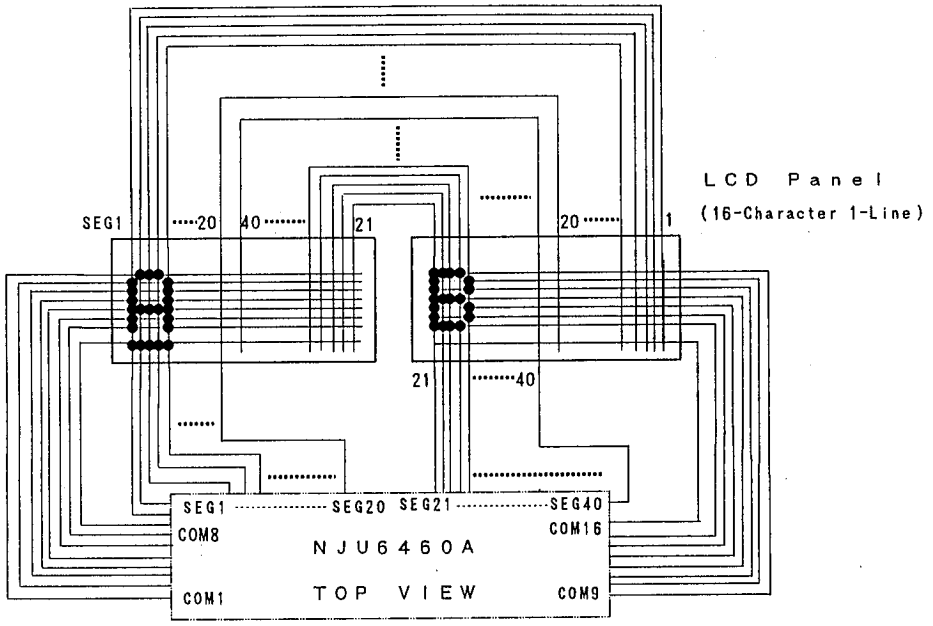


Mode A, 16-Character 1-Line display example
(M0 = 0, M1 = 0)

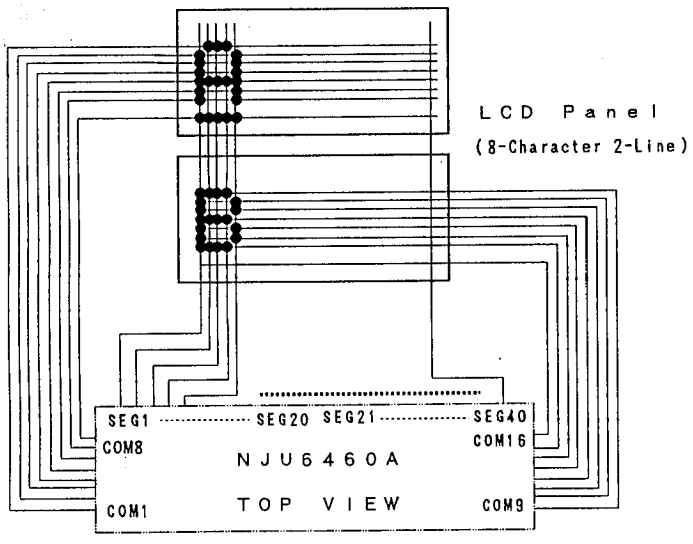


Mode A, 8-Character 2-Line display example
(M0 = 0, M1 = 1)

(2) LCD display interface Pin configuration mode B (TOP VIEW)



Mode B, 16-Character 1-Line display example
(M0 = 1、M1 = 0)



Mode B, 8-Character 2-Line display example
(M0 = 1、M1 = 1)

MEMO