Digital Audio Delay

■ General Description

The NJU26903 is a digital audio delay. The NJU26903 provides delay-time adjustment function and digital audio interface.

■ Package

NJU26903

■ FEATURES

- Tow delay systems, 2-Channel Audio Delay (24 bits data width) per system.
  Delay Time 85msec at fs = 48kHz (128msec at fs = 32kHz , 43msec at fs = 96kHz)
- To make long delay time, the NJU26903 can be connected serially.
  The maximum delay time is 170msec at fs = 48kHz (256msec at fs = 32kHz)
- Non-audio-signal data can be delayed by the NJU26903.

■ Hardware Specification

- Digital Audio Interface : 2 Input ports, 2 Output ports
- Digital Audio Format : I^2S / LJ / RJ BCK : 64fs / 32fs, 24bits , (32fs : 16bits only)
  Slave Mode
- Audio Bit Clock (BCK) Frequency : 13MHz Max (approximate fs=200kHz)
- Package : PCSP20-SGH4 (Pb-Free)
- Input terminal : 3.3V Input tolerant
- Power Supply : 2.5V

■ Function Block Diagram

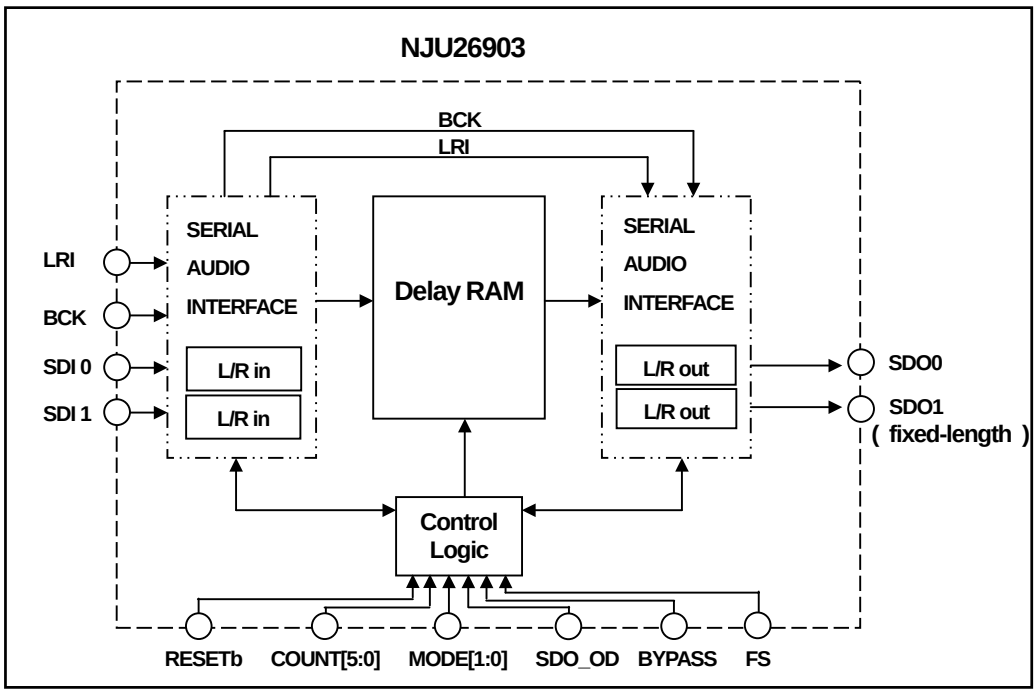


Fig.1 NJU26903 Hardware Block Diagram

■ Pin Configuration

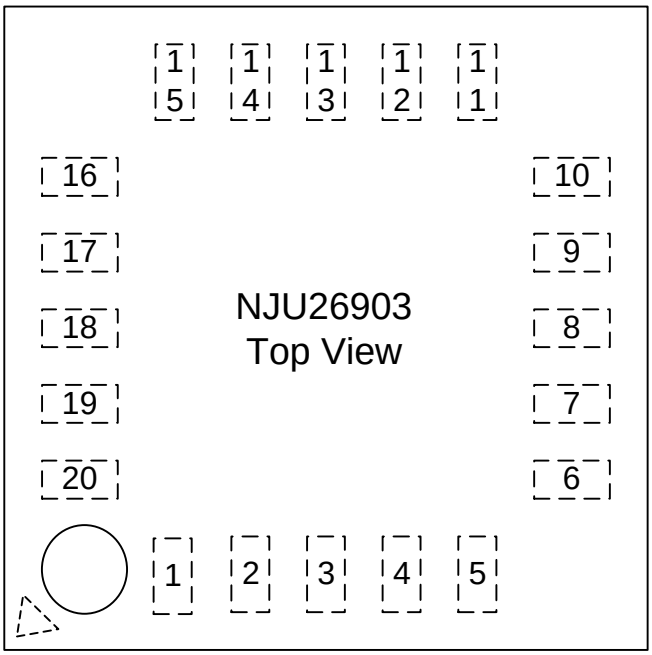


Fig.2 Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Description
1	RESETb	Ipu	Reset (Active low)
2	SDI0	I	Audio Data Input
3	SDI1	I	Audio Data Input
4	LRI	I	LR Clock Input
5	COUNT[2]	Ipu	Delay Time Control 2
6	COUNT[3]	Ipu	Delay Time Control 3
7	BCKI	I	Bit Clock Input
8	COUNT[4]	Ipu	Delay Time Control 4
9	COUNT[5]	Ipu	Delay Time Control 5
10	VSS	-	GND
11	MODE[0]	Ipd	Digital Audio Interface Format Select
12	COUNT[0]	Ipu	Delay Time Control 0
13	MODE[1]	Ipu	Digital Audio Interface Format Select
14	COUNT[1]	Ipu	Delay Time Control 1
15	SDO_OD	Ipd	SDO0/1 pin Open Drain Select
16	BYPASS	Ipd	SDO0/1 pin BYPASS Control
17	FS	Ipu	BCK fs Select
18	SDO0	O	Audio Data Output (CMOS Output / Open Drain Output)
19	SDO1	O	Audio Data Output (CMOS Output / Open Drain Output)
20	VDD	-	Power Supply 2.5V

* I : Input
Ipu: Input (internal pull-up)
Ipd: Input (internal pull-down)
O : Output

■ Absolute Maximum Ratings

Table2 Absolute Maximum Ratings **(V_{SS}=0V, Ta=25°C)**

Parameter	Symbol	Rating	Units
Power Supply Voltage	V_{DD}	-0.3 to +3.05	V
Input Pin Voltage	V_{TMI}	-0.3 to +3.6 ($V_{DD} \geq$ 2.25V) -0.3 to +3.05 (V_{DD} < 2.25V)	V
SDO Pin Voltage * (CMOS Output)	V_{TMO}	-0.3 to +3.05	V
SDO Pin Voltage * (Open Drain Output)	V_{TMOD}	-0.3 to +3.6 ($V_{DD} \geq$ 2.25V) -0.3 to +3.05 (V_{DD} < 2.25V)	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{OPR}	-40 to +85	°C
Storage Temperature	T_{STR}	-40 to +125	°C

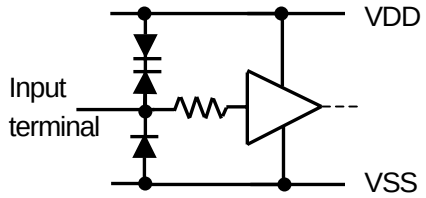
* This specification is applied to V_{TMO} at the SDO pin in case of SDO_OD= “Low”.

■ Electric Characteristics

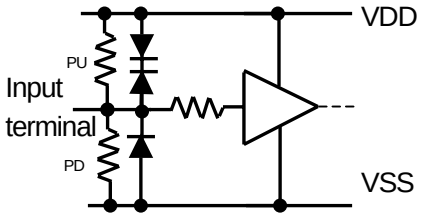
Table 3 Electric Characteristics **(V_{DD}=2.5V, V_{SS}=0V, Ta=25°C)**

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating V_{DD} Voltage	V_{DD}		2.25	2.5	2.75	V
Operating Current	I_{DD}	BCKI:13MHz SDO:C_L=25pF	-	2.0	-	mA
High Level Input Voltage	V_{IH}		2.0	-	3.3	V
Low Level Input Voltage	V_{IL}		0	-	0.5	V
High Level Output Voltage (SDO_OD="Low")	V_{OH}	I_{OH}= -2mA I_{OH}= -100μA	V_{DD}-0.4 V_{DD}-0.1	- -	V_{DD} V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL}= 2mA I_{OL}= 100μA	0 0	- -	0.4 0.1	V
Open Drain Output Current (SDO_OD="High")	I_{OD}	V_{IN}= 3.3V	-15	-	15	μA
Input Current	I_{IN}	V_{IN}= V_{SS} to 3.3V	-15	-	15	μA
Input Current (Internal Pull-up Pin)	$I_{IN(PU)}$	V_{IN}= V_{SS} to 3.3V	-200	-	15	μA
Input Current (Internal Pull-down Pin)	$I_{IN(PD)}$	V_{IN}= V_{SS} to 3.3V	-15	-	400	μA
Input Capacitance	C_{IN}		-	15	-	pF
Input Rise/Fall transition Time	t_r / t_f		-	-	100	ns

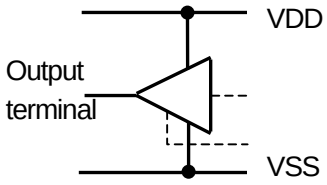
■ Equivalent Circuit



Input Pin
(SDI0,SDI1, LRI, BCKI)



Input Pin
(Internal Pull-up resistance :
RESETb, MODE[1], FS,
COUNT[5], COUNT[4], COUNT[3],
COUNT[2], COUNT[1], COUNT[0],
Internal Pull-down resistance :
MODE[0], SDO_OD, BYPASS)



Output Pin
(SDO0,SDO1)

Fig. 3 I/O Equivalent Circuits

■ Serial Audio Timing

Table 4 Serial Audio Input Timing Parameters **(V_{DD}=2.5V, V_{SS}=0V, Ta=25°C)**

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
BCKI Frequency	f_{BCK}		-	-	13	MHz
BCKI Period Low Pulse Width High Pulse Width	 t_{SIL} t_{SIH}		 35 35	-	-	ns
BCKI to LRI Time	T_{SLI}		15	-	-	ns
LRI to BCKI Time	t_{LSI}		15	-	-	ns
Data Setup Time	t_{DS}		15	-	-	ns
Data Hold Time	t_{DH}		15	-	-	ns
Data Output Delay	t_{DOD}	SDO : C_L=25pF SDO_OD="Low"		-	15	ns

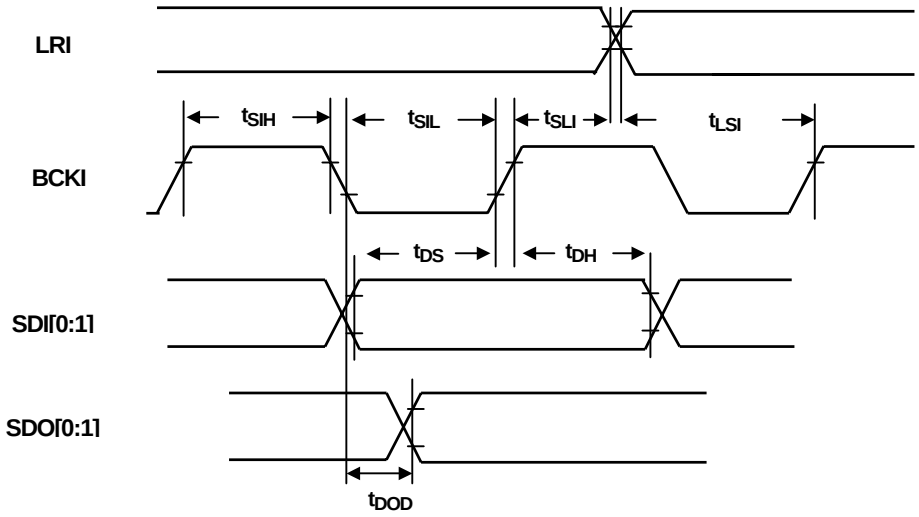


Fig.4 Serial Audio Input / Output Timing

■ Serial Audio Data Transmitting Diagram

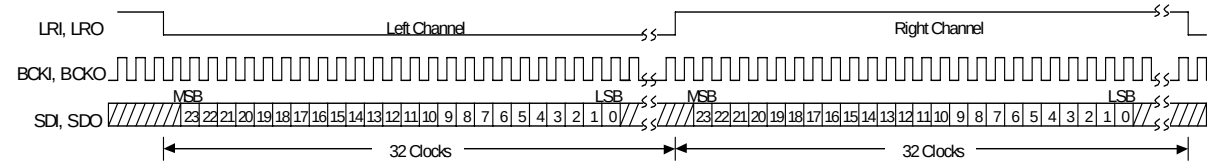


Fig.5-1 I²S Data Format 64fs, 24bit Data

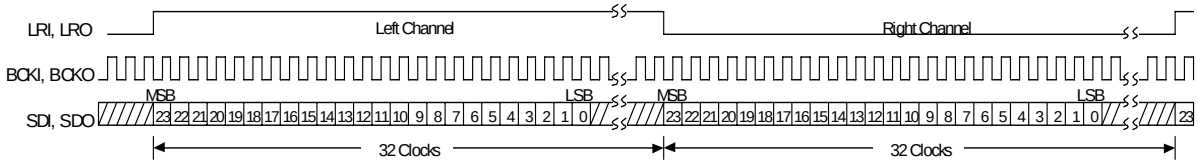


Fig.5-2 Left-Justified Data Format 64fs, 24bit Data

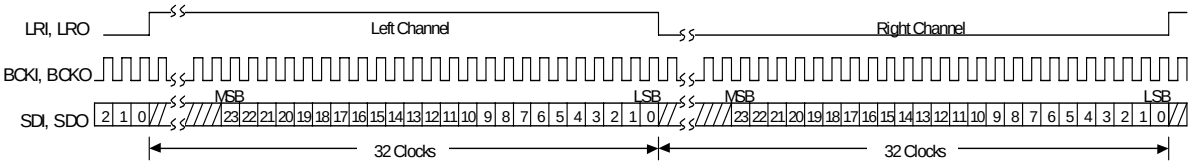


Fig.5-3 Right-Justified Data Format 64fs, 24bit Data

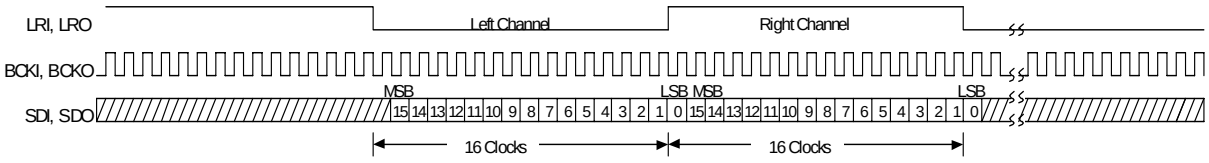


Fig.5-4 I²S Data Format 32fs, 16bit Data

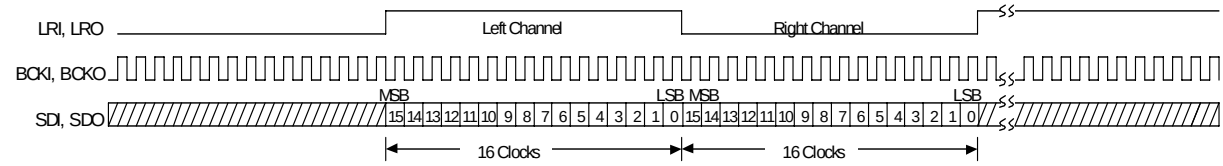


Fig.5-5 Left-Justified Data Format 32fs, 16bit Data

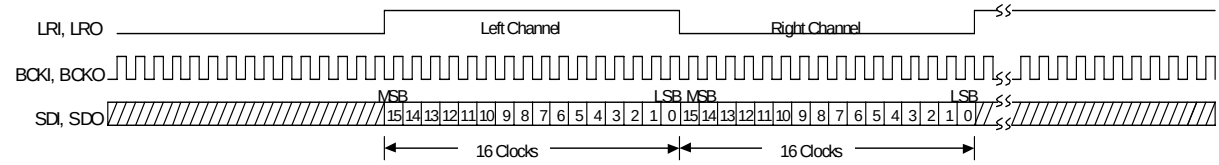


Fig.5-6 Right-Justified Data Format 32fs, 16bit Data

■ Function Description

- SDI[0:1] (#2,3) are the serial audio input pins. The input audio signal should be connected to these pins.
- LRI(#4) is the LR clock input pin. The LR clock frequency is the as same as of the input audio signal.
  In case of I^2S format, if LRI="Low" SDI and SDO data are left channel data,
  if LRI="High" SDI and SDO data are right channel data.
- BCKI(#7) is the bit clock input pin. This BCKI clock frequency is 32 times (32fs) or 64 times (64fs) of the input audio signal frequency. The bit precision is 16 bits in 32fs mode, and 24 bits in 64fs mode.
- MODE [1:0](#13,#11) and FS(#17) pins are used to select serial audio format.
  Refer to Table5 "Mode pin, FS pin Setup" for details.
- SDO[0:1] (#18,19) are the serial audio output pins. The delayed audio data come out through these pins.
- SDO is as the 2.5V CMOS output pin in case of SDO_OD(#15)= "Low". SDO is as the open drain output pin in case of SDO_OD= "High", SDO[0:1] (#18,19) can be pulled up to 3.3V. In case of SDO_OD= "Low" & BYPASS= "High", the bypass mode is selected.
- The next combination is reserved. Do not use this combination. SDO_OD= "High" & BYPASS= "High".
  Refer to Table6 "SDO_OD pin, BYPASS pin Setup" for details.
- COUNT [5:0](#8, #7, #6, #5, #14, #12) pins are used to select delay time. When the setup is changed, SDO[0:1] (#18,19) output "Low" level (mute) voltage during the period selected by COUNT [5:0].
  Refer to 4. Delay Time for details.
- When RESETb is "Low", the NJU26903 is initialized on the rising edge of BCKI. SDO[0:1] output "Low" level (mute) voltage during the period selected by COUNT [5:0].
- In case of not using RESETb, connect RESETb to VDD.
- VDD is the power supply pin. Connect VDD to the 2.5V power supply. VSS is the GND pin. The decoupling capacitor is necessary between VDD and VSS.
- The input pins can interface with 3.3V ICs. (3.3V Input tolerant.)
- After Power supply or serial audio format changing, there is possibility the NJU26903 generates random data for the delay time during the period set by COUNT[5:1] pins. If necessary, the mute circuit should be added or reset NJU26903.

Table 5 Mode pin, FS pin Setting

FS (17pin)	MODE[1] (13pin)	MODE[0] (11pin)	Setup
0	0	0	RJ 16bit 32fs
0	0	1	LJ 16bit 32fs
0	1	0	I^2S 16bit 32fs
1	0	0	RJ 24bit 64fs
1	0	1	LJ 24bit 64fs
1	1	0	I^2S 24bit 64fs
Other			Reserved *1

* : 0=Low, 1=High *1 : Do not use.

Table 6 SDO_OD pin, BYPASS pin Setting

SDO_OD (15pin)	BYPASS (16pin)	NJU26903 Function
0	0	Delay Operation, SDO=CMOS Output
0	1	Bypass Operation, SDO=CMOS Output
1	0	Delay Operation, SDO=Open Drain Output
1	1	Reserved *1

* : 0=Low, 1=High *1 : Do not use.

■ Delay Time

- The NJU26903 provides maximum 4097 samples delay and slave-mode audio interface. The delay time depends on sampling frequency. (Delay time of SDI1-SDO1 is fixed at 4097 samples.)
- The next formula shows how to calculate the delay time.
  Refer to Table7 "Delay Sample Count Setting Example". (SDI0-SDO0)

Delay Sample Counts =
COUNT[0]x2048+COUNT[1]x1024+COUNT[2]x512+COUNT[3]x256+COUNT[4]x128+COUNT[5]x64+65

Table7 Delay Sample Count Setting Example (SDI0 – SDO0)

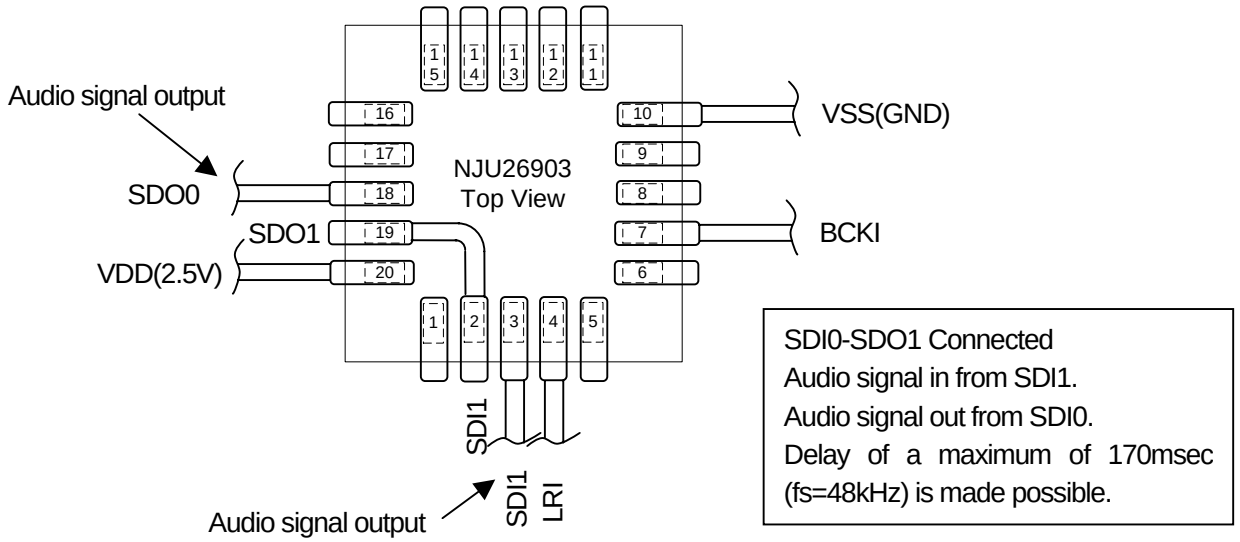
Pin No.	Symbol	count	Setting								
12	COUNT[0]	2048	0	0		0		1		1	1
14	COUNT[1]	1024	0	0		1		1		1	1
5	COUNT[2]	512	0	0	~	1	~	0	~	1	1
6	COUNT[3]	256	0	0		0		0		1	1
8	COUNT[4]	128	0	0		0		0		1	1
9	COUNT[5]	64	0	1		0		1		0	1
Delay Sample Counts			65 (min.)	129	~	1601	~	3201	~	4033	4097 (max.)

* 0=Low, 1=High

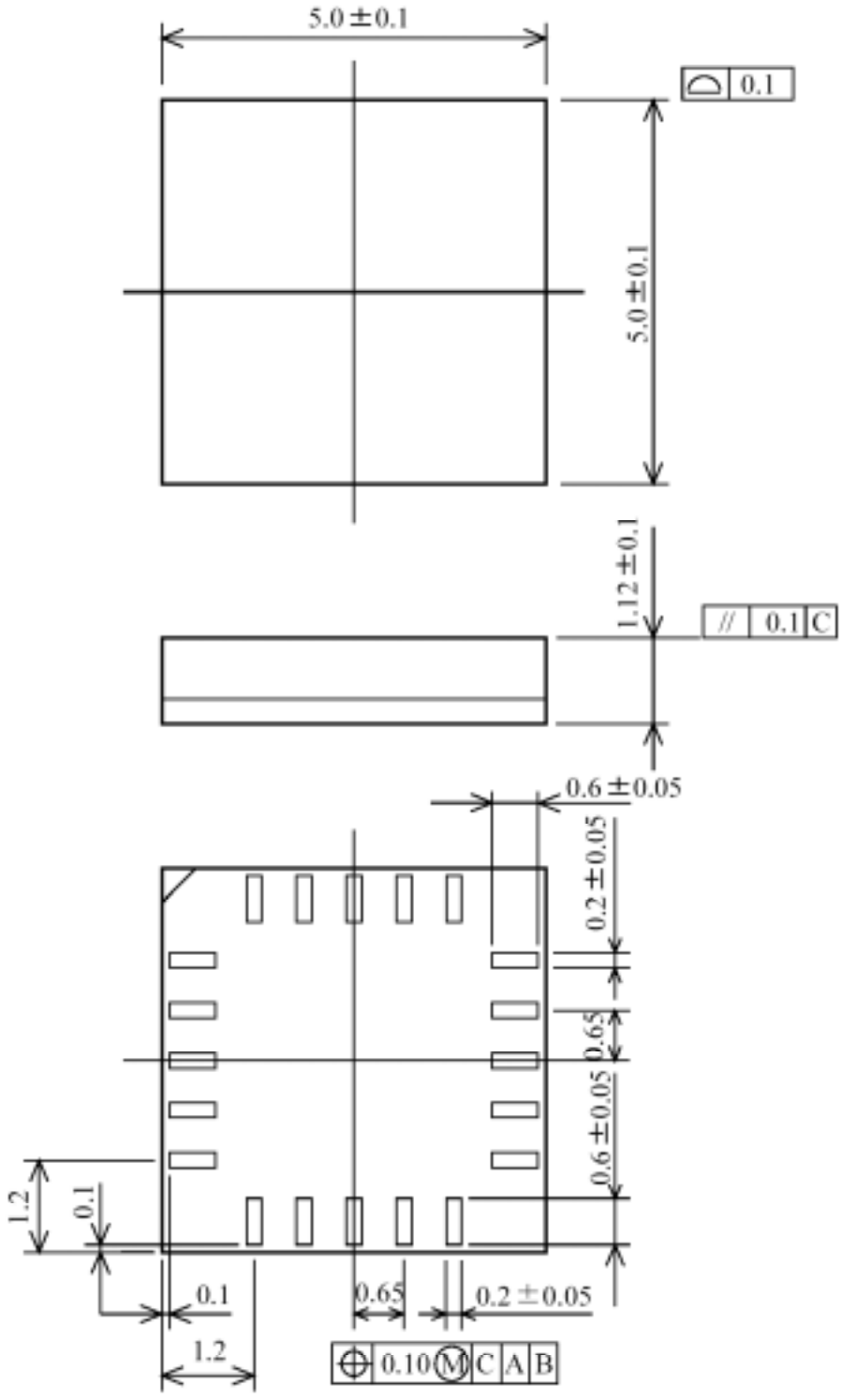
Table 8 Sampling Frequency, Delay sample counts and Delay Time setting

Sampling Frequency	Delay Time (ms)									
	65 (min.)	129	~	1601	~	3201	~	4033	4097 (max.)	Delay Sample Counts
192kHz	0.3	0.7		8.3		16.7		21.0	21.3	
96kHz	0.7	1.3		16.7		33.3		42.0	42.7	
88.4kHz	0.7	1.5	~	18.2	~	36.3	~	45.7	46.5	
48kHz	1.4	2.7		33.4		66.7		84.0	85.4	
44.1kHz	1.5	2.9		36.3		72.6		91.5	92.9	
32kHz	2.0	4.0		50.0		100.0		126.0	128.0	

Example Series connection



■ Package Dimensions



Package	: PCSP20-SGH4 Pb-Free
PCB	: Glass epoxy
Terminal plating	: Au (Cu/Ni/Au)
Mold resin	: epoxy

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