Multi-Function Digital Audio Decoder

■ General Description

The NJU26501 is a multi-function digital audio signal decoder.

The NJU26501 processes the stereo matrix-encoded or compressed signal into spacious sound of up to 7.1(max) channels by Dolby Digital, Dolby Digital EX or DTS with Bass Management System. Also non matrix-encoded audio signal can be processed into effective spacious sound by Dolby Pro Logic II.

The decoded multi-channel signal can be downmixed into 2-channel virtual surround output by the Dolby Virtual technology.

The applications of the NJU26501 are suitable for multi-channel products such as DVD Player, AV AMP, Home Theater and Car Audio, or any kinds of multi-channel audio products.

■ Package

NJU26501FS1

■ FEATURES

- Software

- Dolby Digital / Dolby Digital EX (7.1ch)
- Dolby Pro Logic II
- Virtual Dolby Digital
- Bass Management
- DTS (5.1ch)

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 24.576MHz (Standard), built-in PLL Circuit
- Digital Audio Interface : 2 Input ports / 4 Output ports
- Digital Audio Format : I^2S, Left- justified, Right-justified, 16/18/20/24 bit, BCK : 32/64fs
- Master / Slave Mode : In Master mode, MCK = 256fs, MCK2 = 512fs
- Serial Host Interface : I^2C bus (Standard-mode/100kbps, Fast-mode/400kbps)
  : 4-Wire-Serial bus (Clock, Enable, Input data, Output data)
- Power Supply : V_{DD} = V_{DDPLL} = 1.8V
  : V_{DDIO} = 3.3V
- Input terminal : 5.0V Input tolerant
- Package : QFP52-S1 (Pb-Free)

* The detail hardware specification of the NJU26501 is described in the " NJU26500 Series Hardware Data Sheet".

■ Block Diagram

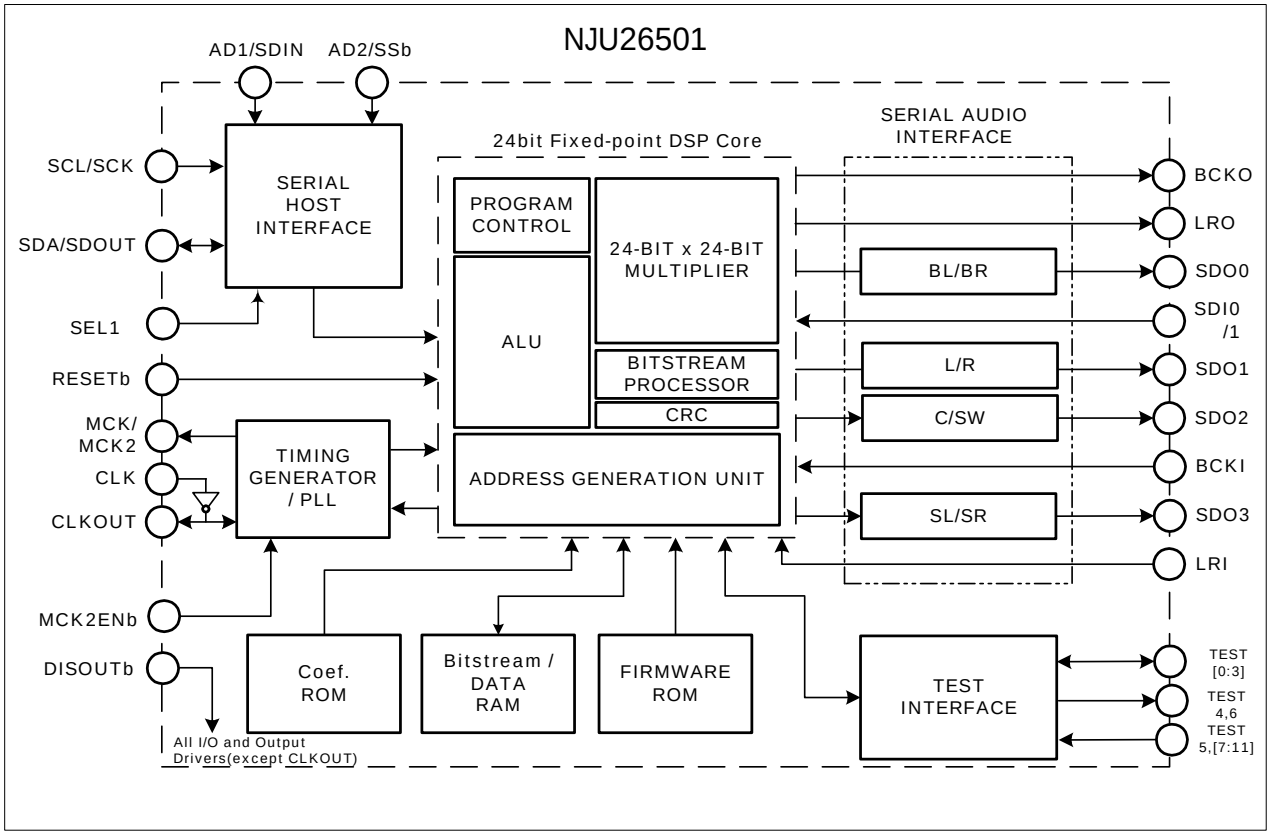
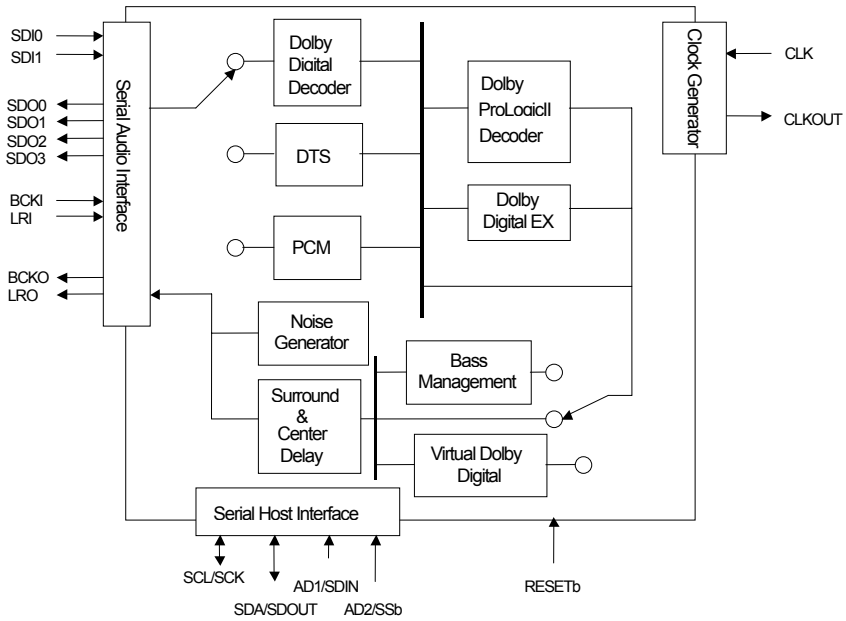


Fig.1 NJU26501 Hardware Block Diagram

■ Function Block Diagram



■ Pin Configuration

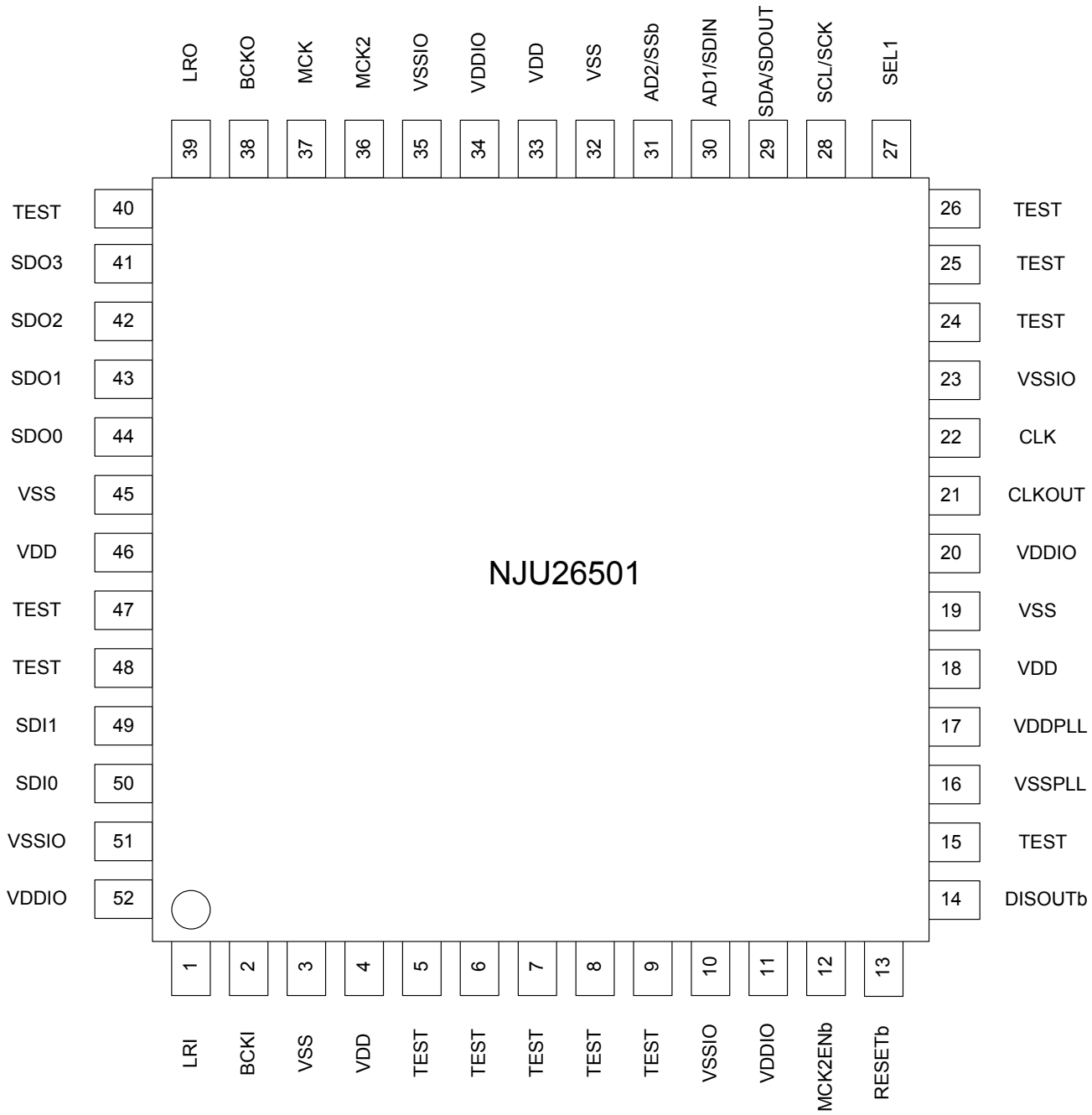


Fig.3 Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Function
1	LRI	I	LR Clock Input
2	BCKI	I	Bit Clock Input
3, 19, 32, 45	VSS	-	Power Supply GND
4, 18, 33, 46	VDD	-	Power Supply 1.8V
5, 6, 7, 8	TEST	I/O	for test (connected with VDDIO or VSSIO through 3.3kΩ resistance.)
9, 24	TEST	O	for test (Not connected : Open)
10, 23, 35, 51	VSSIO	-	I/O Power Supply GND
11, 20, 34, 52	VDDIO	-	I/O Power Supply 3.3V
12	MCK2ENb	Ipd	MCK2 Enable ('0' : MCK2 enable / '1' : MCK2 turns Hi-Z)
13	RESETb	I	Reset (RESETb='Low' : DSP Reset)
14	DISOUTb	Ipu	Disable Output ('0':All outputs (except CLKOUT) turn Hi-Z)
15,25, 26	TEST	Ipd	for test (connected to VSSIO)
16	VSSPLL	-	PLL Power Supply GND
17	VDDPLL	-	PLL Power Supply 1.8V
21	CLKOUT	I/O	OSC Clock Output
22	CLK	I	OSC Clock Input (24.576MHz)
27	SEL1	Ipu	Select Host Interface ('1' : 4-wire serial mode / '0' : I^2C mode)
28	SCL/SCK	I	I^2C SCL (I^2C mode) / Serial clock (4-wire serial mode)
29	SDA/SDOUT	I/O	I^2C SDA (I^2C mode) / Serial Data Out (4-wire serial mode) I^2C bus mode : SDA pin requires a pull-up resistance. 4-wire Serial mode : SDOUT does not require a pull-up resistance.
30	AD1/SDIN	I	I^2C Address (I^2C mode) / Serial Data In (4-wire serial mode)
31	AD2/SSb	I	I^2C Address (I^2C mode) / Serial enable (4-wire serial mode)
36	MCK2	O	Master Clock Output 2 (Buffered output of CLK input)
37	MCK	O	Master Clock Output (2-Divided output of CLK input)
38	BCKO	O	Bit Clock Output
39	LRO	O	LR Clock Output
40	TEST	Ipu	for test (connected to VDDIO)
41	SDO3	O	Audio Data Output ch.3 (Surround channel (LS/RS) output)
42	SDO2	O	Audio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)
43	SDO1	O	Audio Data Output ch.1 (Front channel (L/R) output)
44	SDO0	O	Audio Data Output ch.0 (Back Surround channel (BL/BR) output)
47, 48	TEST	I	for test (connected to VSSIO)
49	SDI1	I	Audio Data Input ch.1
50	SDI0	I	Audio Data Input ch.0

Note : I : Input
Ipd : Input Pull-down
Ipu : Input Pull-Up
O : Output
I/O : Bi-directional

■ Audio Interface

The serial audio interface carries audio data to and from the NJU26501. Industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified are supported.

The NJU26501 serial audio interface includes 2 data input lines: SDI0/SDI1 and 4 data output lines: SDO0/SDO1/SDO2/SDO3. (Table 2. 3.)

Table 2 Serial Audio Input Pin Description

Pin No.	Symbol	Description
50	SDI0	Audio Data Input ch.0
49	SDI1	Audio Data Input ch.1

Table 3 Serial Audio Output Pin Description

Pin No.	Symbol	Description
44	SDO0	Back Surround (BL/BR) Output
43	SDO1	Front (L/R) Output(*)
42	SDO2	Center/Sub Woofer (C/SW) Output
41	SDO3	Surround (LS/RS) Output

(*) In Virtual Dolby Surround mode, only front Lch/Rch outputs are active. The other channels are muted. However, if "LFE Decode" is set on, an output will become possible from Sub Woofer channel.

■ Host Interface

The NJU26501 can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or I^2C bus. Data transfers are in 8 bit packets (1 byte) when using either format.

The SEL1 pin controls the serial bus mode. When the SEL1 is "Low" level during the NJU26501 initialization, I^2C bus is available. When the SEL1 is "High" level during the NJU26501 initialization, 4-Wire serial bus is available.(Table 4) Serial Host Interface Pin Description. (Table 5)

Table 4 Serial Host Interface Pin Description

Pin No.	Symbol	Setting	Host Interface
27	SEL1	"Low"	I^2C bus
		"High"	4-Wire serial bus

Table 5 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C /Serial)	I^2C bus Format	4-Wire Serial bus Format
28	SCL/SCK	Serial Clock	Serial Clock
29	SDA/SDOUT	Serial Data Input/Output (open drain)	Serial Data Output (CMOS)
30	AD1/SDIN	I^2C bus address Bit1	Serial Data Input
31	AD2/SSb	I^2C bus address Bit2	Serial enable

Note : When 4-Wire Serial bus is selected, SDA /SDOUT pin is CMOS output. When I^2C bus is selected, this pin is a bi-directional open drain. This pin, which is assigned for I^2C bus, requires a pull-up resistance.

■ I²C bus

When the NJU26501 is configured for I²C bus communication in SEL1="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistance. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6)

However, please be sure to set AD2 pin as "High". Because, the Dolby function is contained, it is recommended so that bit2 of I²C bus slave address should be set to "1".

Table 6 I²C bus Interface Slave address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	

* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

Note:

In case of the NJU26501, only single-byte transmission is available.

Both "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" data transfer rate are supported.

However, the NJU26501 is not completely based on I²C bus specification from the characteristic of a SDA I/O terminal and a SCL input terminal.

The following (1) to (12) ; "Command + Parameter(2words)".

(1) → Start condition
(2) → Address
(3) → Command
(4) → Stop condition
(5) → Start condition
(6) → Address
(7) → Parameter(1stword)
(8) → Stop condition
(9) → Start condition
(10) → Address
(11) → Parameter(2nd word)
(12) → Stop condition

■ **4-Wire Serial Interface**

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb = "Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSb. SDOUT is always CMOS output. SDOUT does not require a pull-up resistance.

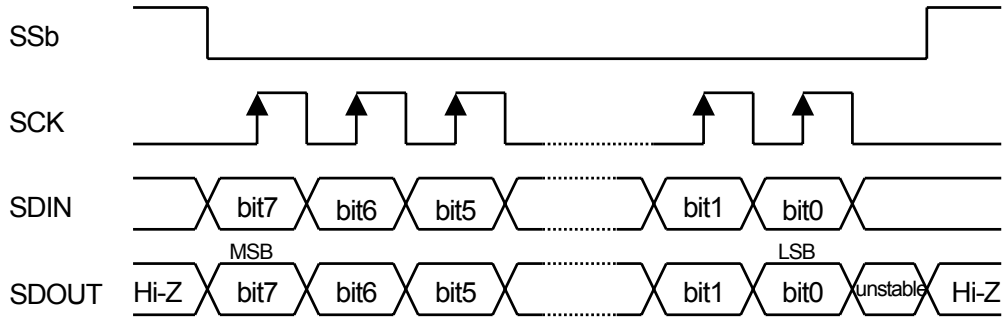


Fig. 4 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High".
When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.
After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High".

■ Host command

Table7. NJU26501 command table

No.	Command
1	Set Task
2	AC3 Decode
3	PCM Scale
4	Maximum Frame Repeat
5	Pro Logic II
6	Bass Management
7	Delay
8	Pink Noise Generator
9	Play
10	Stop
11	Mute
12	Unmute
13	AC3 Status Read
14	Version Number
15	Audio Interface Configuration
16	NOP
17	READ
18	Read Task
19	Input Select
20	Bass Management Trimmer
21	Karaoke
22	Virtual
23	DTS Status Read
24	Bypass Mode Configuration
25	Dolby Digital EX Mode Configuration

Notes :

In respect to detail command information, request New Japan Radio Co., Ltd. and permission of each licenser (Dolby and DTS) is required.

Before a customer provides pre-production prototype for approval of “DTS Product Evaluation Test ", Please be sure to contact New Japan Radio Co.,Ltd. However, the DTS function is upgraded.

■ License Information

1. “Dolby,” “Pro Logic II,” “Dolby Digital,” “Dolby Digital EX,” and the double-D symbol are trademarks of Dolby Laboratories. The NJU26501 may only be supplied to licensees of or companies authorized by Dolby Laboratories. Please refer all licensing inquiries to Dolby Laboratories.

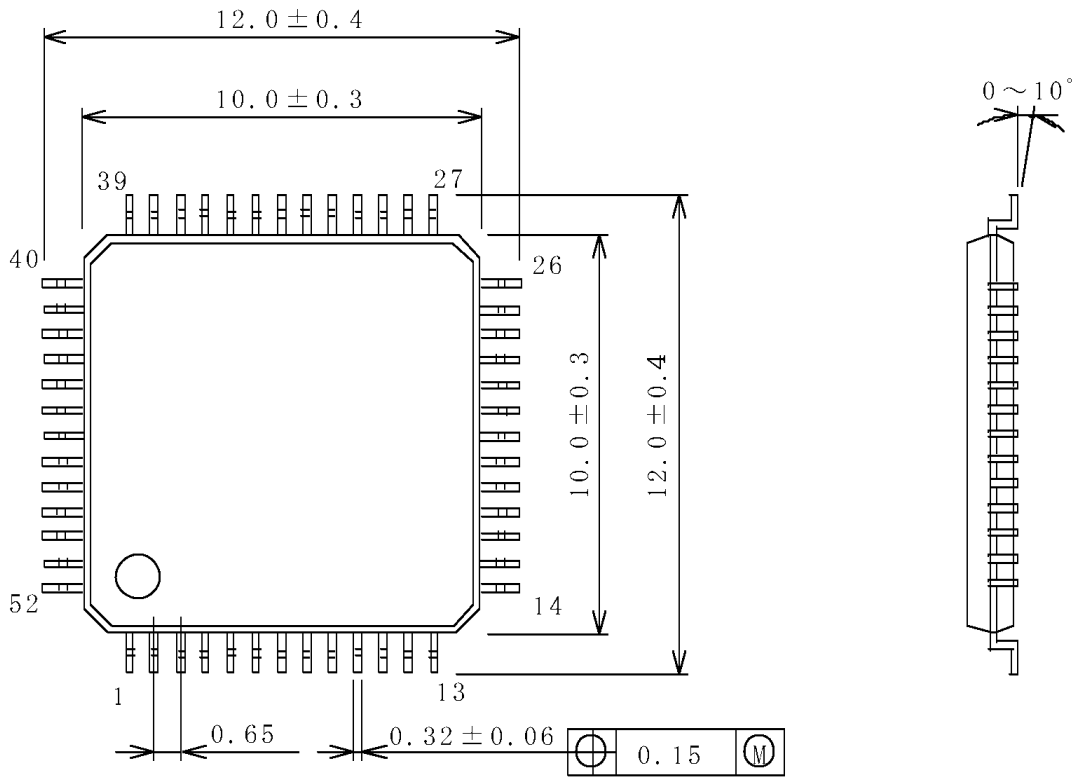
2. “DTS” is a registered trademark of DTS, Inc. ”©1996-2004 Digital Theater System, Inc.”

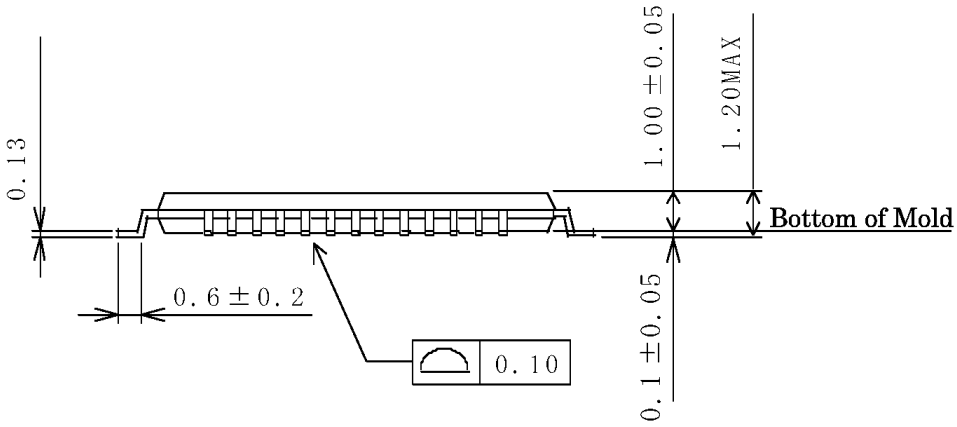
■ Royalty for Dolby and DTS

The NJU26501 provides the Dolby and DTS functions.

The customers must use both functions. If the customers use only one function, for example Dolby or DTS, and also must pay the royalties to Dolby and DTS both.

■ **Package Dimensions (QFP52-S1, Pb-Free)**





Unit : mm

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