High Quality Audio
J-FET Input Dual Operational Amplifier

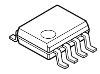
■GENERAL DESCRIPTION

The NJM8901 is a high quality audio dual operational Amplifier with JFET technology, strikes a balance between “MUSES technology” and mass-production technique.

The original process tuning and the assembly technology, based on MUSES technology, make excellent sound and absorbing cost increases.

The characteristics like Low noise (13nV/√Hz), high slew rate (20V/µs) and low distortion (0.003% at Av=10) suitable for audio preamplifiers, active filters, and line amplifiers. In addition, taking advantage of the low input bias current that J-FET has, it is suitable for transimpedance amplifier (I/V converter).

■PACKAGE OUTLINE



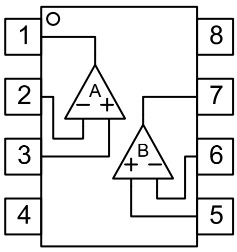
(SOP8 JEDEC 150 mil)

■FEATURES

●Low Noise	13nV/√Hz typ.
	1.6uVrms typ. (RIAA)
●Low Distortion	0.003% typ. (Av=10)
●Wide Gain Bandwidth Product	5MHz typ.
●Slew Rate	20V/µs typ.
●Input Offset Voltage	2mV typ. 10mV max.
●Input Bias Current	30pA typ. 400pA max.
●Open Loop Voltage Gain	110dB typ.
●Operating Voltage	±4V ~±18V
●J-FET Technology	
●Package Outline	SOP8 JEDEC 150 mil

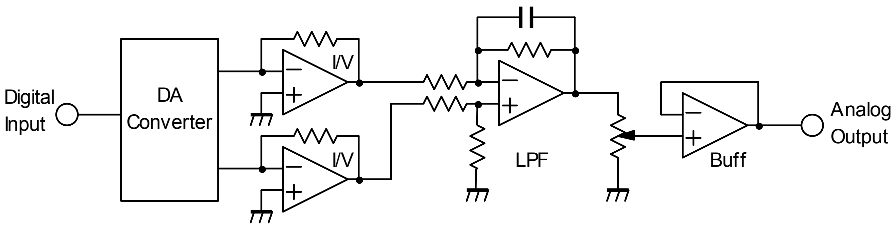
■ PIN CONFIGLATION

(Top View)



PIN FUNCTION
1. A OUTPUT
2. A -INPUT
3. A +INPUT
4. V-
5. B +INPUT
6. B -INPUT
7. B OUTPUT
8.V+

■TYPICAL APPLICATION



DAC Output I/V converter + LPF circuit

■ABSOLUTE MAXIMUM RATINGS (Ta=25ºC)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+/V^-	±18	V
Common Mode Input Voltage Range	V_{ICM}	±15 (Note1)	V
Differential Input Voltage Range	V_{ID}	±30	V
Power Dissipation	P_D	550 (Note2)	mW
Operating Temperature Range	T_{OPR}	-40~+85	ºC
Storage Temperature Range	T_{STG}	-40~+125	ºC

(Note 1) For supply Voltages less than ±15V, the maximum input voltage is equal to the Supply Voltage.
(Note 2) Mounted on the EIA/JEDEC standard board (114.3×76.2×1.6mm, two layer, FR-4).
Please refer to the following Power Dissipation and Ambient Temperature.

■RECOMMENDED OPERATING CONDITION (Ta=25ºC)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+/V^-		±4.0	-	±18	V

■ELECTRIC CHARACTERISTICS

●DC CHARACTERISTICS (V^+/V^-=±15V, Vcm=0V, Ta=25ºC, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{CC}	R_L=∞, No Signal	-	4	6	mA
Input Offset Voltage	V_{IO}	R_S=50Ω (Note3)	-	2	10	mV
Input Bias Current	I_B		-	30	400	pA
Input Offset Current	I_{IO}	(Note3)	-	5	200	pA
Input Resistance	R_{IN}		-	10^{12}	-	Ω
Large Signal Voltage Gain	A_V	R_L≥2kΩ, Vo=±10V	86	110	-	dB
Common Mode Rejection Ratio	CMR	V_{CM}=±12V, Rs≤10kΩ	70	90	-	dB
Supply Voltage Rejection Ratio	SVR	V^+/V^-=±9.0 to ±18V, Rs≤10kΩ	76	100	-	dB
Maximum Output Voltage	V_{OM}	R_L≥10kΩ	±12	+13.5, -13	-	V
Common Mode Input Voltage Range	V_{ICM}	CMR≥70dB	±12	+15, -12.5	-	V

(Note3) Written by the absolute rate.

●AC CHARACTERISTICS (V^+/V^-=±15V, Vcm=0V, Ta=25ºC unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate	SR	R_L≥2kΩ	-	20	-	V/us
Gain Bandwidth Product	GB	f=10kHz	-	5	-	MHz
Equivalent Input Noise Voltage1	e_N	R_S=100Ω , f=1KHz	-	13	-	nV/√Hz
Equivalent Input Noise Voltage2	V_{NI}	RIAA, R_S=2.2kΩ, 30kHz, LPF	-	1.6	3	μVrms
Total Harmonic Distortion	THD	f=1kHz ,A_V=+10, Vo=5Vrms, R_L=2kΩ	-	0.003	-	%
Channel Separation	CS	f=1kHz , A_V=-100, R_S=1kΩ, R_L=2kΩ		130	-	dB

■Application Notes

●Package Power, Power Dissipation and Output Power

IC is heated by own operation and possibly gets damage when the junction power exceeds the acceptable value called Power Dissipation P_D. The dependence P_D on ambient temperature is shown in Fig 1. The plots are depended on following two points. The first is P_D on ambient temperature 25ºC, which is the maximum power dissipation. The second is 0W, which means that the IC cannot radiate any more. Conforming the maximum junction temperature Tjmax to the storage temperature Tstg derives this point. Fig.1 is drawn by connecting those points and conforming the P_D lower than 25ºC to it on 25ºC. The P_D is shown following formula as a function of the ambient temperature between those points.

$$\text{Dissipation Power} \quad P_D = \frac{Tjmax - Ta}{\theta ja} \text{ [W] (Ta=25ºC to Ta=150ºC)}$$

Where, θja is heat thermal resistance which depends on parameters such as package material, frame material and so on. Therefore, P_D is different in each package.

While, the actual measurement of dissipation power on IC is obtained using following equation.

(Actual Dissipation Power) = (Supply Voltage V^+/V^-) X (Supply Current Icc) – (Output Power Po)

This IC should be operated in lower than P_D of the actual dissipation power.

To sustain the steady state operation, take account of the Dissipation Power and thermal design.

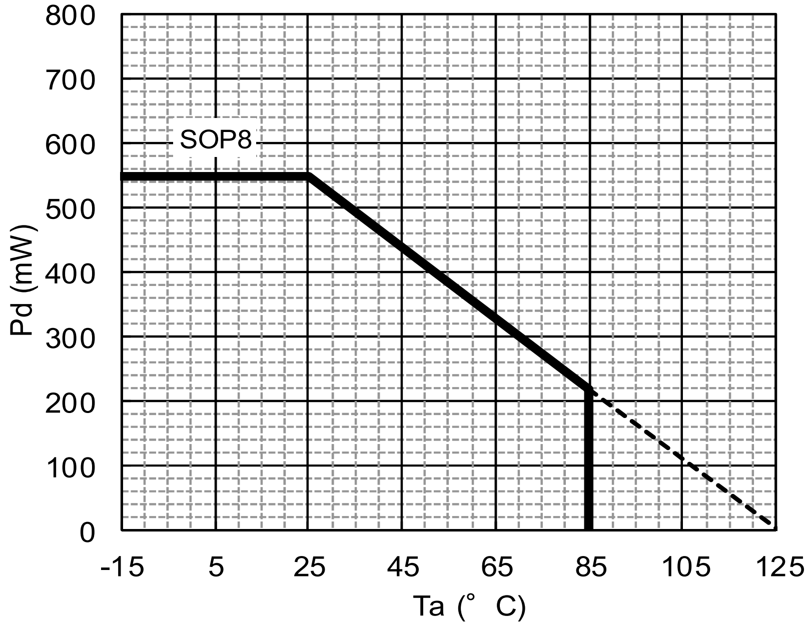
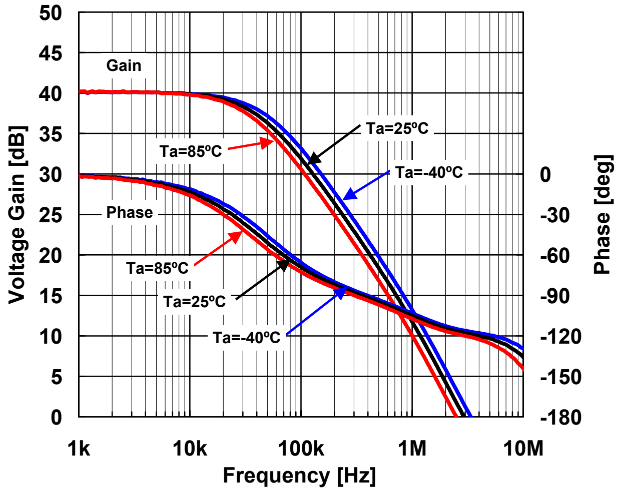


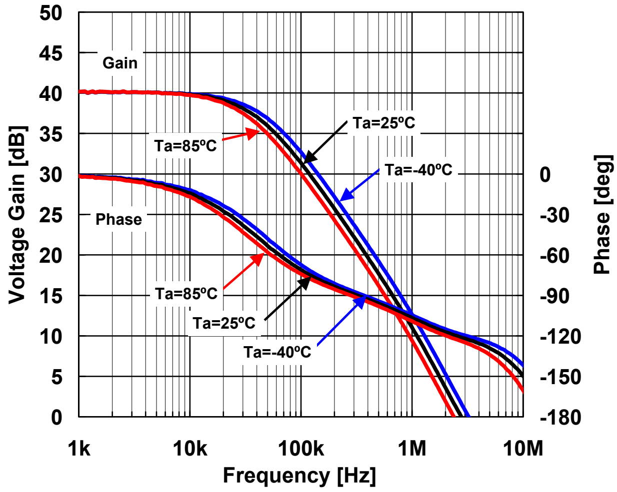
Fig.1 Power Dissipations vs. Ambient Temperature

■ TYPICAL CHARACTERISTICS

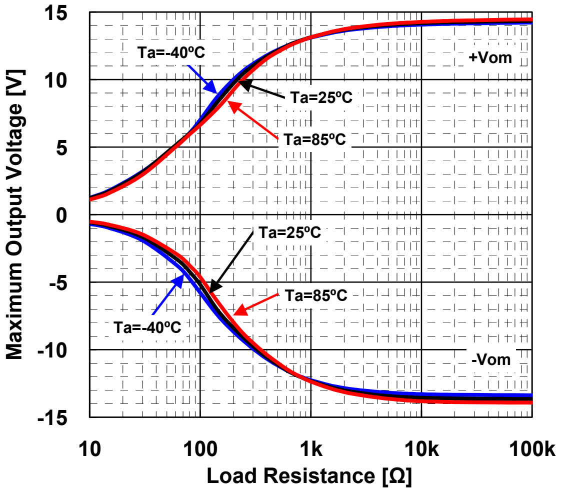
Gain vs. Frequency (Temperature)
V^+/V^-=±15V, A_V=+100, R_L=2kΩ, C_L=10pF



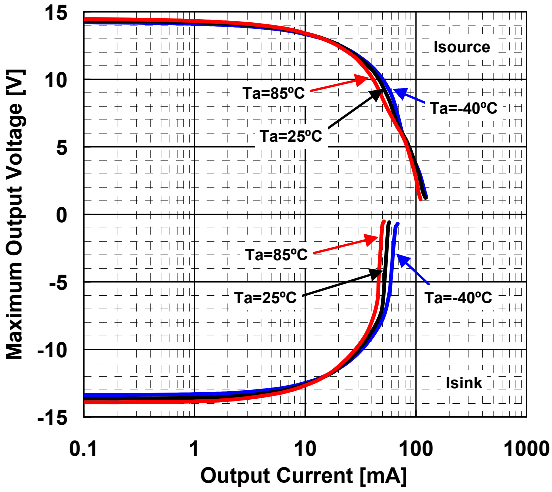
Gain vs. Frequency (Temperature)
V^+/V^-=±4V, A_V=+100, R_L=2kΩ, C_L=10pF



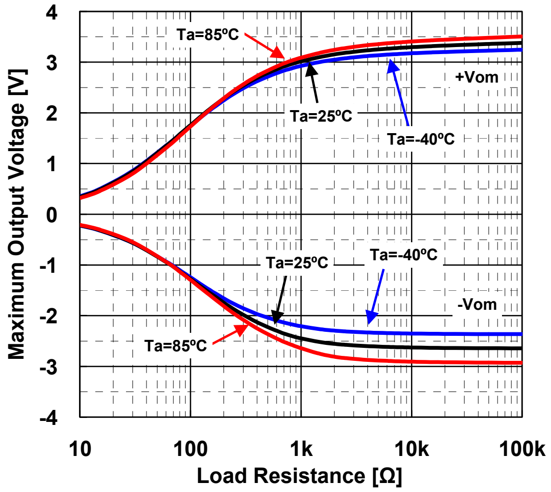
Maximum Output Voltage vs. Load Resistance
(Temperature)
V^+/V^-=±15V, Gv=open



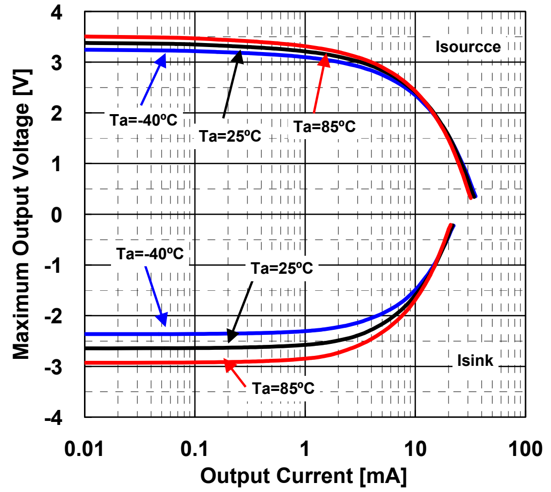
Maximum Output Voltage vs. Output Current
(Temperature)
V^+/V^-=±15V, Gv=open, calculated by Vom/R_L



Maximum Output Voltage vs. Load Resistance
(Temperature)
V^+/V^-=±4V, Gv=open

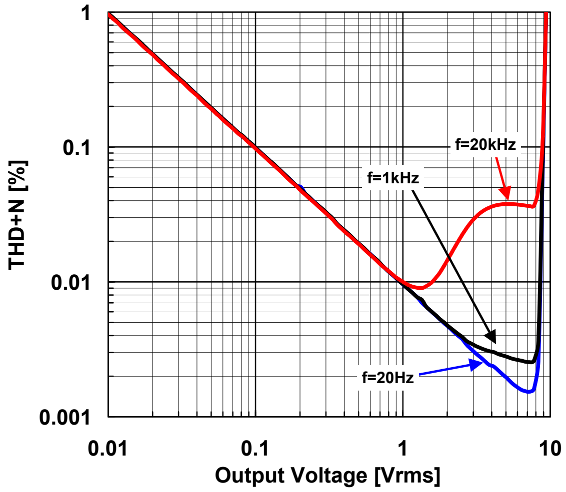


Maximum Output Voltage vs. Output Current
(Temperature)
V^+/V^-=±4V, Gv=open, calculated by Vom/R_L

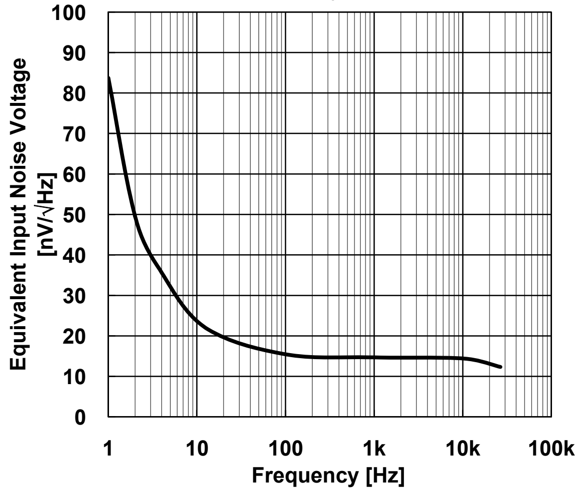


■ TYPICAL CHARACTERISTICS

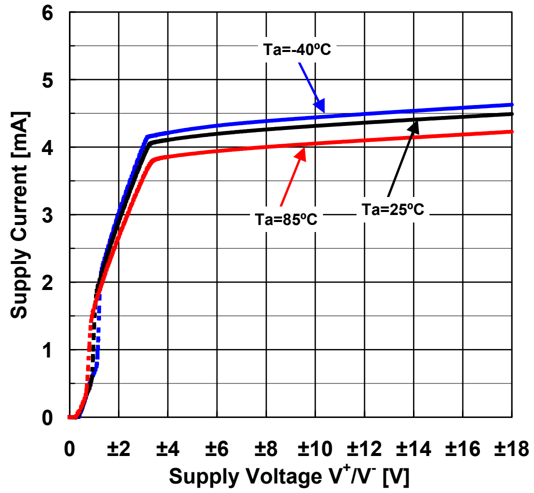
THD+N vs. Output Voltage
V^+/V^-=±15V, A_V=+10, R_L=2kΩ, Ta=25ºC



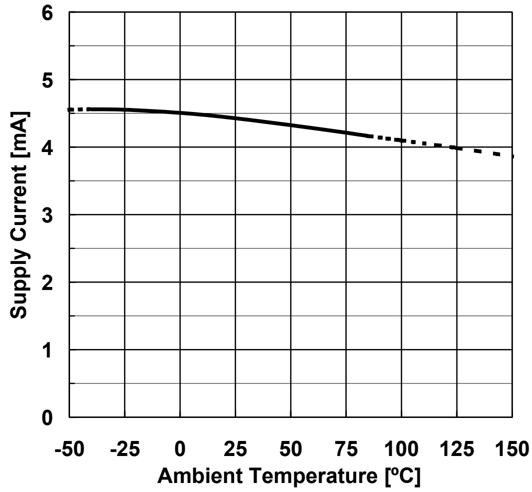
Voltage Noise vs. Frequency
V^+/V^-=±15V, A_V=+100, R_S=100Ω, R_L=∞, Ta=25ºC



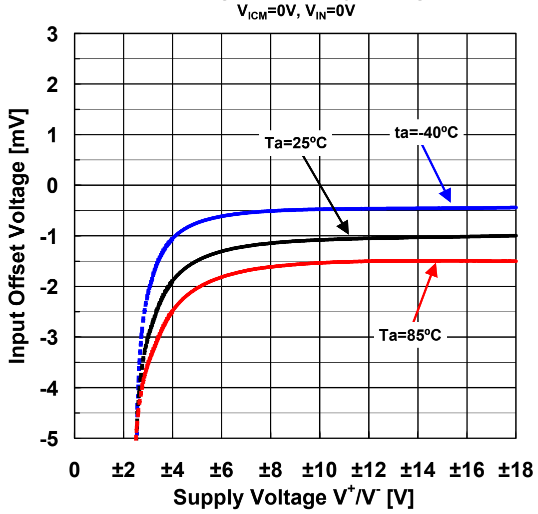
Supply Current vs. Supply Voltage (Temperature)
G_V=0dB, V_{IN}=0V



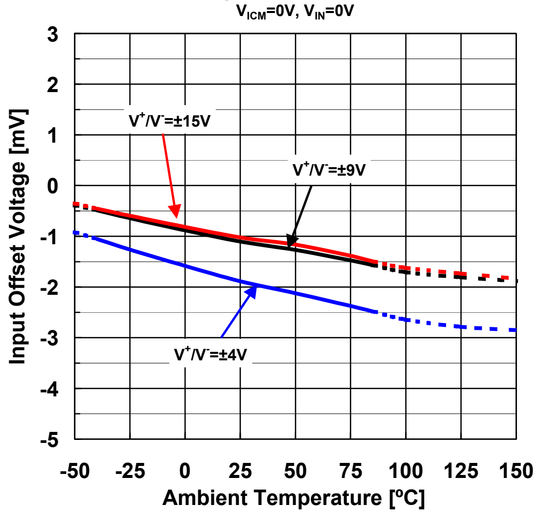
Supply Current vs. Temperature
V^+/V^-=±15V, G_V=0dB, V_{IN}=0V



Input Offset Voltage vs. Supply Voltage (Temperature)
V_{ICM}=0V, V_{IN}=0V

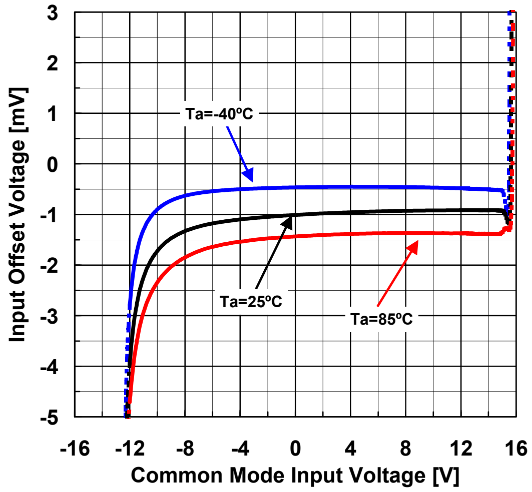


Input Offset Voltage vs. Temperature (Supply Voltage)
V_{ICM}=0V, V_{IN}=0V

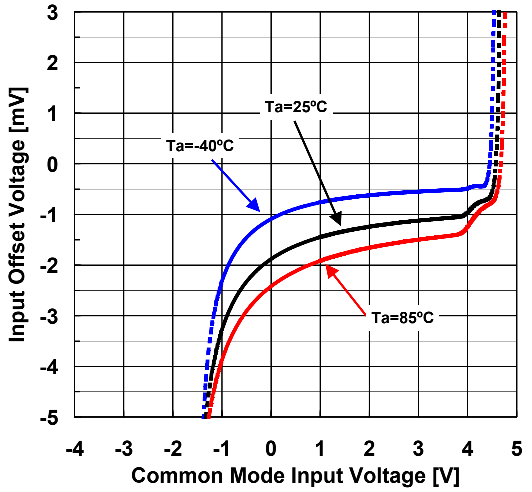


■ TYPICAL CHARACTERISTICS

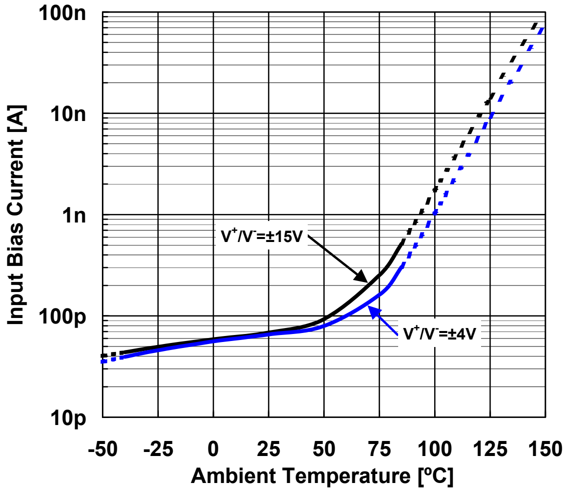
Input Offset Voltage
vs. Common Mode Input Voltage
(Temperature)
$V^+/V^-=\pm15V$



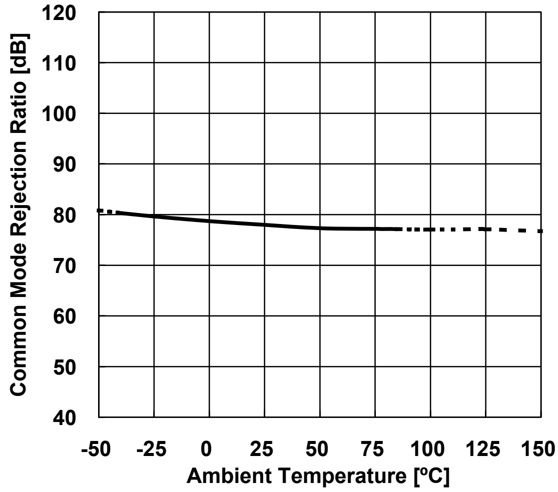
Input Offset Voltage
vs. Common Mode Input Voltage
(Temperature)
$V^+/V^-=\pm4V$



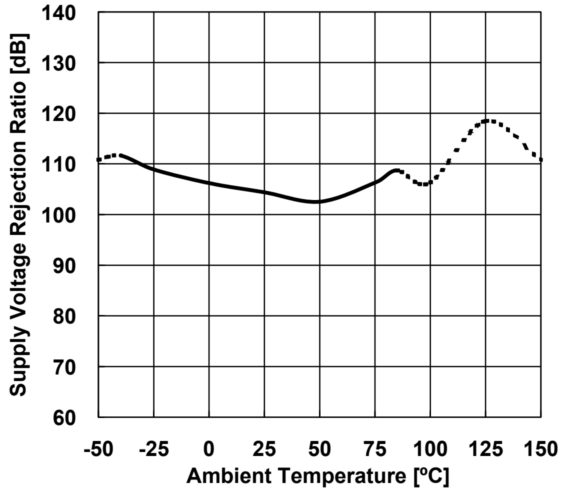
Input Bias Current vs. Temperature (Supply Voltage)
$V_{ICM}=0$



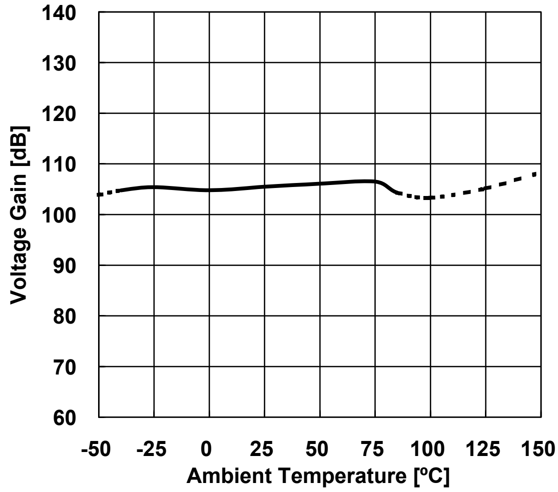
CMR vs. Temperature
$V^+/V^-=\pm15V$, $V_{ICM}=-12V$ to $+12V$



SVR vs. Temperature
$V_{ICM}=0V$, $V^+/V^-=\pm9V$ to $\pm18V$



Open Loop Voltage Gain vs. Temperature
$V^+/V^-=\pm15V$, G_V=open, $V_O=-10V$ to $+10V$, $R_L=2k\Omega$



■ TYPICAL CHARACTERISTICS