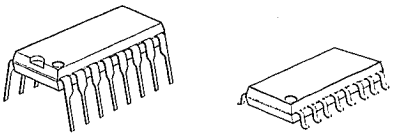
SYNCHRONOUS SEPARATOR WITH AFC

■ GENERAL DESCRIPTION

NJM2257 excutes Horizontal and Vertical synchronous signal separation, and odd/even field signal detection, from composit video signals.

Built-in 1/2 fH Killer Function circuit can make stabilization of the Horizontal signal oscillation output during the Vertical period.

■ PACKAGE OUTLINE



NJM2257D NJM2257M

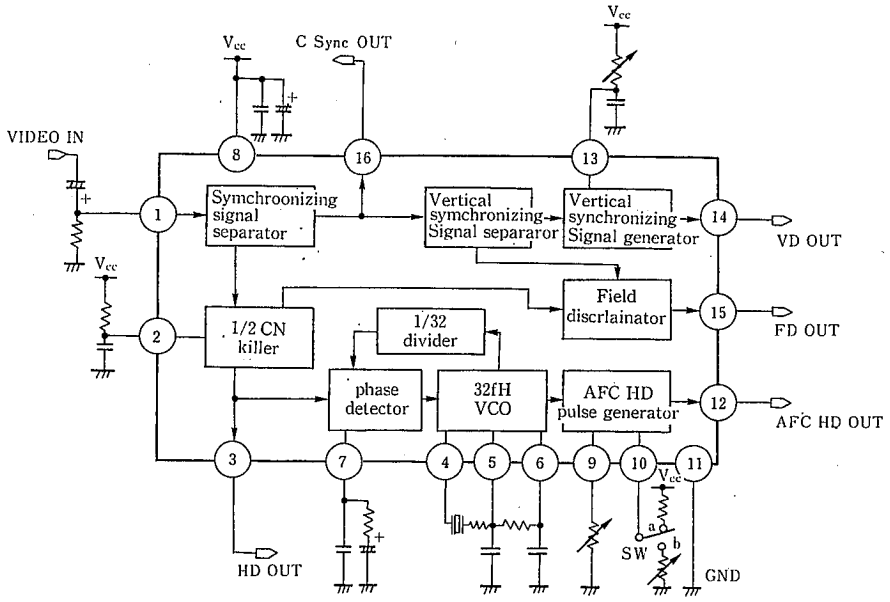
■ FEATURES

- Operating Voltage (+4.5～+5.3V)
- Internal AFC circuit (Horizontal sync. signal.)
- Internal 1/2fH Killer Function
- AFC output Pulse Delay time is Adjustable
- Vertical synchronous pulse width is Adjustable
- Internal Field Discrlainat Function
- Package Outline DIP16, DMP16
- Bipolar Technology

■ APPLICATION

- VTR, TV, AV components etc.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

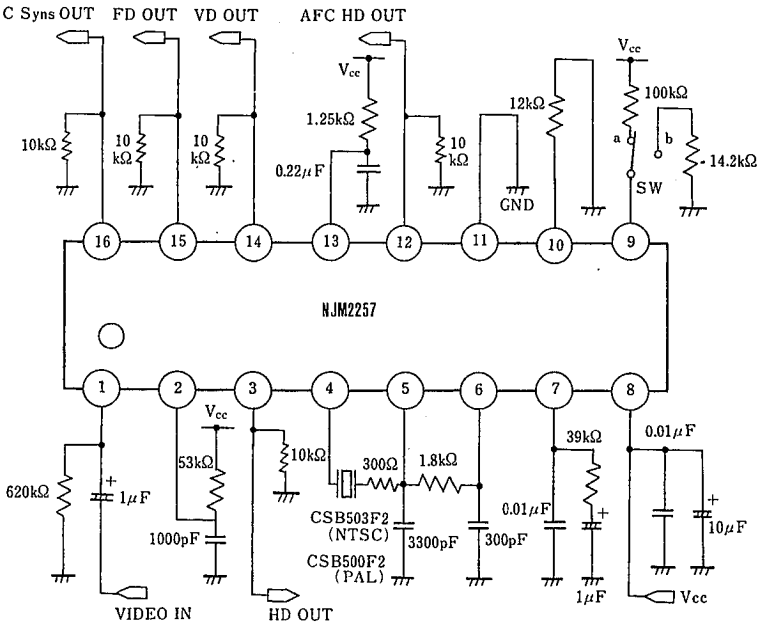
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+7	V
Power Dissipation	P_D	(DIP16) 500	mW
		(DMP16) 350	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Vcc=5V, Ta=25℃)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiessent Current		I_Q		—	23.0	30.0	mA
AFC Free Run Frequency		f_{OH}		15.54	15.74	15.94	KHz
AFC HD pulse width		T_{AHW1}	SW=a	3.5	4.0	4.5	μS
		T_{AHW2}	SW=b	2.5	4.0	5.5	
AFC HD Delet Time		T_{AHD}		−1.0	0.5	2.0	μS
AFC Lock Range		Δf_{HL}		500	700	—	Hz
AFC Cap Charange		Δf_{HP}		400	600	—	Hz
AFC Output Voltage	H	V_{HAH}		4.0	4.2	—	V
	L	V_{HAL}		—	0	0.1	
Sync Sepa Sync. Separation Level		V_{HSR}		—	0.16	0.18	V
Sync Sepa Delay Time		T_{HCD}		0.05	0.20	0.35	μS
Sync Sepa Output Voltage	H	V_{HCH}		4.0	4.2	—	V
	L	V_{HCL}		—	0	0.1	
HD Output Palth Width		T_{HPW}		4.0	5.5	7.0	μS
HD Output Delay Time		T_{HPD}		0.35	0.6	0.8	μS
HD Output Voltage	H	V_{HH}		4.0	4.2	—	V
	L	V_{HL}		—	0	0.1	
V Sync Palth Width		T_{VW}		170	190	210	μS
V Sync Delay Time		T_{VD}		7.0	10.0	13.0	μS
V Sync Output Voltage	H	T_{VH}		4.0	4.2	—	V
	L	V_{VL}		—	0	0.1	
Field Distinction Delay Time	odd	T_{FOD}		246	256	266	μS
	even	T_{FED}		216	226	236	
Field Distinction Output Voltage	odd	V_{FOR}		4.0	4.2	—	V
	even	V_{FER}		—	0	0.1	

■ APPLICATION CIRCUIT



■ APPLICATION NOTES

It shows the characteristics by changing of the following resistor.

- The resistance between 9 Pin and GND
  High resistance——AFC HD pulse is wide
  Low resistance——AFC HD pulse is narrow
- The resistor between 9 Pin and V+
  At the resistor is 100Ω. AFC HD Delay adjustment is off, and AFC HD output width is 4μs (typ.)
- The resistor between 9 Pin and GND is fandamentally 14.2 kΩ, because the purpose of this resistor is pulse width adjusts 4μs

- The resistor between 10 Pin and GND
  High resistance——AFC HD Delay time gains
  Low resistance——AFC HD Delay time loses

- The resistor between 13 Pin and GND
  High resistance——Vsync pulse is wide
  Low resistance——Vsync pulse is narrow

- The resistor joind 2 Pin
  Please adjust the wide of following W is from 33 μs to 37 μs (W=−(C · R)In0.5)

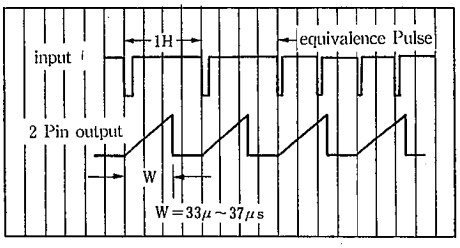
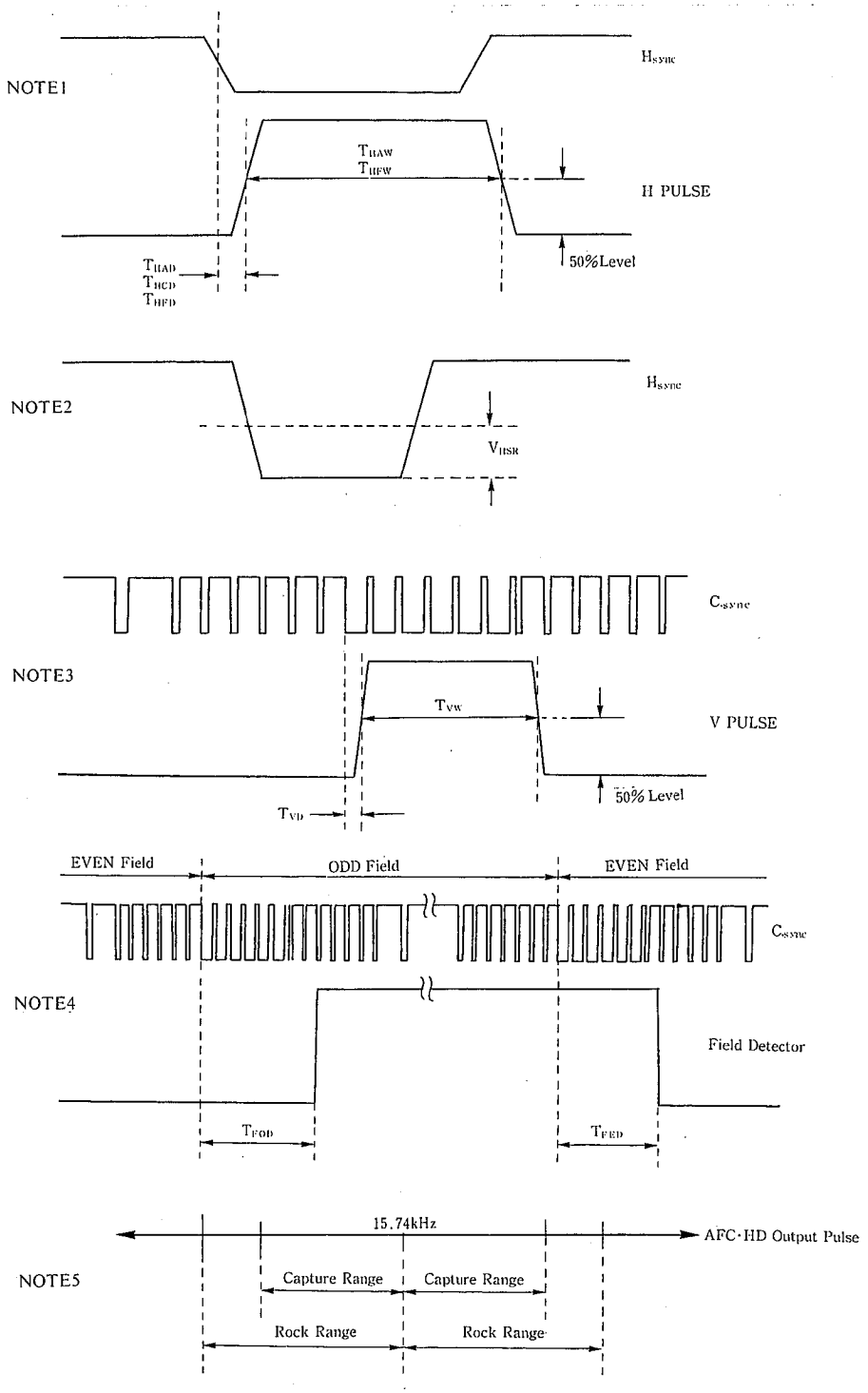
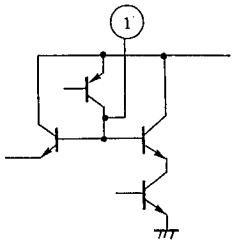
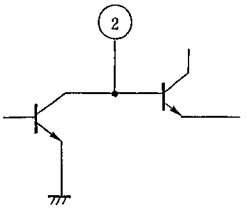
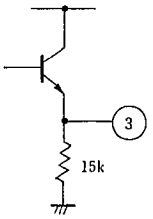
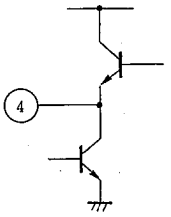
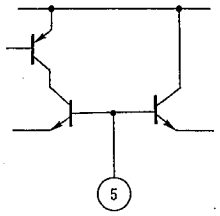


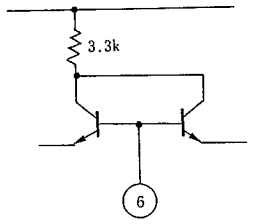
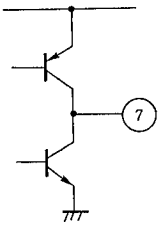
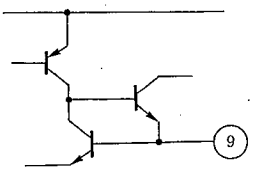
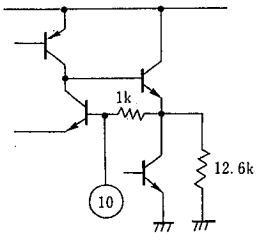
Fig 1 I/O PULSE


NOTE1
Hsync
H PULSE
THAW
THFW
50%Level
THAD
THCD
THFD
NOTE2
Hsync
VHSR
Csync
NOTE3
V PULSE
TVW
50% Level
TVD
EVEN Field
ODD Field
EVEN Field
Csync
NOTE4
Field Detector
TFOD
TFED
15.74kHz
AFC·HD Output Pulse
NOTE5
Capture Range
Capture Range
Rock Range
Rock Range

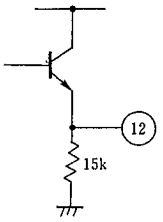
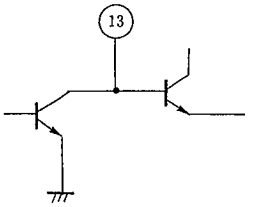
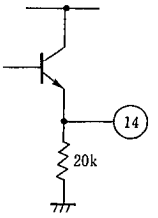
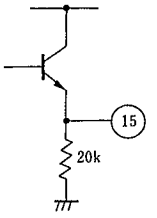
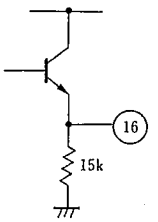
■ TERMINAL EXPLANATION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUINALENT CIRCUIT
1	VIDEO-IN	Composit Video Signal Input	
2	MM-HT	HD & FD puse are Controlled by setting mono multi	
3	HD-OUT	1/2 f_H Killer D Output	
4	VCO-OUT	VCO Output is to be given to Ceramic Oscillator	
5	VCO-FILTER 1	Decide the Volume to be transfered shall by decided of Ceramic Oscittator. (90°late)	

■ TERMINAL EXPLANATION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUINALENT CIRCUIT
6	VCO-FILTER 2	Decide the Volume to be transfered shall by decided of Ceramic Oscittator. (90°late)	
7	L.P.F	L.P.F. of AFC	
8	V^+	Supply Voltage	
9	VR-1	AFC-HD Output Can be adjusted by putting resistor betwee 9~GND (9 to V_{CC}no adjustment). The pulse width cam be adjusted by making changeable of resister (Adjusting mode)	
10	VR-2	AFC-HD Output delay adjustment by putting 10 pin resister changeabl at 9 pin adjustment mode.	
11	GND	G raund	

■ TERMINAL EXPLANATION

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUINALENT CIRCUIT
12	AFC, HD-OUT	AFC·HD Output	
13	MM-VT	Pulse Width of Vsync-OUT is adjusted by setting mono multi time constant.	
14	Vsync-OUT	Vertical Synchronous Signal Output.	
15	FD-OUT discrimination	Field Distiniction Signal Output.	
16	Csync-OUT	Synchronous Separation Output	

■ PIN FUNCTION

PIN NO	FUNCTION BLOCK	OPERATIONAL DESCRIPTION	NDTE
① Pin	Signal Input	Video Signal input	Sync tip clump
② Pin	HD pulse control	HD pulse and FD pulse control by time constant of CR	
③ Pin	HD pulse output	1/2 f_H killer HD pulse output	In a period of vertical synchronizing, a f_H is converted to f_H
④ Pin ⑤ Pin ⑥ Pin	AFC Oscillation	Oscillation of 503KHz by a ceramic oscillator, and divided by 32 to get down to 15.74KHz	
⑦ Pin	AFC control	Lag Lead filter for phase detection	
⑧ Pin	V_{CC}	V_{CC}	
⑨ Pin	AFC HD output Switch (AFC HD pulse width adjustment)	The case that R is connected between 9pin and V_{CC}···Fixed output The case that R is connected between 9pin and GND···Adjustable AFC HD Delay Mode	high Resistance → Wide pulse width Low Resistance → Narrow pulse widh
⑩ Pin	AFC HD Delay adjustment	The case that R is connected between 9pin and GND···Adjustable AFC HD Delay output	High REsistance → Low Resistance →
⑪ Pin	GND	GND	
⑫ Pin	AFC HD output	AFC HD pulse output	Positive polarity
⑬ Pin	VD pulse width adjustment	VD pulse widh control by time constant of CR	
⑭ Pin	VD output	Vertical synchronizing signal output	Positive polarity
⑮ Pin	FD output	Field discriminating signal output	odd field → High Output even field → Low Output
⑯ Pin	C Sync. output	Composite Sync Signal output	Positive polarity

MEMO

[CAUTION]
The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.