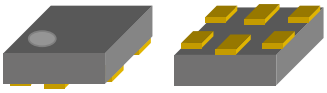
GPS LOW NOISE AMPLIFIER GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1143UA2 is a GPS LNA GaAs MMIC featured very samll size, low noise figure, high gain and low current consumpition. The NJG1143UA2 operates from 1.5V to 3.6V single voltage, has stand-by mode to save the supply current, and requires only three external components. The NJG1143UA2 has a on-chip ESD protection. The NJG1143UA2 is available in a very small, lead-free, halogen-free, 1.0mm x 1.0mm x 0.37 mm, 6-pin EPFFP6-A2 package.

■ PACKAGE OUTLINE



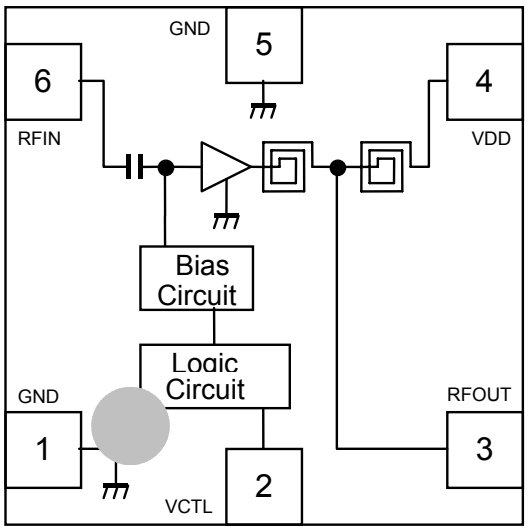
NJG1143UA2

■ FEATURES

● Low supply voltage	+2.85V typ.	(+1.5V~+3.6V)
● Low control voltage	+1.8V typ.	(+1.5V~+3.6V)
● Low current consumption	4.0mA typ.	@V_{DD}=2.85V, V_{CTL}=1.8V
	7μA typ.	@V_{DD}=2.85V, V_{CTL}=0V, Stand-by mode
● High gain	20.0dB typ.	@V_{DD}=2.85V, V_{CTL}=1.8V, f=1575MHz
● Low noise figure	0.70dB typ.	@V_{DD}=2.85V, V_{CTL}=1.8V, f=1575MHz
● Input power at 1dB gain compression point	-16.5dBm typ.	@V_{DD}=2.85V, V_{CTL}=1.8V, f=1575MHz
● High input IP3	-2.0dBm typ.	@V_{DD}=2.85V, V_{CTL}=1.8V, f=1575+1575.1MHz
● Stand-by function		
● Small package size	EPFFP-A2	(Package size: 1.0mmx1.0mmx0.37mm typ.)
● Integrated ESD protection circuit		
● Lead-free and halogen-free		

■ PIN CONFIGURATION

(Top View)



Pin Connection
1. GND
2. VCTL
3. RFOUT
4. VDD
5. GND
6. RFIN

■ TRUTH TABLE

"H"=V_{CTL}(H), "L"=V_{CTL}(L)

VCTL	LNA Mode
H	Active mode
L	Stand-by mode

Note: Specifications and description listed in this datasheet are subject to change without notice.

■ ABSOLUTE MAXIMUM RATINGS

T_a=+25°C, Z_s=Z_l=50Ω

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	V_{DD}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{IN}	V_{DD}=2.85V	+15	dBm
Power dissipation	P_D	4-layer FR4 PCB with through-hole (101.5mmx114.5mm), T_j=150°C	590	mW
Operating temperature	T_{opr}		-40~+85	°C
Storage temperature	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	VDD Terminal	1.5	-	3.6	V
Control Voltage (High)	$V_{CTL(H)}$	VCTL Terminal	1.5	1.8	3.6	V
Control Voltage (Low)	$V_{CTL(L)}$	VCTL Terminal	0	0	0.3	V
Supply Current 1	I_{DD1}	Active mode VDD Terminal V_{DD}=2.85V, V_{CTL}=1.8V	-	4.0	6.5	mA
Supply Current 2	I_{DD2}	Active mode VDD Terminal V_{DD}=1.8V, V_{CTL}=1.8V	-	3.0	4.7	mA
Supply Current 3	I_{DD3}	Stand-by mode VDD Terminal V_{DD}=2.85V, V_{CTL}=0V	-	7.0	15.0	μA
Supply Current 4	I_{DD4}	Stand-by mode VDD Terminal V_{DD}=1.8V, V_{CTL}=0V	-	4.0	10.0	μA
Control Current	I_{CTL}	$V_{CTL=}$1.8V, VCTL Terminal	-	5.0	12.0	μA

■ **ELECTRICAL CHARACTERISTICS 2 (RF, V_{DD}=2.85V)**

(General conditions: V_{DD}=2.85V, V_{CTL}=1.8V, Freq=1.575GHz,T_a=+25°C, Z_s=Z_l=50Ω, with application circuit)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Small Signal Gain 1	Gain1		17.5	20.0	22.0	dB
Noise Figure 1	NF1	Exclude PCB and connector Losses (0.08dB)	-	0.70	0.95	dB
Input Power at 1dB Gain Compression Point 1	P-1dB(IN)_1		-19.0	-16.5	-	dBm
Input 3rd Order Intercept Point 1	IIP3_1	f1=Freq f2=Freq+100kHz Pin=-34dBm	-6.0	-2.0	-	dBm
RF Input Port VSWR 1	$VSWR_i$1		-	1.5	2.0	
RF Output Port VSWR 1	$VSWR_o$1			1.5	2.0	

■ **ELECTRICAL CHARACTERISTICS 3 (RF, V_{DD}=1.8V)**

(General conditions: V_{DD}=1.8V, V_{CTL}=1.8V, Freq=1.575GHz,T_a=+25°C, Z_s=Z_l=50Ω, with application circuit)

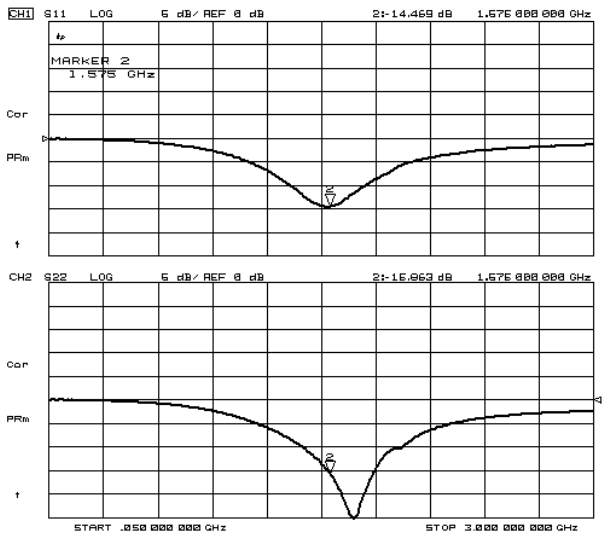
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Small Signal Gain 2	Gain2		16.5	19.0	21.0	dB
Noise Figure 2	NF2	Exclude PCB and connector Losses (0.08dB)	-	0.75	1.10	dB
Input Power at 1dB Gain Compression Point 2	P-1dB(IN)_2		-22.0	-19.5	-	dBm
Input 3rd Order Intercept Point 2	IIP3_2	f1=Freq f2=Freq+100kHz Pin=-34dBm	-10.0	-6.0	-	dBm
RF Input Port VSWR 2	$VSWR_i$2		-	1.5	2.3	
RF Output Port VSWR 2	$VSWR_o$2			1.3	1.7	

■ TERMINAL INFORMATION

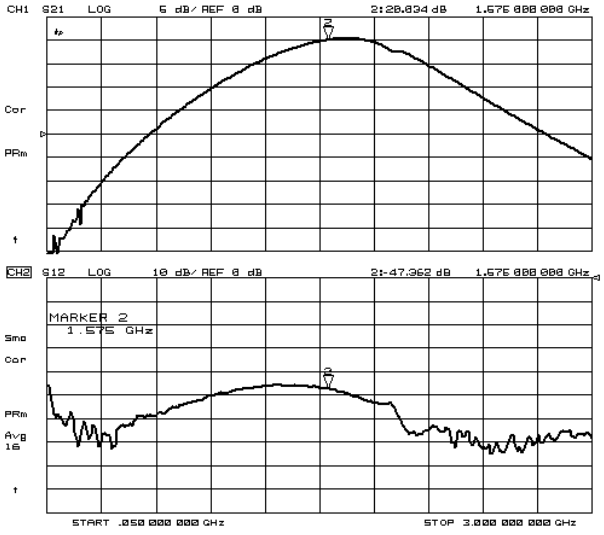
No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. These terminals should be connected to the ground plane as close as possible for excellent RF performance.
2	VCTL	Control voltage terminal. Inputting a logic-high, the LNA turn at LNA active mode. Inputting a logic-low, the LNA turn at stand-by mode.
3	RFOUT	RF output terminal. Requires an external capacitor C1. The capacitor C1 is not only a matching component , but also a DC blocking capacitor.
4	VDD	Supply voltage terminal. Bypass to ground with capacitor C2 as close as possible to the IC.
5	GND	Ground terminal. These terminals should be connected to the ground plane as close as possible for excellent RF performance.
6	RFIN	RF input terminal. Requires a maching inductor L1. Integrated a DC blocking capaciotr.

■ ELECTRICAL CHARACTERRISTICS

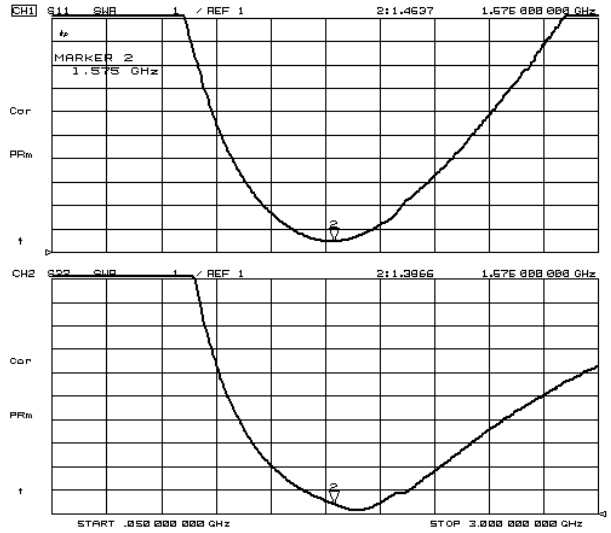
Conditions: V_{DD}=2.85V, V_{CTL}=1.8V, Ta=+25°C, Zs=Zl=50Ω, with application circuit



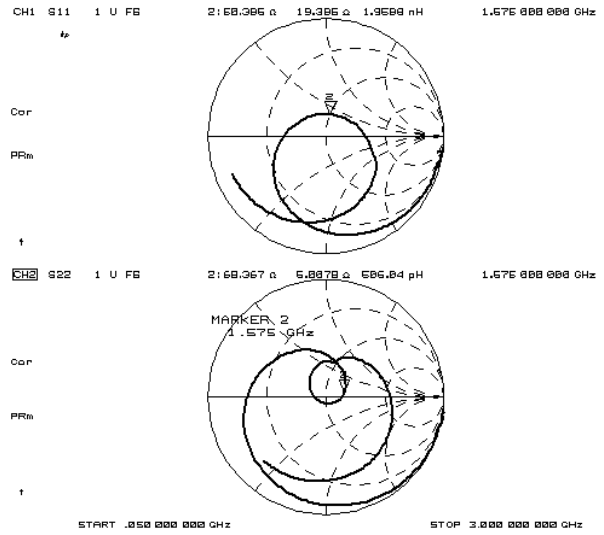
S11, S22



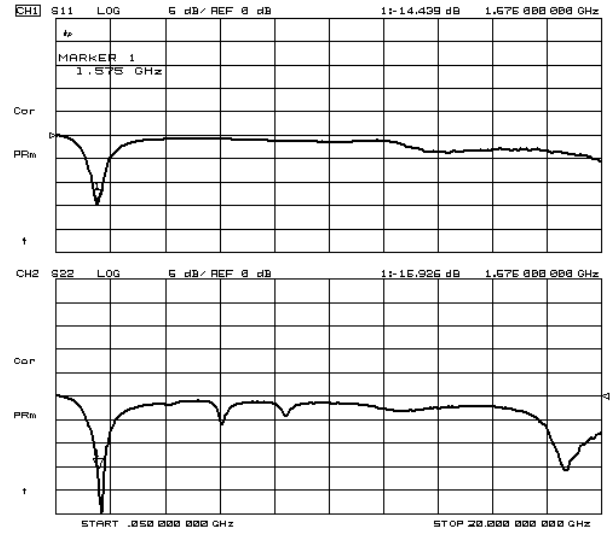
S21, S12



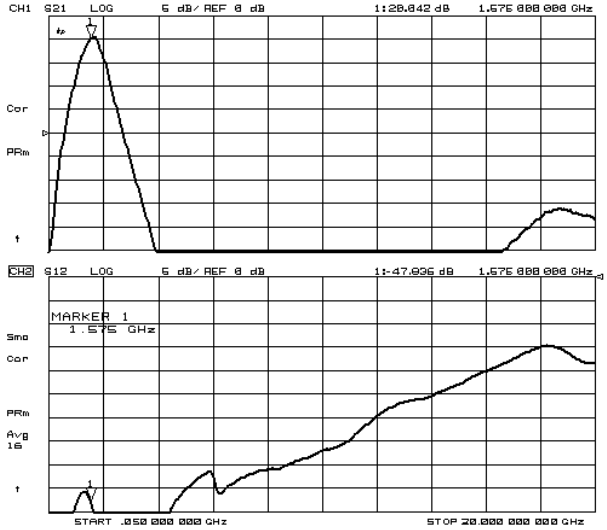
VSWR



Zin, Zout



S11, S22 (f=50MHz~20GHz)



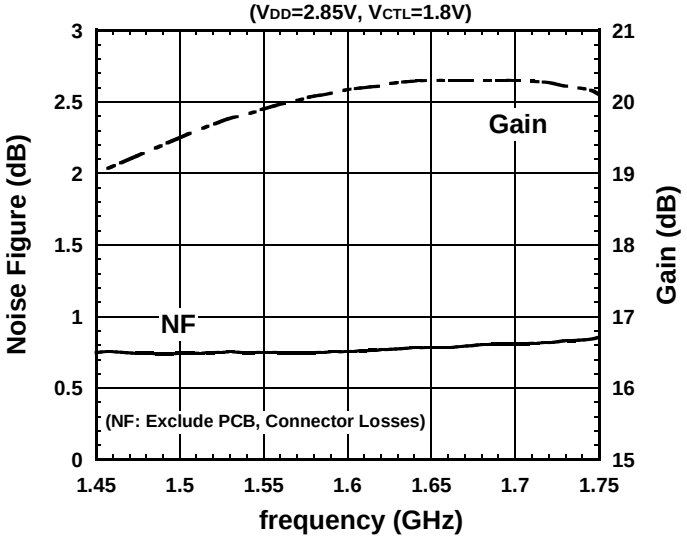
S21, S12 (f=50MHz~20GHz)

■ ELECTRICAL CHARACTERRISTICS

Conditions: V_{DD}=2.85V, V_{CTL}=1.8V, Ta=+25°C, Zs=Zl=50Ω, with application circuit

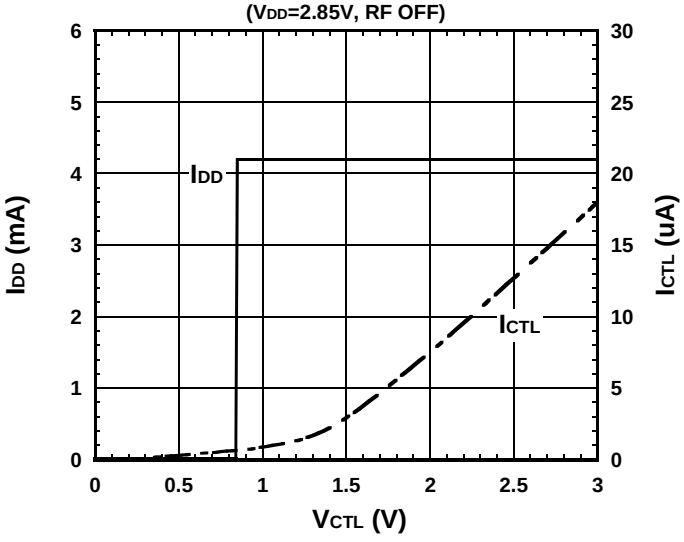
NF, Gain vs. frequency

(V_{DD}=2.85V, V_{CTL}=1.8V)



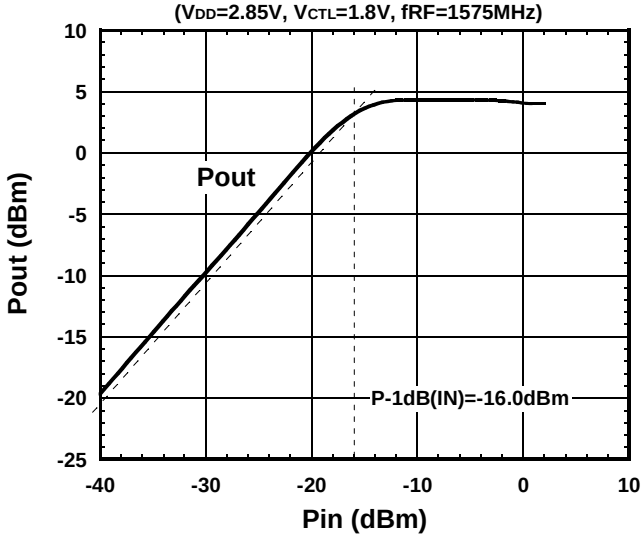
IDD, ICTL vs. VCTL

(V_{DD}=2.85V, RF OFF)



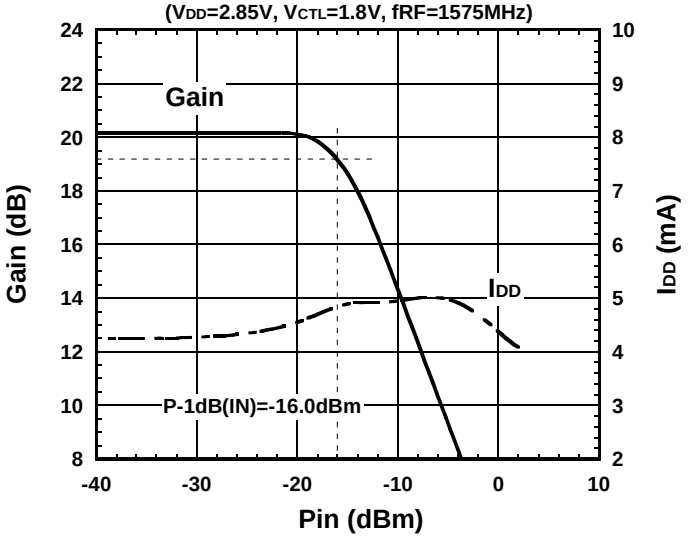
Pout vs. Pin

(V_{DD}=2.85V, V_{CTL}=1.8V, fRF=1575MHz)



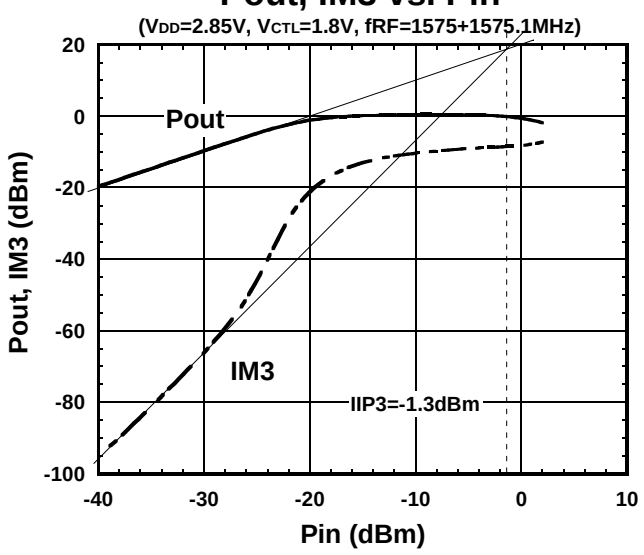
Gain, IDD vs. Pin

(V_{DD}=2.85V, V_{CTL}=1.8V, fRF=1575MHz)



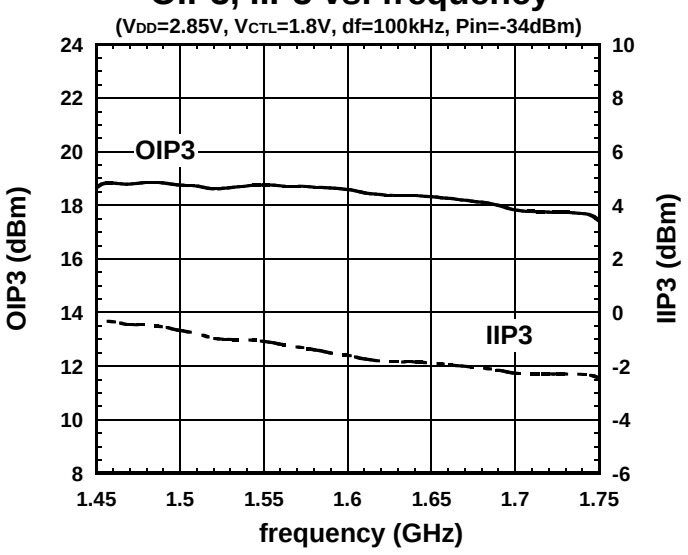
Pout, IM3 vs. Pin

(V_{DD}=2.85V, V_{CTL}=1.8V, fRF=1575+1575.1MHz)



OIP3, IIP3 vs. frequency

(V_{DD}=2.85V, V_{CTL}=1.8V, df=100kHz, Pin=-34dBm)

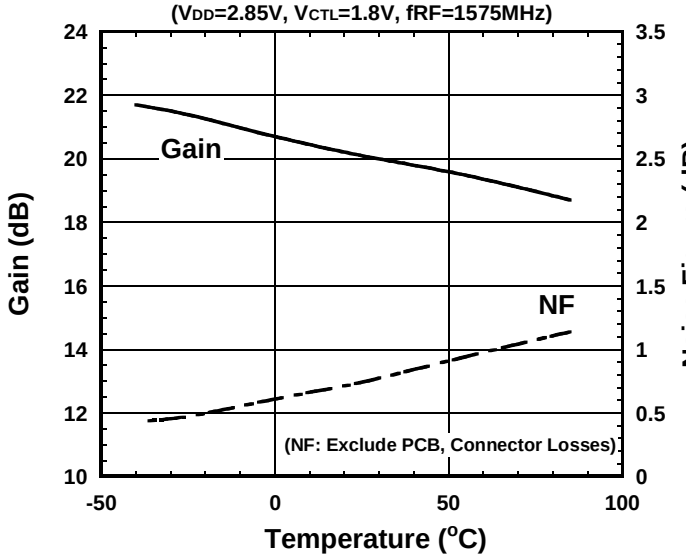


■ ELECTRICAL CHARACTERRISTICS

Conditions: V_{DD}=2.85V, V_{CTL}=1.8V, Ta=+25°C, Zs=Zl=50Ω, with application circuit

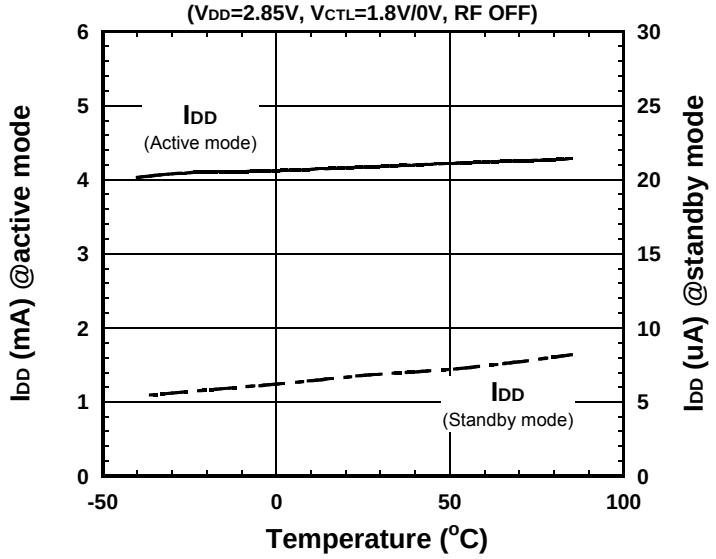
Gain, NF vs. Temperature

(VDD=2.85V, VCTL=1.8V, fRF=1575MHz)



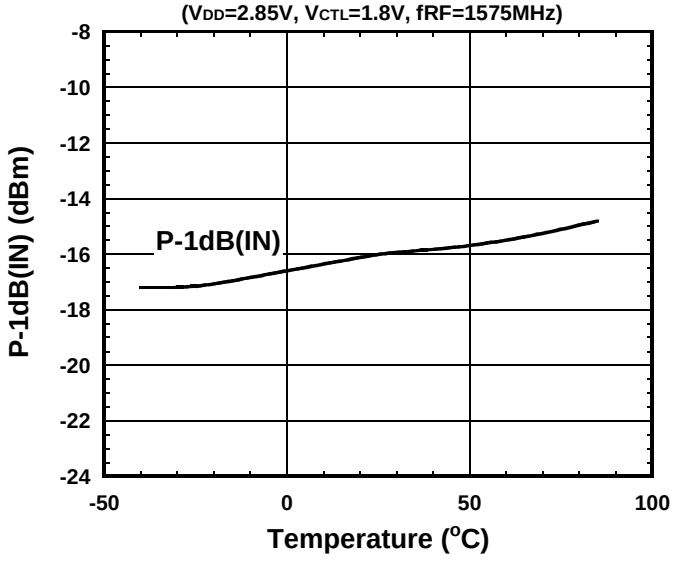
IDD vs. Temperature

(VDD=2.85V, VCTL=1.8V/0V, RF OFF)



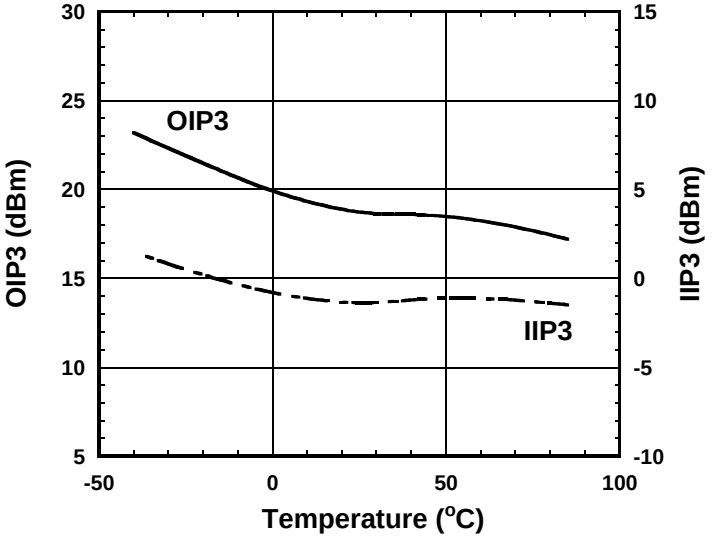
P-1dB(IN) vs. Temperature

(VDD=2.85V, VCTL=1.8V, fRF=1575MHz)



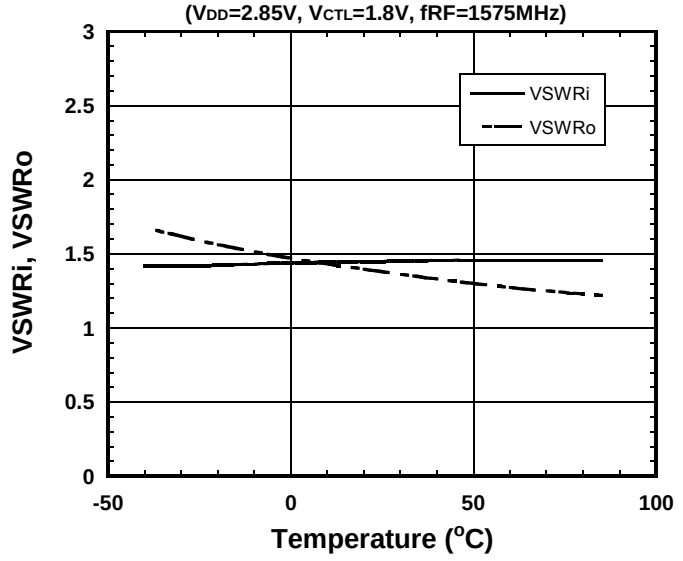
OIP3, IIP3 vs. Temperature

(VDD=2.85V, VCTL=1.8V, fRF=1575+1575.1MHz, Pin=-34dBm)



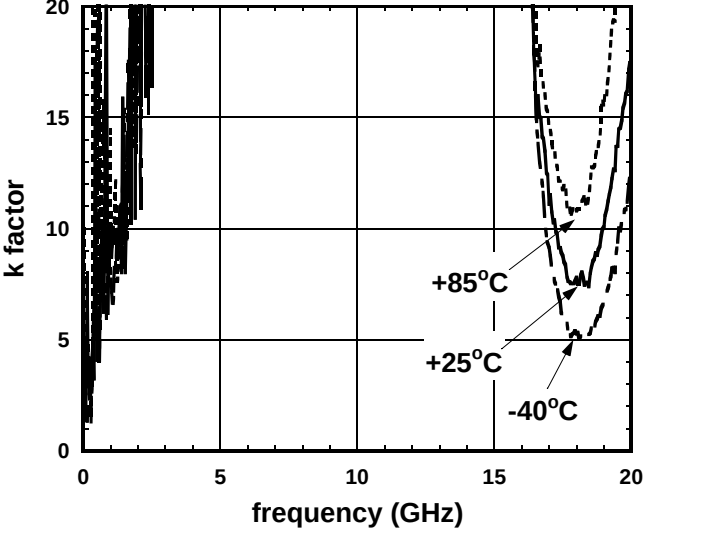
VSWR vs. Temperature

(VDD=2.85V, VCTL=1.8V, fRF=1575MHz)



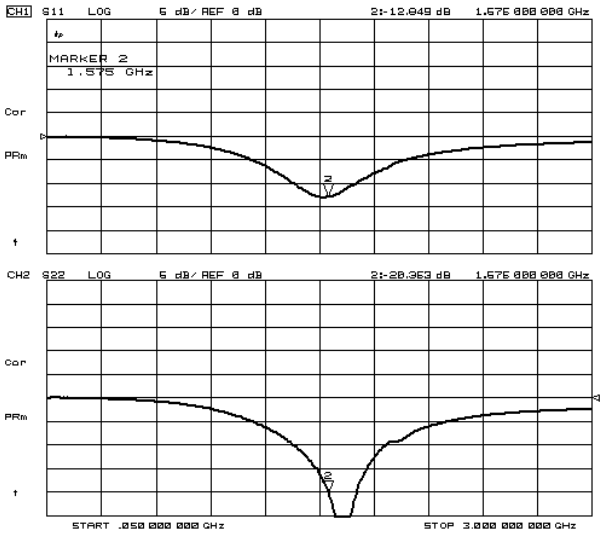
k factor vs. frequency

(VDD=2.85V, VCTL=1.8V)

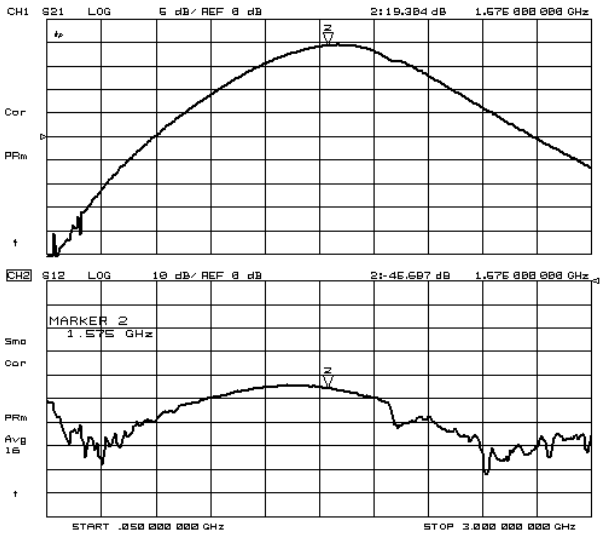


■ ELECTRICAL CHARACTERRISTICS

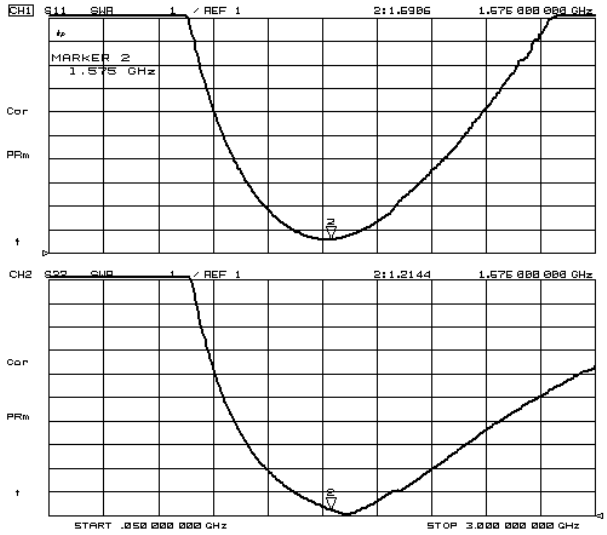
Conditions: V_{DD}=1.8V, V_{CTL}=1.8V, Ta=+25°C, Zs=Zl=50Ω, with application circuit



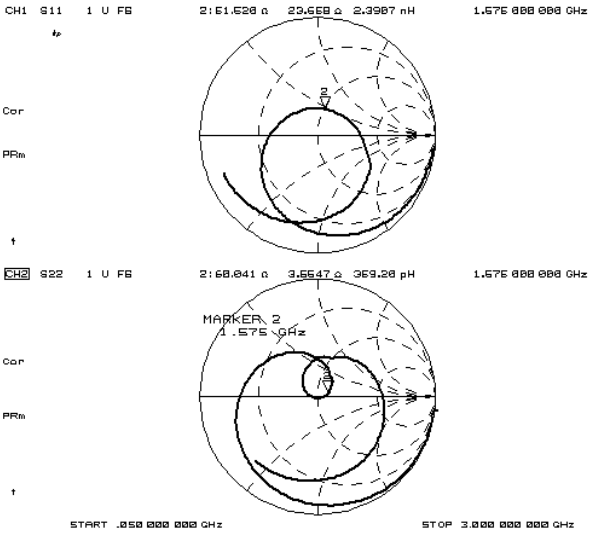
S11, S22



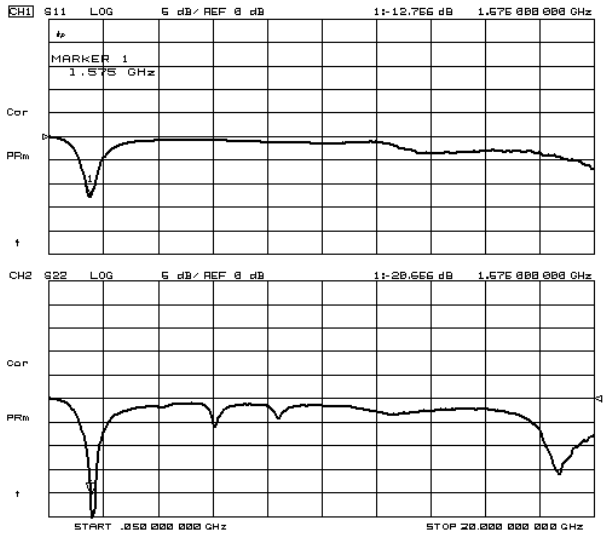
S21, S12



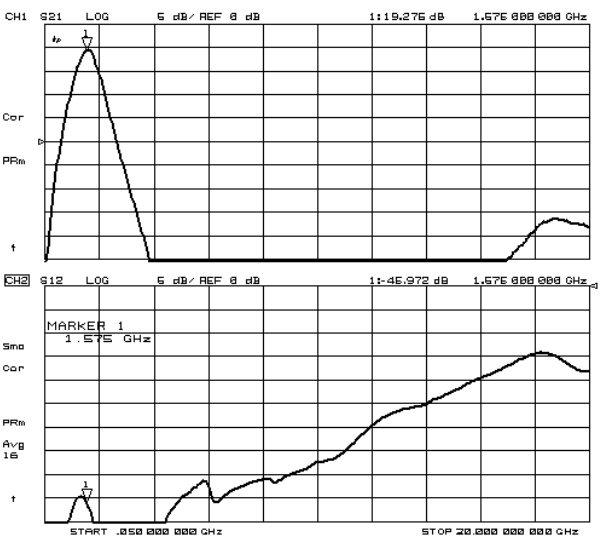
VSWR



Zin, Zout



S11, S22 (f=50MHz~20GHz)



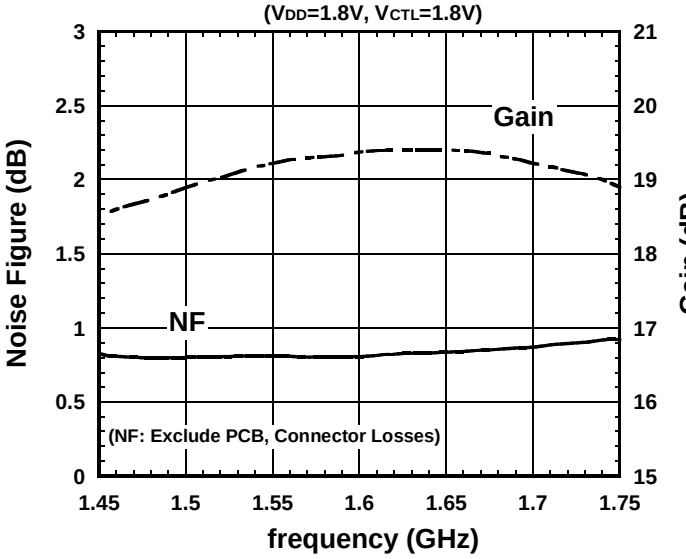
S21, S12 (f=50MHz~20GHz)

■ ELECTRICAL CHARACTERRISTICS

Conditions: V_{DD}=1.8V, V_{CTL}=1.8V, Ta=+25°C, Zs=Zl=50Ω, with application circuit

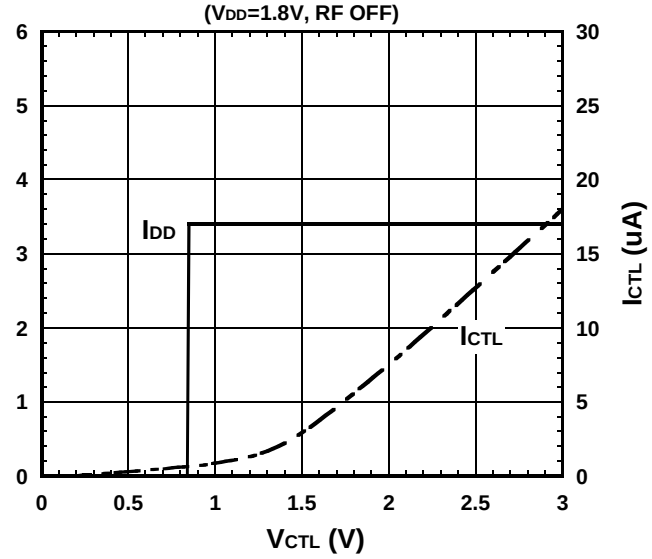
NF, Gain vs. frequency

(VDD=1.8V, VCTL=1.8V)



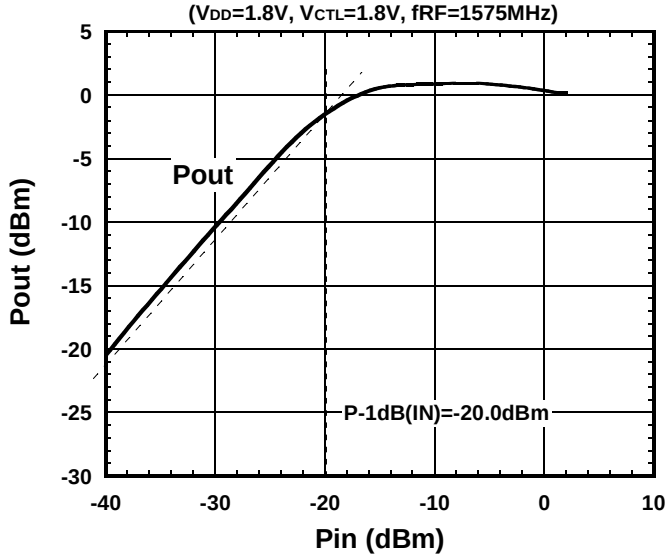
IDD, ICTL vs. VCTL

(VDD=1.8V, RF OFF)



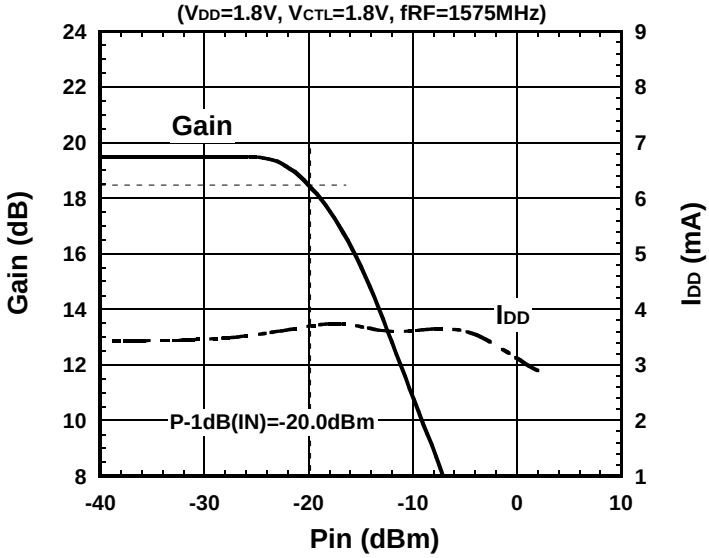
Pout vs. Pin

(VDD=1.8V, VCTL=1.8V, fRF=1575MHz)



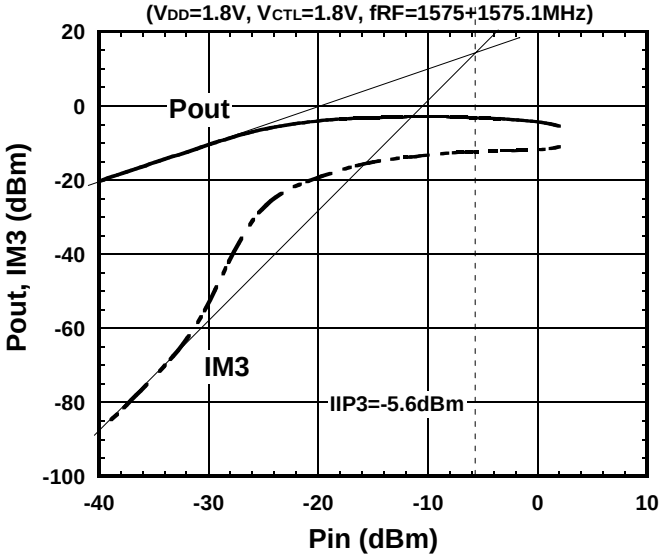
Gain, IDD vs. Pin

(VDD=1.8V, VCTL=1.8V, fRF=1575MHz)



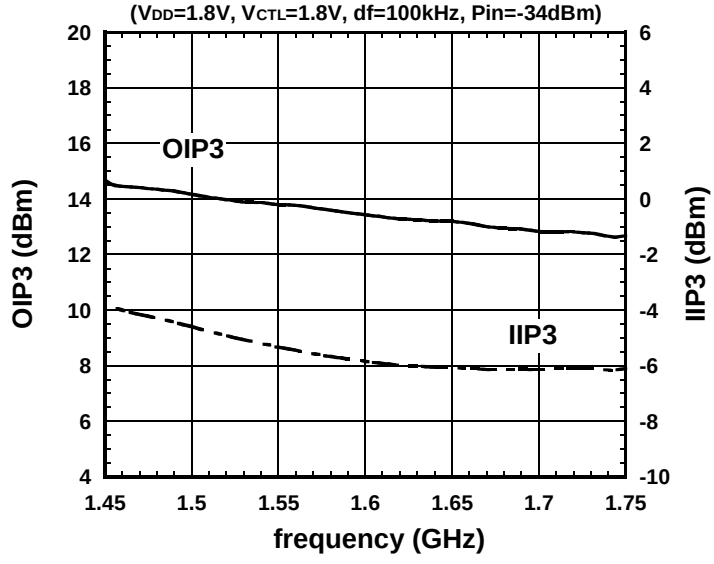
Pout, IM3 vs. Pin

(VDD=1.8V, VCTL=1.8V, fRF=1575+1575.1MHz)



OIP3, IIP3 vs. frequency

(VDD=1.8V, VCTL=1.8V, df=100kHz, Pin=-34dBm)

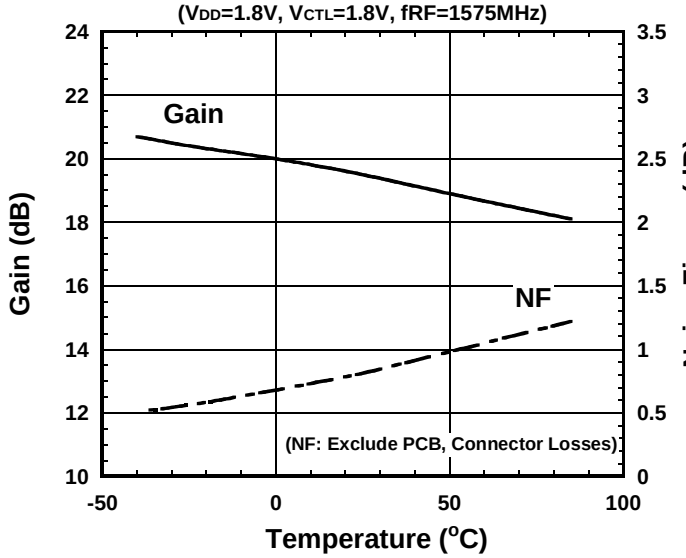


■ ELECTRICAL CHARACTERRISTICS

Conditions: V_{DD}=1.8V, V_{CTL}=1.8V, Zs=Zl=50Ω, with application circuit

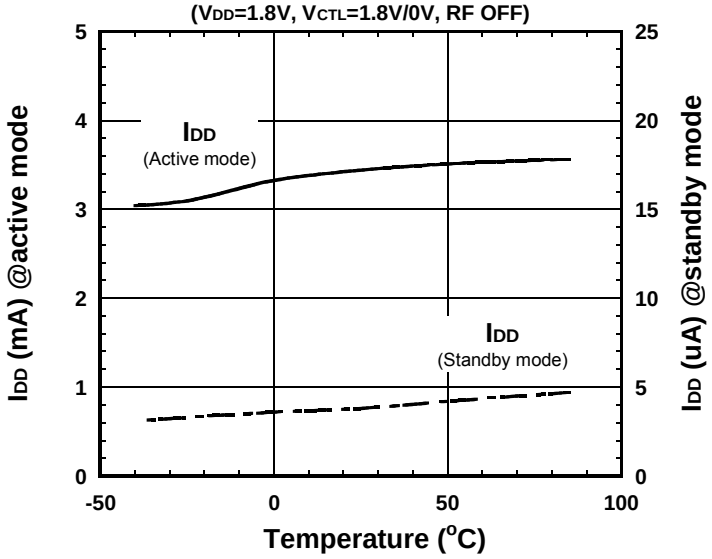
Gain, NF vs. Temperature

(V_{DD}=1.8V, V_{CTL}=1.8V, fRF=1575MHz)



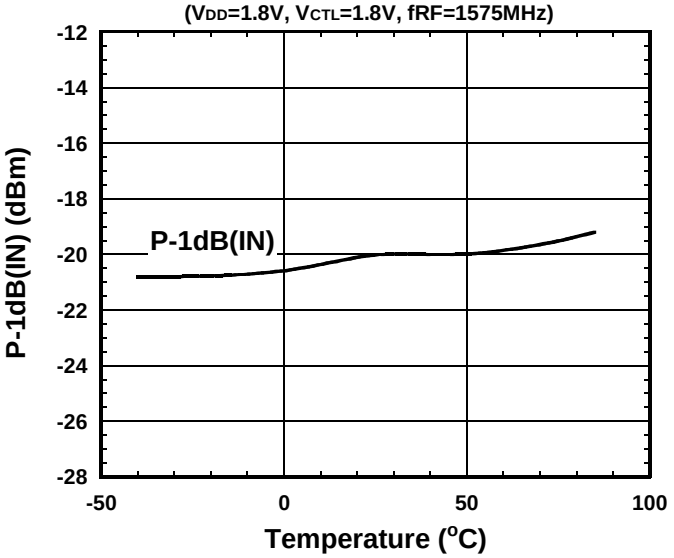
IDD vs. Temperature

(V_{DD}=1.8V, V_{CTL}=1.8V/0V, RF OFF)



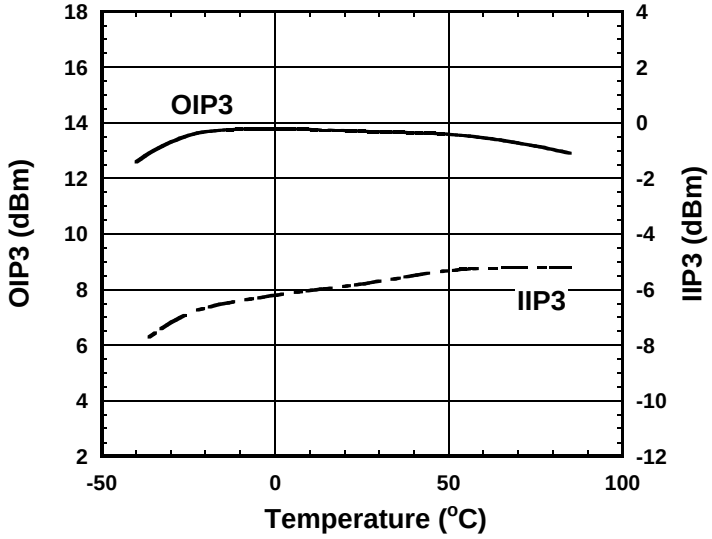
P-1dB(IN) vs. Temperature

(V_{DD}=1.8V, V_{CTL}=1.8V, fRF=1575MHz)



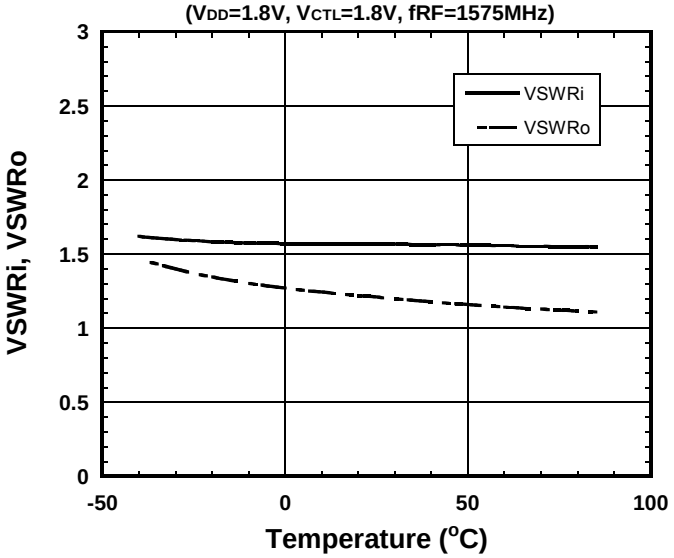
OIP3, IIP3 vs. Temperature

(V_{DD}=1.8V, V_{CTL}=1.8V, fRF=1575+1575.1MHz, Pin=-34dBm)



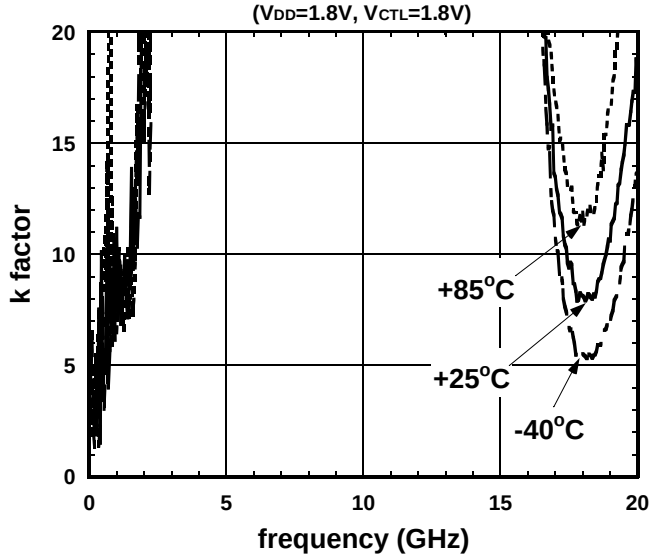
VSWR vs. Temperature

(V_{DD}=1.8V, V_{CTL}=1.8V, fRF=1575MHz)



k factor vs. frequency

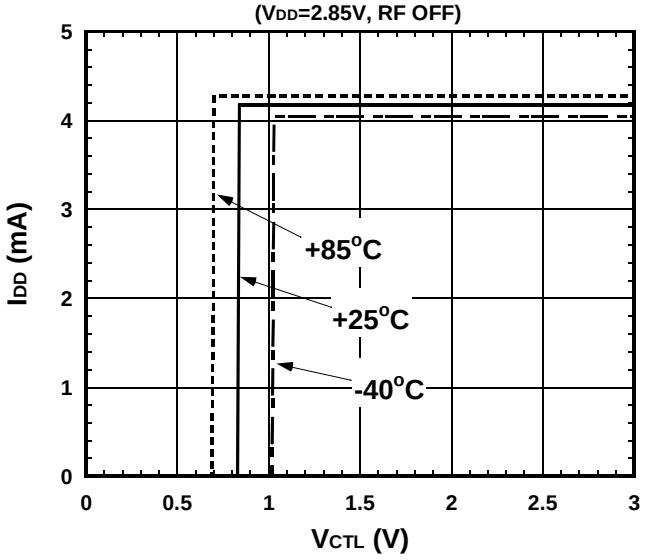
(V_{DD}=1.8V, V_{CTL}=1.8V)



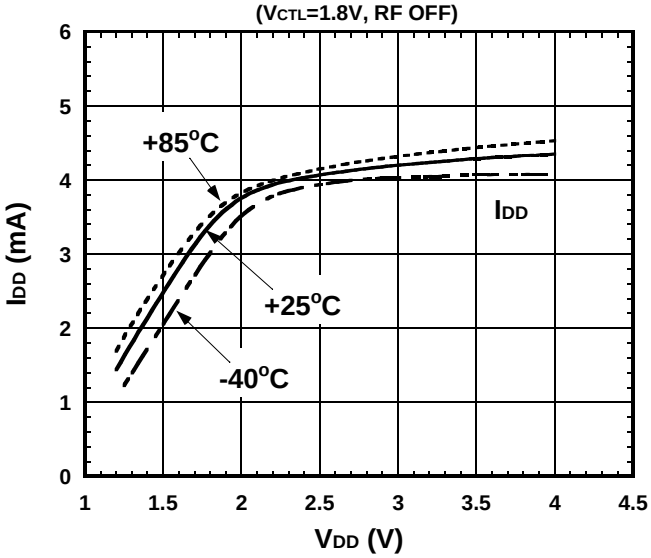
■ ELECTRICAL CHARACTERRISTICS

Conditions: RF OFF, Zs=Zl=50Ω, with application circuit

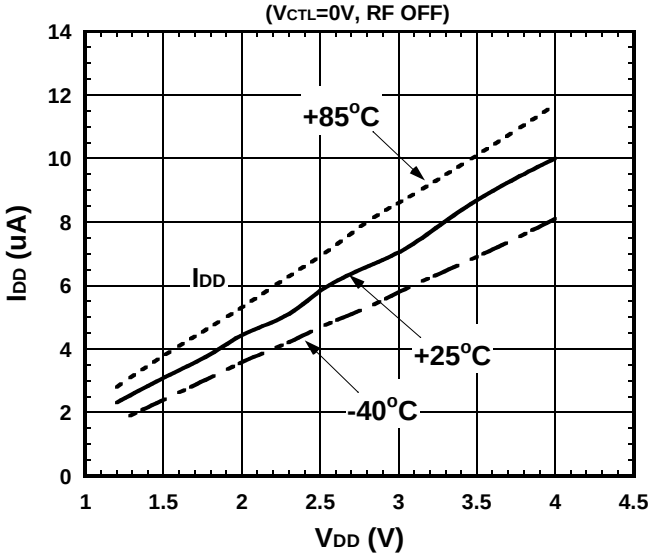
IDD vs. VCTL
(VDD=2.85V, RF OFF)



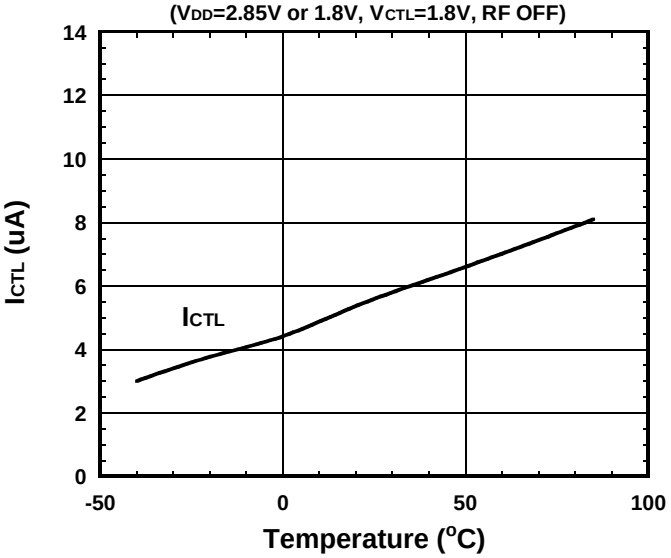
IDD vs. VDD
(VCTL=1.8V, RF OFF)



IDD vs. VDD
(VCTL=0V, RF OFF)



ICTL vs. Temperature
(VDD=2.85V or 1.8V, VCTL=1.8V, RF OFF)

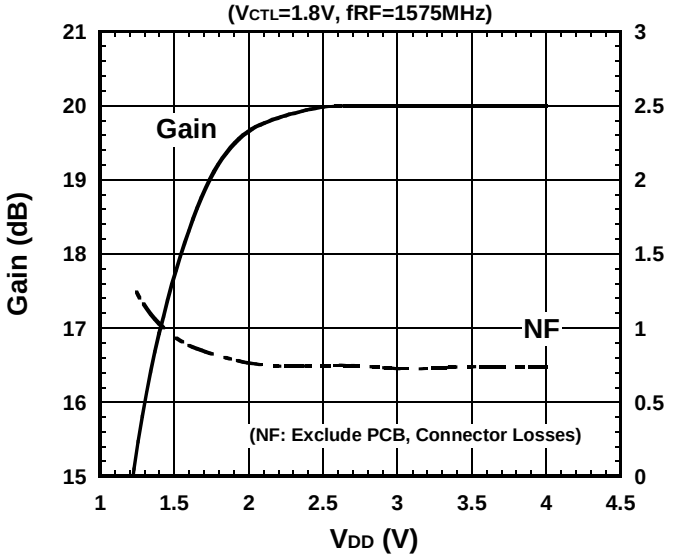


■ ELECTRICAL CHARACTERRISTICS

Condition: V_{CTL}=1.8V, Ta=+25°C, Zs=Zl=50Ω, with application circuit

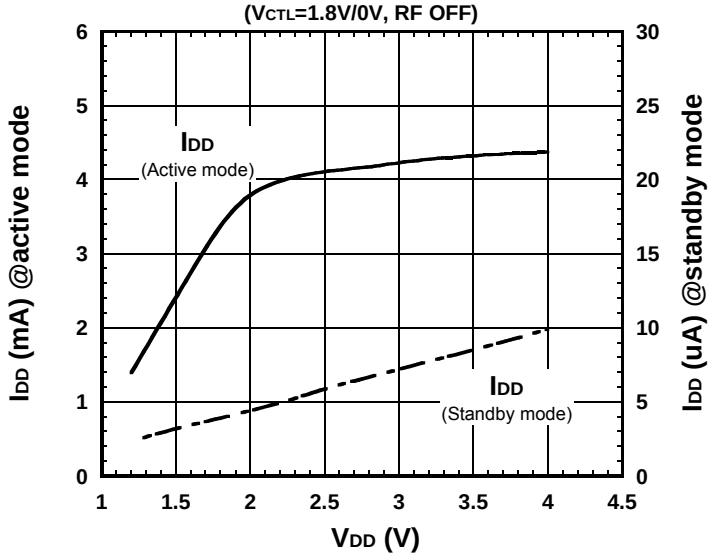
Gain, NF vs. VDD

(VCTL=1.8V, fRF=1575MHz)



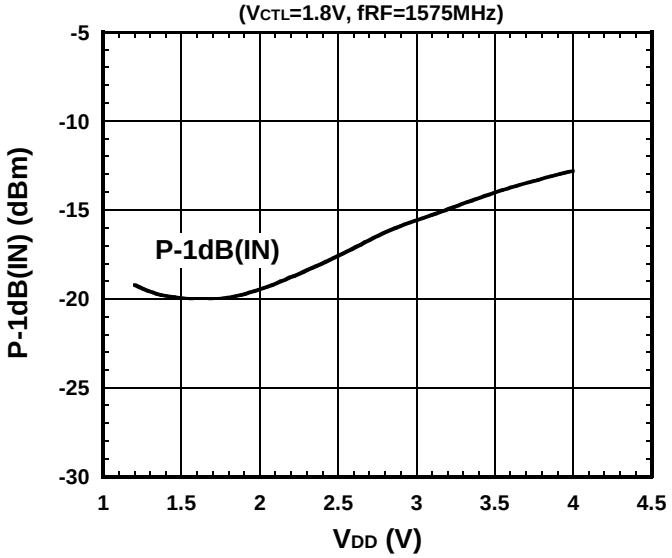
IDD vs. VDD

(VCTL=1.8V/0V, RF OFF)



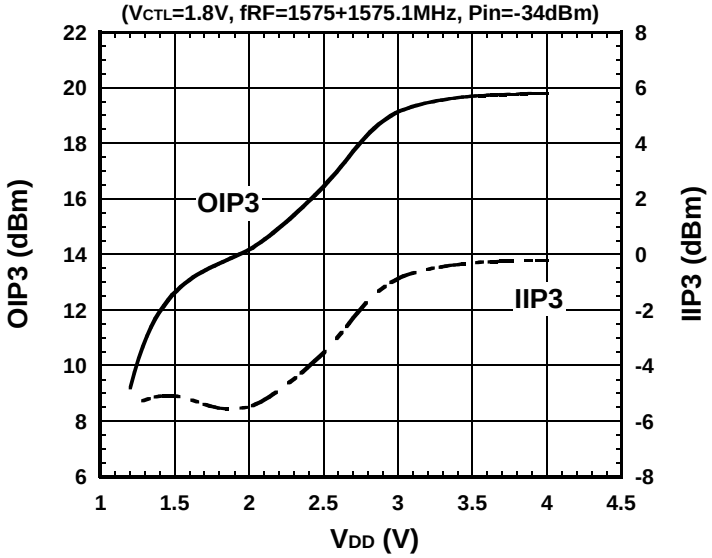
P-1dB(IN) vs. VDD

(VCTL=1.8V, fRF=1575MHz)



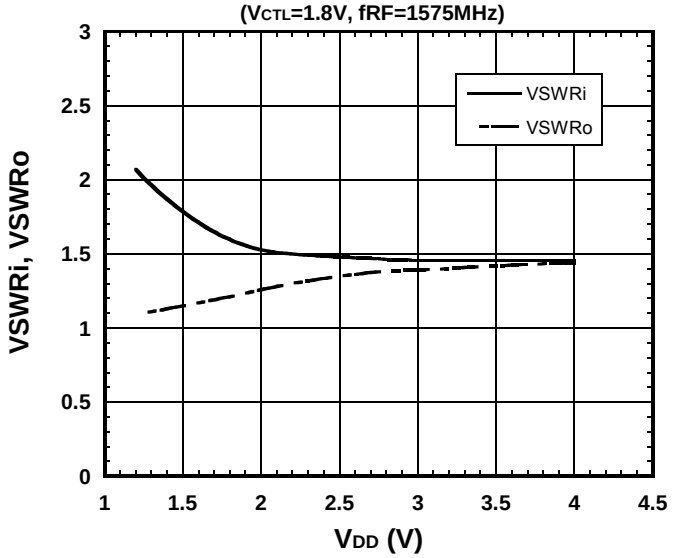
OIP3, IIP3 vs. VDD

(VCTL=1.8V, fRF=1575+1575.1MHz, Pin=-34dBm)



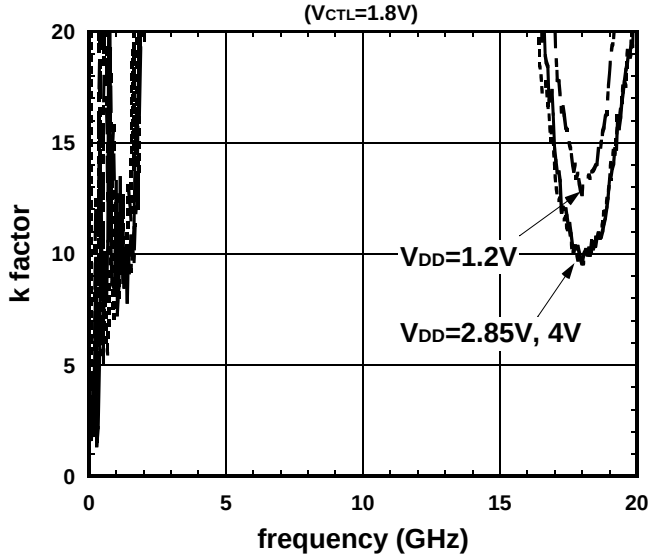
VSWR vs. VDD

(VCTL=1.8V, fRF=1575MHz)

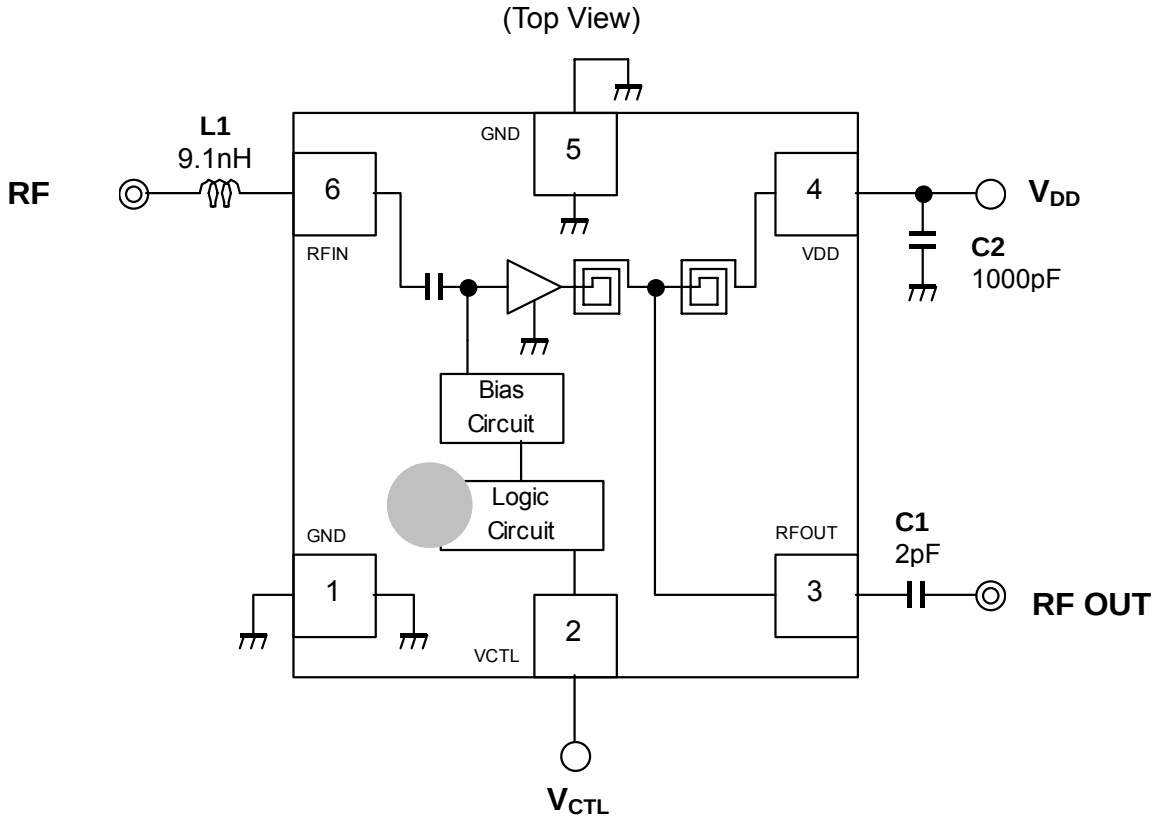


k factor vs. frequency

(VCTL=1.8V)



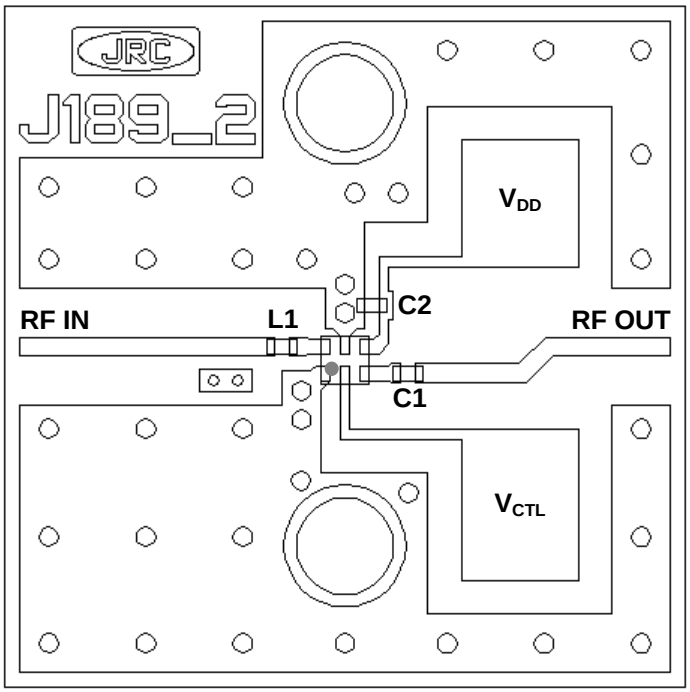
■ APPLICATION CIRCUIT



- L1 is an iutput matching inductor.
- C1 is an output matching capacitor and a DC blocking capacitor.
- C2 is a bypass capacitor.

■ TEST PCB LAYOUT

(Top View)



Parts list

Parts ID	Manufacture
L1	LQP03T_02 Series (MURATA)
C1, C2	GRM03 Series (MURATA)

PCB
Substrate: FR-4
Thickness: 0.2mm
Microstrip line width: 0.4mm (Z_0=50Ω)
Size: 14.0mm x 14.0mm

■ NOISE FIGURE MEASUREMENT CONDITONS

Measuring instruments

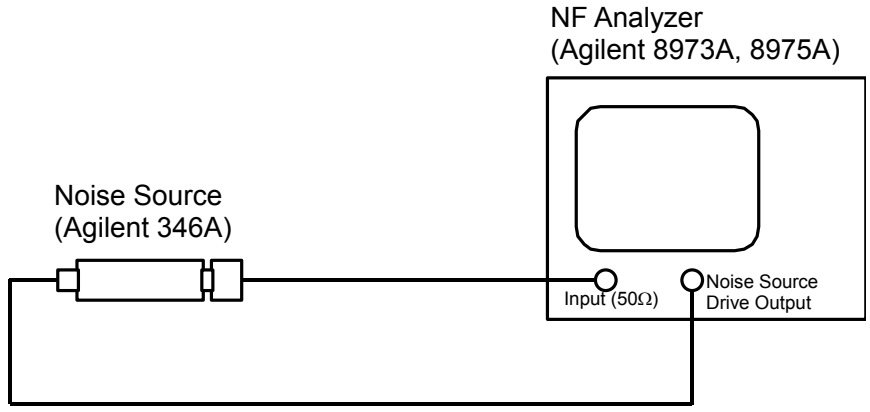
NF Analyzer : Agilent 8973A, 8975A
Noise Source : Agilent 346A

Setting the NF analyzer

Measurement mode form
- Device under test : Amplifier
- System downconverter : off

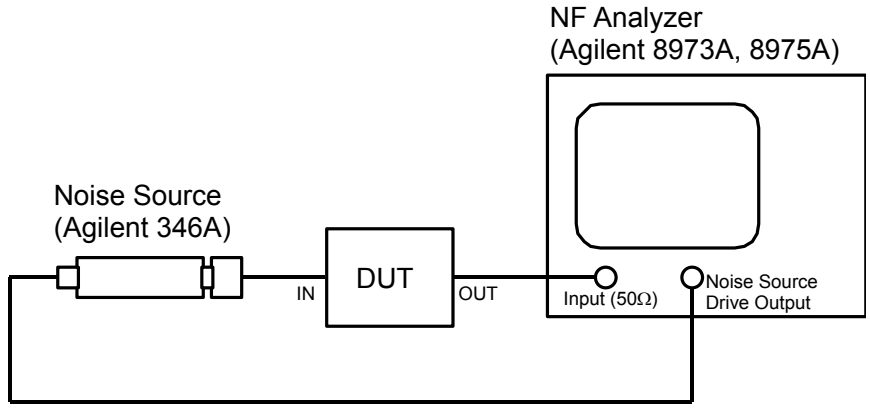
Mode setup form
- Sideband : LSB

Averages : 16
Average mode : Point
Bandwidth : 4MHz
Loss comp : off
Tcold : setting the temperature of noise source (303.15K)



* Noise source and NF analyzer are connected directly.

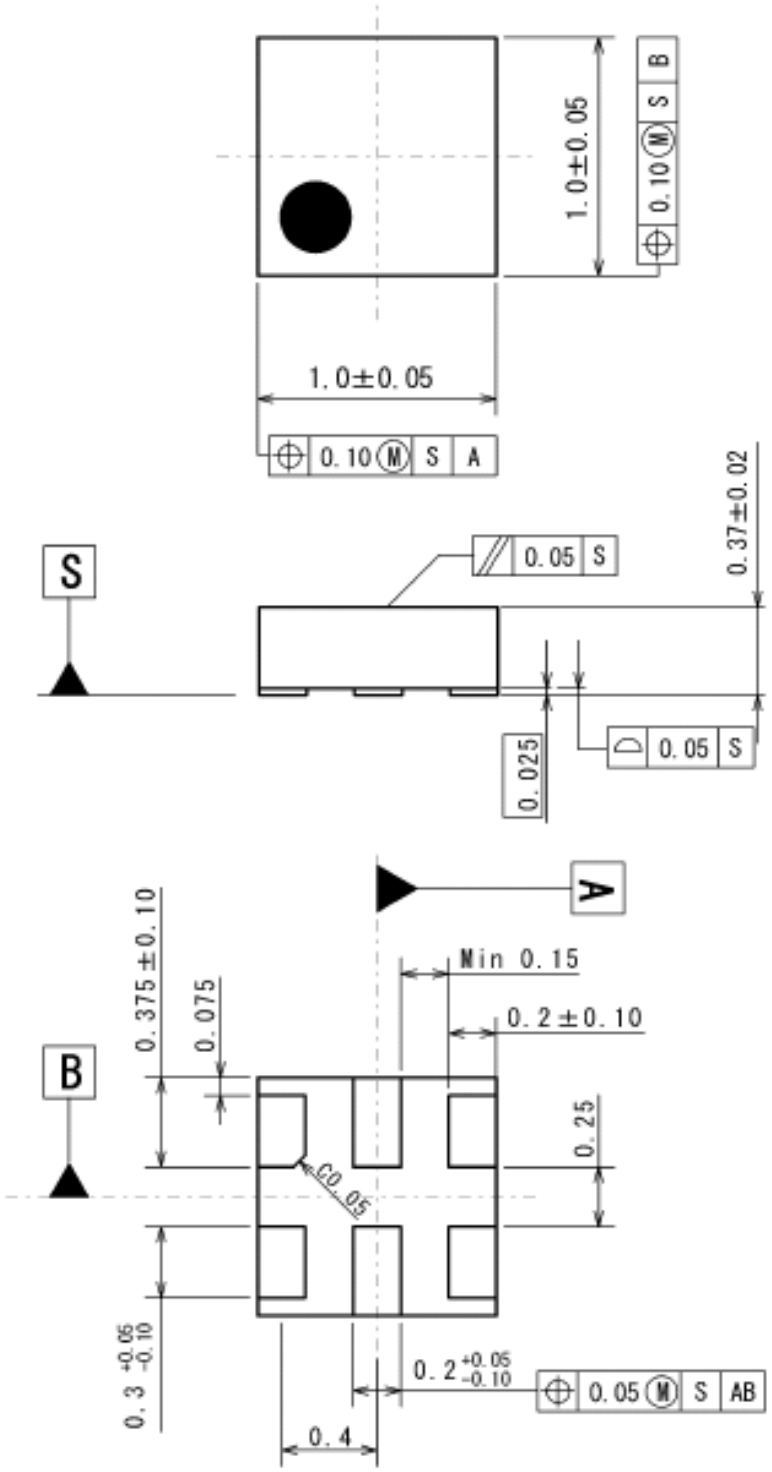
Calibration Setup



* Noise source and DUT, DUT and NF analyzer are connected directly.

Measurement Setup

■ PACKAGE OUTLINE (EPFFP6-A2)



Unit	: mm
Substrate	: FR4
Terminal treat	: Au
Molding material	: Epoxy resin
Weight (typ.)	: 0.855mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.