

NID5001N

Self-Protected FET with Temperature and Current Limit

HDPlus devices are an advanced series of power MOSFETs which utilize ON Semiconductor's latest MOSFET technology process to achieve the lowest possible on-resistance per silicon area while incorporating smart features. Integrated thermal and current limits work together to provide short circuit protection. The devices feature an integrated Drain-to-Gate Clamp that enables them to withstand high energy in the avalanche mode. The Clamp also provides additional safety margin against unexpected voltage transients. Electrostatic Discharge (ESD) protection is provided by an integrated Gate-to-Source Clamp.

Features

- Low $R_{DS(on)}$
- Current Limitation
- Thermal Shutdown with Automatic Restart
- Short Circuit Protection
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Slew Rate Control for Low Noise Switching
- Overvoltage Clamped Protection
- Pb-Free Package is Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	42	Vdc
Drain-to-Gate Voltage Internally Clamped ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	42	Vdc
Gate-to-Source Voltage	V_{GS}	± 14	Vdc
Drain Current – Continuous	I_D	Internally Limited	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2)	P_D	64 1.0 1.56	W
Thermal Resistance, Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.95 120 80	$^\circ\text{C/W}$
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 25\text{ Vdc}$, $V_{GS} = 5.0\text{ Vdc}$, $I_L = 4.5\text{ Apk}$, $L = 120\text{ mH}$, $R_G = 25\text{ }\Omega$)	E_{AS}	1215	mJ
Operating and Storage Temperature Range	T_J , T_{stg}	-55 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR4 PCB, steady state.
2. Mounted onto a 2" square FR4 board
(1" square, 2 oz. Cu 0.06" thick single-sided, $t = \text{steady state}$).

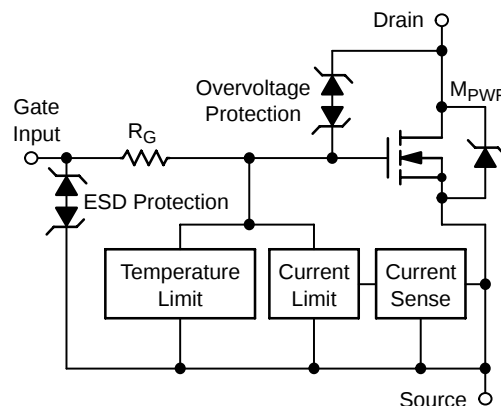


ON Semiconductor®

<http://onsemi.com>

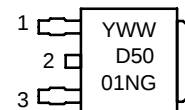
V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX (Limited)
42 V	23 m Ω @ 10 V	33 A*

*Max current may be limited below this value depending on input conditions.



DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM



Y = Year
WW = Work Week
D5001N = Device Code
G = Pb-Free Package

1 = Gate
2 = Drain
3 = Source

ORDERING INFORMATION

Device	Package	Shipping†
NID5001NT4	DPAK	2500/Tape & Reel
NID5001NT4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NID5001N

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Clamped Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) (V _{GS} = 0 Vdc, I _D = 250 μAdc, T _J = 150°C)	V _{(BR)DSS}	42 42	46 44	50 50	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 32 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 32 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}		1.5 6.5	5.0	μAdc
Gate Input Current (V _{GS} = 5.0 Vdc, V _{DS} = 0 Vdc)	I _{GSSF}		50	100	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.2 mAdc) Threshold Temperature Coefficient	V _{GS(th)}	1.0	1.8 5.0	2.0	Vdc -mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 5.0 Adc, T _J @ 25°C) (V _{GS} = 10 Vdc, I _D = 5.0 Adc, T _J @ 150°C)	R _{DS(on)}		23 43	29 55	mΩ
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 5.0 Vdc, I _D = 5.0 Adc, T _J @ 25°C) (V _{GS} = 5.0 Vdc, I _D = 5.0 Adc, T _J @ 150°C)	R _{DS(on)}		28 50	34 60	mΩ
Source-Drain Forward On Voltage (I _S = 5 A, V _{GS} = 0 V)	V _{SD}		0.80	1.1	V

SWITCHING CHARACTERISTICS

Turn-on Time	V _{GS} = 5.0 Vdc, V _{DD} = 25 Vdc I _D = 1.0 Adc, Ext R _G = 2.5 Ω	T _(on)		32	40	μs
Turn-off Time		T _(off)		68	75	
Turn-on Time	V _{GS} = 10 Vdc, V _{DD} = 25 Vdc, I _D = 1.0 Adc, Ext R _G = 2.5 Ω	T _(on)		11	15	
Turn-off Time		T _(off)		86	95	
Slew Rate On	R _L = 4.7 Ω, V _{in} = 0 to 10 V, V _{DD} = 12 V	-dV _{DS} /dt _{on}		0.5		V/μs
Slew-Rate Off	R _L = 4.7 Ω, V _{in} = 10 to 0 V, V _{DD} = 12 V	dV _{DS} /dt _{off}		0.35		V/μs

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Current Limit	(V _{GS} = 5.0 Vdc) V _{DS} = 10 V (V _{GS} = 5.0 Vdc, T _J = 150°C)	I _{LIM}	21 12	30 19	36 30	Adc
	(V _{GS} = 10 Vdc) V _{DS} = 10 V (V _{GS} = 10 Vdc, T _J = 150°C)		29 13	41 24	49 31	
Temperature Limit (Turn-off)	V _{GS} = 5.0 Vdc	T _{LIM(off)}	150	175	200	°C
Temperature Limit (Circuit Reset)	V _{GS} = 5.0 Vdc	T _{LIM(on)}	135	160	185	°C
Temperature Limit (Turn-off)	V _{GS} = 10 Vdc	T _{LIM(off)}	150	165	185	°C
Temperature Limit (Circuit Reset)	V _{GS} = 10 Vdc	T _{LIM(on)}	135	150	170	°C

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electro-Static Discharge Capability Human Body Model (HBM) Machine Model (MM)	ESD	4000 400			V
---	-----	-------------	--	--	---

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL PERFORMANCE CURVES

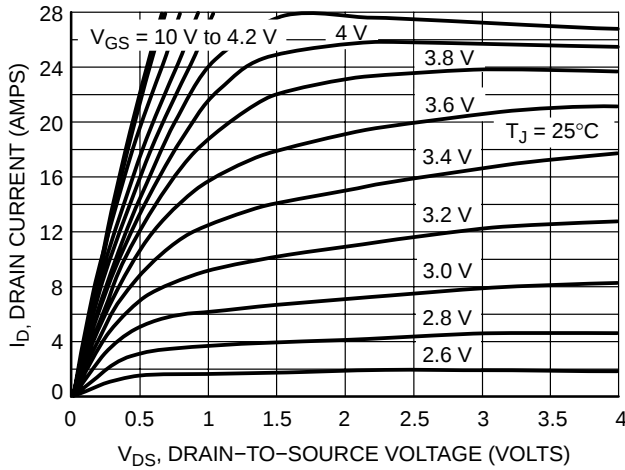


Figure 1. On-Region Characteristics

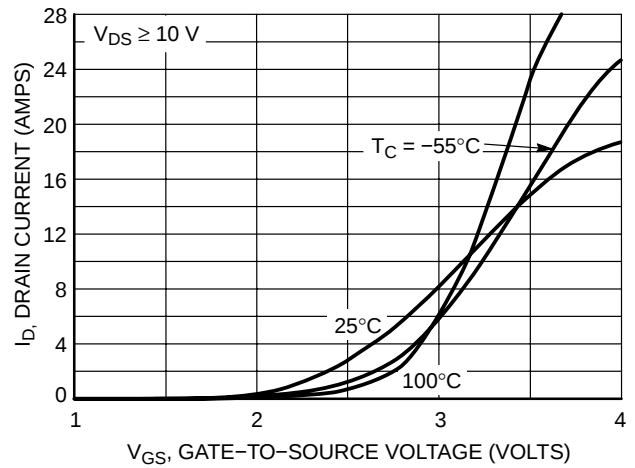


Figure 2. Transfer Characteristics

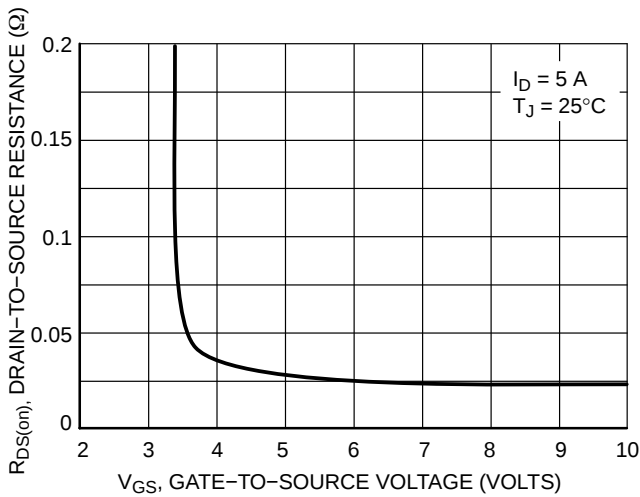


Figure 3. On-Resistance vs. Gate-to-Source Voltage

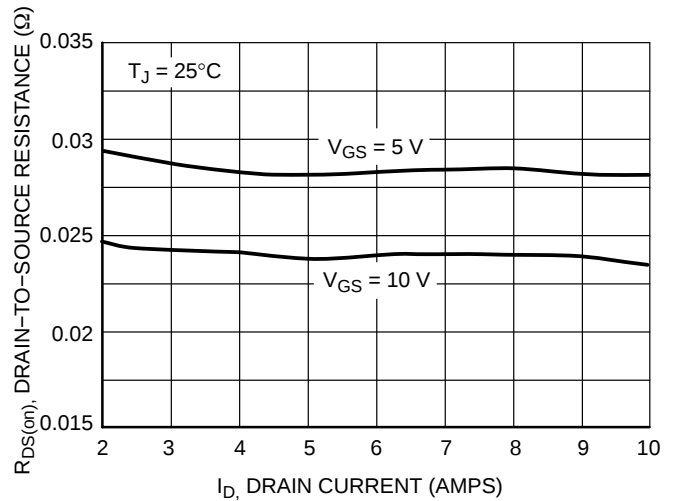


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

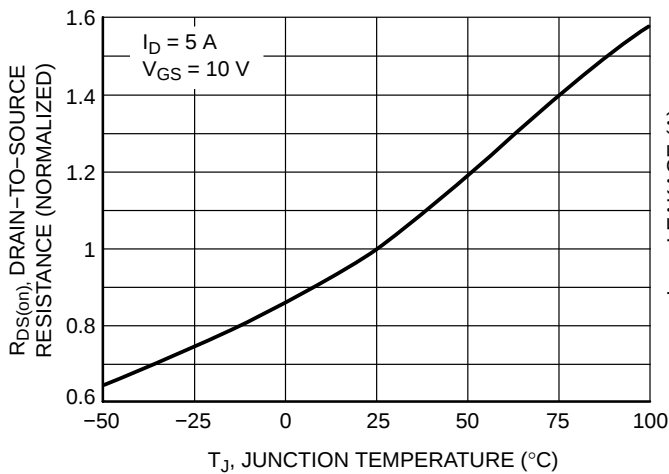


Figure 5. On-Resistance Variation with Temperature

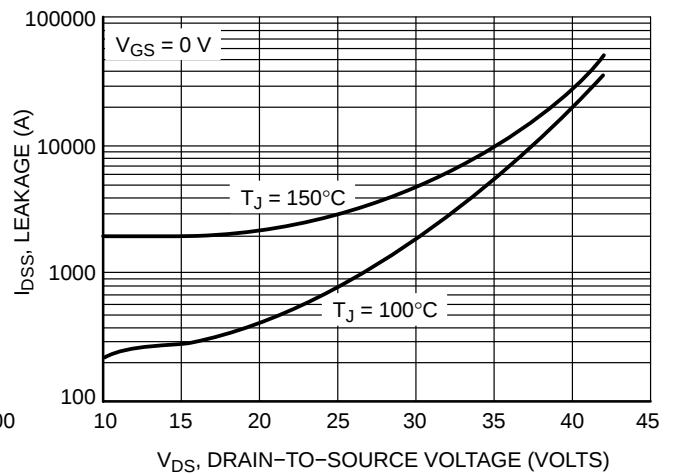


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

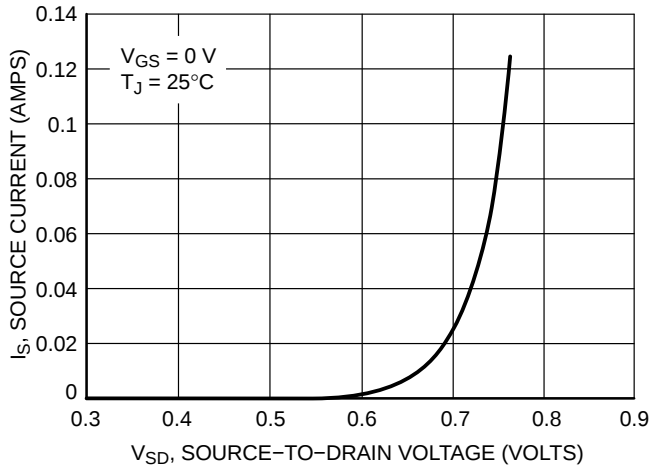


Figure 7. Diode Forward Voltage vs. Current

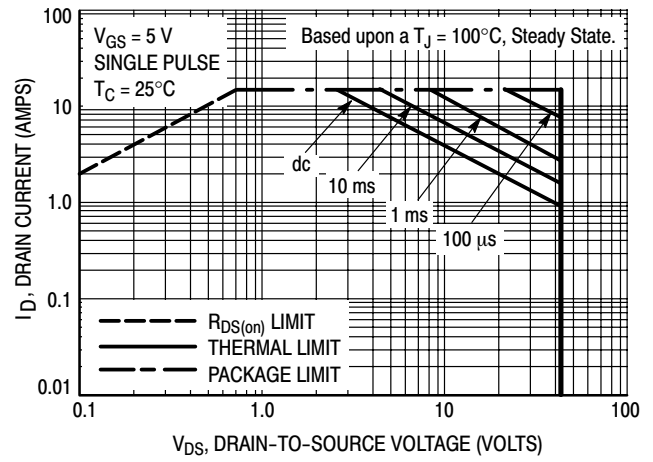
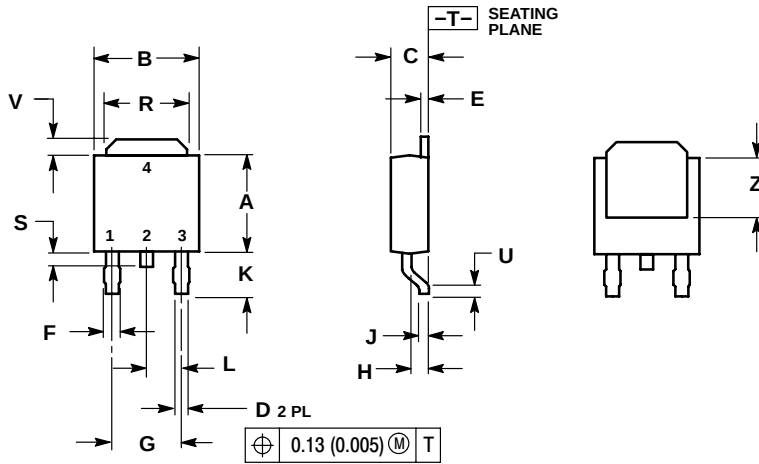


Figure 8. Maximum Rated Forward Biased Safe Operating Area

NID5001N

PACKAGE DIMENSIONS

DPAK CASE 369C-01 ISSUE O

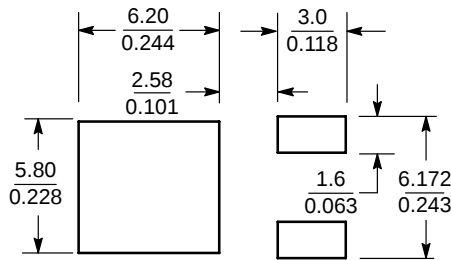


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.