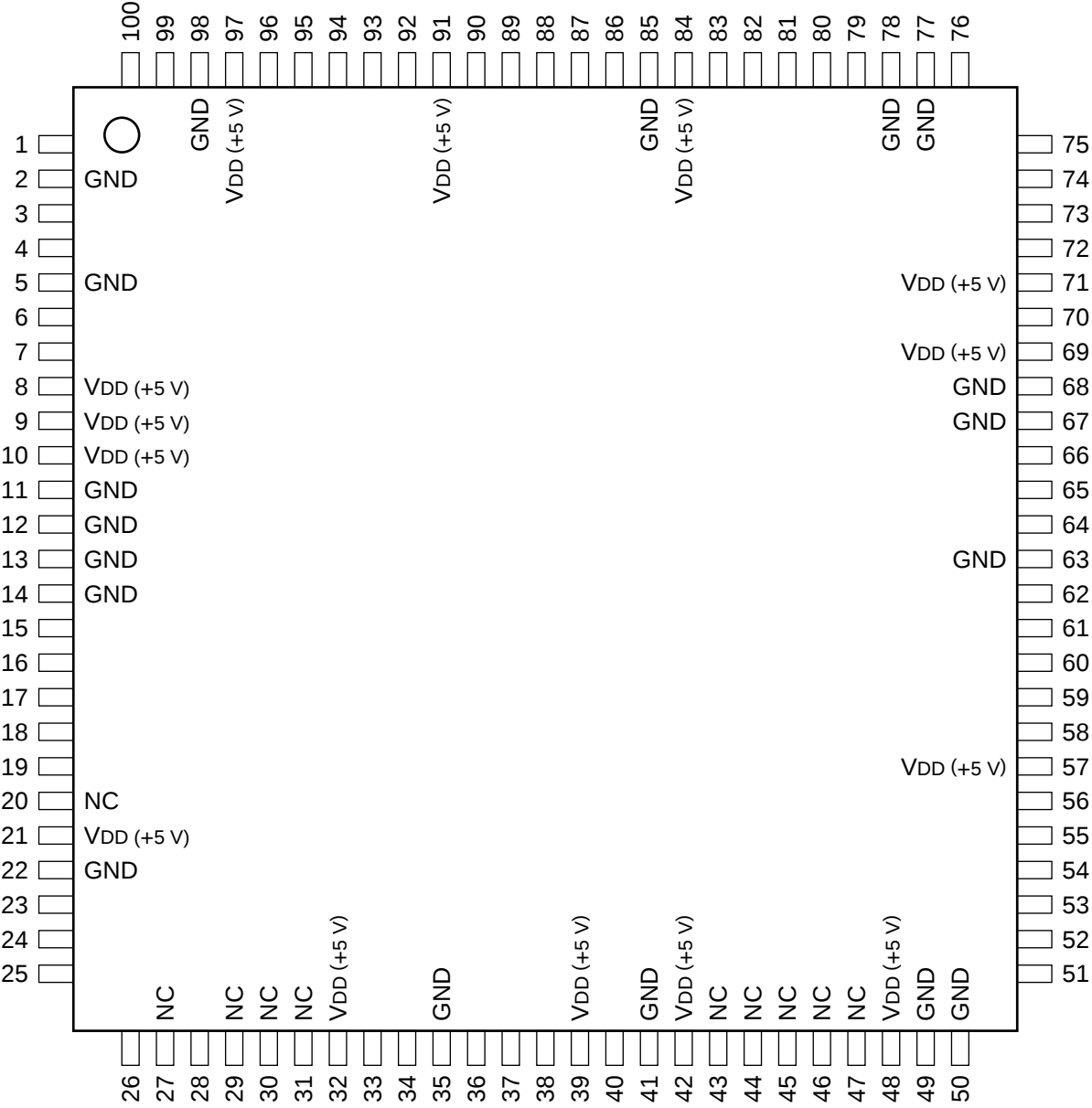
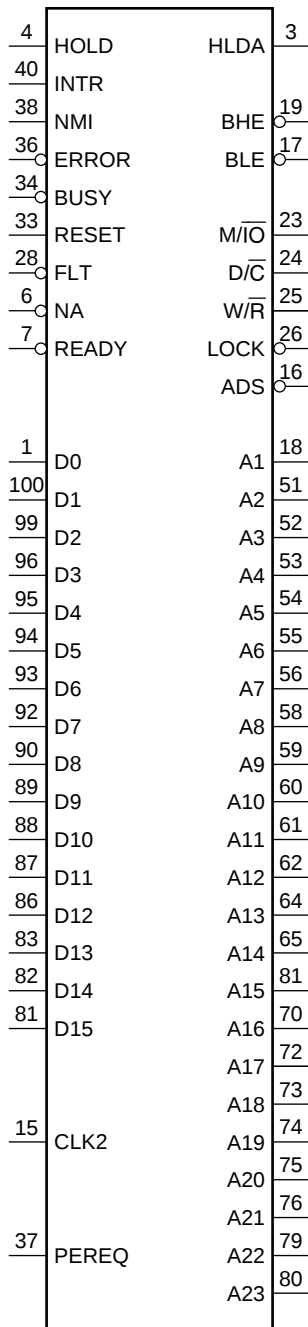


C-MOS 32-BIT MICROPROCESSOR
—TOP VIEW—



(V_{DD} = +5.5 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	DO	26	O	LOCK	51	O	A2	76	O	A21
2	—	GND	27	—	NC	52	O	A3	77	—	GND
3	O	HLDA	28	I	FLT	53	O	A4	78	—	GND
4	I	HOLD	29	—	NC	54	O	A5	79	O	A22
5	—	GND	30	—	NC	55	O	A6	80	O	A23
6	I	NA	31	—	NC	56	O	A7	81	I/O	D15
7	I	READY	32	—	V _{DD}	57	—	V _{DD}	82	I/O	D14
8	—	V _{DD}	33	I	RESET	58	O	A8	83	I/O	D13
9	—	V _{DD}	34	I	BUSY	59	O	A9	84	—	V _{DD}
10	—	V _{DD}	35	—	GND	60	O	A10	85	—	GND
11	—	GND	36	I	ERROR	61	O	A11	86	I/O	D12
12	—	GND	37	I	PEREQ	62	O	A12	87	I/O	D11
13	—	GND	38	I	NMI	63	—	GND	88	I/O	D10
14	—	GND	39	—	V _{DD}	64	O	A13	89	I/O	D9
15	I	CLK2	40	I	INTR	65	O	A14	90	I/O	D8
16	O	ADS	41	—	GND	66	O	A15	91	—	V _{DD}
17	O	BLE	42	—	V _{DD}	67	—	GND	92	I/O	D7
18	O	A1	43	—	NC	68	—	GND	93	I/O	D6
19	O	BHE	44	—	NC	69	—	V _{DD}	94	I/O	D5
20	—	NC	45	—	NC	70	O	A16	95	I/O	D4
21	—	V _{DD}	46	—	NC	71	—	V _{DD}	96	I/O	D3
22	—	GND	47	—	NC	72	O	A17	97	—	V _{DD}
23	O	M/IO	48	—	V _{DD}	73	O	A18	98	—	GND
24	O	D/C	49	—	GND	74	O	A19	99	I/O	D2
25	O	W/R	50	—	GND	75	O	A20	100	I/O	D1

**INPUT**

BUSY : BUSY SIGNALS
 CLK2 : CLOCK2
 ERROR : ERROR SIGNALS
 FLT : FLOAT SIGNALS
 HOLD : BUS HOLD REQUEST
 INTR : INTERRUPT REQUEST
 NA : NEXT ADDRESS
 NMI : NON-MASKABLE INTERRUPT REQUEST
 PEREQ : PROCESSOR EXTENSION REQUEST
 READY : BUS READY
 RESET : RESET STATE

OUTPUT

A1 - A23 : ADDRESS BUS
 ADS : ADDRESS STATUS
 BLE : BYTE ENABLE
 BHE : BYTE ENABLE
 D/ $\overline{\text{C}}$: DATA/CONTROL
 HLDA : BUS HOLD ACKNOWLEDGE
 LOCK : BUS LOCK
 M/ $\overline{\text{IO}}$: MEMORY I/O
 W/ $\overline{\text{R}}$: WRITE/READ

INPUT/OUTPUT

D0 - D15 : DATA BUS

