NEX91207-Q100

Automotive 70 mA, 40 V tracking LDO with 5 mV tracking tolerance

Rev. 1 — 12 February 2025 Product data sheet

1. General description

The NEX91207-Q100 is a Low-Dropout (LDO) voltage-tracking regulator with a precise tracking tolerance of 5 mV (max) and excellent load and line transient responses. It is specifically designed to power off-board sensors in automotive applications such as power train systems, safety, and Body Control Modules (BCMs). The device supports a wide input voltage range from 4 V to 40 V (up to 45 V transient) to withstand cold-crank and load-dump transient conditions.

The device output tracks the reference voltage applied to the ADJ/EN pin with an accuracy of ±5 mV over the specified temperature range. The high tracking accuracy ensures a precise power supply for off-board sensors and modules, improving the performance of radiometric sensors such as pressure and position sensors.

The device switches to standby mode by pulling down the ADJ/EN pin, which enables an ultra-low shutdown current of 0.75 μA typical to extend battery life. The device integrates protection features such as battery reverse polarity protection (-42 V), output reverse current protection, output short-to-battery and ground protection, current limit, and thermal shutdown. These protections guard against the high risk of cable failures in an off-board power system.

The device operates across a temperature range from -40 °C to 125 °C ambient and -40 °C to 150 °C junction. It is available in two package options with different thermal resistance, including SOT8105-1 (SOT23-5S) and SOT8104-1 (SOT23-5).

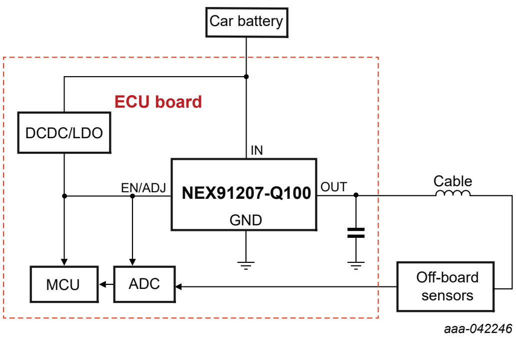


Fig. 1. Typical application

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Temperature grade 1 (T_{amb}): -40 °C to 125 °C
  - Junction temperature (T_j): -40 °C to 150 °C
- Input voltage range: 4 V to 40 V
  - Absolute maximum input range: -42 V to +45 V
- Wide output voltage range: 2 V to 40 V
  - Absolute maximum output range: -5 V to +45 V
- Tight output tracking tolerance: ±5 mV
- Maximum output current: 70 mA
- Low dropout voltage:
  - 215 mV typical at 70 mA (V_{OUT} = 5 V)
- Low quiescent current (I_Q):
  - 40 μA typical quiescent current at light loads
  - 0.75 μA typical shut-down current
- Active output discharge with a typical discharge current of 700 μA
- Stable with a wide range of ceramic output-stability cap:
  - ESR from 0.001 Ω to 3 Ω; output capacitor from 1 μF to 220 μF
- Integrated various fault protections:
  - Reverse polarity protected input
  - Reverse current protection
  - Thermal shutdown
  - Short-circuit to ground and battery protection
  - Over-current protection
- Package options:
  - SOT8105-1 (SOT23-5S (NSOT23-5)): $R_{θJA}$= 131.7 °C/W
  - SOT8104-1 (SOT23-5): $R_{θJA}$= 175.6 °C/W

3. Applications

- Supply for off-board sensors
- High precision voltage tracking
- Body Control Modules (BCMs)
- Power switch for off-board loads

Table 1. Device information

Part number	Package	Body size (nom)
NEX91207DE-Q100	SOT23-5S	2.93 mm x 1.50 mm
NEX91207DF-Q100	SOT23-5	2.93 mm x 1.63 mm

nexperia

4. Ordering information

Table 2. Ordering information

Type number	Package			
	Temperature range (T_j)	Name	Description	Version
NEX91207DE-Q100	-40 °C to +150 °C	SOT23-5S	SOT23-5S (NSOT23-5): 5 pins; 2.926 mm x 1.50 mm x 1.10 mm body	SOT8105-1
NEX91207DF-Q100	-40 °C to +150 °C	SOT23-5	SOT23-5: 5 pins; 0.95 mm pitch; 2.926 mm x 1.626 mm x 1.25 mm body	SOT8104-1

5. Marking

Table 3. Marking codes

Type number	Marking code
NEX91207DE-Q100	N7E
NEX91207DF-Q100	N7E

6. Pin configuration and description

6.1. Pin configuration

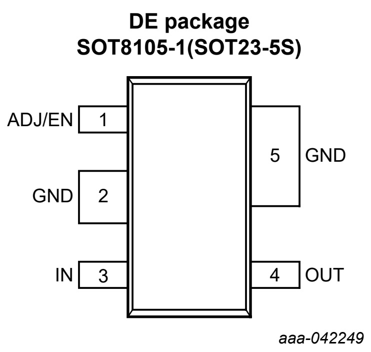


Fig. 2. Pin configuration (SOT8105-1) package

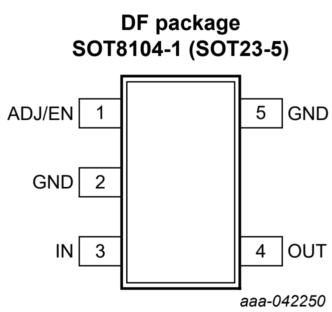


Fig. 3. Pin configuration (SOT8104-1) package

6.2. Pin description

Table 4. Pin description

Symbol	Pin	I/O	Description
ADJ/EN	1	I	ADJ or enable pin. For ADJ function, can be connected directly to the reference voltage or through a resistor divider for lower voltage. Place a capacitor close to the ADJ pin to eliminate line interferences. For enable function, a low voltage signal disable the device, while a high voltage signal enables it.
GND	2, 5	G	Ground pin. This pin is connected to ground internally.
IN	3	I	Input power-supply voltage pin. Place a small ceramic capacitor as close to the input of the device as possible to reduce line interference.
OUT	4	O	Tracking output voltage pin. Place a capacitor as close to the output of the device as possible, follow the capacitance and ESR requirements described in Table 8.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	unregulated input voltage		-42	+45	V
V_{OUT}	tracking output voltage		-5	+45	V
$V_{ADJ/EN}$	enable/adjustable voltage		-0.3	+45	V
T_j	operating junction temperature		-40	+150	°C
T_{amb}	operating ambient temperature		-40	+125	°C
T_{stg}	storage temperature		-65	+165	°C

[1] Stresses beyond those conditions under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8. ESD ratings

Table 6. ESD ratings

		Conditions	Value	Unit
V_{ESD}	electrostatic discharge voltage	Human-body model (HBM), per AEC Q100-002 [1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	V

[1] AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

9. Thermal Information

Table 7. Thermal information

Thermal resistance according to JEDEC51-5 and -7.

Symbol	Parameter	Package		Unit
		SOT8105-1 (SOT23-5S)	SOT8104-1 (SOT23-5)	
$R_{\theta JA}$	junction to ambient thermal resistance	131.7	175.6	°C/W
$R_{\theta JC(top)}$	junction to case(top) thermal resistance	105.5	128.2	°C/W
$R_{\theta JB}$	junction to board thermal resistance	23.5	50.8	°C/W
Ψ_{JT}	junction to top char parameter	10.1	21.9	°C/W

10. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	input voltage		4	-	40	V
V_{OUT}	output voltage		2	-	40	V
I_{OUT}	output current	[1]	-	-	70	mA
V_{ADJ}	adjust input voltage range (voltage tracking range)		2	-	40	V
C_{IN}	input capacitance		0.47	1	-	µF
C_{OUT}	output capacitance	[2]	1	-	220	µF
ESR	output capacitor ESR requirements	[3]	0.001	-	3	Ω
T_{amb}	ambient temperature		-40	-	+125	°C
T_j	junction temperature		-40	-	+150	°C

[1] Maximum output current when device is not thermal shutdown.
[2] Effective output capacitance of 1 µF minimum required for stability.
[3] Relevant ESR value at f = 10 kHz, if using a large ESR capacitor it is recommended to decouple this with a 100 nF ceramic capacitor to improve transient performance.

11. Electrical characteristics

Table 9. Electrical characteristics

At recommended operating conditions; T_{amb} = -40 °C to +125 °C; T_j = -40 °C to +150 °C; C_{OUT} = 2.2 µF; V_{IN} = 13.5 V; I_{OUT} = 100 µA; V_{ADJ} = 5 V; (unless otherwise noted) voltages are referenced to GND (ground = 0 V).

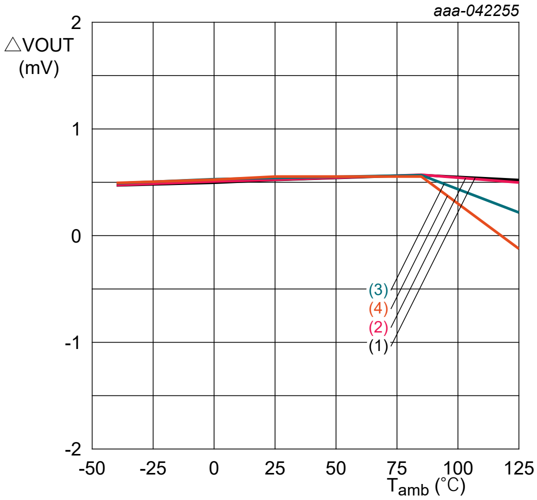
Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Power supply						
V_{IN}	input voltage range		4	-	40	V
$V_{IN(UVLO)}$	under voltage lockout threshold	V_{IN} rising	3.1	3.6	3.9	V
		Hysteresis		400		mV
I_Q	quiescent current	V_{IN} = 5.5 V to 40 V, I_{OUT} = 100 µA; V_{ADJ} = 5 V	-	40	70	µA
I_{SHUT}	shutdown current	V_{IN} = 4 V to 40 V, V_{ADJ} = 0 V	-	0.75	3.5	µA
$I_{R(IN)}$	reverse current at IN	V_{IN} = 0 V, V_{OUT} = 20 V, V_{ADJ} = 5 V	-1	-	-	µA
$I_{R(-IN)}$	reverse current at negative IN	V_{IN} = -20 V, V_{OUT} = 0 V, V_{ADJ} = 5 V	-4	-	-	µA
ADJ/EN input						
V_{EN_L}	logic input low level		-	-	0.7	V
V_{EN_H}	logic input high level		2	-	-	V
$I_{ADJ/EN}$	ADJ/EN pin current		-	-	800	nA

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +125 °C			Unit
				Min	Typ[1]	Max	
Output							
ΔV_{OUT}	output accuracy	V_{IN} = 500 mV + V_{OUT} to 40 V ($V_{IN} \geq$ 4 V); I_{OUT} = 100 µA to 70 mA		-5	-	5	mV
$\Delta V_{OUT(\Delta VIN)}$	line regulation	V_{IN} = 5.5 V to 40 V; I_{OUT} = 10 mA, V_{ADJ} = 5 V		-	-	0.5	mV
$\Delta V_{OUT(\Delta IOUT)}$	load regulation	V_{IN} = 5.5 V to 40 V; I_{OUT} = 100 µA to 70 mA, V_{ADJ} = 5 V		-	-	0.5	mV
V_{DO}	dropout voltage	V_{DO} = V_{IN} - V_{OUT}, I_{OUT} = 70 mA; V_{ADJ} = 5 V, V_{IN} = V_{ADJ}		-	215	340	mV
I_{OUT}	output current	V_{IN} = V_{ADJ} + 500 mV		-	-	70	mA
I_{DIS}	discharge current	V_{OUT} = 5 V, V_{IN} = 13.5 V		-	700	-	µA
I_{CL}	output current limit	V_{IN} = 13.5 V, output short to 90% × V_{ADJ}		80	105	130	mA
PSRR	power-supply ripple rejection	V_{IN} = 13.5 V, V_{ADJ} = 5 V, I_{OUT} = 10 mA, C_{OUT} = 2.2 µF, frequency = 100 Hz	[2]	-	90	-	dB
V_n	output noise voltage	V_{ADJ} = 5 V, I_{OUT} = 1 mA, BW = 10 Hz to 100 kHz, 5 µVRMS reference	[3]	-	50	-	µVRMS
Operating temperature range							
T_{SD}	junction thermal shutdown temperature	Rising junction temperature	[2]	-	175	-	°C
T_{HYST}	thermal shutdown hysteresis		[2]	-	20	-	°C

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Guaranteed by bench test, not fully tested in production.
[3] Guaranteed by design.

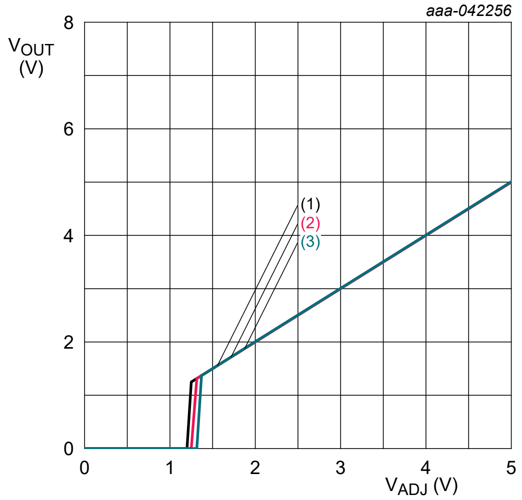
12. Typical characteristics

At recommended operating conditions, voltages are referenced to GND (ground = 0 V); typical values are at 25 °C (unless otherwise noted). V_{IN} = 13.5 V; V_{ADJ} = 5 V; C_{IN} = 1 µF; C_{OUT} = 2.2 µF; unless otherwise specified.



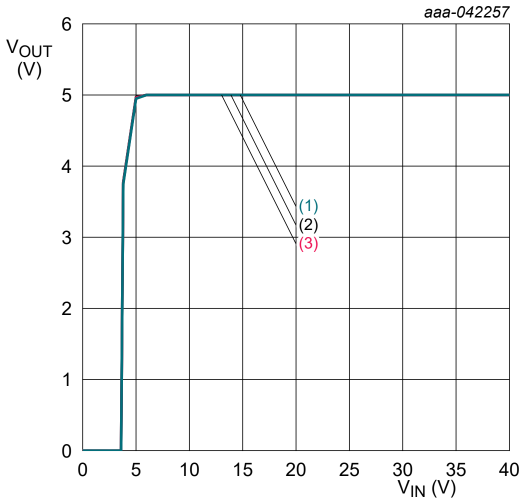
(1) I_{OUT} = 100 µA
(2) I_{OUT} = 10 mA
(3) I_{OUT} = 50 mA
(4) I_{OUT} = 70 mA

Fig. 4. Tracking accuracy vs ambient temperature



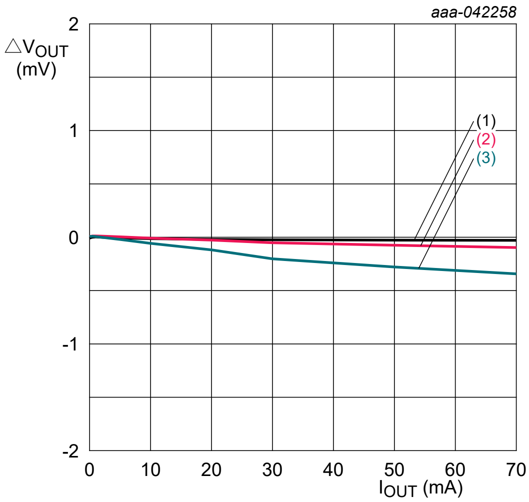
V_{IN} = 13.5 V, I_{OUT} = 10 mA
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 5. Output voltage vs adjustable reference voltage



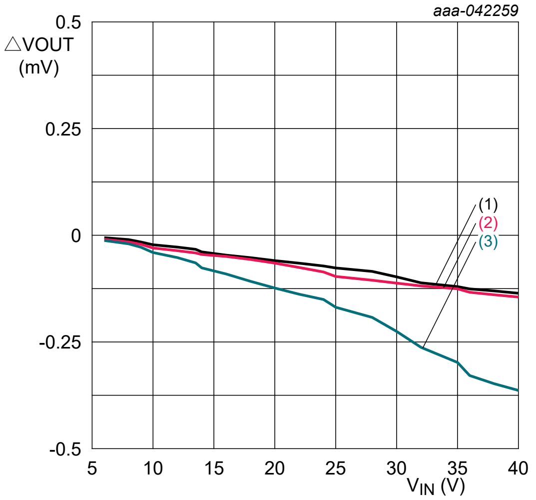
(1) V_{ADJ} = 5 V, I_{OUT} = 10 mA
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 6. Output voltage vs input voltage



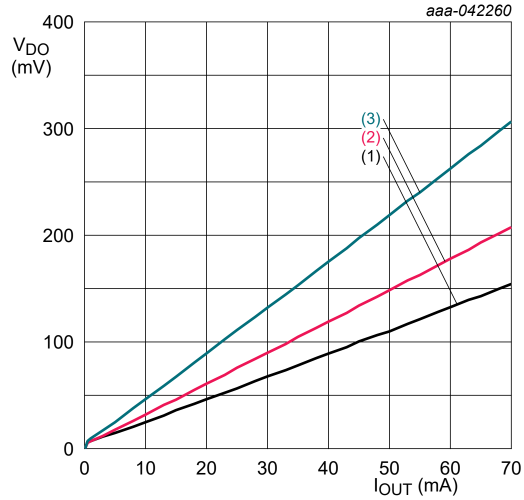
V_{IN} = 13.5 V, V_{ADJ} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 7. Load regulation



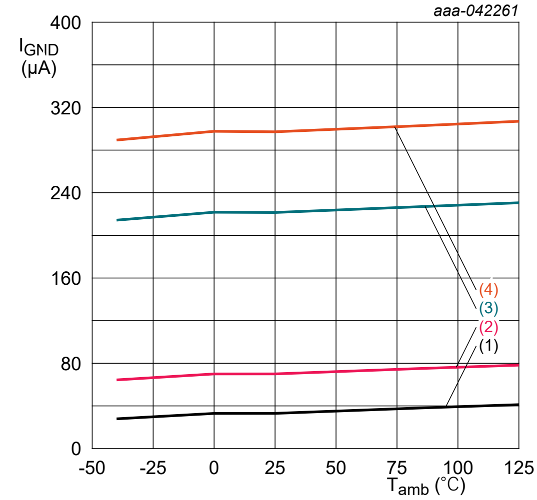
V_{ADJ} = 5 V; I_{OUT} = 10 mA
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 8. Line regulation



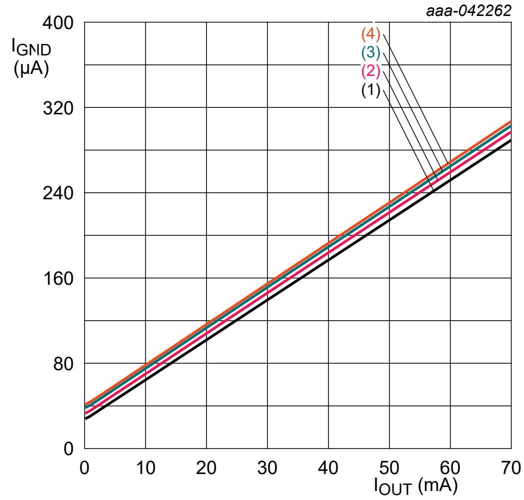
V_{ADJ} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 9. Dropout voltage vs output current



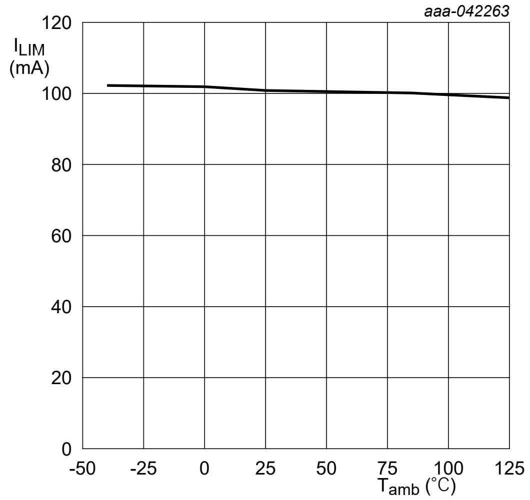
V_{ADJ} = 5 V
(1) I_{OUT} = 100 µA
(2) I_{OUT} = 10 mA
(3) I_{OUT} = 50 mA
(4) I_{OUT} = 70 mA

Fig. 10. Ground current vs ambient temperature



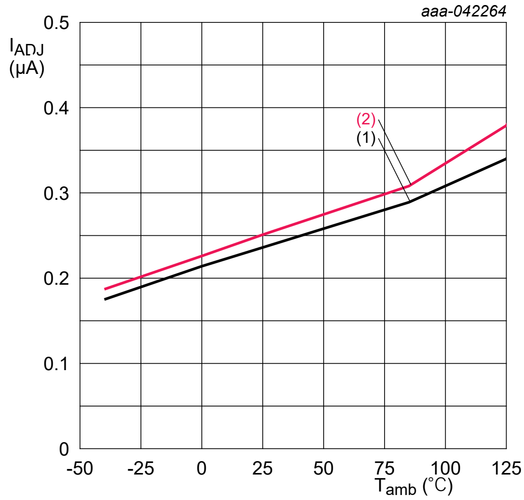
V_{ADJ} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 85 °C
(4) T_{amb} = 125 °C

Fig. 11. Ground current vs output current



V_{IN} = 13.5 V, V_{ADJ} = 5 V

Fig. 12. Current limit vs temperature

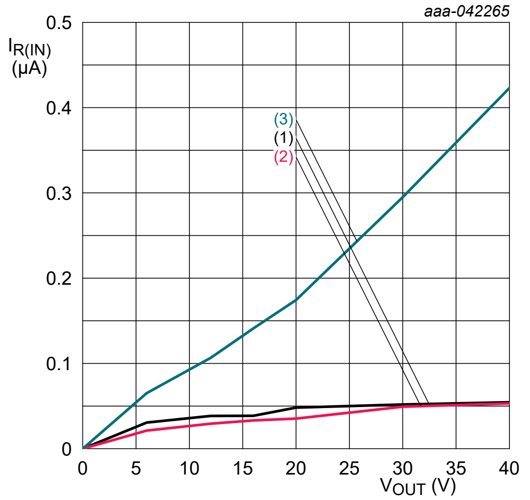


V_{IN} = 13.5 V

(1) V_{ADJ} = 5 V

(2) V_{ADJ} = 13.5 V

Fig. 13. Adjustable pin Current vs ambient temperature



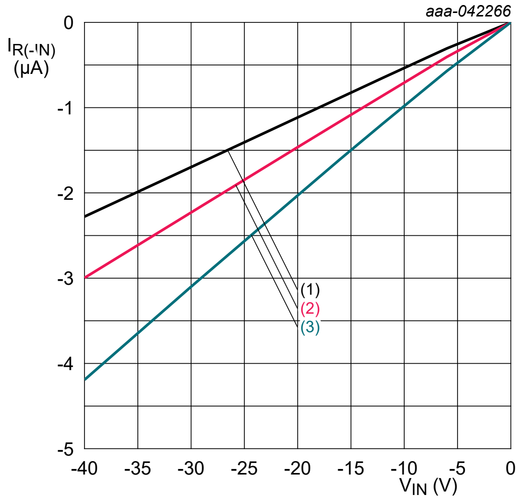
V_{ADJ} = 5 V, V_{IN} = 0 V

(1) T_{amb} = -40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 125 °C

Fig. 14. Reverse current vs output voltage



V_{ADJ} = 5 V, V_{OUT} = 0 V

(1) T_{amb} = -40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 125 °C

Fig. 15. Reverse current vs input voltage

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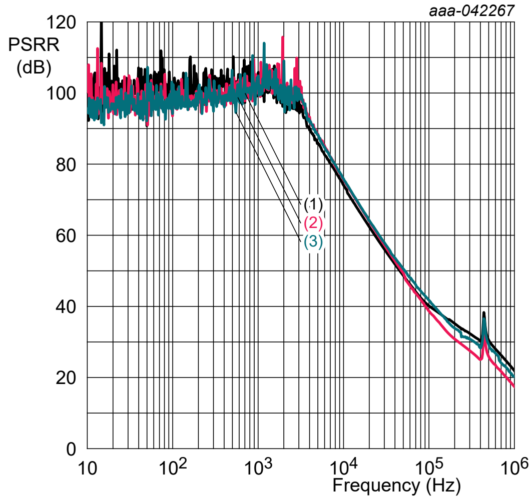

V_{IN} = 13.5 V, V_{ADJ} = 5 V
C_{IN} = 0.1 µF, C_{OUT} = 2.2 µF
(1) I_{OUT} = 10 mA
(2) I_{OUT} = 50 mA
(3) I_{OUT} = 70 mA

Fig. 16. PSRR

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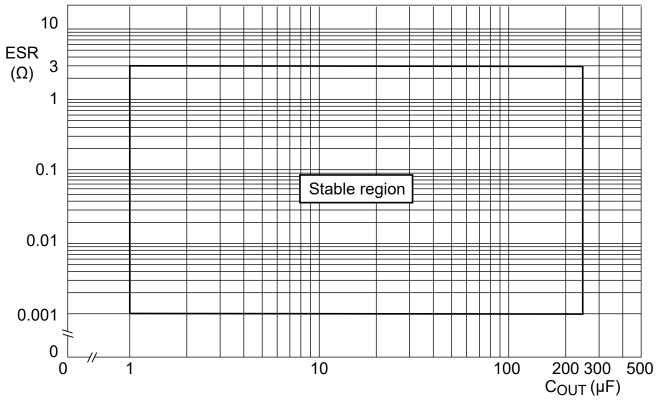

1 mΩ ≤ ESR ≤ 3 Ω, 1 µF ≤ C_{OUT} ≤ 220 µF

Fig. 17. ESR vs load capacitance

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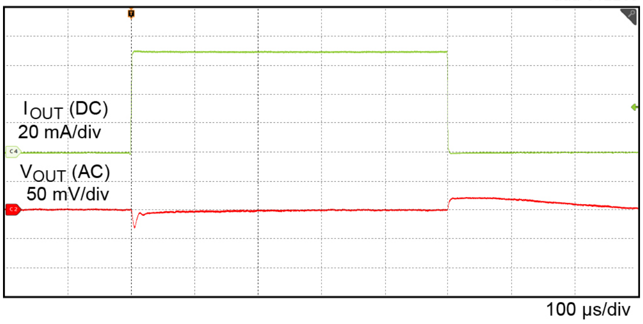

V_{IN} = 13.5 V, I_{OUT} = 0 mA to 70 mA,
slew rate = 1 A/µs, V_{ADJ} = 5 V, C_{OUT} = 10 µF

Fig. 18. Load transient

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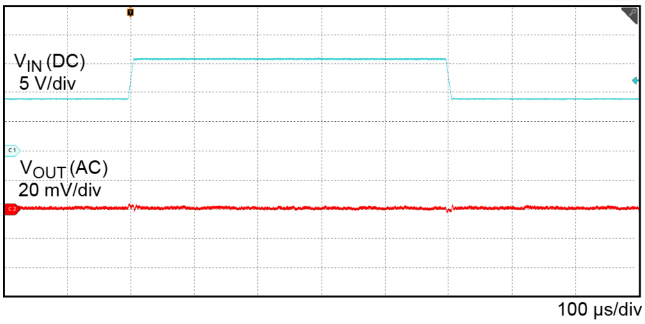

V_{IN} = 9 V to 16 V slew rate = 1 V/µs,
V_{ADJ} = 5 V, I_{OUT} = 70 mA, C_{OUT} = 10 µF

Fig. 19. Line transient

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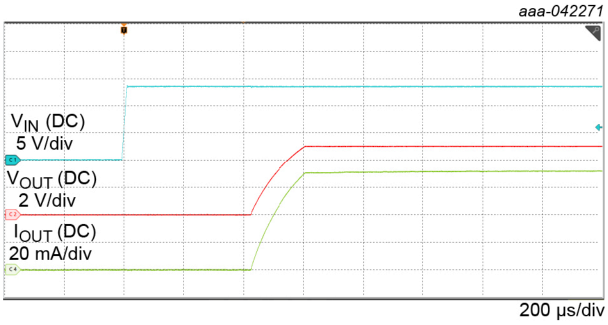

V_{ADJ} = 5 V, I_{OUT} = 70 mA,
C_{OUT} = 2.2 µF, V_{IN} from 0 to 13.5 V

Fig. 20. Start up by VIN

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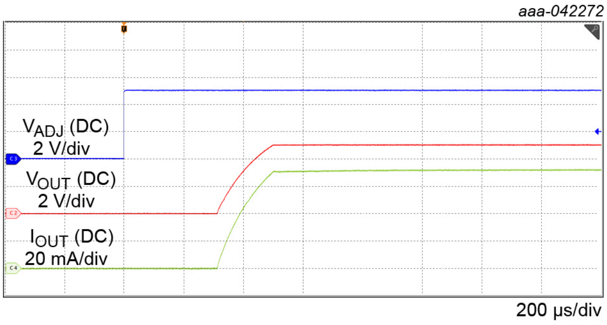


V_{IN} = 13.5 V, I_{OUT} = 70 mA,
C_{OUT} = 2.2 µF, V_{ADJ} from 0 to 5 V

Fig. 21. Start up by ADJ/EN

13. Detailed description

13.1. Overview

The NEX91207-Q100 is a Low-Dropout (LDO) tracking regulator with ultra-low tracking tolerance. It is designed to supply off-board systems, such as sensors in power train or passive safety applications. The device offers multiple protection features, including reverse polarity protection and safeguards against shorts to the battery and ground.

13.2. Function block diagram

The NEX91207-Q100 function block diagram is shown in Fig. 22.

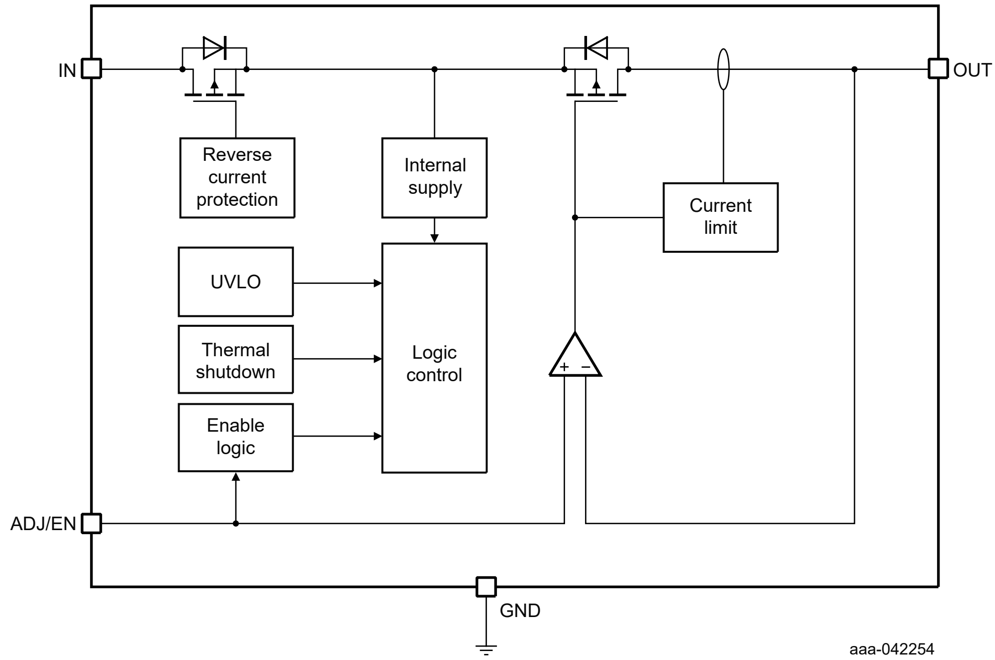


Fig. 22. Function block diagram

13.3. Feature description

13.3.1. Tracking Output (V_{OUT})

The output voltage tracks closely to the reference voltage applied to EN/ADJ pin. V_{OUT} begins to rise to match the V_{ADJ} once V_{ADJ} exceeds the enable threshold. V_{OUT} remains stable within ±5 mV to V_{ADJ} once it reaches to the V_{ADJ} level. The device can support output voltage up to 40 V, and output current up to 70 mA.

13.3.2. Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit is to stop the operation of the device when the input voltage falls below the typical threshold $V_{IN\ (UVLO)}$. The UVLO circuit includes hysteresis to prevent the device from shutting down if input voltage drops briefly after power up, as specified in the Electrical Characteristics table. If the input voltage experiences a negative transient that drops below the UVLO threshold and then recovers, the regulator will shut down and restart following the normal power-up sequence once the input voltage exceeds the required level.

13.3.3. Current limit operation

The device features an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. When the device is in current limit mode, the output voltage is not regulated. During a current limit event, the device heats up due to increased power dissipation. When the device reaches the current limit (I_{CL}), the pass transistor dissipates power according to the formula [V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device will turn off. Once it cools down, the internal thermal shutdown circuit will turn the device back on. If the output current fault condition persists, the device will cycle between current limit and thermal shutdown.

13.3.4. Thermal protection

The NEX1207-Q100 integrates an internal temperature sensor to monitor the junction temperature (T_j). If T_j exceeds the thermal shutdown temperature (T_{SD}) of 175 °C, the device ceases operation. The device will resume functioning when T_j drops below the hysteresis threshold of approximately 20 °C.

Thermal shutdown may be triggered during startup due to large inrush currents charging substantial output capacitance, or under heavy loads where high (V_{IN} – V_{OUT}) regulations result in significant power dissipation across the die. Proper heat sinking should be considered in these high power dissipation scenarios.

13.3.5. Output short to battery and reverse protection

The NEX91207-Q100 is designed to withstand output short-to-battery conditions without damage as shown in Fig. 23. And a short to battery might also occur when the device is powered by a lower separated input voltage supply as shown in the Fig. 24. For instance, when the device is powered by a lower, separate input voltage supply, such as 9 V, and the output short to a 13.5 V (typical) battery occurs while the output is set to 5 V, the device remains protected. In this scenario, the reverse current from OUT to IN is blocked and the continuous reverse current flowing through the input is typically limited to less than 5 µA.

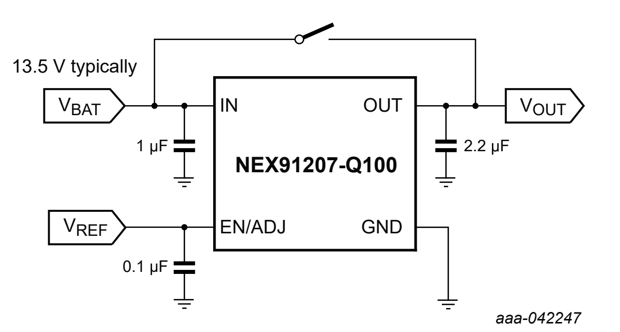


Fig. 23. Output short to battery

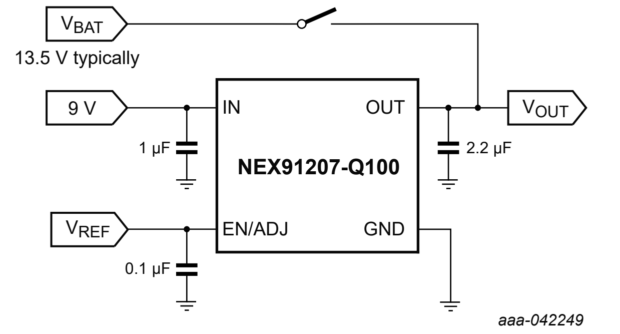


Fig. 24. Output short to battery with lower input voltage

13.3.6. Active output discharge

The device integrates active output discharge function when device is enabled, which ensures the output voltage quickly return to the nominal output voltage during over-voltage fluctuations, such as during load transient from heavy load to light load. When output voltage is over the nominal output voltage, the device will turn on a FET that connects 6 kΩ of resistance to ground. Even without an actual load, the output will source typical 700 µA through the resistor in this situation.

13.3.7. Tracking output with an enable circuit

When the input voltage at the EN/ADJ pin falls below the 0.7 V threshold, the NEX91207-Q100 is disabled and enters a sleep mode, drawing only 0.75 µA from the power supply. In typical applications, the reference voltage is often sourced from another regulator (such as a DC-DC converter or LDO voltage rail). This setup allows flexible enable/disable control via external I/O and circuitry, as shown in Fig. 25. In this example, the NEX90230-Q100, a 300 mA LDO with ultra-low quiescent current, serves as both the reference voltage source for the NEX91207-Q100 and the power supply for the ADC. The operating mode of the device is controlled by an MCU I/O pin, as illustrated in the Fig. 25.

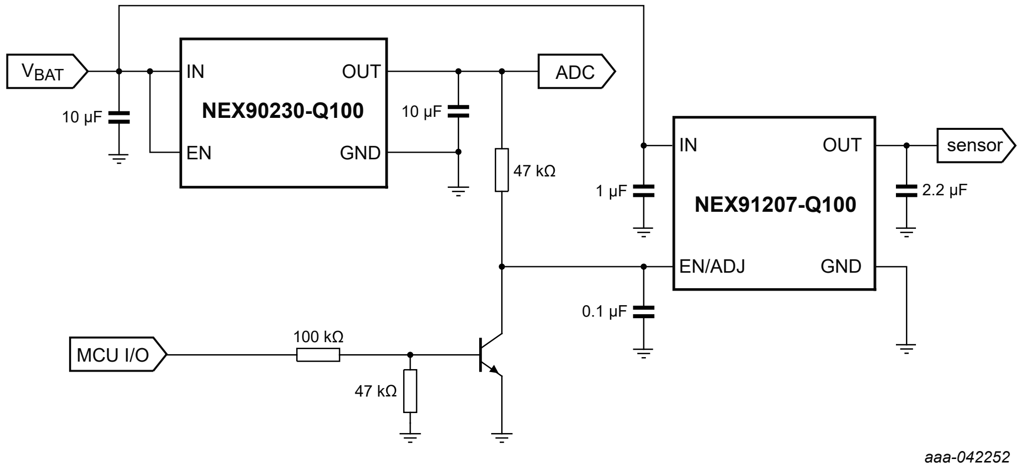


Fig. 25. Tracking an LDO with an enable circuit

13.4. Application implementation

13.4.1. Design requirements

A typical application is applied in automotive and power supply for a off-board sensor or multi sensor, which normally requires 5 V or 3.3 V output. The design parameters are listed in Table 10.

Table 10. Design parameters

Parameters	Values
Input voltage	4 V to 40 V
ADJ reference voltage	2 V to 20 V
Output voltage	2 V to 20 V
Output current	70 mA max
Output capacitor range	1 µF to 220 µF
Output capacitor ESR range	1 mΩ to 3 Ω

13.4.2. Typical application

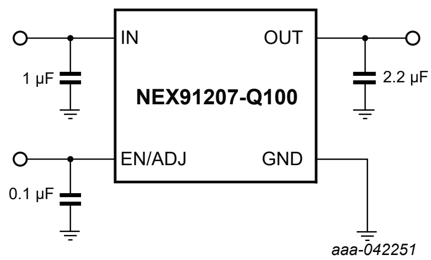


Fig. 26. NEX91207-Q100 typical application

13.4.2.1. Detailed design procedure

To begin the design process, determine the following requirements.

- Operation input voltage range
- Reference voltage
- Output voltage
- Output current rating

- Input capacitor
- Output capacitor

13.4.2.1.1. Input capacitor

The NEX91207-Q100 recommends an input decoupling capacitor connected from IN to GND and close to the IC terminals through is not required for stability, the value of which depends on the end-applications. The input supplies have a high impedance in some applications, thus placing the input capacitor on the input supply helps reduce the input impedance.

In addition, the input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. And several input capacitors can be placed in parallel to lower the impedance over frequency if the supply has a high impedance over a larger range of frequencies noise. The bigger-value input capacitors recommended when larger, fast rising time load/line transient are anticipated or larger distance located from input power supply source. Lastly, the voltage rating of input capacitors must be greater than the maximum input voltage.

13.4.2.1.2. Output capacitor

To ensure the stability of the NEX91207-Q100, the device requires an output capacitor with an effective value 1 μF to 220 μF from OUT to GND and ESR range between 0.001 Ω and 3 Ω. It recommends selecting X7R and X5R type ceramic capacitor with low ESR to improve the load transient response and ripple performance.

14. Layout

14.1. Layout guidelines

For optimal overall performance, follow these guidelines for LDO layout:

- Place all circuit components on the same side of the circuit board and as close as possible to their respective LDO pin connections.
- Position ground return connections for the input and output capacitors, as well as the LDO ground pin, close to each other and connect them using a wide copper surface on the component side.
- Avoid using vias and long traces to connect the input and output capacitors, as this can negatively impact system performance.
- In most applications, the ground plane is essential to meet thermal requirements.

A ground reference plane should be either embedded in the PCB itself or located on the bottom side of the PCB, opposite the components. This reference plane ensures output voltage accuracy, provides noise shielding, and acts as a thermal plane to spread or dissipate heat from the LDO device when connected to the thermal pad.

14.2. Layout example

Fig. 27 shows a layout example of NEX91207-Q100 (SOT23-5S) device.

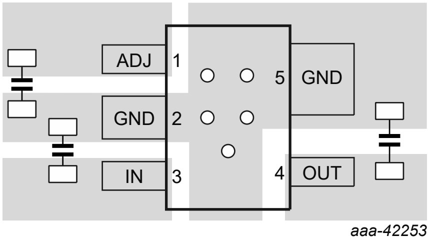
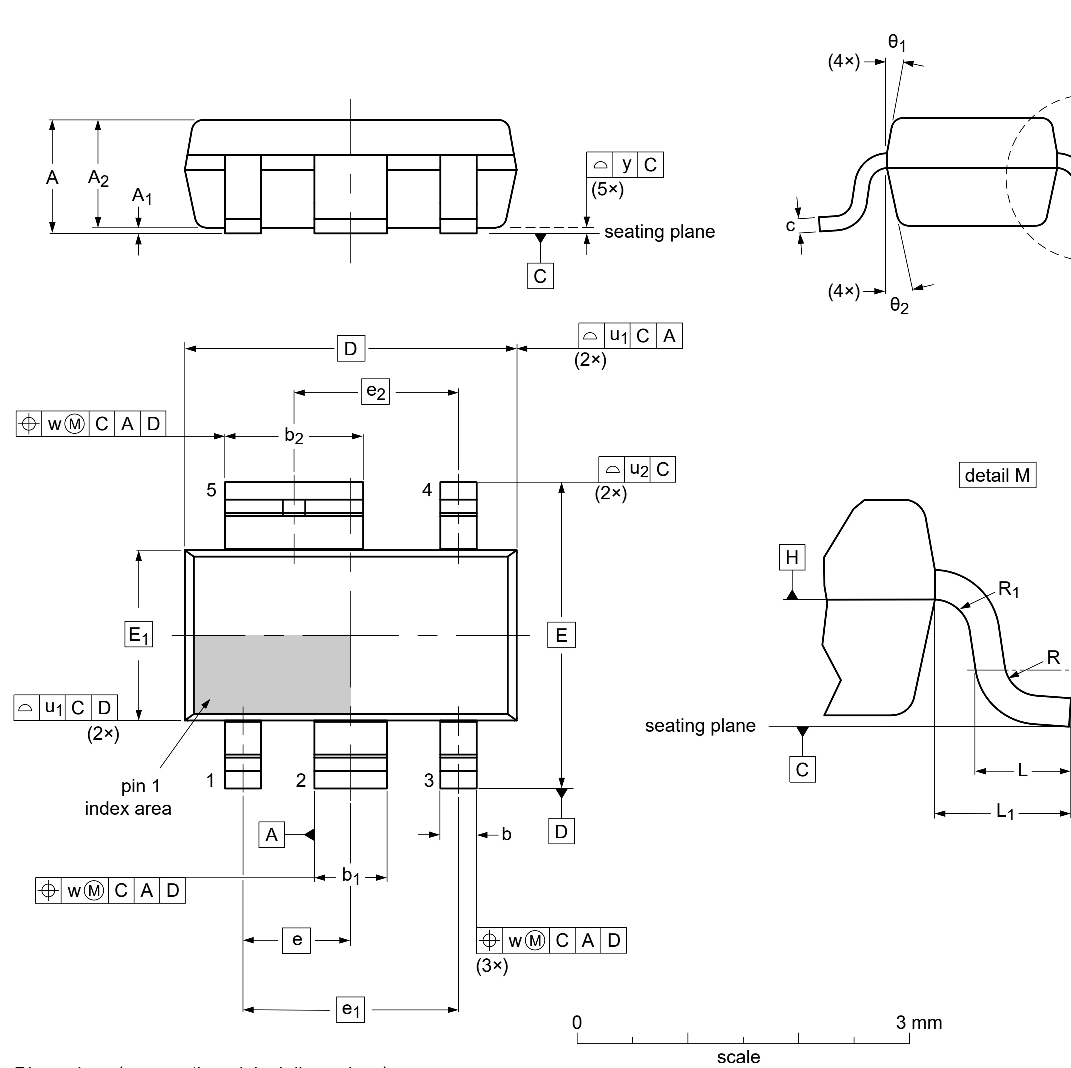


Fig. 27. NEX91207-Q100 layout example

15. Package outline

SOT23-5S (NSOT23-5): 5 pins; 2.926 mm x 1.50 mm x 1.10 mm body **SOT8105-1**



	θ	$θ_1$	$θ_2$
max	8°	12°	14°
nom		10°	12°
min	0°	8°	10°

Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	b_1	b_2	c	D	E	E_1	e	e_1	e_2	L	L_1	R	R_1	y	u_1	u_2	w
mm	max	1.10	0.10	1.00	0.39	0.69	1.29	0.20							0.60		0.20	0.20				
	nom			0.95					2.926 BSC	2.70 BSC	1.50 BSC	0.95 BSC	1.90 BSC	1.45 BSC	0.37	0.60 REF			0.10	0.10	0.15	0.20
	min		0.00	0.85	0.25	0.55	1.15	0.12							0.30		0.05	0.05				

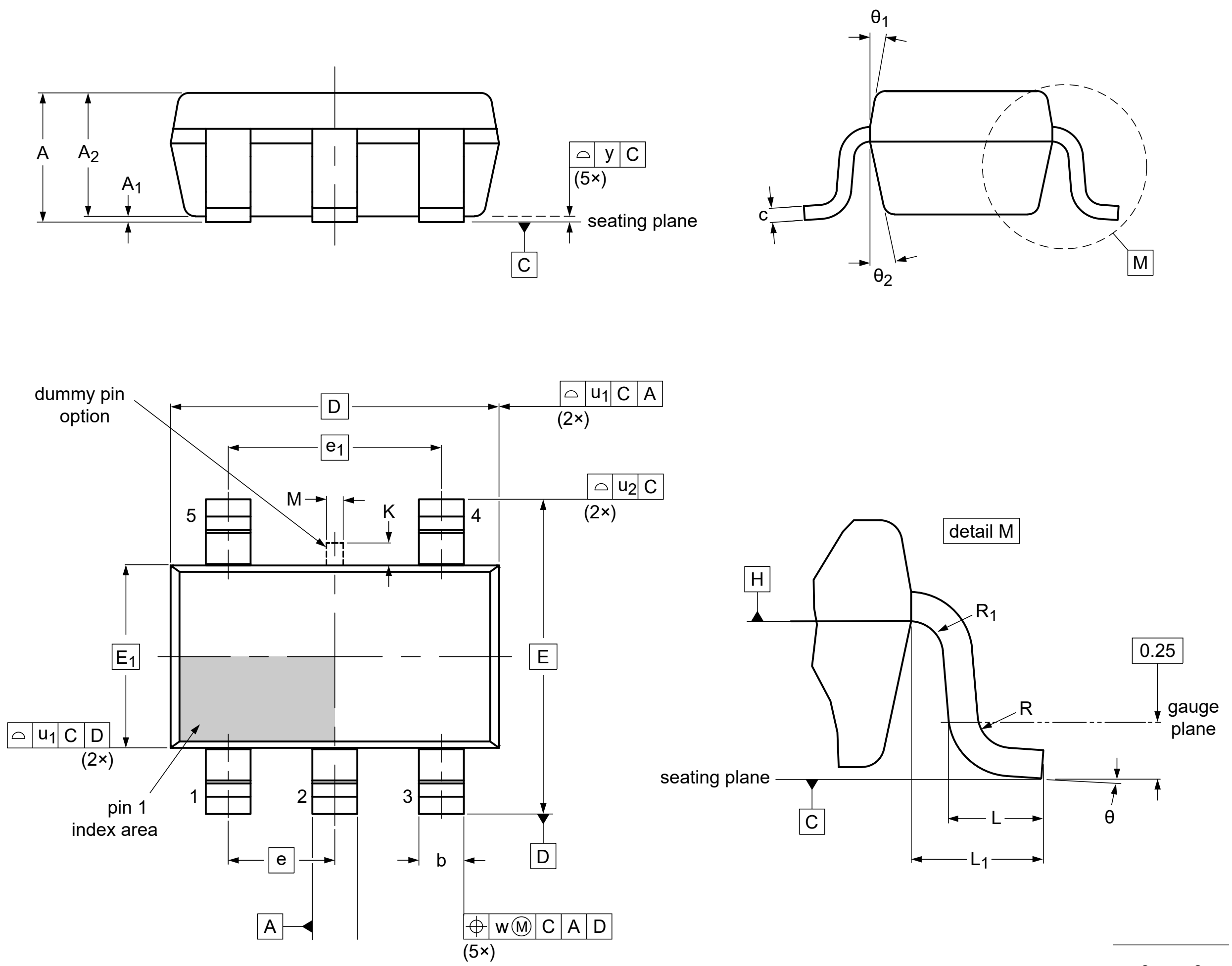
Note
1. Plastic or metal protrusions of 0.25 mm per side are not included for dimensions D and E.
2. D and E_1 dimensions are determined at datum H.
3. Damber protrusion shall be 0.08 mm. Total in excess of “b” dimension at maximum material condition.

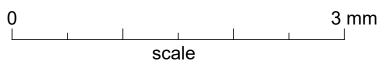
sot8105-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8105-1						25-01-07

Fig. 28. Package outline SOT8105-1 (SOT23-5S)

SOT23-5: 5 pins; 0.95 mm pitch; 2.926 mm x 1.626 mm x 1.25 mm body SOT8104-1





θ1	θ2
12°	14°
10°	12°
8°	10°

Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	b	c	D	E	E_1	e	e_1	K	L	L_1	M	R	R_1	y	u_1	u_2	w	θ
	max	1.25	0.15	1.20	0.45	0.20						0.20	0.60		0.20	0.20	0.20					8°
mm	nom			1.10			2.926 BSC	2.80 BSC	1.626 BSC	0.95 BSC	1.90 BSC		0.40	0.59 REF	0.15			0.10	0.10	0.20	0.20	
	min		0.00	1.00	0.34	0.12						0	0.30		0.10	0.05	0.05					0°

Note
1. Plastic or metal protrusions of 0.25 mm per side are not included for dimensions D and E.
2. D and E_1 dimensions are determined at datum H.
3. Damber protrusion shall be 0.08 mm. Total in excess of “b” dimension at maximum material condition.

sot8104-1_po

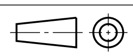
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8104-1		MO-178				25-01-08

Fig. 29. Package outline SOT8104-1 (SOT23-5)

16. Abbreviations

Table 11. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
BCM	Body Control Module
CDM	Charged Device Model
ESR	Equivalent Series Resistance
HBM	Human Body Model
LDO	Low-DropOut
PCB	Printed Circuit Board
UVLO	UnderVoltage LockOut

17. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX91207_Q100 v. 1	20250212	Product data sheet	-	

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 12 February 2025