

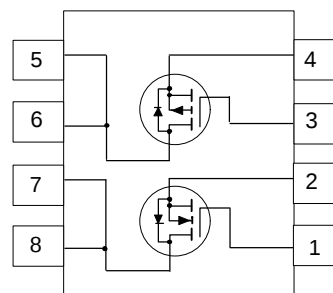
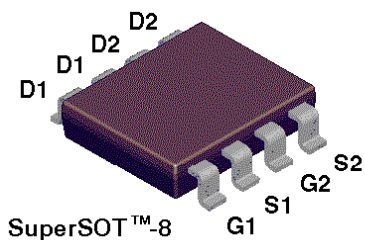
NDH8520C Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 2.8 A, 30 V, $R_{DS(ON)}=0.07\Omega$ @ $V_{GS}=10$ V
 $R_{DS(ON)}=0.1\Omega$ @ $V_{GS}=4.5$ V P-Channel -2.2 A, -30 V,
 $R_{DS(ON)}=0.11\Omega$ @ $V_{GS}=-10$ V
 $R_{DS(ON)}=0.18\Omega$ @ $V_{GS}=-4.5$ V.
- Proprietary SuperSOT™-8 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-30	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1)	2.8	-2.2	A
	- Pulsed	10	-10	
P_D	Power Dissipation for Single Operation (Note 1)	0.8		W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	156	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	N-Ch	30			V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V T_J = 55°C	N-Ch			1	μA
						10	μA
		V _{DS} = -24 V, V _{GS} = 0 V T_J = 55°C	P-Ch			-1	μA
						-10	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	All			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA T_J = 125°C	N-Ch	1	1.6	2.8	V
				0.8	1.2	2	
		V _{DS} = V _{GS} , I _D = -250 μA T_J = 125°C	P-Ch	-1	-1.5	-3	
				-0.8	-1.2	-2.2	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 2.8 A T_J = 125°C	N-Ch		0.05	0.07	Ω
					0.07	0.125	
		V _{GS} = 4.5 V, I _D = 2.3 A			0.077	0.1	
		V _{GS} = -10 V, I _D = -2.2 A T_J = 125°C	P-Ch		0.1	0.11	
					0.14	0.2	
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	N-Ch	10			A
				3			
		V _{GS} = -10 V, V _{DS} = -5 V	P-Ch	-10			
				-4			
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 2.8 A	N-Ch		5.8		S
		V _{DS} = -10 V, I _D = -2.2 A	P-Ch		3.8		
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		270		pF
			P-Ch		340		
C _{oss}	Output Capacitance	P-Channel V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		170		pF
			P-Ch		218		
C _{rss}	Reverse Transfer Capacitance		N-Ch		55		pF
			P-Ch		100		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
t _{D(on)}	Turn - On Delay Time	N-Channel V _{DD} = 10 V, I _D = 1 A, V _{GEN} = 10 V, R _{GEN} = 6 Ω P-Channel V _{DD} = -10 V, I _D = -1 A, V _{GEN} = -10 V, R _{GEN} = 6 Ω	N-Ch		8	15	ns
			P-Ch		8	15	
t _r	Turn - On Rise Time		N-Ch		15	28	ns
			P-Ch		18	35	
t _{D(off)}	Turn - Off Delay Time		N-Ch		15	28	ns
			P-Ch		28	50	
t _f	Turn - Off Fall Time	N-Ch		5	10	ns	
		P-Ch		20	35		
Q _g	Total Gate Charge	N-Channel V _{DS} = 15 V, I _D = 2.8 A, V _{GS} = 10 V	N-Ch		9.4	17	nC
			P-Ch		10.9	14.5	
Q _{gs}	Gate-Source Charge	P-Channel V _{DS} = -15 V, I _D = -2.2 A, V _{GS} = -10 V	N-Ch		0.8		nC
			P-Ch		1.4		
Q _{gd}	Gate-Drain Charge	N-Ch		3		nC	
		P-Ch		3.6			
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I _S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.67	A
			P-Ch			-0.67	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.67 A (Note2)	N-Ch		0.7	1.2	V
		V _{GS} = 0 V, I _S = -0.67 A (Note2)	P-Ch		-0.76	-1.2	

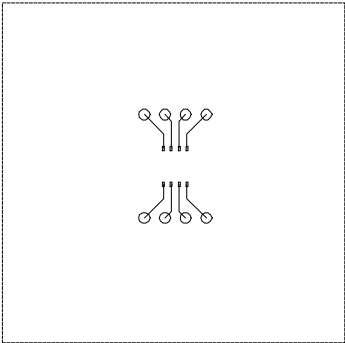
Notes:

1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J A}(t)} = \frac{T_J - T_A}{R_{\theta J} + t R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical R_{θJA} for single device operation using the board layout shown below on 4.5"x5" FR-4 PCB in a still air environment:

156°C/W when mounted on a 0.0025 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

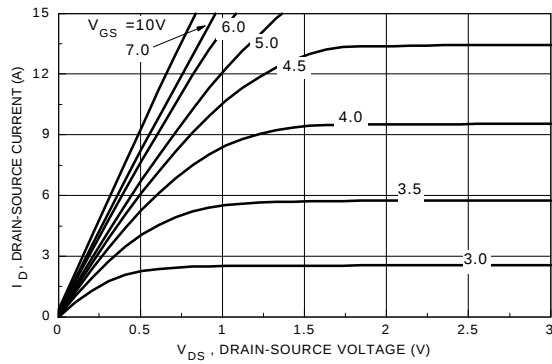


Figure 1. N-Channel On-Region Characteristics.

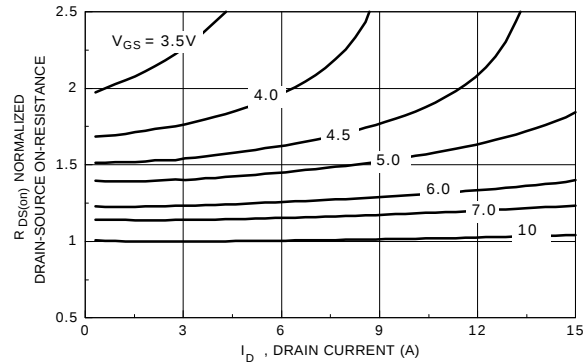


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

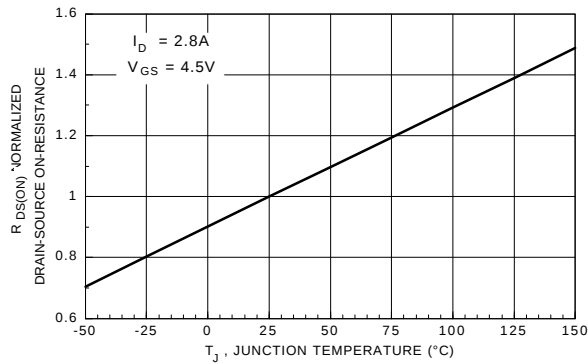


Figure 3. N-Channel On-Resistance Variation with Temperature.

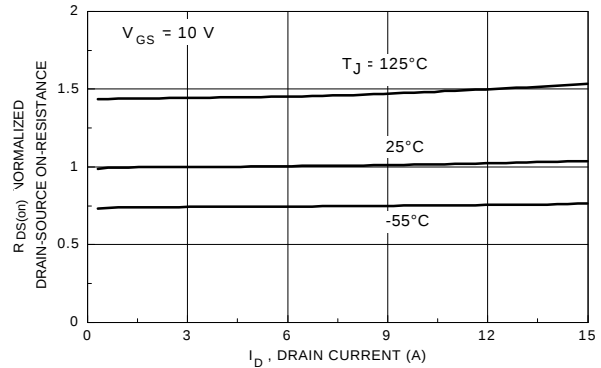


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

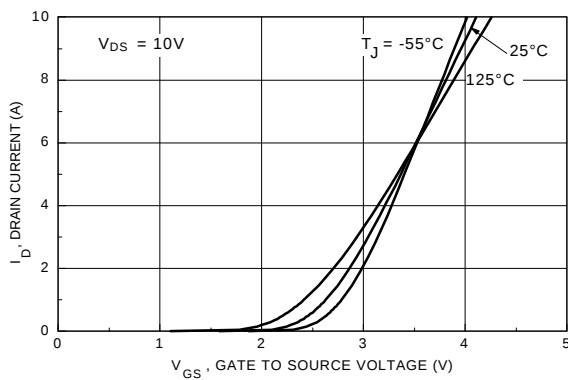


Figure 5. N-Channel Transfer Characteristics.

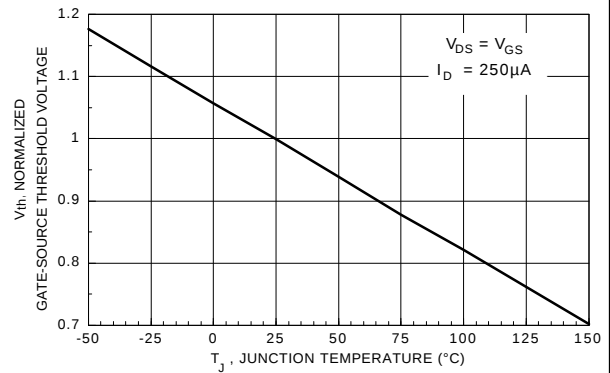


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

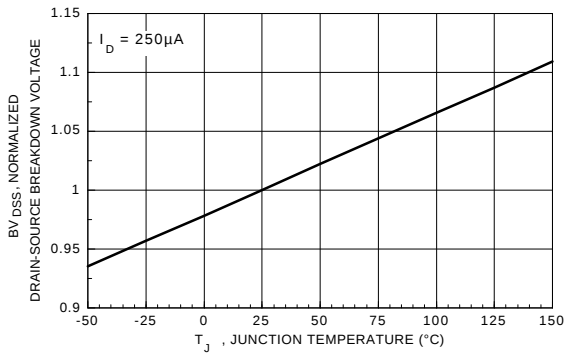


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

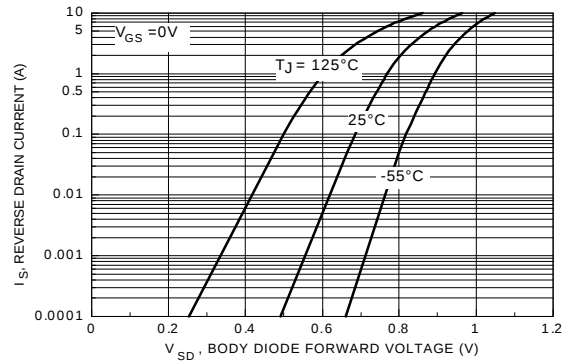


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

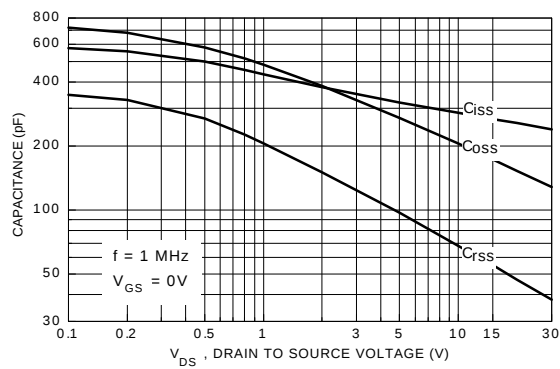


Figure 9. N-Channel Capacitance Characteristics.

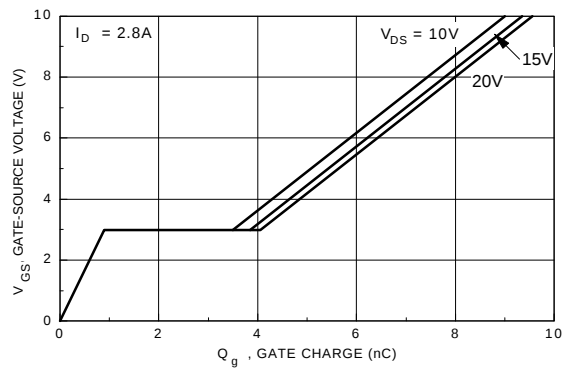


Figure 10. N-Channel Gate Charge Characteristics.

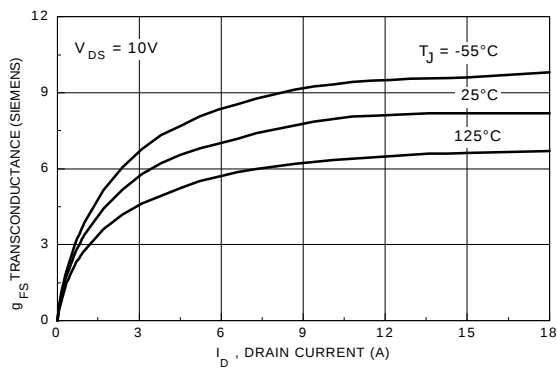


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

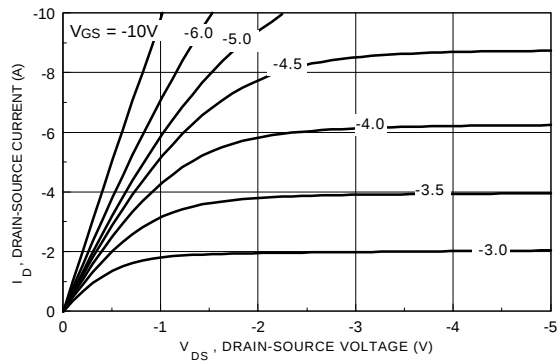


Figure 12. P-Channel On-Region Characteristics.

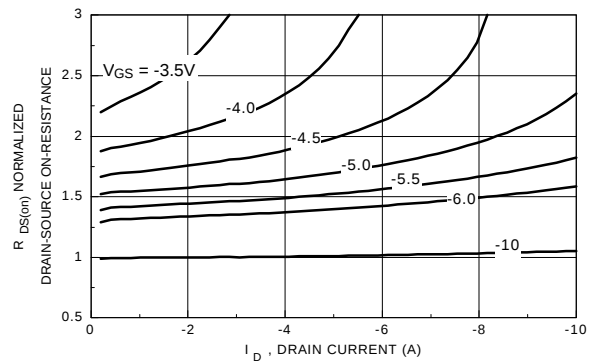


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

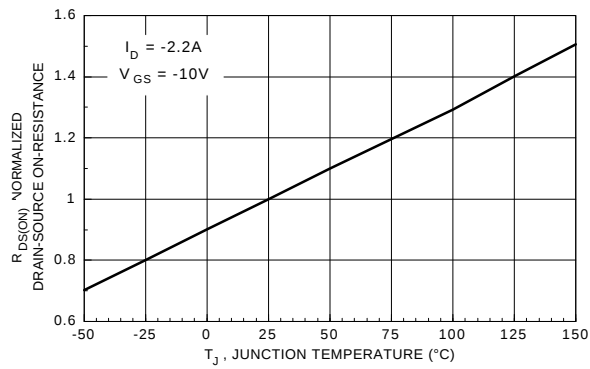


Figure 14. P-Channel On-Resistance Variation with Temperature.

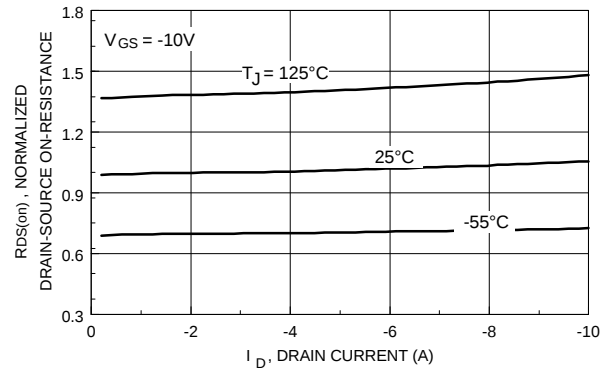


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

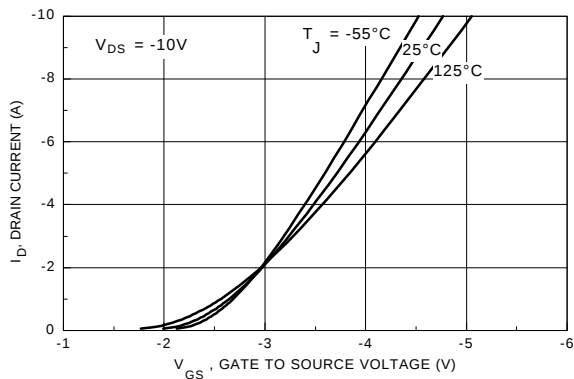


Figure 16. P-Channel Transfer Characteristics.

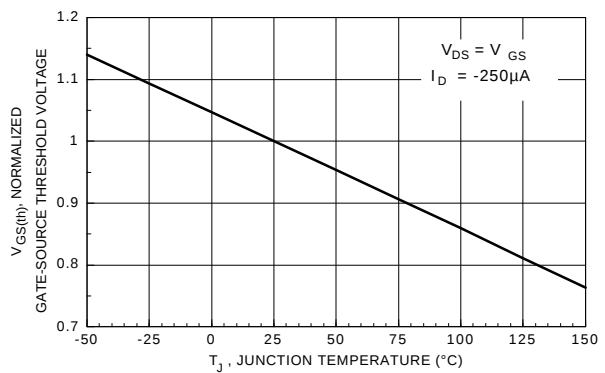


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

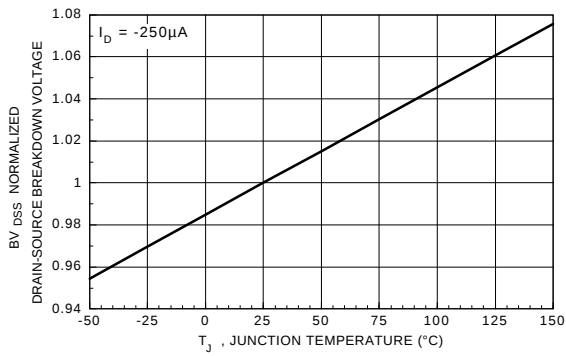


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

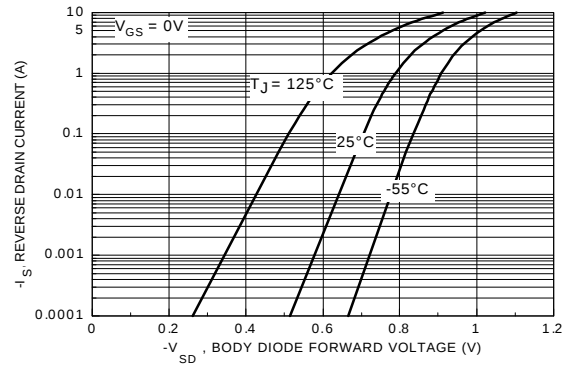


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

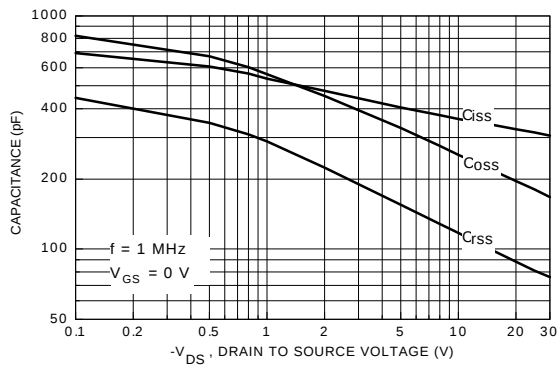


Figure 20. P-Channel Capacitance Characteristics.

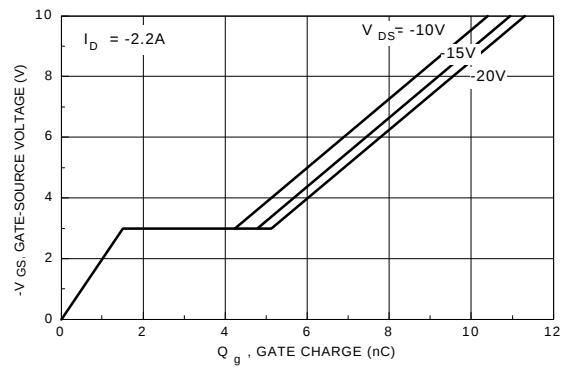


Figure 21. P-Channel Gate Charge Characteristics.

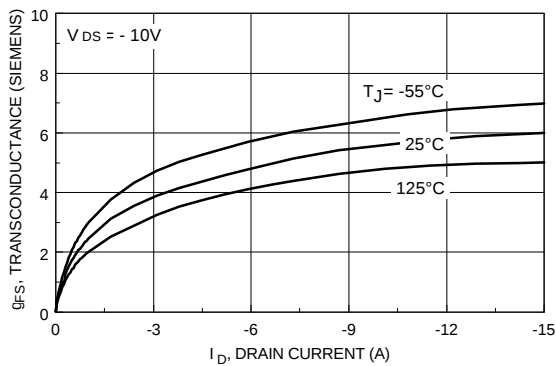


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

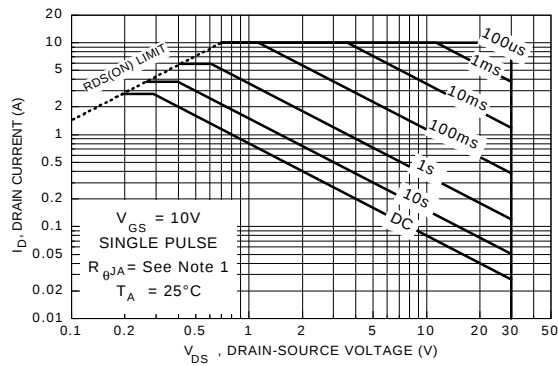


Figure 23. N-Channel Maximum Safe Operating Area.

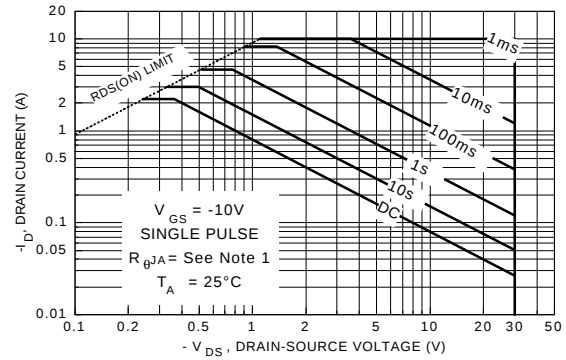


Figure 24. P-Channel Maximum Safe Operating Area.

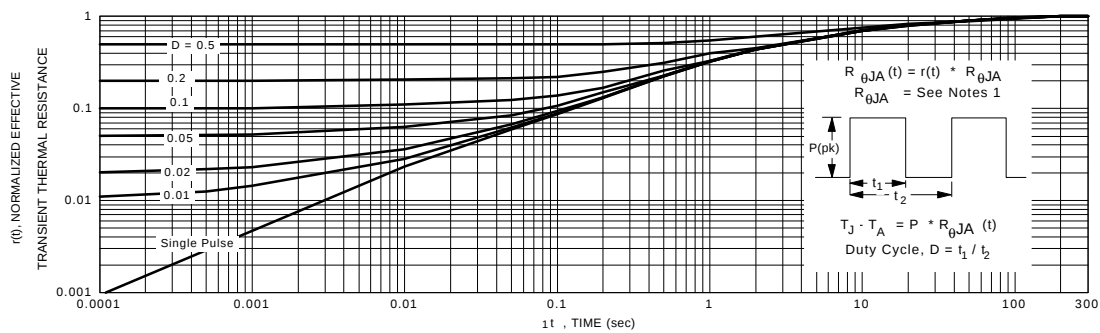


Figure 25. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note1. Transient thermal response will change depending on the circuit board design.

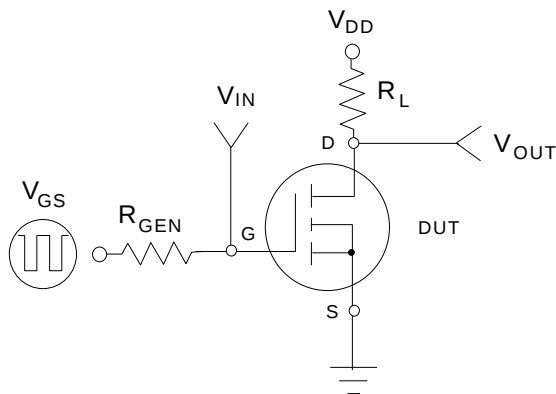


Figure 26. N or P-Channel Switching Test Circuit.

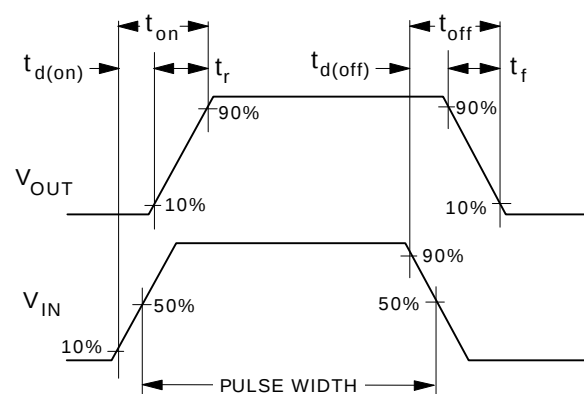
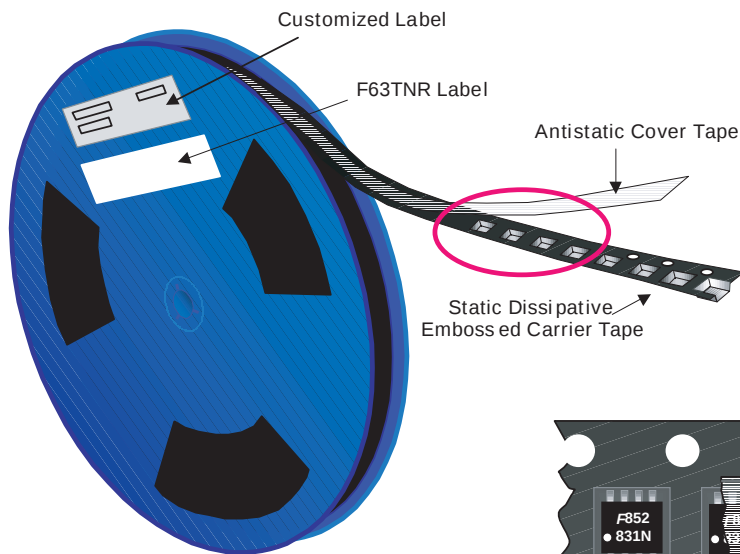


Figure 27. N or P-Channel Switching Waveforms.

SuperSOT™-8 Tape and Reel Data and Package Dimensions



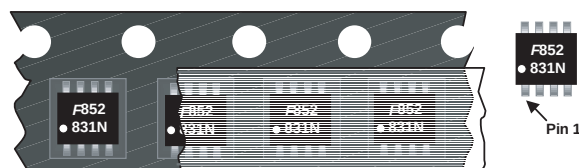
SSOT-8 Packaging Configuration: Figure 1.0



Packaging Description:

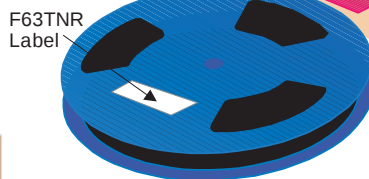
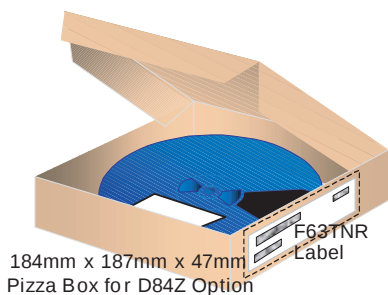
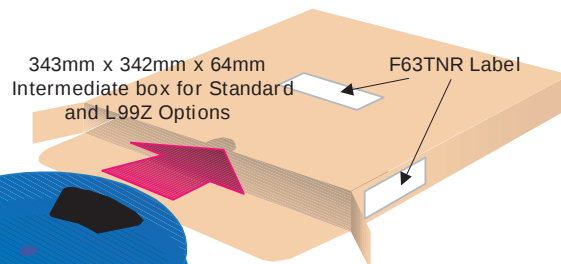
SSOT-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



SSOT-8 Unit Orientation

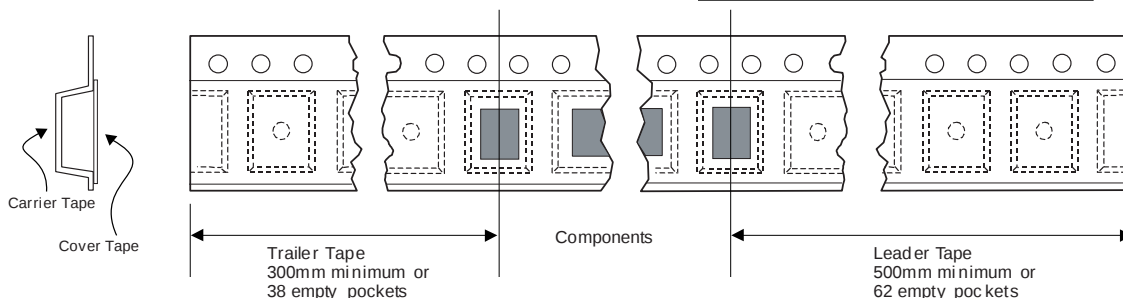
SSOT-8 Packaging Information		
Packaging Option	Standard (no flow code)	D84Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	500
Reel Size	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	184x187x47
Max qty per Box	6,000	1,000
Weight per unit (gm)	0.0416	0.0416
Weight per Reel (kg)	0.5615	0.0980
Note/Comments		



F63TNR Label sample

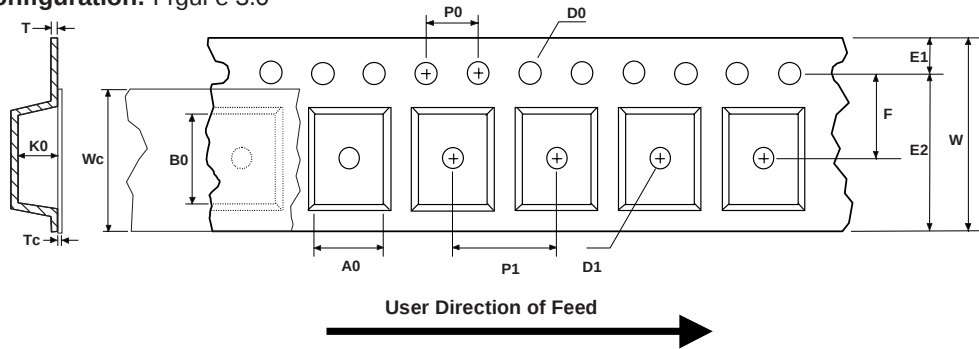
LOT: CBVK741B019	QTY: 3000
FSID: FDR835N	SPEC:
D/C1: D9842	QTY1:
D/C2:	QTY2:
SPEC REV: CPN:	N/F: F (F63TNR)3

SSOT-8 Tape Leader and Trailer Configuration: Figure 2.0



SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

SSOT-8 Embossed Carrier Tape Configuration: Figure 3.0

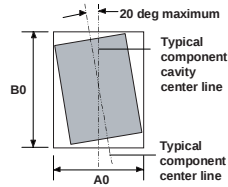


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SSOT-8 (12mm)	4.47 +/-0.10	5.00 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.280 +/-0.150	9.5 +/-0.025	0.06 +/-0.02

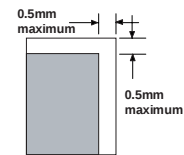
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

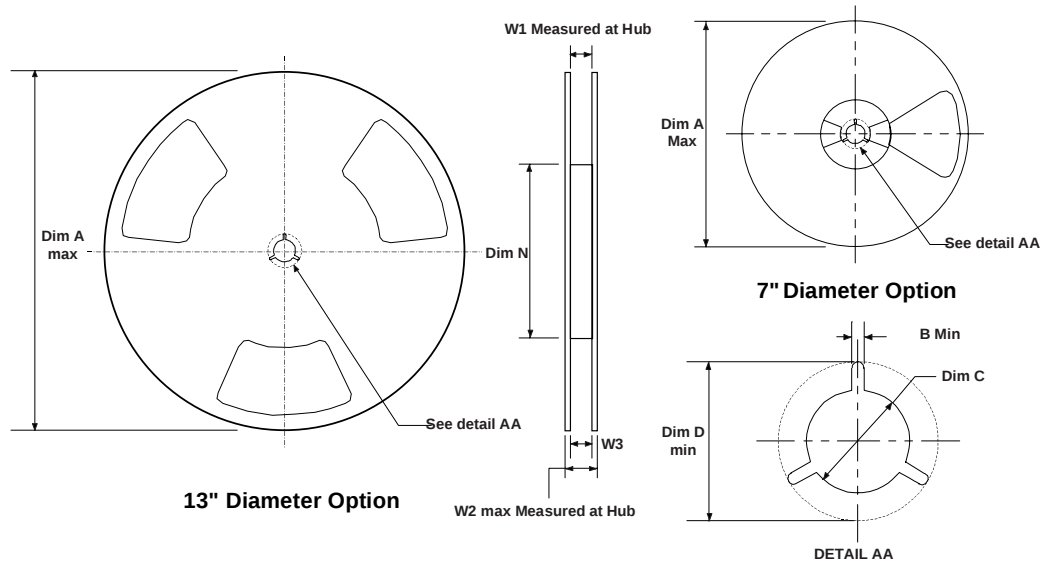


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

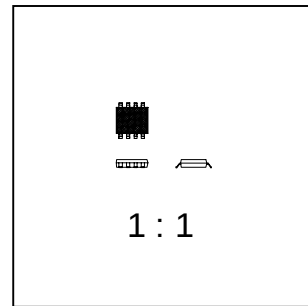
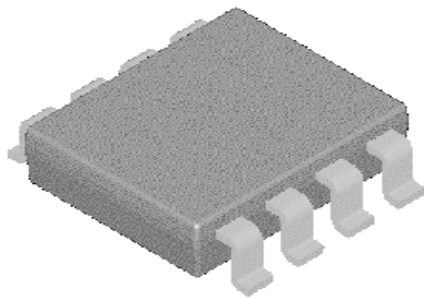
SSOT-8 Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	51.2 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	51.2 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

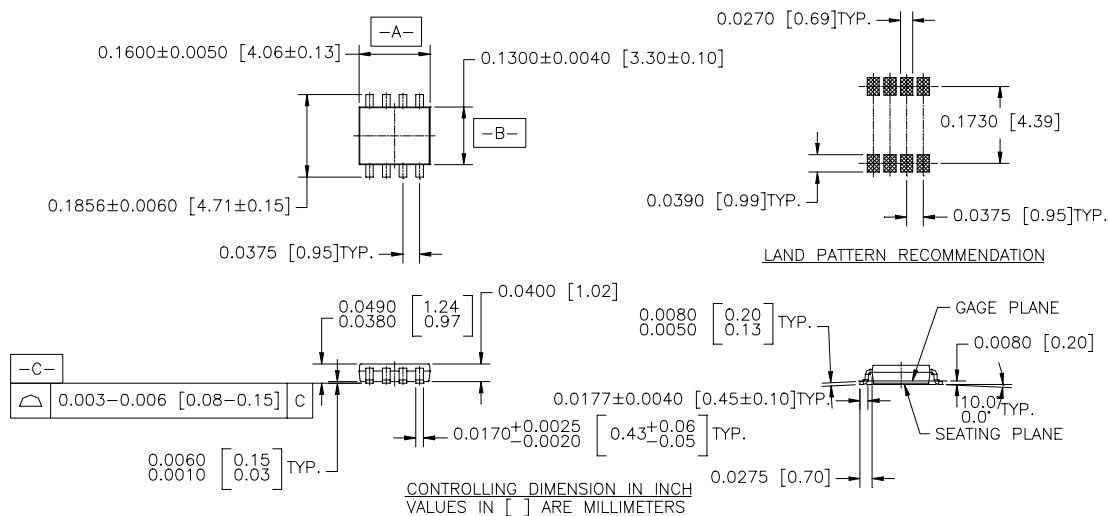
SuperSOT™-8 (FS PKG Code 34, 35)



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0416



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH TI BE 200 MICROINCHES / 5.08 MICROMETERS
MINIMUM TIN/LEAD (SOLDER) ON COPPER.
2. NO JEDEC REGISTRATION AS JAN. 1996

SUPER SOT, 8 LEADS

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE[™]
CoolFET[™]
CROSSVOLT[™]
E²CMOS[™]
FACT[™]
FACT Quiet Series[™]
FAST[®]
FAST[™]
GTO[™]
HiSeC[™]

ISOPLANAR[™]
MICROWIRE[™]
POP[™]
PowerTrench[™]
QFET[™]
QS[™]
Quiet Series[™]
SuperSOT[™]-3
SuperSOT[™]-6
SuperSOT[™]-8

TinyLogic[™]
UHC[™]
VCX[™]

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.