Nuvoton Maximum 3A, Ultra Low Dropout Regulator NCT3730S/ NCT3730S-L



NCT3730S/ S-L

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1. GENERAL DESCRIPTION

The NCT3730S/S-L is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 3A(peak). It operates with a VIN as low as 1.0V and control voltage 3V with output voltage programmable as low as 0.8V. The significant feature includes ultra low dropout, ideal for applications where VOUT is very close to VIN. Additionally, there is an enable pin to further reduce power dissipation while shutdown. The NCT3730S/S-L provides excellent regulation over variations in line, load and temperature, and provides a Power Good indicator to indicate if the voltage level of output voltage reaches 90% of its rating value.

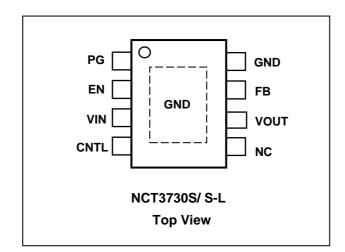
2. FEATURES

- Maximum 3A Ultra Low-Dropout Voltage Regulator
- High Accuracy Output Voltage ±1.5%
- Adjustable Output from 0.8V
- Typically 210mV Dropout at 3A
- Input Voltage as low as 1.0V
- Power Good Indicator
- Thermal and Over Current Protection
- EN internal Pull High (NCT3730S) and Internal Pull Low Available (NCT3730S-L)
- SOP-8 150mil with Exposed Pad Package
- Lead Free (ROHS Compliant) and Halogen Free Package

3. APPLICATIONS

- Desktop PCs, Notebooks, and Workstations
- Graphics Card
- Set Top Boxes, Digital TVs and Printers
- Portable instruments
- uP/ASIC/DSP/FPGA Core and I/O Supplies

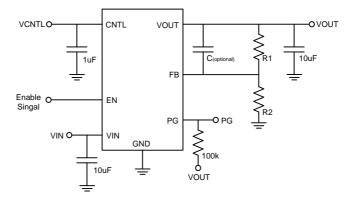
4. PIN CONFIGURATION AND DESCRIPTION



PIN NO.	PIN NAME	I/O	FUNCTION	
1	PG	0	Power Good indicator.	
2	EN	I	Chip Enable Input.	
3	VIN	Р	Supply Input Voltage.	
4	CNTL	Р	Supply Input Voltage for Control Circuit.	
5	NC	N/A	No Internal Connection.	
6	VOUT	Р	Output Voltage. VOUT = 0.8*(1+R1/R2)	
7	FB	I	Feedback Input.	
8	GND	Р	Ground.	

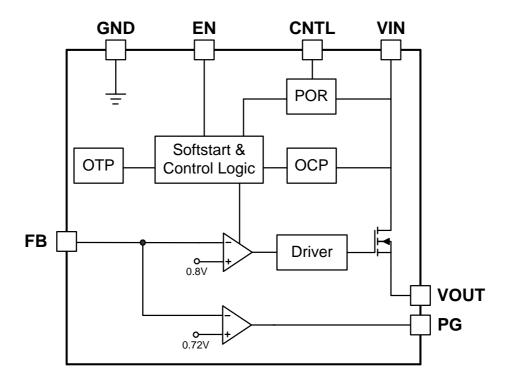


5. TYPICAL APPLICATION CIRCUIT



VOUT = 0.8*(1+R1/R2)

6. BLOCK DIAGRAM



7. FUNCTIONAL DESCRIPTION

The NCT3730S/S-L is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little pcb real estate. Additional features include an enable pin to allow for a very low power consumption at disable, and a fully adjustable output.

Output Voltage Selection

The output voltage of NCT3730S/S-L is adjustable from 0.8V to (VIN-VDROP) by external voltage divider resisters as shown in Typical Application Circuit. The value of resisters R1 and R2 should be more than $10k\Omega$ to reduce the power loss. The CNTL must be greater than (VOUT + 1.5V).

Input capacitor

A minimum of 10uF ceramic capacitor is recommended to be placed directly next to the VIN pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance of about \geq 10uF may be added closely to the input supply pin of the NCT3730S/S-L to ensure that VIN does not sag, improving load transient response.

Output capacitor

A minmum bulk capacitance of \geq 10uF, along with a 0.1uF ceramic decoupling capacitor is recommended. Increaseing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the NCT3730S/S-L is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Noise immunity

In very electrically noisy environments, it is recommended that 0.1uF ceramic capacitors be placed from VIN to GND and VOUT to GND as close to device pins as possible.

Power Good

The power good function is an open-drain output. Connects $100k\Omega$ pull up resistor to VOUT to obtain an output voltage. The PG pin will output high immediately after the output voltage arrives 90% of normal output voltage. The PG pin will output high with typical 4ms delay time.

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Enable

The NCT3730S/S-L goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 10uA typical. If the EN pin is floating, NCT3730S and NCT3730S-L operating behaviors are different. For NCT3730S, the EN pin function pulls high level internally. So the regulator will be turn on when EN pin is floating. As for NCT3730S-L, the EN pin function pulls low level internally. So the regulator will be turn off when EN pin is floating.

Current Limit

The NCT3730S/S-L contains an independent current limit and the short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, limiting the output current while higher than 4.5A typical. When the output voltage is less than 0.25V, the short circuit current protection starts the current fold back function and maintains the loading current 1.5A. The output can be shorted to ground indefinitely without damaging the part.

Thermal Consideration

The NCT3730S/S-L has a thermal shutdown circuitry to limit the junction temperature. When the junction temperature exceeds 150°C, the thermal shutdown circuit disables the output, allowing the device to cool down. The output circuitry is enabled again after the junction temperature cools down by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal protection is designed to protect the IC in the event of over temperature conditions. For reliabile operation, the junction temperature cannot exceed 125°C.

The definition of power dissipation in chip is as following equation:

 $\mathsf{P}_\mathsf{D} = (\mathsf{V}_\mathsf{IN} - \mathsf{V}_\mathsf{OUT}) \times \mathsf{I}_\mathsf{OUT} + \mathsf{V}_\mathsf{IN} \times \mathsf{I}_\mathsf{Q}$

 P_D represents the power dissipation.

The power dissipation depends on the thermal resistance of chip package, PCB layout, the airflow and temperature difference between junction and ambient. Refers to JEDEC51-1, The power dissipation can be calculated by following equation:

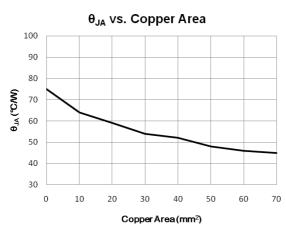
 $\mathsf{P}_{\mathsf{D}(\mathsf{MAX})} = (\mathsf{T}_{\mathsf{J}(\mathsf{MAX})} - \mathsf{T}_{\mathsf{A}}) / \theta_{\mathsf{J}\mathsf{A}}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125 °C , TA is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. θ_{JA} for ESOP-8 package is 75°C/W on JEDEC51-7 (4 layers, 2S2P) thermal test board with minimum copper area. The maximum power dissipation at $T_A = 25$ °C can be calculated as:

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$P_{D(MAX)} = (125^{\circ}C - 25^{\circ}C) / 75^{\circ}C/W = 1.33W$

 θ_{JA} highly depends on IC package, PCB layout, the aireflow. Thermal resistance θ_{JA} can be improved by adding copper under the exposed pad of ESOP-8 while the IC package is fixed. The copper under the exposed pad of ESOP-8 is an effective heatsink and is useful for improving thermal conductivity. Figure show the relationship between thermal resistance θ_{JA} vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at TA = 25°C, PCB copper thickness = 2oz. The 70mm² copper plane reduce θ_{JA} from 75°C/W to 45°C/W and increases maximum power disspation from 1.33W to 2.22W.



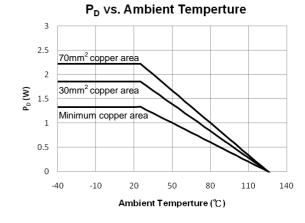


Figure01. Thermal Resistance $\theta_{JA} \mbox{ vs.}$ Copper Area of ESOP Packages

Figure02. Power dissipation vs. ambient temperature

8. ELECTRICAL CHARACTERISTIC

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Input Supply Voltage, VCNTL and VIN	-0.3 to 6V	V
Other Pins	-0.3 to 6V	V
Power Dissipation, PD @ TA=25°C	Internal Limited	W
Package Thermal Resistance, SOP8-EP, θ_{JA}	75	°C/W
θ _{JC}	15	°C/W
Storage Temperature	-50 to 150	°C
Junction Temperature	150	°C

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Р	ARAMETER	RATING	UNIT
	Human Body Mode	2	kV
ESD Protection	Machine Mode	200	V
	Latch-up	100	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 Recommended Operating Conditions

PARAMETER	RATING	UNIT
CNTL Voltage, VCNTL	3.0 to 5.5	V
Supply Voltage, VIN	1.0 to VCNTL	V
Output Current, IOUT	0 to 3	А
Operating Temperature	-40 to 85	°C
Junction Temperature	-40 to 125	°C

8.3 DC Electrical Characteristics

(VIN = VOUT + 500mV, VEN = VIN = 5V, CIN = COUT = 10uF, TA = TJ = 25° C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Supply voltage							
Control Input Voltage	V _{CNTL}	VOUT = VREF	3.0		5.5	V	
POR Threshold		VCNTL Rising		2.7		V	
POR Hysteresis				0.2		V	
Power Input Voltage	V _{IN}	VOUT = VREF	1.0		5.5	V	
Control Input Current in shutdown	I _{CNTL_SD}	VCNTL = VIN = 5.0V, IOUT = 0A, VOUT = VREF	20 30		30	uA	
Control Input Current	I _{CNTL}	VCNTL = VIN = VEN = 5.0V, IOUT = 0A, VOUT = VREF	400 600		600	uA	
Quiescent Current	Ι _Q	VCNTL = VIN = VEN = 5.0V, IOUT = 0A, VOUT = VREF	0.6 1		mA		
Feedback Voltage							
Reference Voltage V _{FB} VCN		VCNTL = VIN = VEN = 5.0V, IOUT = 0A, VOUT = VREF	0.788	0.8	0.812	V	
Feedback Input Current	I _{FB}	I _{FB} 20			nA		
VIN Line Regulation		1.2V < VIN < 5.0V, VCNTL = VEN = 5.0V, IOUT = 0A, VOUT = VREF	0.01 0.1		%/V		
VCNTL Line Regulation		3.0V < VCNTL < 5.0V, VIN = 1.2V, IOUT = 0A, VOUT = VREF	0.2 0.6		%/V		

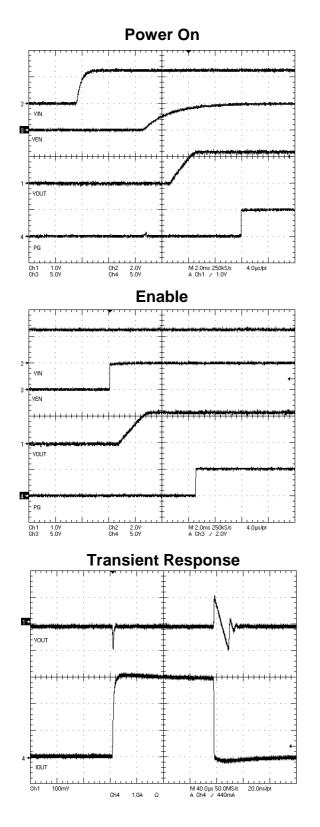
NCT3730S/ S-L

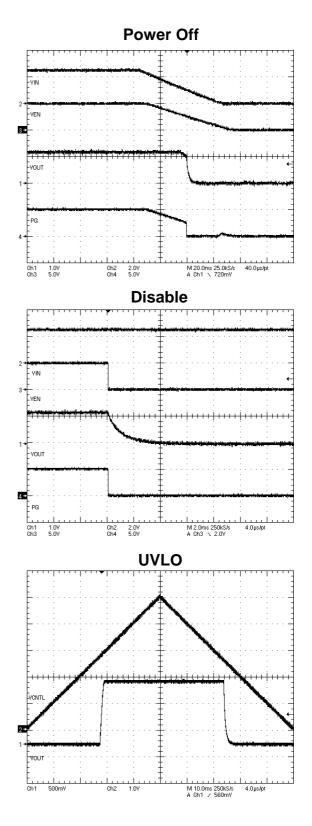
PARAMETER SYMBOL		CONDITIONS	MIN	TYP	MAX	UNIT
Load Regulation		0A < I _{LOAD} < 3A, VCNTL = VIN = VEN = 5.0V, VOUT = VREF		0.8	1.5	%/A
Load Regulation over Temperature		0mA < ILOAD < 3A, VCNTL = VIN = VEN = 5.0V, VOUT = VREF, -40 < TJ < 125, by design		1.4	3	%
Dropout Voltage	V _{DROP}	IOUT = 2.0A, VCNTL = VEN = 5.0V, VOUT = VREF			250	mV
Dropout Voltage	V _{DROP}	IOUT = 3.0A, VCNTL = VEN = 5.0V, VOUT = VREF		210	350	mV
VOUT Pull Low Resistance		VCNTL = VIN = 5.0V, VEN = 0V		90		Ω
Enable						
Enable High Level	V _{EN}		1.4			V
Enable Low Level	V _{SD}				0.4	V
Enable Current	rent I_{EN} VEN = 0V or 5V for NCT3730S/S-L, VCNTL = 5.0V			12	20	uA
Softstart Time			1.5	3.0	4.5	ms
PG						
FB Power OK Threshold	r OK Threshold V _{POKTH} IOUT = 0A, VCNTL = VIN = VEN = 5.0V, VOUT = VREF 9		90		%	
Power OK Hysteresis	V _{POKHYS}	IOUT = 0A, VCNTL = VIN = VEN = 5.0V, VOUT = VREF		8		%
PG sink Capability IPG = 10		IPG = 10mA		0.2	0.4	V
PG Delay Time		From VOUT >92% VNOM to PG rising		4		ms
Overcurrent Protection	on					
OCP Threshold Level	I _{OCP} VCNTL = VIN = VEN = 5.0V, VOUT 4.5			А		
Short Circuit Output Current		VCNTL = VIN = VEN = 5.0V, VOUT = 0V		1.5		А
Thermal Protection				1		•
Themal Shutdown Temperature	T _{SD}	IOUT = 0A, VCNTL = VIN = VEN = 5.0V, VOUT = VREF 150		150		°C
Thermal Shutdown Hysteresis	T _{SDHYS}	IOUT = 0A, VCNTL = VIN = VEN = 5.0V, VOUT = VREF		50		°C

Note1. The dropout voltage is defined as VIN – VOUT, which is measured when VOUT is VOUT(normal) – 100mV.

Note2. The device is not guaranteed to function ouside its operating conditions.

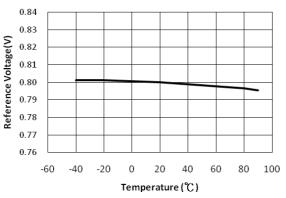
9. TYPICAL OPERATING WAVEFORMS





Publication Release Date: Feb, 2011 Version: A4

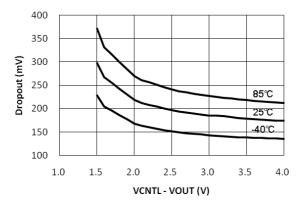
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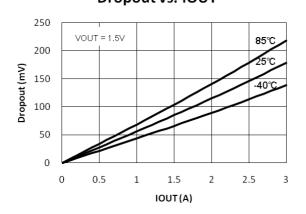
CNTL POR Threshold Voltage vs. Temperature 2.90 2.85 POR Threshold Voltage(V) 2.80 2.75 2.70 2.65 Rising 2.60 2.55 Falling 2.50 2.45 2.40 -40 -20 0 20 40 60 80 100 Temperature (℃)

Reference Voltage vs. Temperature

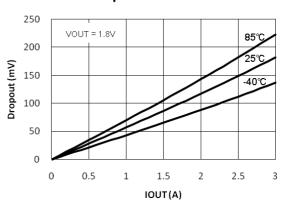
Dropout vs. VCNTL-VOUT



Dropout vs. IOUT



Dropout vs. IOUT

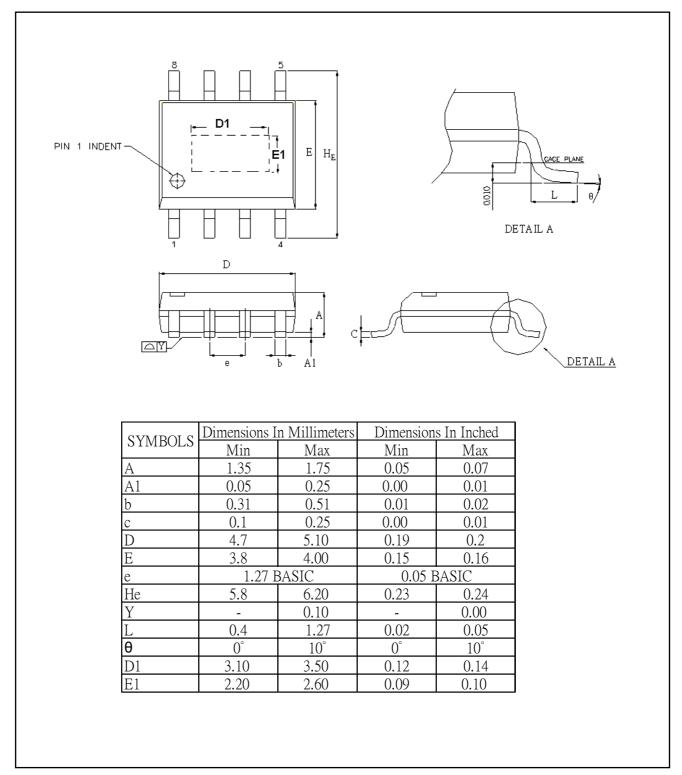


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10. PACKAGE DIMENSION

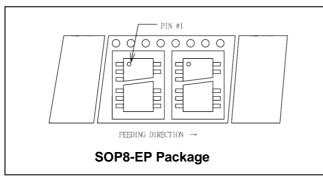
SOP8-EP (150mil)



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10.1 Taping Specification

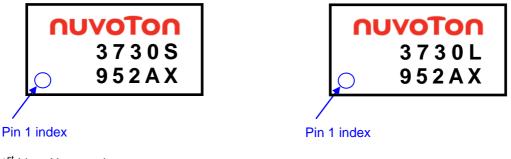


11. ORDERING INFORMATION

Part Number	Package Type	Supplied as	Production Flow
NCT3730S	SOP8-EP (Green Package)	2,500 units/T&R	Commercial, -40 $^\circ\!C$ to 85 $^\circ\!C$
NCT3730S-L	SOP8-EP (Green Package)	2,500 units/T&R	Commercial, -40°C to 85°C

12. 6TOP MARKING SPECIFICATION

12.1 Adjustable Output Voltage



1st Line: Nuvoton logo

2nd Line: 3730S (Part number NCT3730S); 3730L (Part number NCT3730S-L)

3rd line: Tracking code

- <u>952</u>: packages assembled in Year 2009, week 52
- <u>A</u>: assembly house ID
- <u>X</u>: internal use only

VERSION	DATE	PAGE	DESCRIPTION
A0	01/04/2010	All	New Create.
A1	07/20/2010	P4, 5, 6	Add Thermal consideration & modify some typos.
A2	09/30/2010	P3, 8, 9	Add waveform & modify some description.
A3	11/26/2010	All	Add NCT3730S-L part number and relative data.
A4	02/18/2011	All	Revised some description.

13. REVISION HISTORY

Important Notice

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