

RGB/LVDS-to-eDP Converter

1 Features

Embedded-DisplayPort (eDP) Output

2-lane/4-lane eDP @ 1.62/2.7Gbps per lane
FHD to WQXGA (2560*1600) supported
Up to 6dB pre-emphasis

RGB Input

18/24bit RGB Interface
Pixel clock up to 270MHz
SDR/DDR supported
Pin order reversal supported

LVDS Input

Dual-channel 6/8bit LVDS (Sync) interface
400Mbps to 1Gbps per data pair
Built-in termination
Channel and polarity swap supported

Reference Clock

Any freq. between 19MHz and 100MHz
Crystal or single-ended clock input
Built-in 5000ppm SSC generator

Misc

I²C/SPI for chip configuration
Built-in eDP handshake protocol
I²C-AUX channel for TCON/DPCD/EDID control
Built-in video test pattern

Power

1.2V core supply
2.5V or 3.3V IO supply
RGB IO can go down to 1.8V

Power consumption ~ 70mW

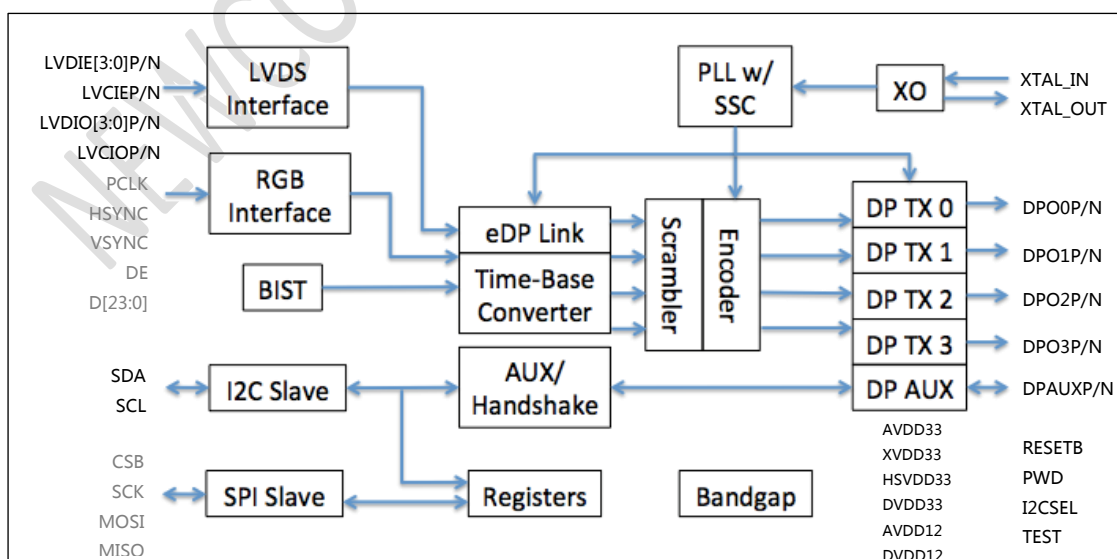
@ 2048*1536*24bit*60Hz, LVDS mode

Deep-sleep mode power <1mW

Package

QFN-56 (7mm x 7mm) package
RoHS Compliant

2 Block Diagram



3 General Description

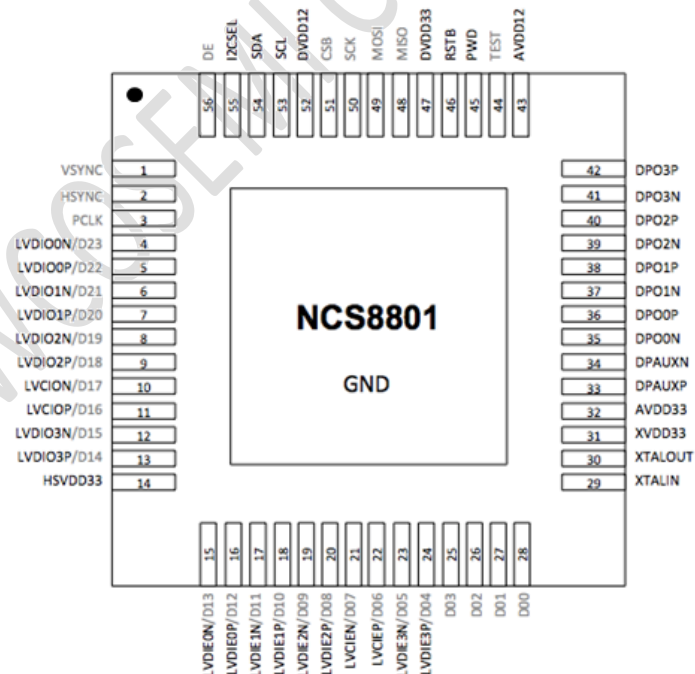
NCS8801 is an ultra-low-power RGB/LVDS-to-DisplayPort/eDP converter, which is designed for mobile devices including smartphones, tablets, laptops, etc. to support high-definition DP/eDP displays.

NCS8801 supports 4-lane DP/eDP output which is typically required to support QXGA (2048*1536) and above at 60Hz frame rate.

Thanks to the various proprietary circuit design techniques used in the chip, NCS8801 consumes only 70mW when operating at 2048*1536, 24bit, 60Hz, LVDS input, 4-lane eDP output mode. Mobile devices appreciate this low power consumption.

All the functions including both RGB and LVDS interfaces pack into a small 7mm*7mm QFN56 package which saves the precious space in mobile devices.

4 Pin Diagram



5.1 Pin Description (LVDS+I²C Mode)

No.	Pin Name	Description
1	VSYNC	Connect to ground in LVDS mode
2	HSYNC	Connect to ground in LVDS mode
3	PCLK	Connect to ground in LVDS mode
4	LVDDIO0N	LVDS data channel 0 negative, odd pixel
5	LVDDIO0P	LVDS data channel 0 positive, odd pixel
6,7	LVDDIO1N,P	LVDS data channel 1, odd pixel
8,9	LVDDIO2N,P	LVDS data channel 2, odd pixel
10,11	LVDDION,P	LVDS clock channel, odd pixel
12,13	LVDDIO3N,P	LVDS data channel 3, odd pixel
14	HSVDD33	2.5/3.3V power supply for LVDS
15,16	LVDDIE0N,P	LVDS data channel 0, even pixel
17,18	LVDDIE1N,P	LVDS data channel 1, even pixel
19,20	LVDDIE2N,P	LVDS data channel 2, even pixel
21,22	LVDDIEN,P	LVDS clock channel, even pixel
23,24	LVDDIE3N,P	LVDS data channel 3, even pixel
25~28	D3~D0	Connect to ground in LVDS mode
29	XTALIN	Crystal or clock input
30	XTALOUT	Crystal
31	XVDD33	2.5/3.3V power supply for crystal oscillator
32	AVDD33	2.5/3.3V power supply for analog
33	DPAUXP	eDP AUX channel positive
34	DPAUXN	eDP AUX channel negative
35	DPO0N	eDP data channel 0 negative
36	DPO0P	eDP data channel 0 positive
37,38	DPO1N,P	eDP data channel 1
39,40	DPO2N,P	eDP data channel 2
41,42	DPO3N,P	eDP data channel 3
43	AVDD12	1.2V power supply for analog
44	TEST	Not connected
45	PWD	Power down, active high
46	RSTB	Reset, active low
47	DVDD33	2.5/3.3V power supply for digital I/Os
48	MISO	Not connected in I ² C mode
49	MOSI	Connect to ground in I ² C mode
50	SCK	Connect to ground in I ² C mode
51	CSB	Connect to DVDD33 in I ² C mode
52	DVDD12	1.2V power supply for digital core
53	SCL	I ² C clock
54	SDA	I ² C data
55	I2CSEL	Connect to DVDD33 in I ² C mode
56	DE	Connect to ground in LVDS mode
Thermal	GND	Ground

5.2 Pin Description (RGB+I²C Mode)

No.	Pin Name	Description
1	VSNC	Vertical synchronization
2	HSNC	Horizontal synchronization
3	PCLK	Pixel clock
4~11	D23~D16	RGB data 23~16, R[7:0] in default mode
12~13	D15~D14	RGB data 15~14, G[7:6] in default mode
14	HSVDD33	1.8/2.5/3.3V power supply for RGB interface
15~20	D13~D8	RGB data 13~8, G[5:0] in default mode
21~28	D7~D0	RGB data 7~0, B[7:0] in default mode
29	XTALIN	Crystal or clock input
30	XTALOUT	Crystal
31	XVDD33	2.5/3.3V power supply for crystal oscillator
32	AVDD33	2.5/3.3V power supply for analog
33	DPAUXP	eDP AUX channel positive
34	DPAUXN	eDP AUX channel negative
35	DPO0N	eDP data channel 0 negative
36	DPO0P	eDP data channel 0 positive
37,38	DPO1N,P	eDP data channel 1
39,40	DPO2N,P	eDP data channel 2
41,42	DPO3N,P	eDP data channel 3
43	AVDD12	1.2V power supply for analog
44	TEST	Not connected
45	PWD	Power down, active high
46	RSTB	Reset, active low
47	DVDD33	2.5/3.3V power supply for digital IOs
48	MISO	Not connected in I ² C mode
49	MOSI	Connect to ground in I ² C mode
50	SCK	Connect to ground in I ² C mode
51	CSB	Connect to DVDD33 in I ² C mode
52	DVDD12	1.2V power supply for digital core
53	SCL	I ² C clock
54	SDA	I ² C data
55	I2CSEL	Connect to DVDD33 in I ² C mode
56	DE	Data enable
Thermal	GND	Ground

6 Electrical Specifications

6.1 Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD33	2.5/3.3V power supply for analog	2.38	3.3	3.46	V
DVDD33	2.5/3.3V power supply for digital	2.38	3.3	3.46	V
XVDD33	2.5/3.3V power supply for crystal oscillator	2.38	3.3	3.46	V
HSVDD33	2.5/3.3V power supply for RGB mode	1.71	3.3	3.46	V
	2.5/3.3V power supply for LVDS mode	2.38	3.3	3.46	V
AVDD12	1.2V power supply for analog	1.14	1.2	1.26	V
DVDD12	1.2V power supply for digital core	1.14	1.2	1.26	V
f _{CLK-XTAL}	crystal or single-ended clock input freq.	19	24	100	MHz
Temp	Ambient temperature	-20	25	85	°C
ESD	HBM			3	kV
	CDM			250	V
	MM			200	V

6.2 Power Consumption

Mode	Power		
	VDD33	VDD12	Power
2048*1536 @ 60Hz	4mA	56.4mA	66.4mW ¹
Deep-sleep	-	0.24mA	0.29mW

Note: 1. VDD33=2.5V, VDD12=1.2V, LVDS input, 4-lane*1.6Gbps eDP output, TX diff p-p voltage 200mV.

6.3 eDP Main Channel Electrical Specification

Symbol	Description	Min	Typ	Max	Units
UI_HBR	Unit interval for high bit rate(2.7 Gbps/ lane)		370		ps
UI_LBR	Unit interval for low bit rate(1.62 Gbps/ lane)		617		ps
Down-spread amp.	Link clock down spreading	0		5000	ppm
Down-spread freq.	Link clock down spreading frequency	30		33	kHz
V _{TXpp}	Differential peak-to-peak	0.1	0.6	1.2	V
T _{TX-EYE}	TX eDP output minimum eye width	0.726			UI
	No pre-emphasis		0		dB
	3.5 dB pre-emphasis Level		3.5		dB
	6.0 dB pre-emphasis Level		6		dB
V _{TX-DC-CM}	TX DC common mode voltage	0		1.2	V
C _{TX}	AC coupling capacitor	75	100	200	nF

6.4 eDP AUX channel Electrical Specifications

Symbol	Description	Min	Typ	Max	Units
UI	AUX unit interval	0.4	0.5	0.6	us
Pre-charge pulses	Number of pre-charge pulses	10		16	
T _{AUX-BUS-PARK}	AUX CH bus park time	10			ns
V _{AUX-DIFFpp}	AUX peak-to-peak voltage	0.4		1.2	V
V _{AUX-DC-CM}	AUX DC common mode voltage	0		1.2	V
C _{AUX}	AUX AC coupling capacitor	75	100	200	nF

6.5 LVDS Electrical Specification

Symbol	Description	Min	Typ	Max	Units
Rate _{LVDS}	LVDS data rate per pair	400		1000	Mbps
f _{CLK-LVDS}	LVDS input clock frequency	57		143	MHz
V _{TH-LVDS}	Differential input high threshold			0.1	V
V _{TL-LVDS}	Differential input low threshold	-0.1			V
V _{CM-LVDS}	LVDS common mode voltage	0.9		1.4	V

6.6 RGB Electrical Specification

Symbol	Description	Min	Typ	Max	Units
f _{CLK-RGB-SDR}	RGB input clock frequency in SDR mode			270	MHz
f _{CLK-RGB-DDR}	RGB input clock frequency in DDR mode			135	MHz
V _{IH}	High level input voltage	HSVDD33-0.3		HSVDD33 ¹	V
V _{IL}	Low level input voltage	0		0.3	V

Note: 1. HSVDD33 can go down to 1.8V in RGB mode.

7 Register Table

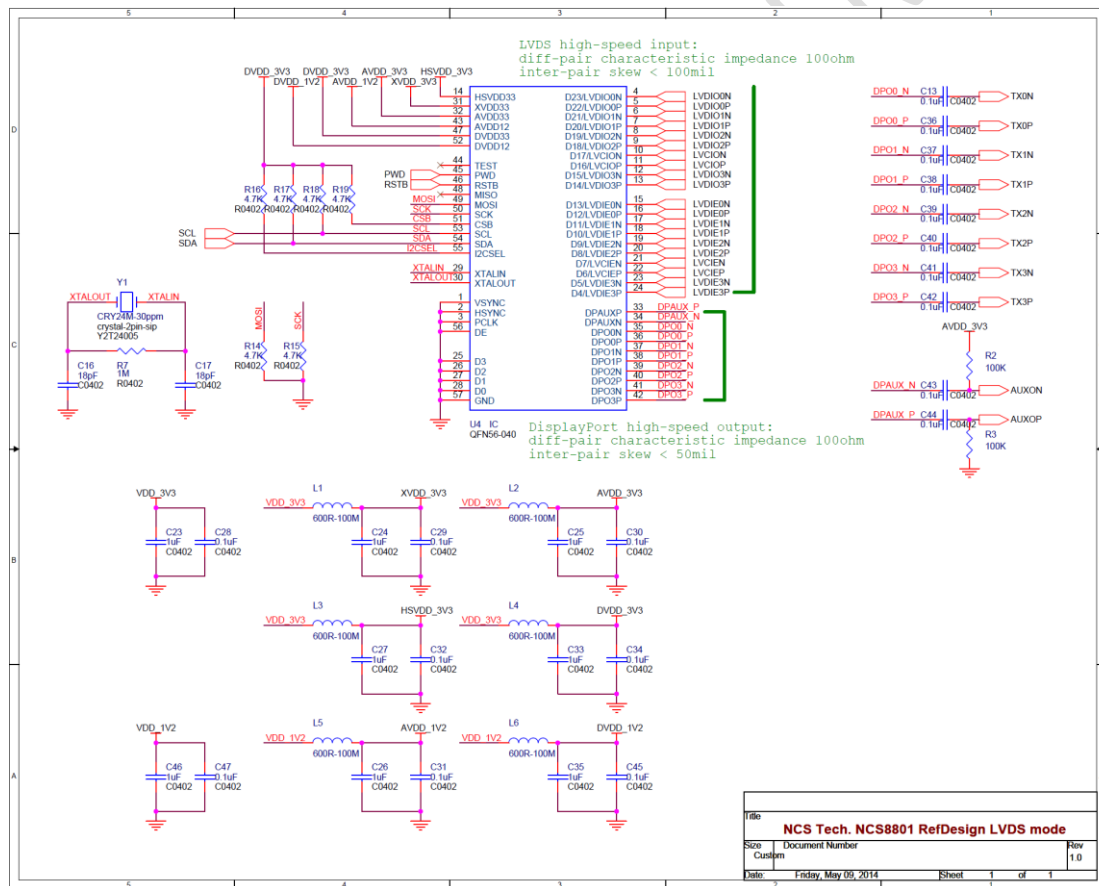
Addr.	R/W	Description	Default (HEX)
0x00	R/W	Bit0: pixel bit width 0: 24bit 1: 18bit Bit1: eDP lane configuration 0: 4 lanes 1: 2 lanes Bit2: eDP lane speed 0: 2.7Gbps 1: 1.62Gbps Bit3: hardware training 0: disable 1: enable	04
0x05	R/W	Bit0: eDP main ch lane 0 polarity inverse Bit1: eDP main ch lane 1 polarity inverse Bit2: eDP main ch lane 2 polarity inverse Bit3: eDP main ch lane 3 polarity inverse	00
0x09	R/W	Bit0: No video mode 0: normal 1: no video mode	00
0x0C	R/W	Bit0: input mode select 0: LVDS mode 1: RGB mode Bit1: LVDS data mode select 0: NS mode 1: JEIDA mode	01
0x0D	R/W	Bit0: eDP lane order reverse (4 lane mode only) 0: normal 1: lane0_new<=lane3 lane1_new<=lane2 lane2_new<=lane1 lane3_new<=lane0	00
0x0F	R/W	Bit0: LVDS DATA polarity inverse Bit1: LVDS O/E channel swap	00
0x10	R/W	Htotal (Hsync + HBP + Hactive + HFP) upper-byte	08
0x11	R/W	Htotal (Hsync + HBP + Hactive + HFP) lower-byte	A0
0x12	R/W	Hstart (Hsync + HBP) upper-byte	00
0x13	R/W	Hstart (Hsync + HBP) lower-byte	0A
0x14	R/W	Hactive (Hactive) upper-byte	08
0x15	R/W	Hactive (Hactive) lower-byte	00
0x16	R/W	Vtotal (Vsync + VBP + Vactive + VFP) upper-byte	06
0x17	R/W	Vtotal (Vsync + VBP + Vactive + VFP) lower-byte	0D
0x18	R/W	Vstart (Vsync + VBP) upper-byte	00
0x19	R/W	Vstart (Vsync + VBP) lower-byte	0A

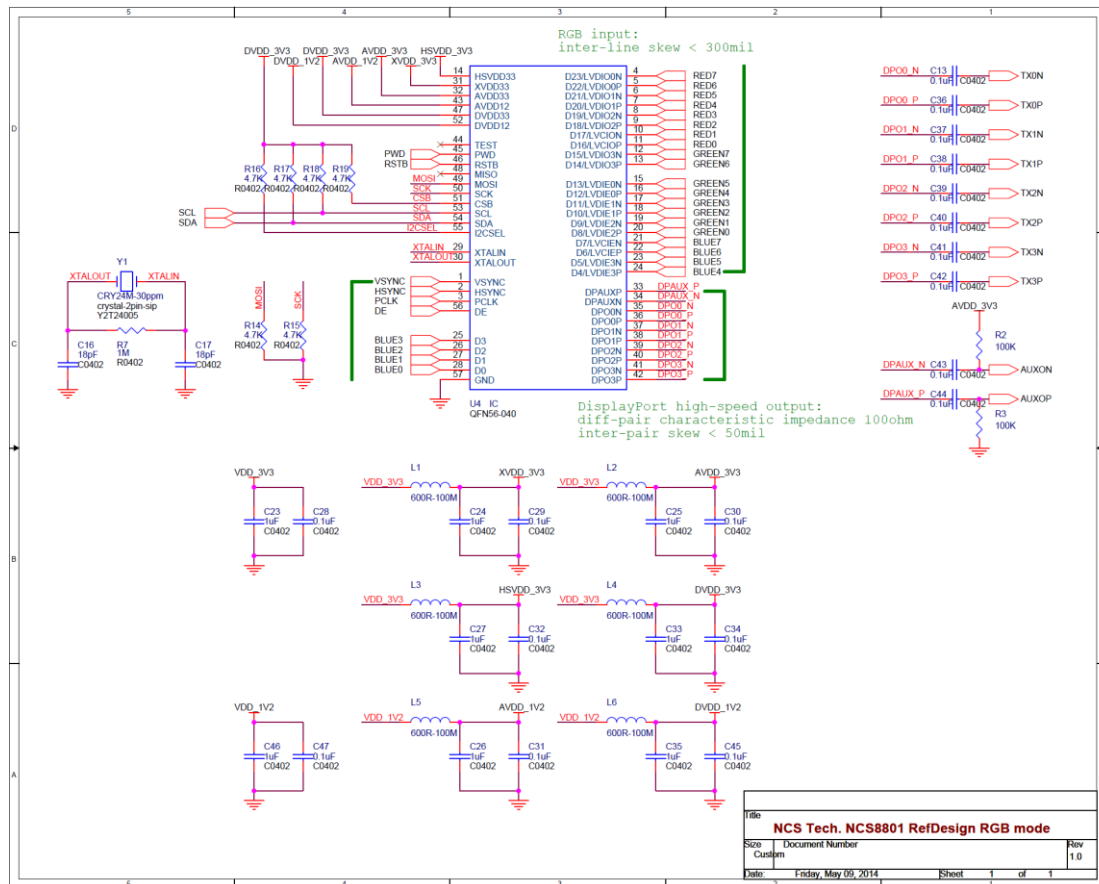
0x1A	R/W	Vactive upper-byte	06
0x1B	R/W	Vactive lower-byte	00
0x1C	R/W	Hsync polarity control MSB: H_polarity 0: Hsync active high, 1: Hsync active low	80
0x1D	R/W	Hsync width (Hsync)	05
0x1E	R/W	Vsync polarity control MSB: V_polarity 0: Vsync active high, 1: Vsync active low	80
0x1F	R/W	Vsync width (Vsync)	01
0x20	R/W	Bit0: BIST mode enable	00
0x21	R/W	R component in BIST mode	00
0x22	R/W	G component in BIST mode	00
0x23	R/W	B component in BIST mode	00
0x2C	R	eDP lane0/1 training results Bit0: lane0_CR_done Bit1: lane0_channel_EQ_done Bit2: lane0_symbol_locked Bit4: lane1_CR_done Bit5: lane1_channel_EQ_done Bit6: lane1_symbol_locked	00
0x2D	R	eDP lane2/3 training results	00
0x30	R/W	Bit7: eDP lane speed 0: 1.6Gbps 1: 2.7Gbps Bit0: soft analog reset 0: soft analog reset 1: normal	31
0x35	R/W	Bit6: eDP lane speed 0: 1.6Gbps 1: 2.7Gbps	01
0x3C	R/W	eDP TX amplitude (differential peak-to-peak) 0x06: 200mV 0x0d: 400mV 0x18: 600mV 0x23: 800mV	17
0x3E	R/W	eDP TX termination Bit4: termination control enable Bit0~3: termination resistance 0x6: 125ohm 0x8: 100ohm 0xa: 80ohm	00
0x4B	R/W	Bit2: LVDS mode enable 0: disable 1: enable Bit1: RGB timing mode 0: SDR mode 1: DDR mode	00

		Bit0: RGB SDR timing 0: rising edge 1: falling edge	
0x7F	R/W	Bit0: digital reset 0: soft digital reset 1: normal	01

8 Applications

8.1 Typical Application Schematics

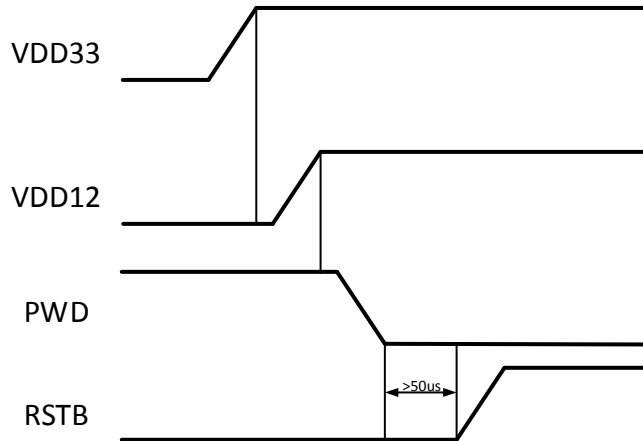




8.2 PCB Layout Rules

- Due to the high data rate of the eDP signal, characteristic impedance throughout the signal path needs to be well controlled. It is highly suggested to control the differential characteristic impedance of the PCB trace to be within $100\text{ohm} \pm 10\%$. Low speed connectors are highly suggested to be avoided in the eDP signal path, especially in the 2.7Gbps mode.
- The requirement on the LVDS side is less stringent but impedance discontinuities including Y-branching are highly suggested to be minimized.
- The crosstalk and length of the RGB traces needs to be minimized.
- The intra-pair mismatch in all differential pairs needs to be avoided.
- eDP inter-lane skew is suggested to be controlled under 50mil.
- LVDS inter-lane skew is suggested to be controlled under 100mil.
- RGB inter-line skew is suggested to be controlled under 300mil.

8.3 Power-on Sequence



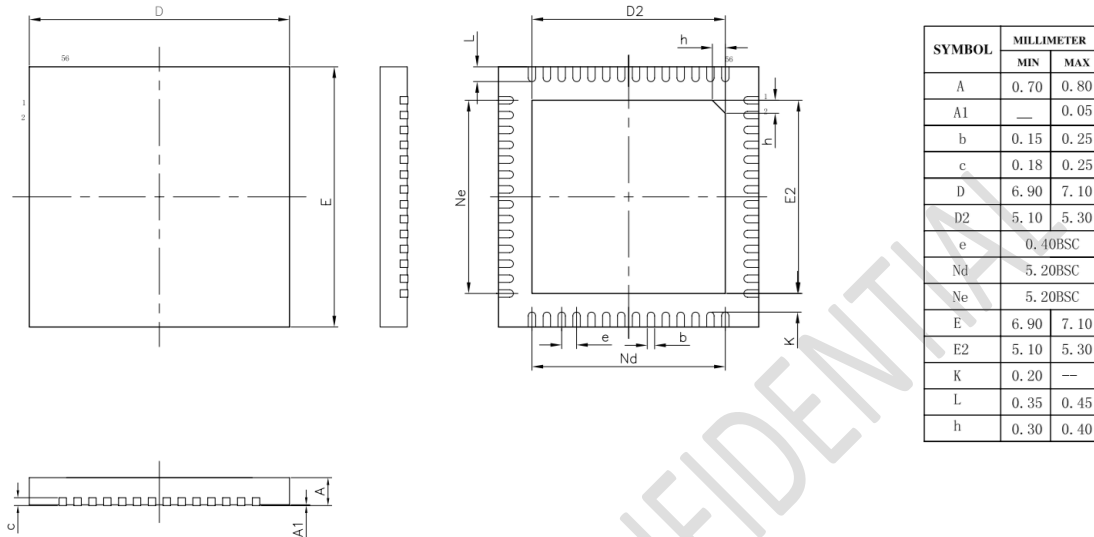
8.4 Typical Initialization Procedure

(I2C device ID of the chip is 0x70, write to address 0xE0, read from address 0xE1).

- Configure register 0x09 to 01, to enter no video mode.
- Configure register 0x4B, to choose between RGB and LVDS modes.
- Configure register 0x0C, to choose between RGB and LVDS modes.
- Configure registers 0x10-0x1F according to the display timing.
- Configure register 0x35 to 41 if the lane rate is 2.7Gbps.
- Configure register 0x30 to B0 if the lane rate is 2.7Gbps.
- Configure register 0x30 to B1 if the lane rate is 2.7Gbps.
- Configure register 0x00 according to the display mode, with bit 3 set to 1.
- Configure register 0x09 to 00, to exit no video mode.

9 Package

NCS8801 is packaged in 7mm*7mm 56-pin QFN, QFN56L (0707*0.75-0.40). The package dimensions are shown below. (Unit: mm)



10 Revision History

Rev. #	Date	Author	Comments
0.8	08/19/2013	Deyi Pi	First beta release
0.92	12/10/2013	Xin Zhang	Second beta release
1.0	03/17/2014	Xin Zhang	Initial release with application notes added. Register 35 revised. Signal amplitude levels updated.
1.1	04/29/2014	Xin Zhang	Registers 09, 2C, 2D, 30, 3C, 3E, 7F added to the table.

This document contains information on a new product. Specifications and information herein are subject to change without notice.