8 MHz, Rail-To-Rail, CMOS Operational Amplifier

NCS20161, NCS20162, NCS20164, NCV20161, NCV20162, NCV20164

The NCS20161, NCS20162, and NCS20164 are a family of single, dual and quad operational amplifiers (op amps) that provide 8 MHz gain−bandwidth product while consuming 500 μA of quiescent current per channel. The NCS2016x has an input offset voltage of 0.3 mV and operates from 1.8 V to 5.5 V supply over a wide temperature range (−40°C to 125°C). The rail−to−rail input and output operation allows the use of the entire supply voltage range. Thus, this series of op amps offers superior performance over many industry standard parts. These devices are AEC−Q100 qualified when denoted by the NCV prefix.

With low current consumption and low supply voltage operation in industry standard packages, the NCS20161 series is ideal for sensor signal conditioning and low voltage current sensing applications in automotive, consumer and industrial markets.

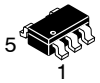
Features

- Gain−Bandwidth Product: 8 MHz
- Low Supply Current per Channel: 500 μA typ (V_S = 5.5 V)
- Low Input Offset Voltage: ±0.3 mV
- Wide Supply Range: 1.8 V to 5.5 V
- Wide Temperature Range: −40°C to +125°C
- Rail−to−Rail Input and Output
- Unity Gain Stable
- Available in Single, Dual and Quad Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

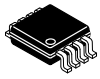
Applications

- Automotive
- Battery Powered / Portable
- Sensor Signal Conditioning
- Low Voltage Current Sensing
- Filter Circuits
- Unity Gain Buffer

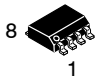
SC70−5
CASE 419A



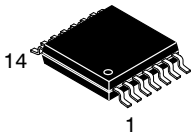
TSOP−5/SOT23−5
CASE 483



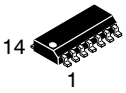
Micro8™/MSOP8
CASE 846A



SOIC−8
CASE 751



TSSOP−14
CASE 948G



SOIC−14
CASE 751A

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

This document contains information on some products that are still under development. **onsemi** reserves the right to change or discontinue these products without notice.

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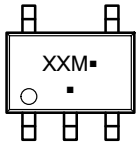
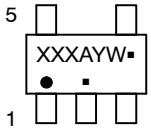
MARKING DIAGRAMS

Single Channel Configuration
NCS20161, NCV20161

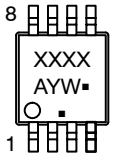


SC70−5
CASE 419A

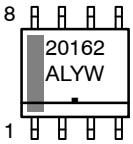


TSOP−5/SOT23−5
CASE 483

Dual Channel Configuration
NCS20162, NCV20162

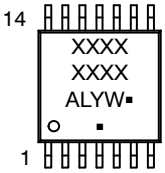


Micro8™/MSOP8
CASE 846A

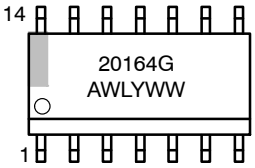


SOIC−8
CASE 751

Quad Channel Configuration
NCS20164, NCV20164



TSSOP−14
CASE 948G

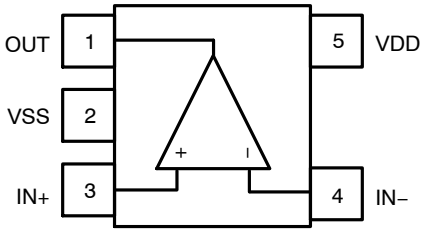


SOIC−14
CASE 751A

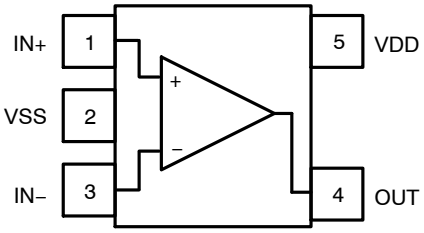
XXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

Single Channel Configuration
NCS20161, NCV20161

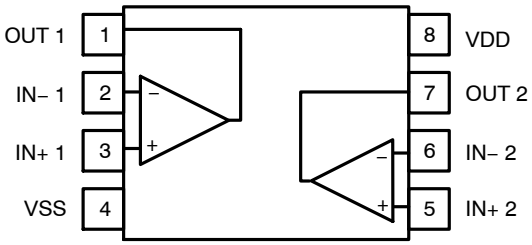


SOT23−5 (TSOP−5)
SN2 Pinout



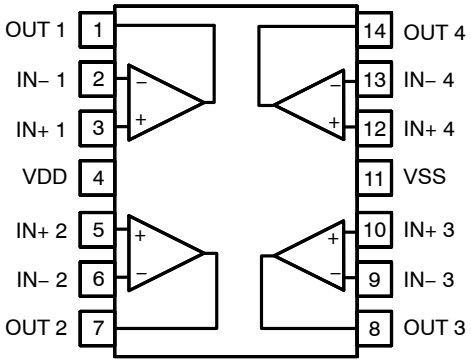
SC70−5
SQ3 Pinout

Dual Channel Configuration
NCS20162, NCV20162



Micro8/MSOP8, SOIC−8

Quadruple Channel Configuration
NCS20164, NCV20164



TSSOP−14, SOIC−14

Figure 1. Pin Connections

ORDERING INFORMATION

Device*	Configuration	Automotive	Marking	Package	Shipping†
NCS20161SQ3T2G**	Single	No	TBD	SC70	3000 / Tape and Reel
NCS20161SN2T1G**			TBD	SOT23−5/TSOP−5	3000 / Tape and Reel
NCV20161SQ3T2G**		Yes	TBD	SC70	3000 / Tape and Reel
NCV20161SN2T1G**			TBD	SOT23−5/TSOP−5	3000 / Tape and Reel
NCS20162DMR2G**	Dual	No	TBD	Micro8/MSOP8	4000 / Tape and Reel
NCS20162DR2G			20162	SOIC−8	2500 / Tape and Reel
NCV20162DMR2G**		Yes	TBD	Micro8/MSOP8	4000 / Tape and Reel
NCV20162DR2G			20162	SOIC−8	2500 / Tape and Reel
NCS20164DR2G	Quad	No	20164G	SOIC−14	2500 / Tape and Reel
NCS20164DTBR2G**			TBD	TSSOP−14	2500 / Tape and Reel
NCV20164DR2G		Yes	20164G	SOIC−14	2500 / Tape and Reel
NCV20164DTBR2G**			TBD	TSSOP−14	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

**In Development. Contact local sales office for more information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Limit	Unit
Supply Voltage (V_{DD} – V_{SS})	V_S	−0.3 to 6	V
Common Mode Input Voltage	V_I	V_{SS}−0.3 to V_{DD}+0.3	V
Differential Input Voltage	V_{ID}	V_{DD} – V_{SS}+0.2	V
Maximum Input Current	I_I	±10	mA
Maximum Output Current (Note 2)	I_O	±100	mA
Continuous Total Power Dissipation (Note 2)	P_D	200	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Mounting Temperature (Infrared or Convection – 20 sec)	T_{mount}	260	°C
ESD Capability (Note 3) Human Body Model Charge Device Model	HBM CDM	2500 1500	V
Latch−Up Current (Note 4)	I_{LU}	100	mA
Moisture Sensitivity Level (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS for Safe Operating Area.
2. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of the maximum output current rating over the long term may adversely affect reliability. Shorting output to either VDD or VSS will adversely affect reliability.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard Js−001−2017 (AEC−Q100−002)
   ESD Charged Device Model tested per JEDEC standard JS−002−2014 (AEC−Q100−011)
4. Latch−up Current tested per JEDEC standard JESD78E (AEC−Q100−004)
5. Moisture Sensitivity Level tested per IPC/JEDEC standard: J−STD−020A

OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage (V_{DD} – V_{SS})	V_S	1.8	5.5	V
Differential Input Voltage	V_{ID}	–	V_S	V
Common Mode Input Voltage Range	V_{CM}	V_{SS} – 0.1	V_{DD} + 0.1	V
Ambient Temperature	T_A	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS (Note 6)

Package	Junction−to−Ambient Thermal Resistance θ_{JA}	Junction−to−Case Top Thermal Resistance Ψ_{JT}	Junction−to−Board Thermal Resistance Ψ_{JB}	Unit
SOIC−8	205	32	116	°C/W
SOIC−14	138	8	100	°C/W

6. Thermal parameters are based on a 2s2p board following JESD51−7 (JEDEC).

ELECTRICAL CHARACTERISTICS AT V_S = 1.8 V to 5.5 V

T_A = 25°C; R_L ≥ 10 kΩ connected to mid−supply; V_{CM} = V_{OUT} = mid−supply unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C. (Note 7)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	V_S = 5 V	–	±0.3	±2.1	mV
		V_S = 5 V	–	–	±**2.6**	mV
Offset Voltage Drift	dV_{OS}/dT	V_S = 5 V	–	±**1.5**	–	µV/°C
Input Bias Current (Note 7)	I_{IB}		–	±5	–	pA
Input Offset Current (Note 7)	I_{OS}		–	±5	–	pA
Channel Separation		DC	–	100	–	dB
Input Capacitance	C_{IN}		–	4	–	pF
Common Mode Rejection Ratio	CMRR	V_S = 5.5 V, V_{CM} = V_{SS} − 0.1 V to V_{DD} − 1.4 V	**80**	**103**	–	dB
		V_S = 5.5 V, V_{CM} = −0.1 V to 5.6 V	**57**	**79**	–	
		V_S = 1.8 V, V_{CM} = V_{SS} − 0.1 V to V_{DD} − 1.4 V	–	**91**	–	
		V_S = 1.8 V, V_{CM} = −0.1 V to 1.9 V	–	**71**	–	
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}	V_S = 1.8 V, V_{SS} + 0.04 V < V_O < V_{DD} − 0.04 V, R_L = 10 kΩ	–	100	–	dB
		V_S = 5.5 V, V_{SS} + 0.05 V < V_O < V_{DD} − 0.05 V, R_L = 10 kΩ	101	108	–	
		V_S = 1.8 V, V_{SS} + 0.06 V < V_O < V_{DD} − 0.06 V, R_L = 2 kΩ	–	97	–	
		V_S = 5.5 V, V_{SS} + 0.15 V < V_O < V_{DD} − 0.15 V, R_L = 2 kΩ	–	113	–	
Short Circuit Current	I_{SC}	Output sourcing current V_S = 5 V	–	40	–	mA
		Output sinking current, V_S = 5 V	–	50		
Output Voltage Swing from V_{DD}	V_{DD} − V_{OH}	V_S = 5.5 V, R_L = 10 kΩ	–	3	20	mV
		V_S = 5.5 V, R_L = 2 kΩ	–	–	60	
Output Voltage Swing from V_{SS}	V_{OL} − V_{SS}	V_S = 5.5 V, R_L = 10 kΩ	–	3	20	mV
		V_S = 5.5 V, R_L = 2 kΩ	–	–	60	
AC CHARACTERISTICS						
Unity Gain Bandwidth	UGBW	V_S = 5 V, G = +1	–	8	–	MHz
Slew Rate at Unity Gain	SR	V_S = 5 V, G = +1	–	3.5	–	V/µs
Phase Margin	Φ_m	V_S = 5 V, G = +1	–	52	–	°
Gain Margin	A_m		–	11	–	dB
Settling Time to 0.1%	t_S	V_S = 5 V, V_{IN} = 2 V step, G = +1, C_L = 100 pF	–	0.5	–	µs
Settling Time to 0.01%	t_S	V_S = 5 V, V_{IN} = 2 V step, G = +1, C_L = 100 pF	–	1	–	µs
Overload Recovery Time	t_{OR}	V_S = 5 V, V_{IN} x gain > V_S	–	1	–	µs
Open Loop Output Impedance	Z_{OL}	V_S = 5 V, f = 10 MHz	–	240	–	Ω
NOISE CHARACTERISTICS						
Total Harmonic Distortion plus Noise	THD+n	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz	–	0.0008	–	%
Input Referred Voltage Noise	e_n	V_S = 5 V, f = 1 kHz	–	20	–	nV/√Hz
		V_S = 5 V, f = 10 kHz	–	10	–	

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT V_S = 1.8 V to 5.5 V (continued)
T_A = 25°C; R_L ≥ 10 kΩ connected to mid−supply; V_{CM} = V_{OUT} = mid−supply unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C. (Note 7)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE CHARACTERISTICS						
Input Referred Current Noise	i_n	f = 1 kHz	–	20	–	fA/√Hz
Input Voltage Noise, Peak−to−Peak	E_n	V_S = 5 V, f = 0.1 Hz to 10 Hz	–	5	–	μVPP
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V – 5.5 V, V_{CM} = V_{SS}	–	8	80	μV/V
Power Supply Quiescent Current	I_Q	Per channel, no load	–	500	**800**	μA

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID−SUPPLY, C_L = 20 PF, R_L = 10 KΩ TO MID−SUPPLY, UNLESS OTHERWISE NOTED)

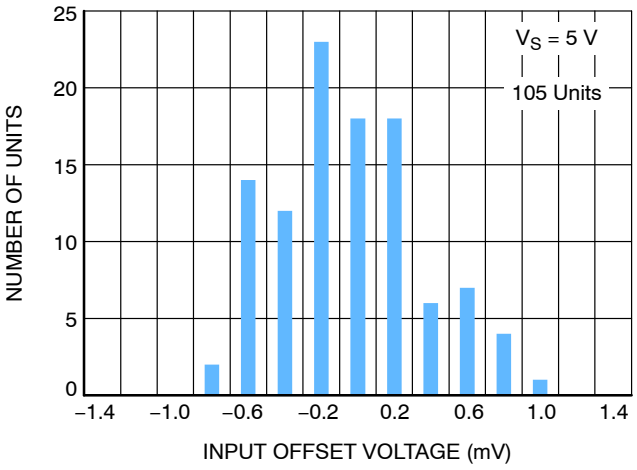


Figure 2. Input Offset Voltage Distribution

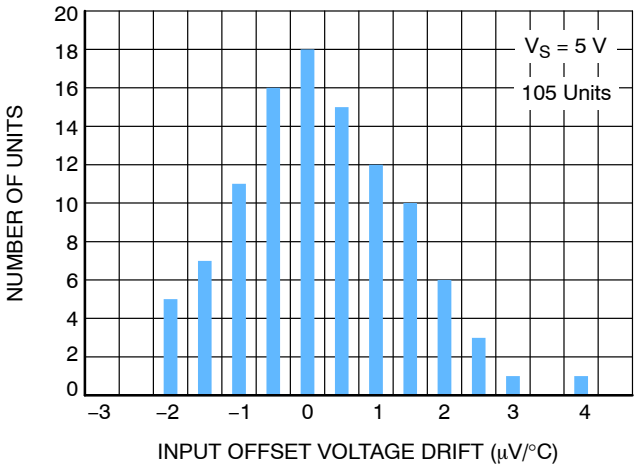


Figure 3. Input Offset Voltage Drift Distribution

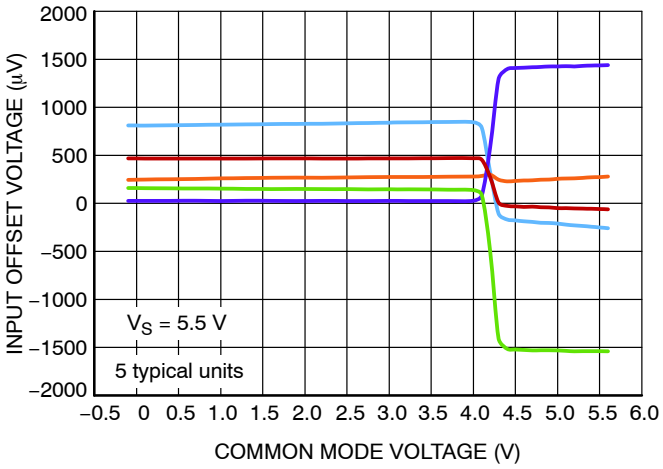


Figure 4. Input Offset Voltage vs. Common Mode Voltage at 5.5 V Supply

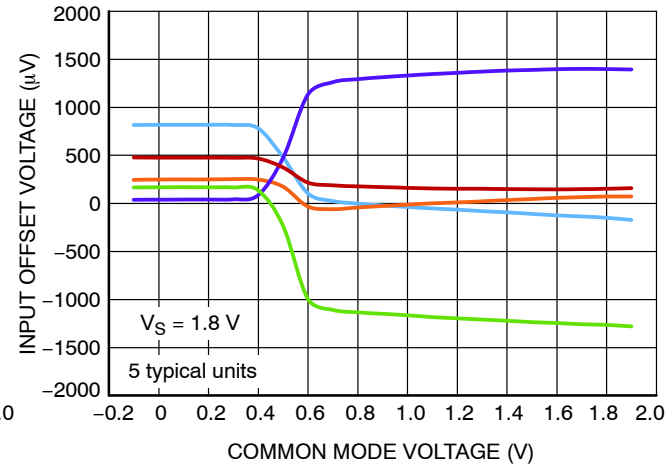


Figure 5. Input Offset Voltage vs. Common Mode Voltage at 1.8 V Supply

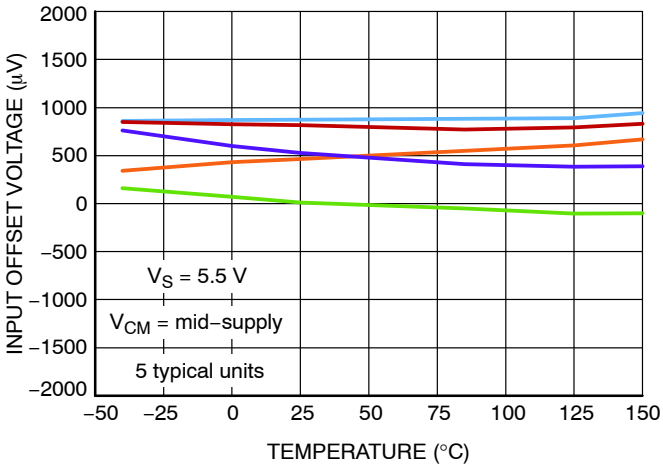


Figure 6. Input Offset Voltage vs. Temperature at 5.5 V Supply

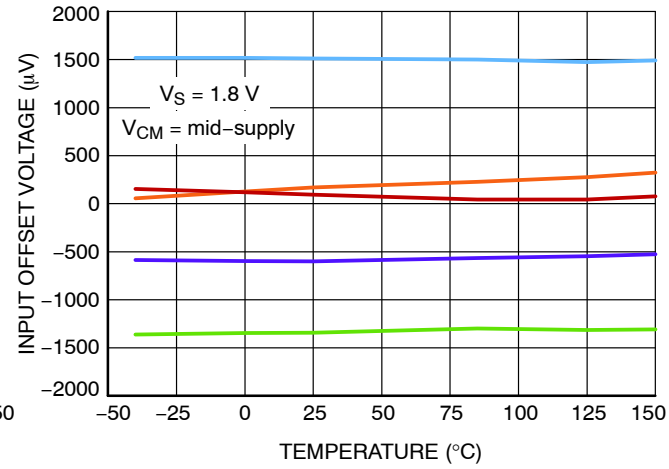


Figure 7. Input Offset Voltage vs. Temperature at 1.8 V Supply

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID−SUPPLY, C_L = 20 PF, R_L = 10 KΩ TO MID−SUPPLY, UNLESS OTHERWISE NOTED)

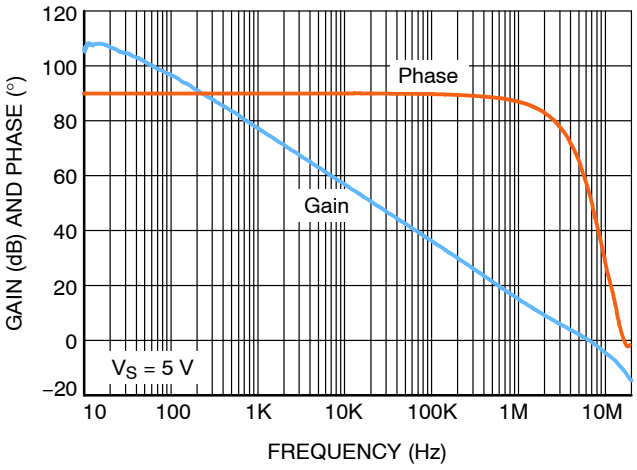


Figure 8. Open Loop Gain vs. Frequency

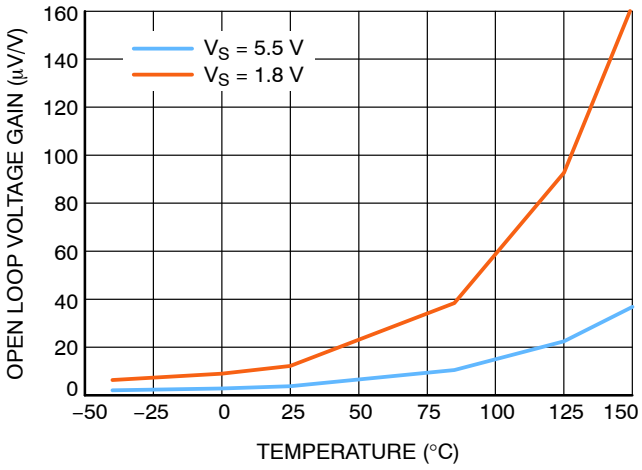


Figure 9. Open Loop Gain vs. Temperature

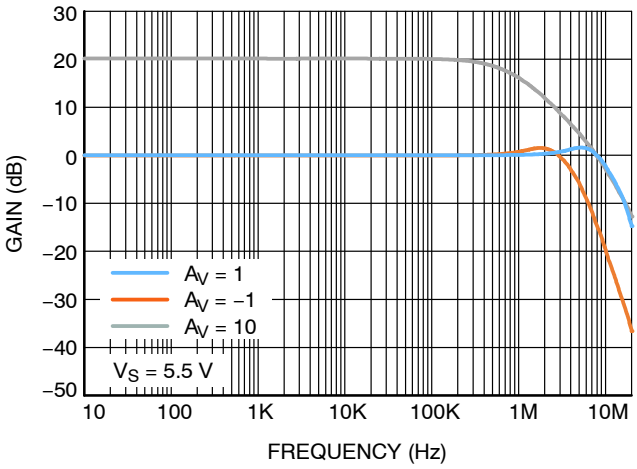


Figure 10. Closed Loop Gain vs. Frequency

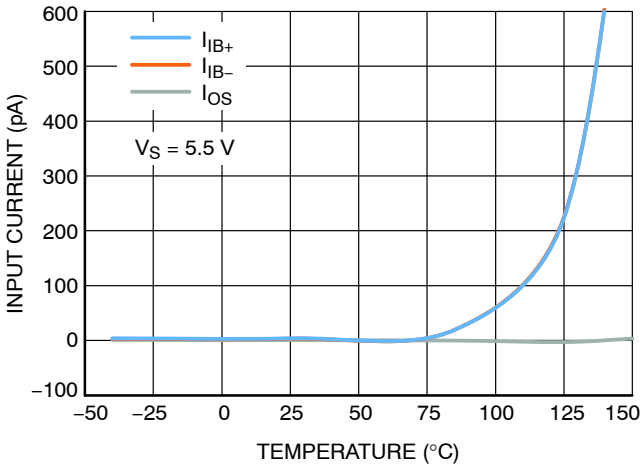


Figure 11. Input Current vs. Temperature

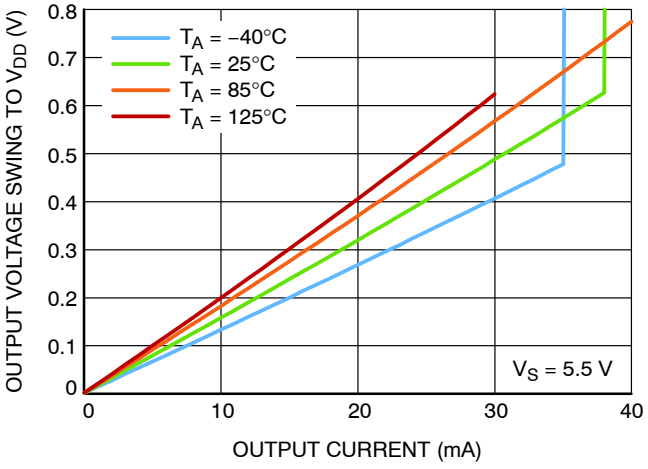


Figure 12. Output Voltage Swing High

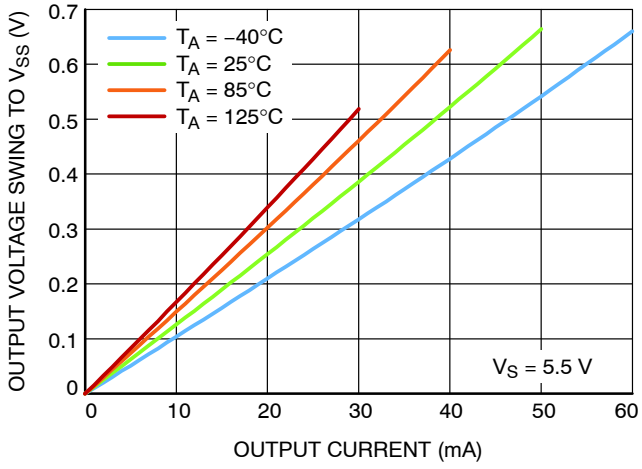


Figure 13. Output Voltage Swing Low

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID−SUPPLY, C_L = 20 PF, R_L = 10 KΩ TO MID−SUPPLY, UNLESS OTHERWISE NOTED)

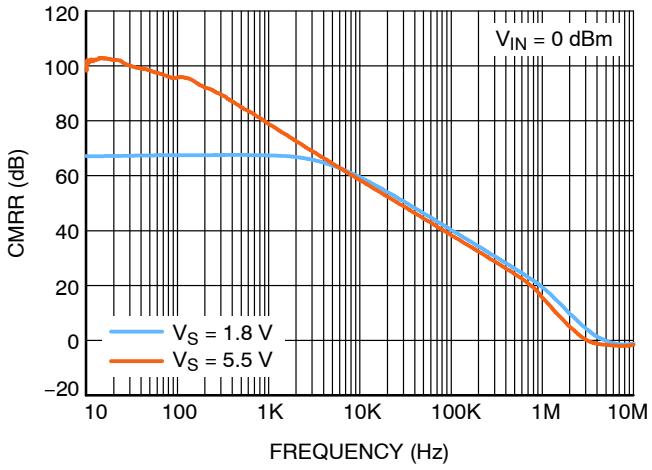


Figure 14. CMRR vs Frequency

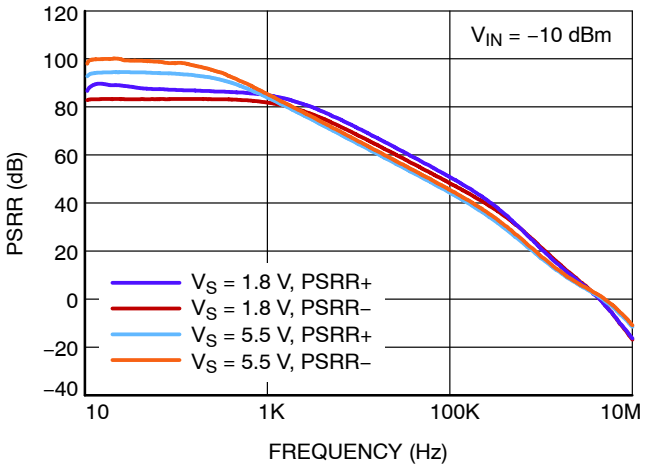


Figure 15. PSRR vs. Frequency

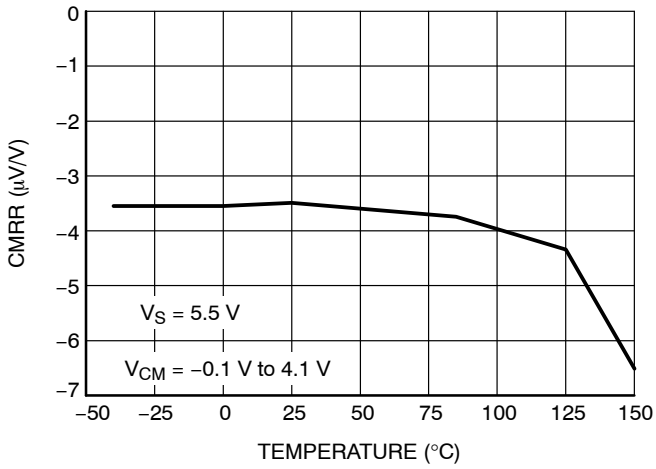


Figure 16. CMRR vs Temperature

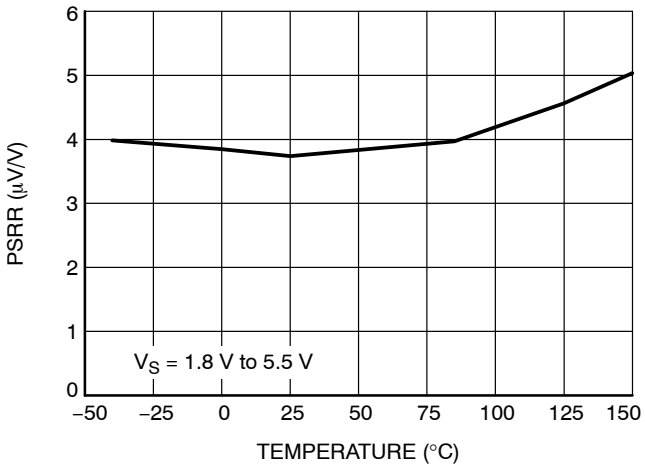


Figure 17. PSRR vs. Temperature

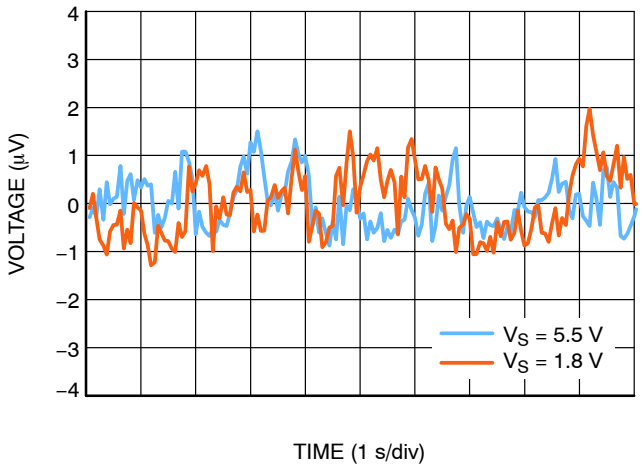


Figure 18. 0.1 Hz to 10 Hz Noise

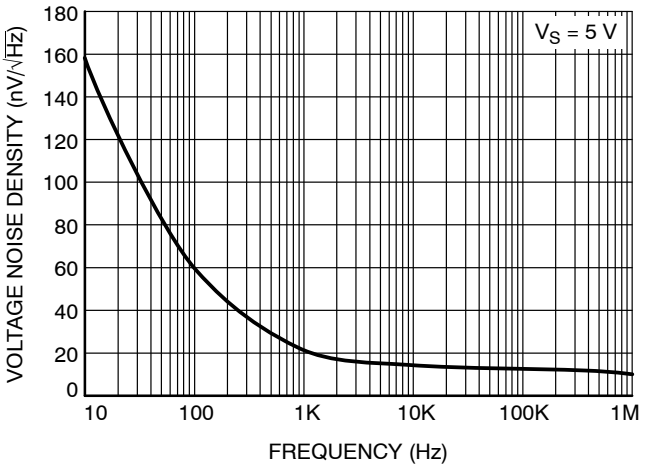


Figure 19. Voltage Noise Density vs. Frequency

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID−SUPPLY, C_L = 20 PF, R_L = 10 KΩ TO MID−SUPPLY, UNLESS OTHERWISE NOTED)

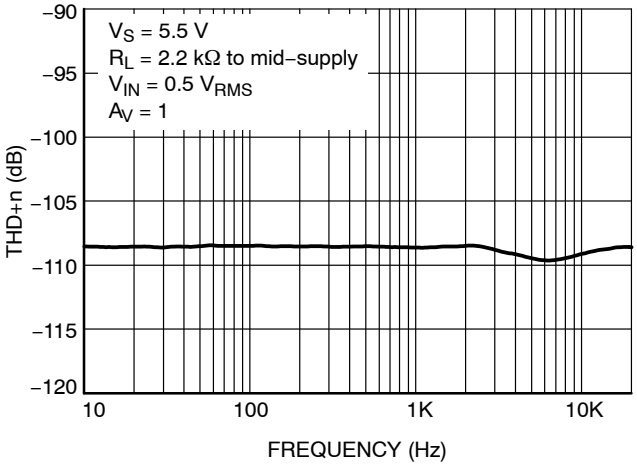


Figure 20. THD+n vs. Frequency

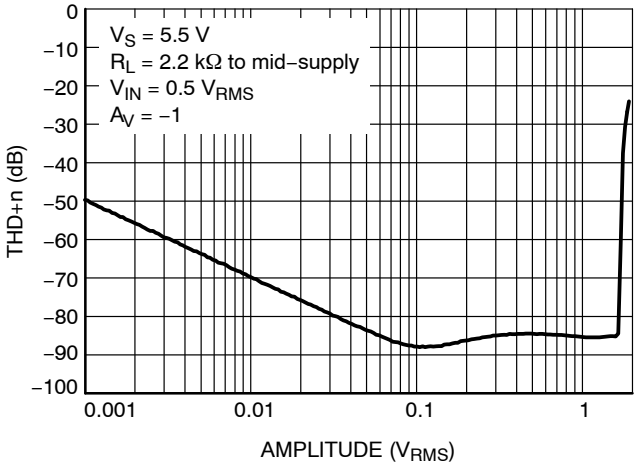


Figure 21. THD+n vs. Output Amplitude

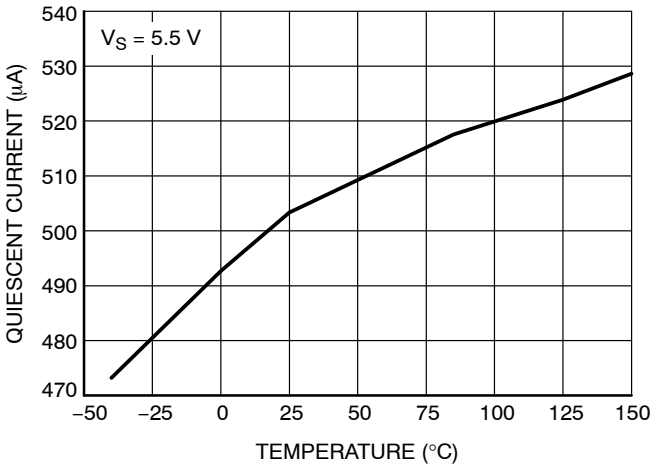


Figure 22. Quiescent Current Per Channel vs. Temperature

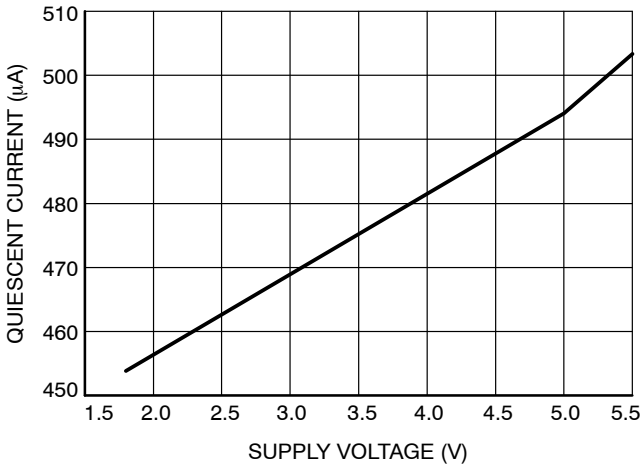


Figure 23. Quiescent Current Per Channel vs. Supply Voltage

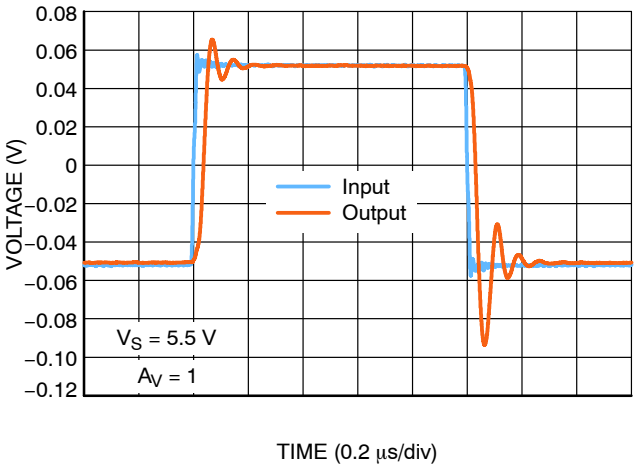


Figure 24. Small Signal Step Response

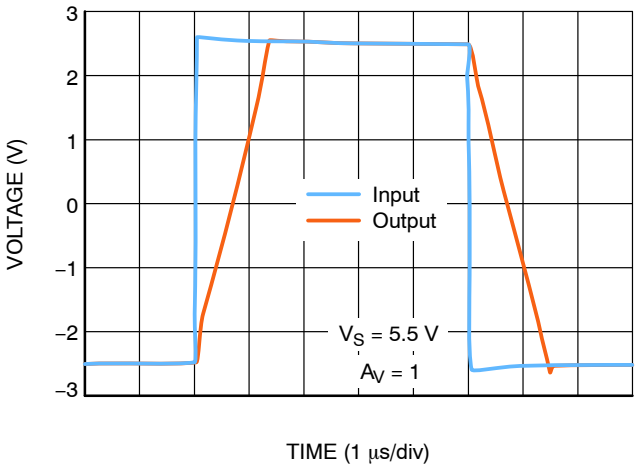


Figure 25. Large Signal Step Response

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID−SUPPLY, C_L = 20 PF, R_L = 10 KΩ TO MID−SUPPLY, UNLESS OTHERWISE NOTED)

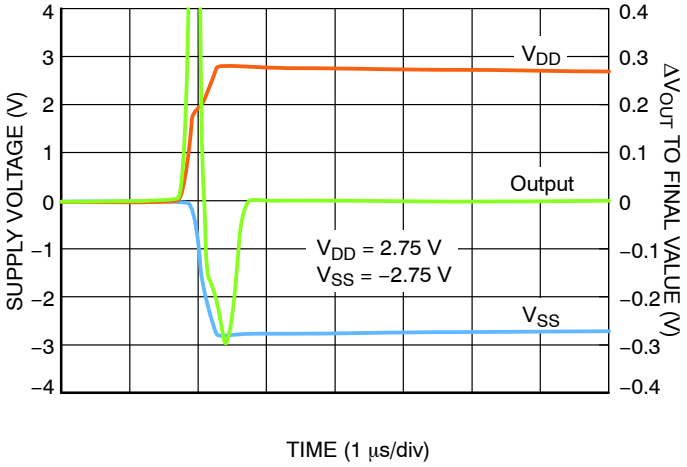


Figure 26. Power Up

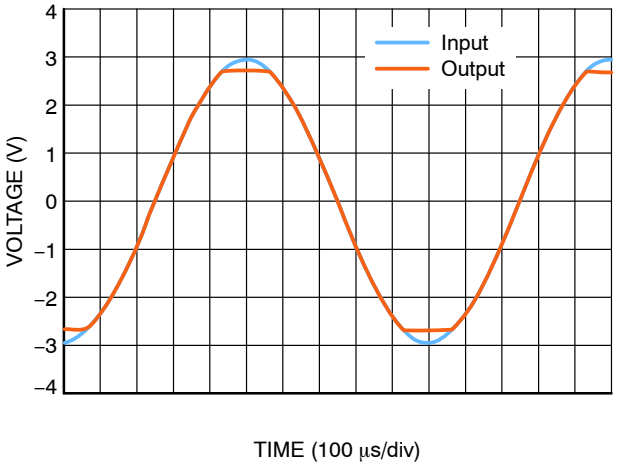


Figure 27. No Phase Reversal

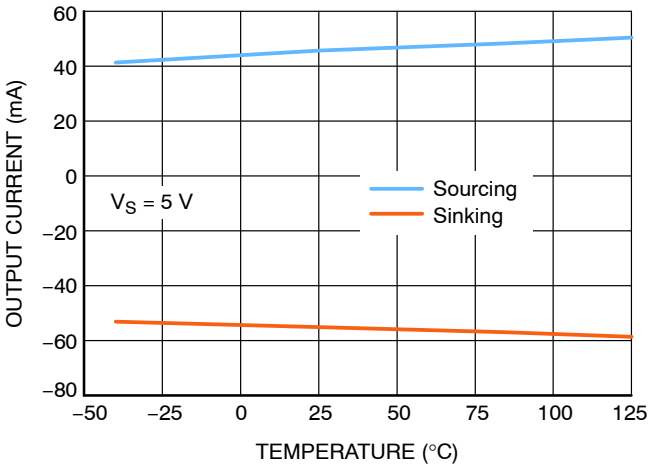


Figure 28. Short Circuit Current vs. Temperature

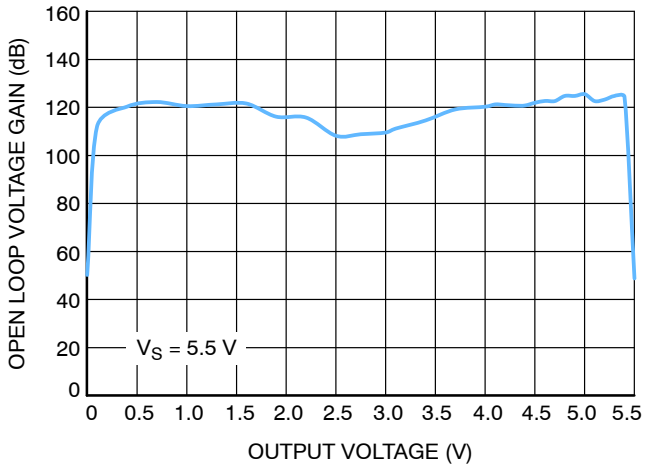


Figure 29. Open Loop Gain vs. Output Voltage

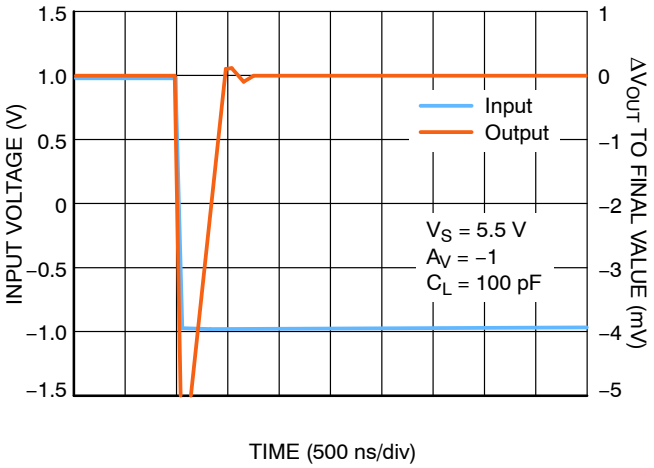


Figure 30. Output Low−to−High Settling Time

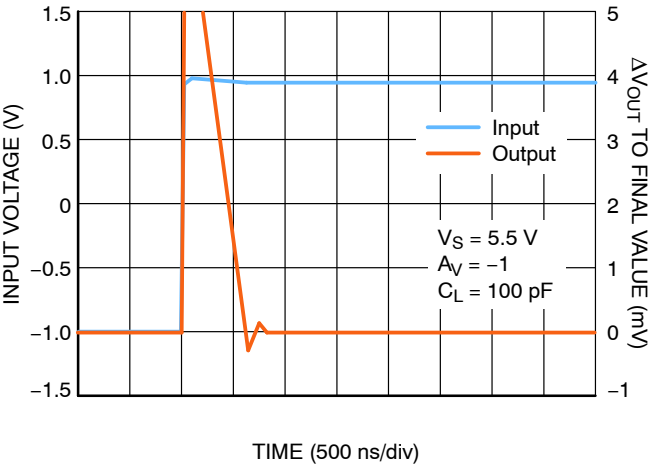


Figure 31. Output High−to−Low Settling Time

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID−SUPPLY, C_L = 20 PF, R_L = 10 KΩ TO MID−SUPPLY, UNLESS OTHERWISE NOTED)

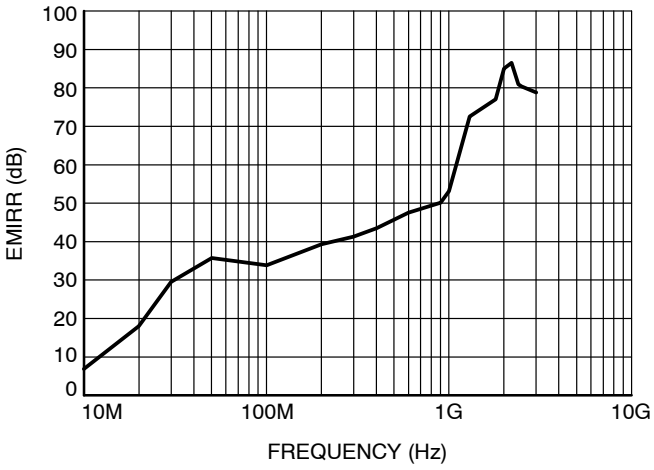


Figure 32. EMIRR vs. Frequency

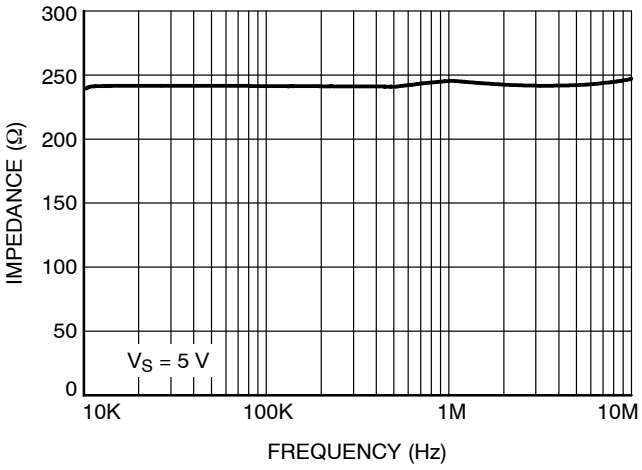


Figure 33. Open Loop Output Impedance vs. Frequency

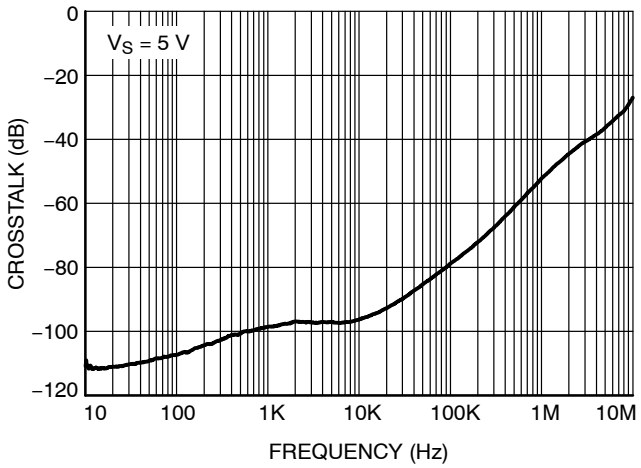


Figure 34. Channel Separation vs. Frequency

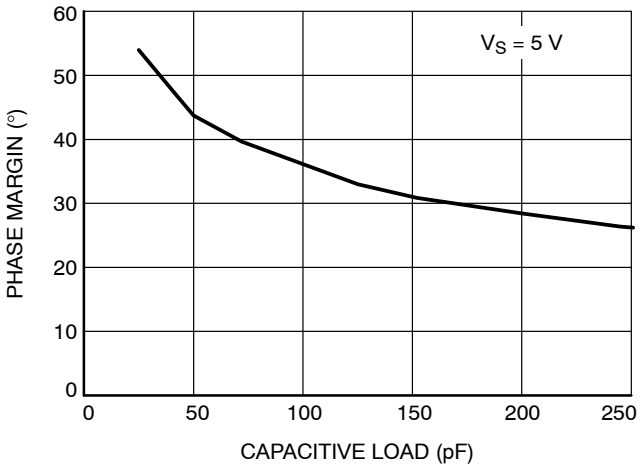


Figure 35. Phase Margin vs. Capacitive Load

TYPICAL CHARACTERISTICS

(AT T_A = 25°C, V_{CM} = MID−SUPPLY, C_L = 20 PF, R_L = 10 KΩ TO MID−SUPPLY, UNLESS OTHERWISE NOTED)

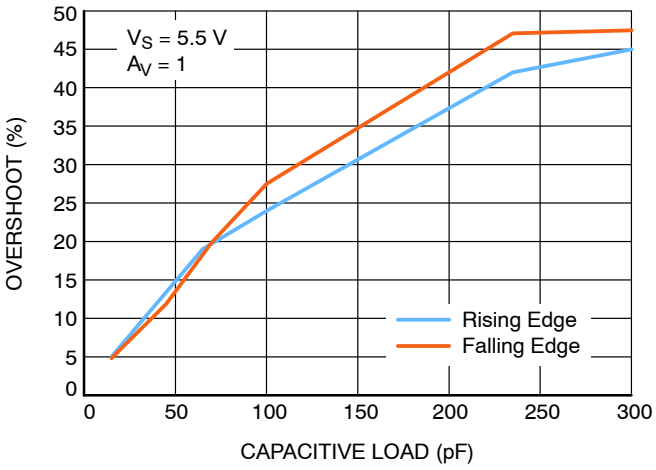


Figure 36. Overshoot vs. Capacitive Load for A_V = 1

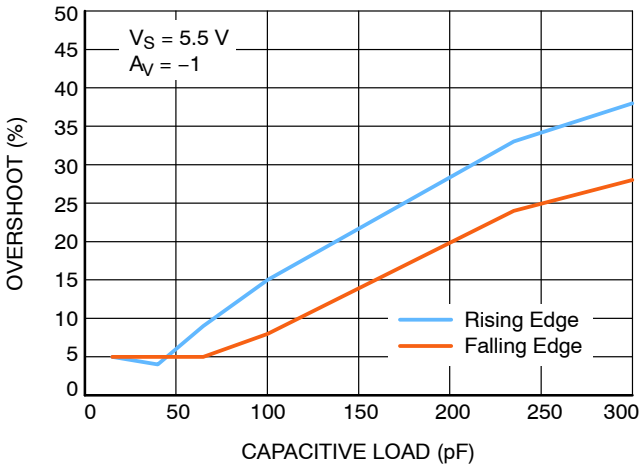


Figure 37. Overshoot vs. Capacitive Load for A_V = −1

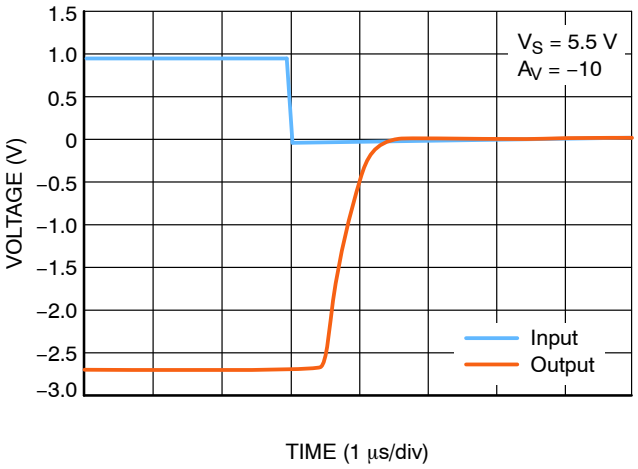


Figure 38. Negative Overvoltage Recovery

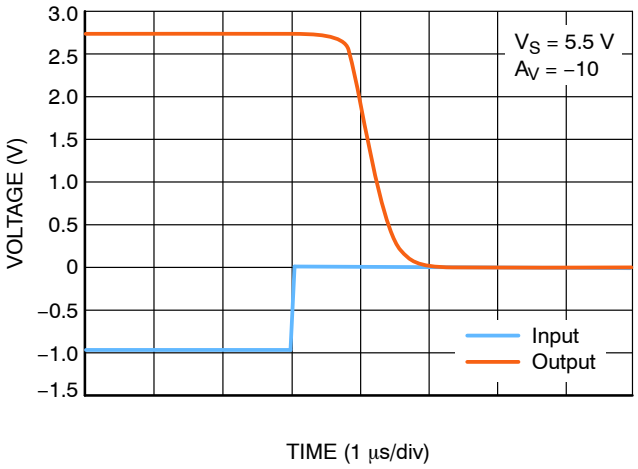


Figure 39. Positive Overvoltage Recovery

APPLICATION INFORMATION

The NCS20161 family of operational amplifiers is manufactured using **onsemi**'s CMOS process. Products in this class are general purpose, unity−gain stable amplifiers and include single, dual and quad configurations.

Rail−to−Rail Input with No Phase Reversal

The NCS2016x operational amplifiers are designed to prevent phase reversal or any similar issues when the input pins potential exceed the supply voltages by up to 100 mV.

The input stage of the NCS20161 family consists of two differential CMOS input stages connected in parallel: the first is constructed using paired PMOS devices and it operates at low common mode input voltages (V_{CM}); the second stage is build using paired NMOS devices to operate at high V_{CM}. The transition between the two input stages occurs at a common mode input voltage of approximately V_{DD}−1.3V.

Limiting Input Voltages

In order to prevent damage and/or improper operation of these amplifiers, the application circuit must never expose the input pins to voltages or currents higher than the Absolute Maximum Ratings.

The internal ESD structure includes special diodes to protect the input stages while maintaining a low input bias current (I_{IB}). The input protection circuitry clamp the inputs when the signals applied exceed more than one diode drop below VSS or one diode drop above VDD. Very fast ESD events (within the limits specified) trigger the protection structure so the operational amplifier is not damaged.

In order to safe guard against excessive voltages across the op amp's inputs, external clamp diodes can be used as shown in Figure 40. The four low−drop fast diodes (Schottky preferred) are used in parallel with the internal structure to divert the excessive energy to the supply rails where it can be easily dissipated or absorbed by the supply capacitors. The application designer should also take into account that these external diodes add leakage currents and parasitic capacitance that must be considered when evaluating the end−to−end performance of the amplifier stage.

Limiting Input Currents

In order to prevent damage/ improper operation of these amplifiers, the application circuit must limit the current flowing through the input pins. A possible solution is presented in Figure 40 by means of the two added series resistors. The minimum value for the input resistors should be calculated using Ohm's Law so they limit the input pin current to less than the absolute maximum values specified. The application designer should take into account that these resistors also add parasitic inductance that must be considered when evaluating performance.

Combining the current limiting resistors with the voltage limiting diodes creates a solid input protection structure, that can be used to insure reliable operation of the amplifier even in the hardest conditions.

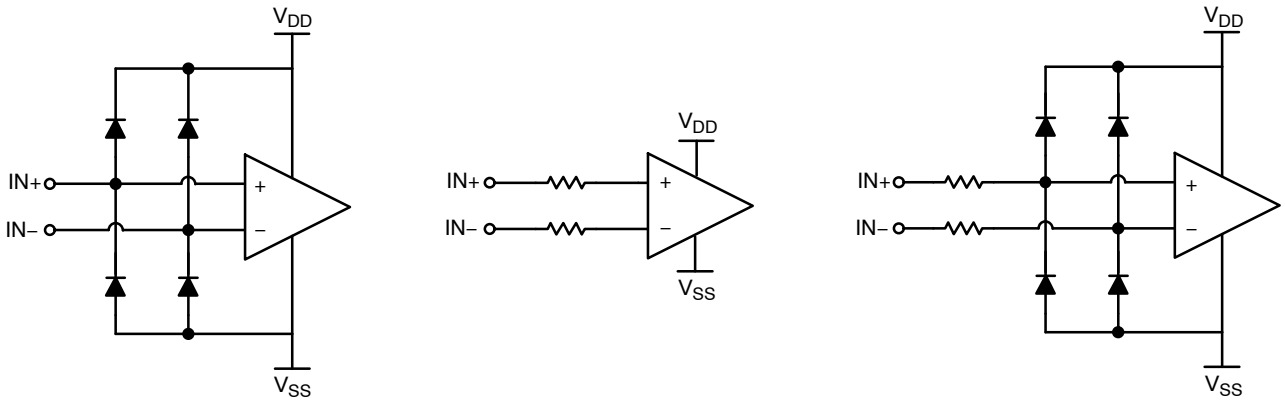


Figure 40. Typical Protection of the Operational Amplifier Inputs

Rail−to−Rail Output

The maximum output voltage swing is dependent of the particular output load. According to the specification, the output can reach within 20 mV of either supply rail when load resistance is 10 kΩ. The V_{OL} and V_{OH} graphs shows the load drive capabilities of the part under different conditions. Output current is internally limited to the typical values listed in the Electrical Characteristics table.

Capacitive Loads

Driving capacitive loads can create stability problems for voltage feedback op amps, as it is a known possible cause for:

- degraded phase margin
- lowered bandwidth
- gain peaking of the frequency response
- overshoot and ringing of the step response

While the NCS2016x series op amps are capable of driving capacitive loads up to 100 pF, adding a small resistor in series to the output (R_{ISO} in Figure 41) will increase the phase margin. This leads to higher stability by making the equivalent load more resistive at high frequencies.

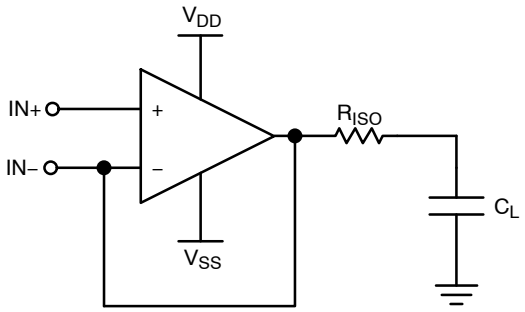


Figure 41. Driving Capacitive Loads

Simulating the application with **onsemi**'s Spice model is a good starting point for selecting the isolation resistor's value. Bench testing the frequency and step response can be used to fine−tune the value according to the desired characteristic.

Unity Gain Bandwidth

Interfacing a high impedance sensor's output to a relatively low−impedance ADC input usually requires an intermediate stage to avoid unwanted interference of the two devices, and this stage needs to have a high input impedance, a low output impedance, and high output current.

The unity gain buffer is recommended here (Figure 42). The ADC's internal sampling capacitor requires a buffer front−end to recharge it faster than the sampling time, and this problem is even worse if more channels are sampled by the same ADC using an internal multiplexer. In order to achieve a settling time shorter than the multiplexed sampling rate, an RC stage is recommended between the buffer and the ADC input. The R_{ISO} resistor's value should be low enough to charge the capacitor quickly, but at the same time large enough to isolate the capacitive load from the amplifier output to preserve phase margin. When transients are generated by the sensor's output, first the two amplifier inputs see a high differential voltage between them, then the output settles and brings the inverting input back to the correct voltage.

Let us take an example of a 0.1 V to 4 V sensor signal. To successfully accommodate it, the differential input range of the NCS2016x is close to the supply range and the output will match the input. The differential input voltage is limited only by the ESD protection structure and not by back−to−back diodes between inputs.

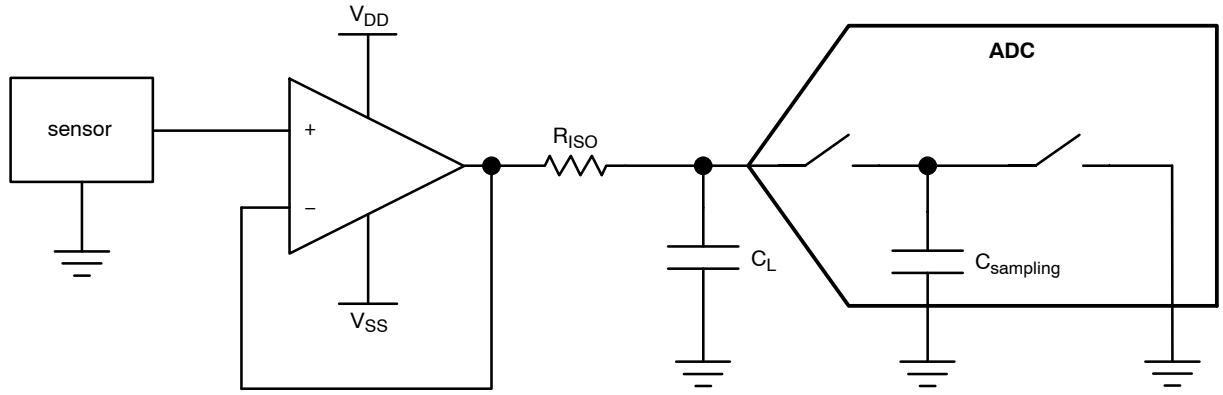


Figure 42. Unity Gain Buffer Stage for Sampling with ADC

Power Supply Bypassing

For AC, the power supply pins (VDD and VSS for split supply, VDD for single supply) should be bypassed locally with a quality capacitor in the range of 100 nF as close as possible to the amplifier supply pins. Ceramic capacitors are recommended for their low ESR and good high frequency response.

For DC, a bulk capacitor in the range of 1 μF placed within inches distance from the op amp can provide the additional current needed to drive higher loads.

Unused Operational Amplifiers

Occasionally not all the op amp channels offered in the quad packages are needed for a specific application. They can be connected as "buffering ground" as shown in Figure 43, a solution that does not need any extra parts. Connecting them differently (inputs split to rails, left floating, etc.) can sometimes cause unwanted oscillation, crosstalk, increased current consumption, or add noise to the supply rails.

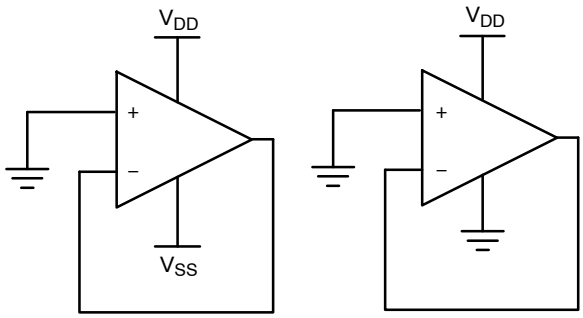


Figure 43. Unused Operational Amplifiers

PCB Surface Leakage

If it is critical to obtain the lowest input bias current, the PCB's surface leakage should be considered. Dry environment surface current increases further when the board is exposed to humidity, dust or chemical contamination. For harsh environment conditions, protecting the entire board surface (with all the exposed metal pins and soldered areas) is advised. Conformal coating or potting the board in resin proves effective in most cases.

An alternate solution for reduced leakage is the use of guard rings around sensitive pins and pads. A proper guard ring should have low impedance and be biased to the same voltage as the sensitive pin so that no current flows in between them.

For an inverting amplifier, the non−inverting input is usually connected to supply's ground (or virtual ground at half the rail voltage in single supply applications) so it can represent a good ring solution. When routing the PCB traces, create a closed perimeter around the inverting input pad (which carries the signal) and connect it to the non−inverting input.

For a non−inverting amplifier, use a similarly shaped (rectangle or circle) copper trace around the non−inverting input pad (which carries the signal) and connect it to the inverting input pin, which presents a much lower impedance thanks to the feedback network.

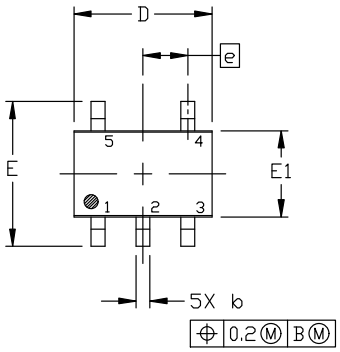
PCB Routing Recommendations

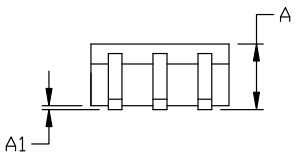
In addition to amplifying the useful signal, op amps can also pick the high frequency noise together with the signal and amplify it accordingly, if the design allows it. In order to reach the values specified in the Electrical Characteristics tables and to avoid high frequency interference issues, it is recommended that the PCB layout follows the basic guidelines listed below:

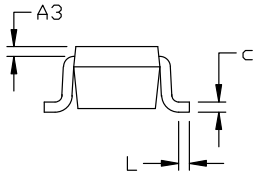
- A dedicated layer for the ground plane should be used whenever possible and all supply decoupling capacitors should connect to it by vias
- Copper traces should be as short as possible
- High current paths should not be shared by small signal or low current traces
- If present, switching power supply blocks should be kept away from the analog sensitive areas to avoid potential conducted and radiated noise issues
- When different circuit taxonomies share the same board, it is recommended to keep separated the power areas, the digital areas and the small signal analog areas. Small−signal components in the signal path should be placed as close as possible to the amplifier input pins
- Metal shielding the sensitive areas and the "offender" blocks may be required in some cases

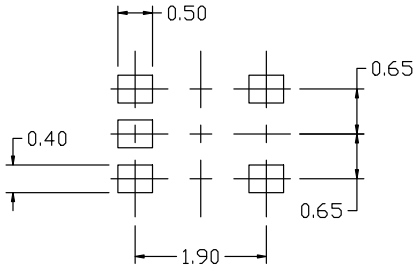
PACKAGE DIMENSIONS

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M









RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

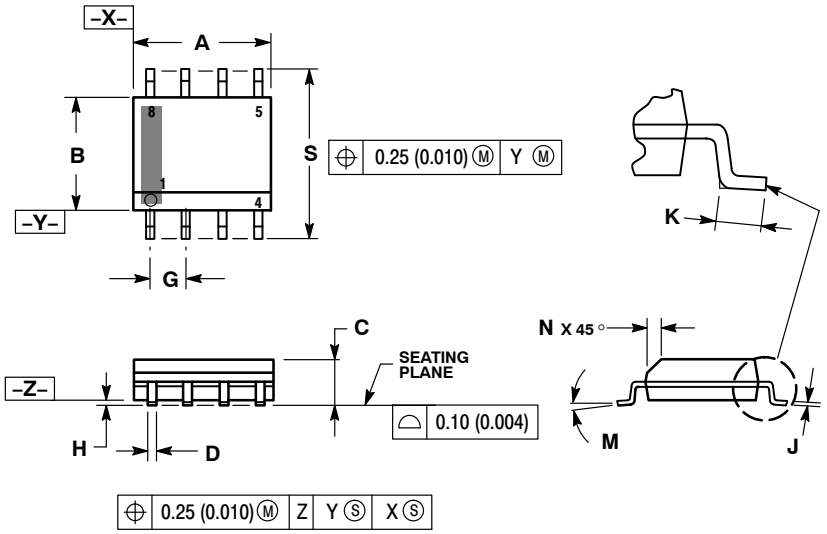
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AK

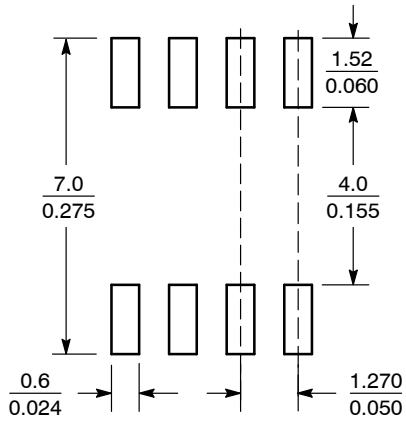


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*

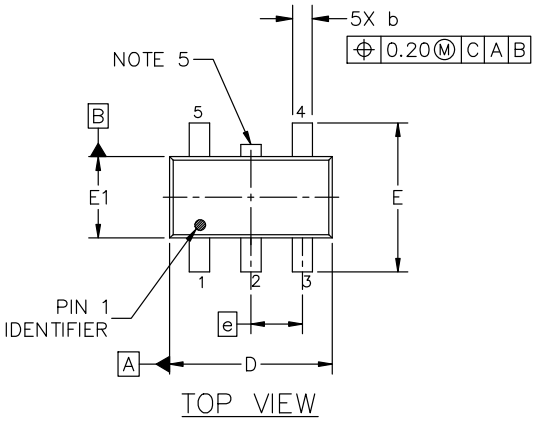


SCALE 6:1 (mm / inches)

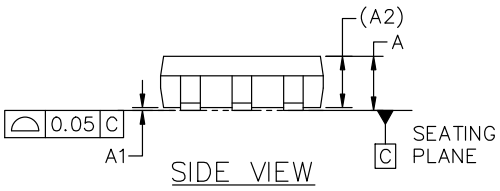
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

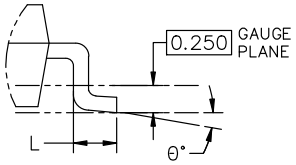
TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P



TOP VIEW



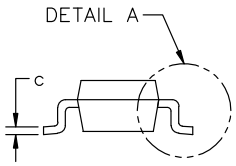
SIDE VIEW



DETAIL "A"
SCALE 2:1

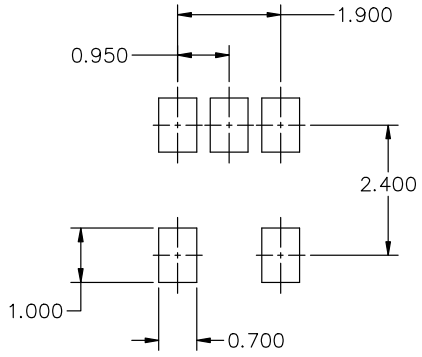
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

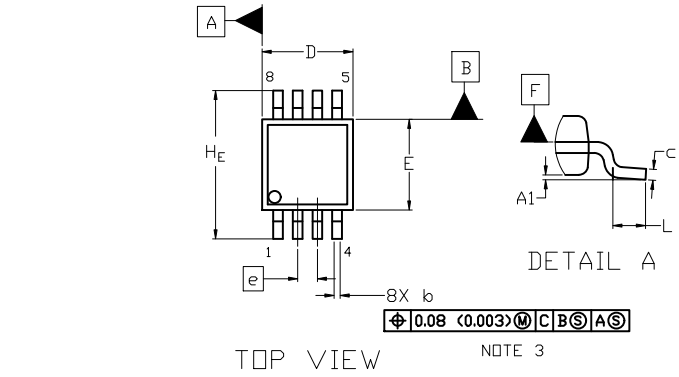


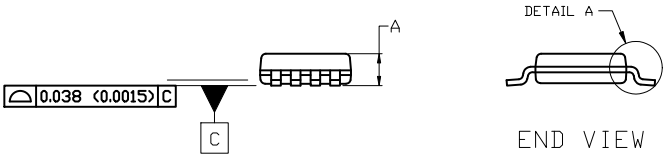
RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

PACKAGE DIMENSIONS

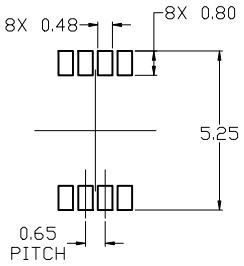
Micro8
CASE 846A−02
ISSUE K





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



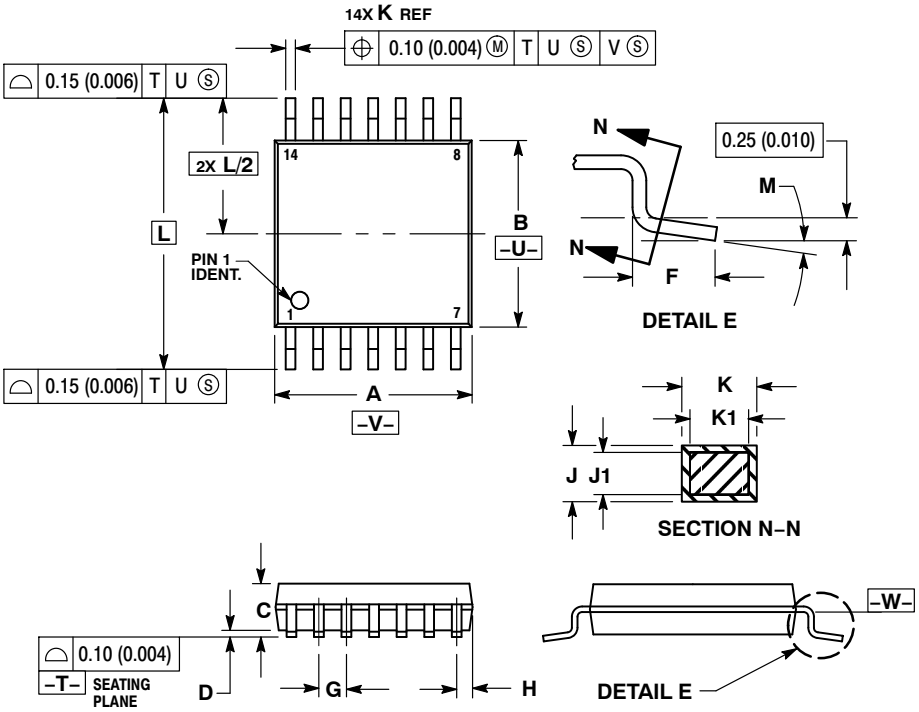
RECOMMENDED
MOUNTING FOOTPRINT

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

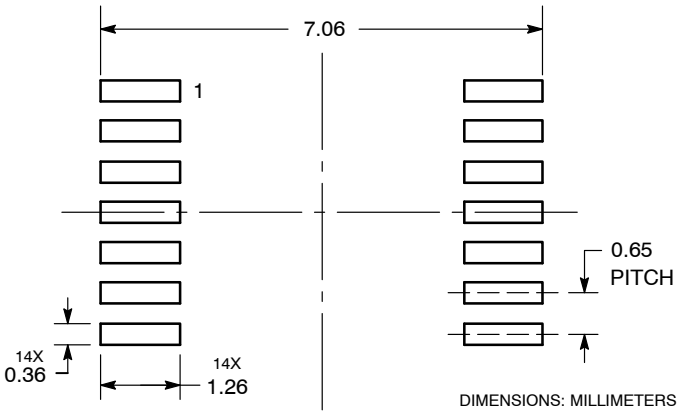
TSSOP−14 WB
CASE 948G
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

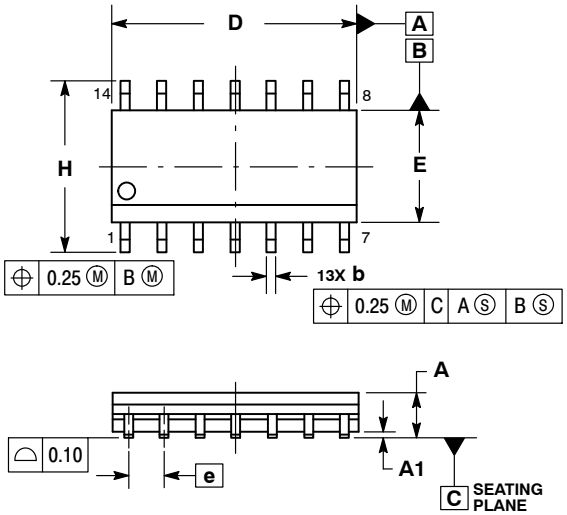
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

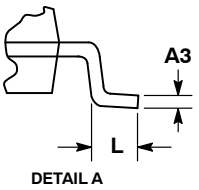
SOLDERING FOOTPRINT

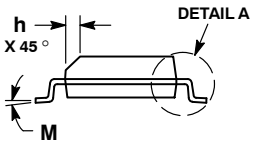


PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE L



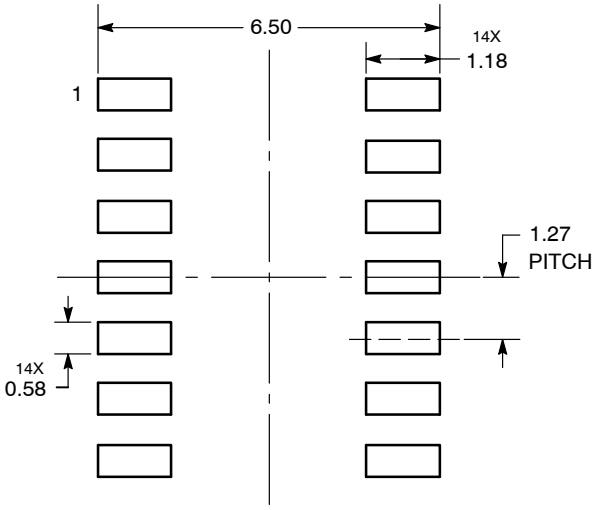




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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