NCR 53C710, 53C710-1 SCSI I/O Processor

Data Manual

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0.99	8/90	Draft
1.0	9/90	Preliminary Version
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2.1	6/92	Moved Chapter 6, Electrical Specifications, to separate manual.

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Preface

This manual provides descriptions and operational information for the NCR 53C710 and 53C710-1. The 53C710 supports Bus Mode 1 (asynchronous) DMA timings up to 25 MHz, and Bus Mode 2 (synchronous) DMA timings up to 33 MHz. The 53C710-1 supports asynchronous timings up to 33 MHz and synchronous timings up to 40 MHz. Electrical characteristics and timings for the 53C710 and 53C710-1 are provided in the 53C710 and 53C710-1 Electrical Specifications Manual.

This information has been checked for both accuracy and reliability. NCR reserves the right to change specifications or discontinue altogether without notice, any hardware or software product, or the technical content herein.

Additional Information

NCR 53C710, 53C710-1 Electrical Specifications Manual

NCR 53C710 Programmer's Guide

NCR SCSI Engineering Note 829, Comparison of 53C710 to 53C700

SCSI Specifications

This data manual is not a SCSI specification. It assumes some prior knowledge of current and proposed SCSI standards. To obtain a copy of the proposed standard or background information on SCSI, write to:

ANSI
11 West 42nd Street
New York, NY 10018
(212) 642-4900

Ask for document number: X3.131 – 1986 (SCSI-1)

Global Engineering Documents
2805 McGaw
Irvine, CA 92714
(800) 854-7179 or (714) 261-1455

Ask for document number:
X3.131-199x (SCSI-2)

ENDL Publications
14426 Black Walnut Court
Saratoga, California 95070
(408) 867-6642

Document Name:
SCSI Bench Reference

Prentice Hall
Englewood Cliffs, New Jersey 07632
(201) 767-5937

Ask for document number: ISBN 0-13-796855-8

Document Name: SCSI - Understanding the Small Computer System Interface

NCR SCSI Electronic Bulletin Board
(719) 574-0424

Table of Contents

Chapter 5
Instruction Set of the I/O Processor

Appendix A
53C710 Register Summary

Appendix B
Bit and Register Differences Between the 53C710 and the 53C700

Appendix C
53C710 Mechanical Data

NCR Microelectronic Products Division Sales Locations

Chapter 1

SCSI I/O Processor Description

General Description

The NCR 53C710 is the second member of the 53C700 family of intelligent, single-chip, third generation SCSI host adapters. A high performance SCSI core and an intelligent 32-bit bus master DMA core are integrated with a SCSI SCRIPTS processor to accommodate the flexibility requirements of SCSI-1, SCSI-2, and future SCSI standards. The 53C710 solves the protocol overhead problems that have plagued all previous intelligent and non-intelligent adapter designs.

The 53C710 is designed to completely implement a multi-threaded I/O algorithm in either a workstation or file server environment, completely free of processor intervention except at the end of an I/O transfer. In addition, the 53C710 allows SCSI SCRIPTS instructions to be relocated if necessary, and requires no dynamic alteration of SCRIPTS instructions at the start of an I/O operation. All of the SCRIPTS code may be placed on a PROM. The 53C710 allows easy firmware upgrades and is compatible with the 53C700.

The 53C710 supports two different host processor interfaces. Bus Mode 1 closely resembles the Motorola 68030 interface, and Bus Mode 2 closely resembles the 68040 interface. The modes are selected by using the bus mode select pin.

The NCR 53C710 features NCR's TolerANT™ Active Negation Technology, which allows optional active negation of SCSI signals during information transfer phases. When enabled, TolerANT causes the SCSI REQ, ACK, Data and parity signals to be actively pulled up to approximately three volts by transistors on each pin. The benefits of this technolgy include reduced noise when the signal is going high (deasserted), increased performance due to balanced duty cycles, and improved Fast SCSI transfer rates. Active Negation is enabled by setting the EAN bit in the CTEST0 register. It can be used in both single-ended and differential mode. TolerANT is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

53C710 Features Summary

Performance

- Supports variable block size and scatter/gather data transfers
- Supports 32-bit word data bursts with variable burst lengths
- High-speed SCSI bus transfers
  Over 5 MB/S asynchronous
  10 MB/S synchronous
- 42.66 MB/S sustained host bus bandwidth
- Enhanced SCRIPTS capabilities:
  Relative jump
  Table indirect data mode
  Read/write system memory
  Read/write registers
  Arithmetic operations
  Memory-to-memory DMA transfers
- Register parity during slave reads
- Glitchless SCSI on power-up/down
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts
- Unique interrupt status reporting reduces ISR overhead
- Cache-line burst mode
- 64-byte DMA FIFO
- Active negation of SCSI Data, Parity REQ and ACK signals with NCR's TolerANT technology improves rise times and Fast SCSI transfer rates in both single-ended and differential modes.

Integration

- Full 32-bit DMA bus master
- High performance SCSI core
- Integrated SCRIPTS processor
- Allows intelligent host adapter performance on a motherboard

Ease of Use

- Reduces SCSI development effort
- Emulates existing intelligent host adapters
- Support for Big and Little Endian byte ordering
- Easily adapted to the SCSI Common Access Method (CAM) by "executing" data structures
- Fully compatible with existing 53C700 SCRIPTS
- Development tools and SCSI SCRIPTS provided
- All interrupts are maskable and pollable

Flexibility

- High level programmer's interface (SCSI SCRIPTS)
- Allows tailored SCSI sequences to be executed from main memory or from a host adapter board.
- Flexible sequences to tune I/O performance or to adapt to unique SCSI devices
- Accommodates changes in the logical I/O interface definition
- Low level programmability (register oriented)
- Allows a target to disconnect and later be reselected with no interrupt to the system processor
- Allows a multithreaded I/O algorithm to be executed in SCSI SCRIPTS with a fast I/O context switch
- Can auto-switch between initiator and target roles dynamically
- Allows indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM.
- Separate SCSI and system clocks

Reliability

- 2 K volts minimum ESD protection
- Typical 350 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- 250 ms byte-to-byte SCSI activity timer
- Voltage feed through protection (minimum leakage current through SCSI pads)
- 20% of signals are power and ground
- Ground isolation of I/O pads and chip logic

Testbility

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- Self-selection capability
- SCSI bus signal continuity checking

Figure 1-1. 53C710 Block Diagram

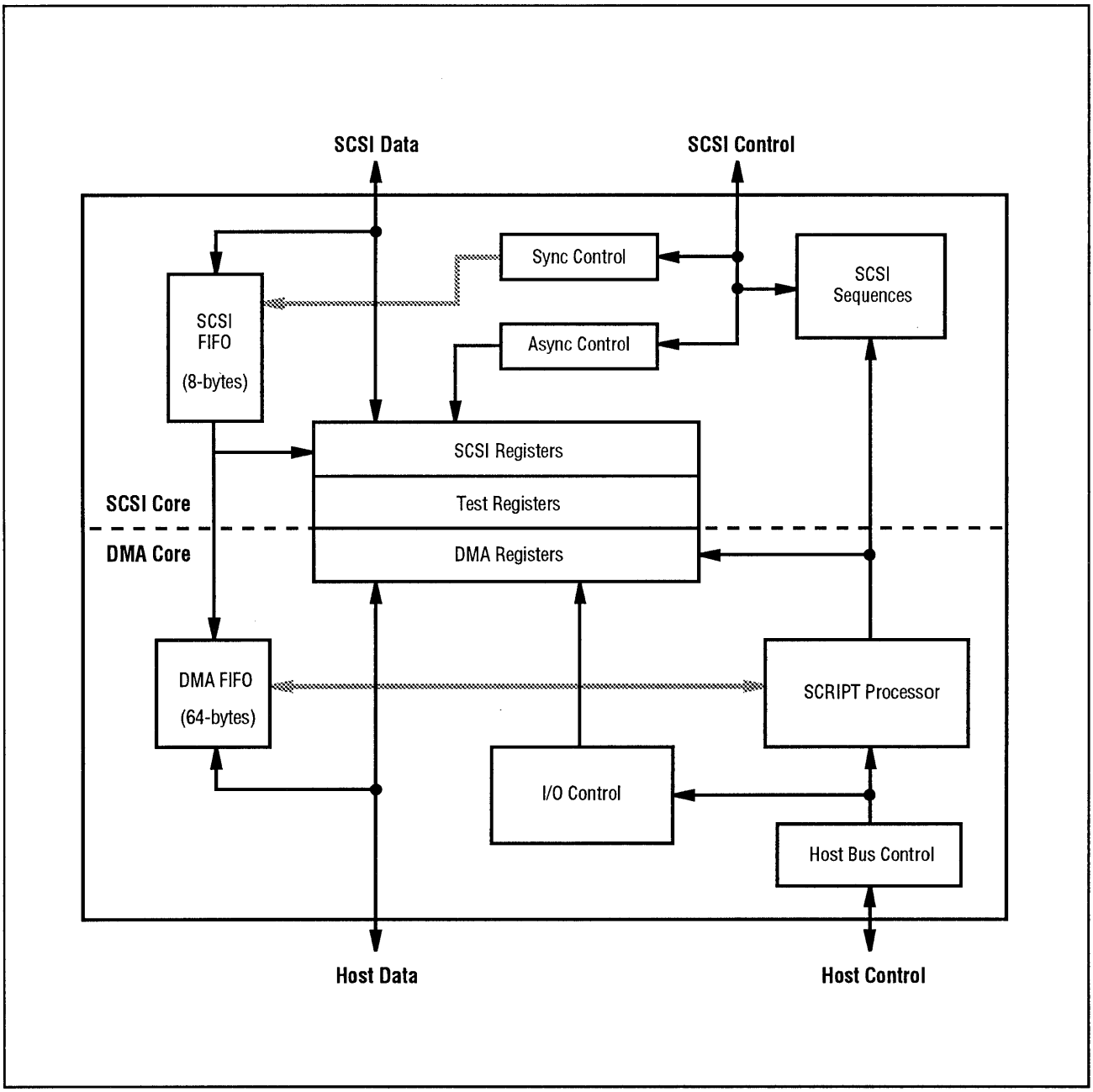
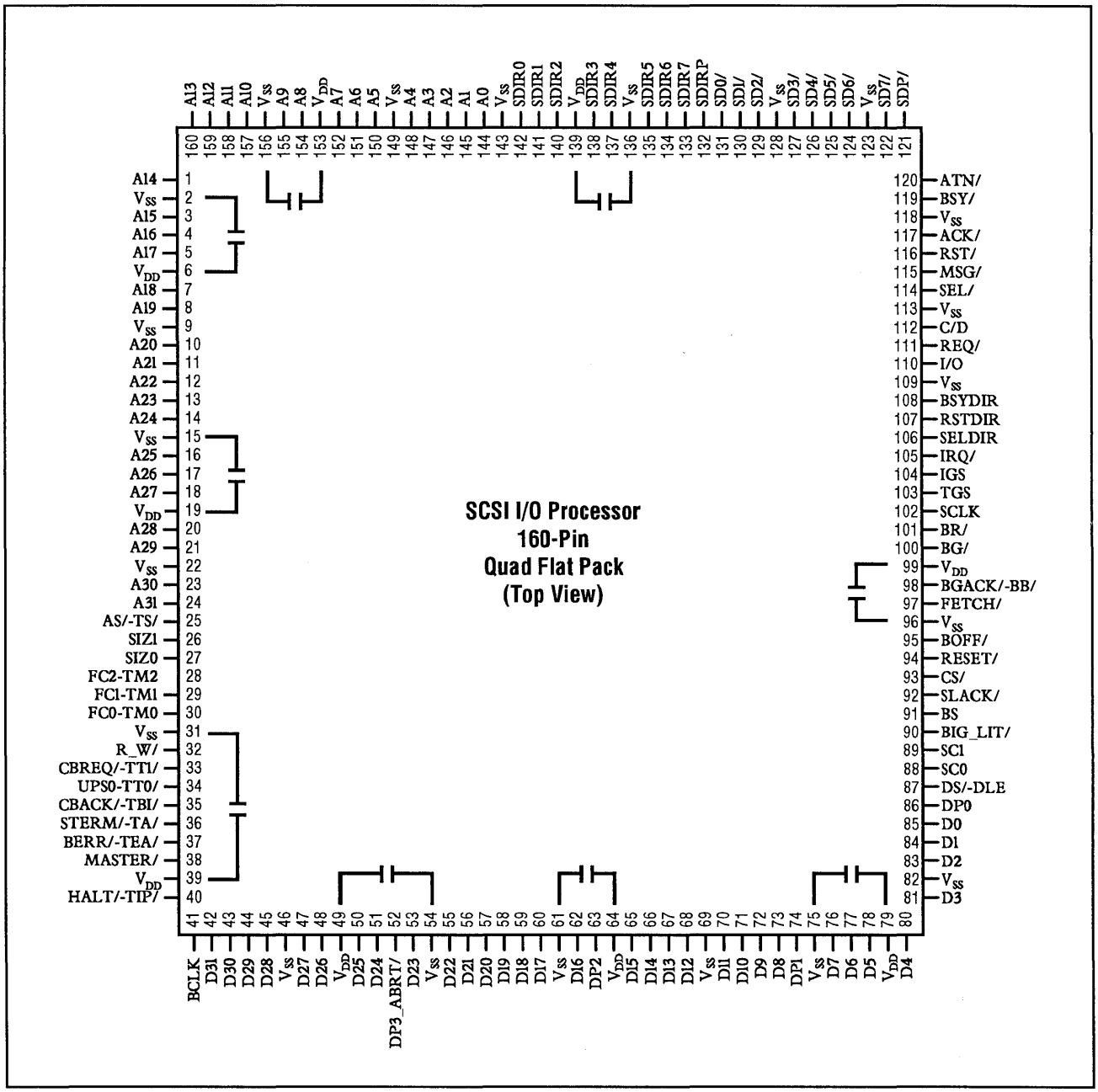


Figure 1-2. 53C710 Pin Configuration



Note: *The decoupling capacitor arrangement shown above is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the 53C710, a multilayer PC board with power & ground planes is required.*

Chapter 2

Functional Description

The 53C710 is composed of three tightly coupled functional blocks: the SCSI Core; the DMA Core; and the SCRIPTS Processor.

SCSI Core

The SCSI core supports synchronous transfer rates of up to 10.0 MB/S, and asynchronous transfer rates greater than 5 MB/S. The programmable SCSI interface makes it easy to fine tune the system for specific mass storage devices or SCSI-2 requirements.

The SCSI core offers low level register access or a high-level control interface. Like first generation SCSI devices, the 53C710 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target. The 53C710 can test the SCSI pins for physical connection to the board or the SCSI bus.

Unlike previous generation devices, the SCSI core can be controlled by the integrated DMA core through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus Phases and in general, implement all aspects of the SCSI protocol.

DMA Core

The DMA core is a bus master DMA device that directly attaches to 68030 and 68040 processors, and to other processors (80386, 80486, etc.) with minimum logic.

The 53C710 supports 32-bit memory and automatically supports misaligned DMA transfers. A 64-byte FIFO allows the 53C710 to support one, two, four, or eight longwords to be burst across the memory bus interface. This DMA interface does not support dynamic bus sizing.

The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor which supports uninterrupted scatter/gather memory operations.

SCRIPTS Processor

The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol. It allows both DMA and SCSI instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTS can control the actions of the SCSI and DMA cores and are executed from 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 nanoseconds (ns). This compares with 2-8 milliseconds (ms) required for traditional intelligent host adapters. The SCRIPTS processor offers performance and customized algorithms. Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (i.e. scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2/SCSI-3 logical bus definitions without sacrificing I/O performance.

SCSI SCRIPTS are independent of the CPU and system bus in use. For a more detailed introduction to SCSI SCRIPTS, refer to the NCR 53C710 *Programmer's Guide.*

Loopback Mode

The 53C710 loopback mode allows testing of both initiator and target operations and, in effect, lets the chip talk to itself. When the Loopback Enable bit is set in the CTEST4 register, the 53C710 allows control of all SCSI signals, whether the 53C710 is operating in initiator or target mode. For more information on the loopback function, refer to the NCR 53C710 *Programmer's Guide.*

Parity Options

The 53C710 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and can deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

Control

1) Assert ATN/ on Parity Errors – Bit 1 in the SCNTL0 register.

   This bit causes the 53C710 to automatically assert SCSI ATN/ when it detects a parity error while operating as an initiator.

2) Enable Parity Generation – Bit 2 in the SCNTL0 register.

   This bit determines whether the 53C710 generates parity sent to the SCSI bus or allows parity to "flow through" the chip to/from the SCSI bus and system bus.

3) Enable Parity Checking – Bit 3 in the SCNTL0 register.

   This bit enables the 53C710 to check for parity errors. The 53C710 checks for odd parity.

4) Assert Even SCSI Parity – Bit 2 in the SCNTL1 register.

   This bit determines the SCSI parity sense generated by the 53C710.

5) Disable Halt on ATN/ or a Parity Error (Target Mode Only) – Bit 7 in SXFER register.

   This bit causes the 53C710 to immediately halt operations when a parity error is detected in target mode.

6) Enable Parity Error Interrupt – Bit 0 in the SIEN register.

   This bit determines whether the 53C710 will generate an interrupt when it detects a parity error.

Observation

7) Parity Error – Bit 0 in the SSTAT0 register.

   This status bit is set whenever the 53C710 has detected a parity error on either the SCSI bus or the system bus.

8) Status of SCSI Parity Signal – Bit 0 in the SSTAT1 register.

   This status bit represents the live SCSI Parity Signal (SDP/).

9) Latched SCSI Parity Signal – Bit 3 in the SSTAT2 register.

   This status bit contains the SCSI parity of the byte latched in the SIDL.

10) DMA FIFO Parity – Bit 3 in the CTEST2 register.

    This status bit represents the parity bit in the DMA FIFO after data is read from the FIFO by reading the CTEST6 register.

11) DMA FIFO Parity – Bit 3 in the CTEST7 register.
    This write-only bit is written to the DMA FIFO after writing data to the DMA FIFO by writing the CTEST6 register.

12) SCSI FIFO Parity – Bit 4 in the CTEST2 register.

    This status bit represents the parity bit in the SCSI FIFO after data is read from the FIFO by reading the CTEST3 register.

Table 2-1. Parity Control

EVP	EPG	EPC	ASEP	Description
0	0	0	0	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data and host data.
0	0	0	1	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data, and odd parity when sending host data.
0	0	1	0	Checks for odd parity on both SCSI data received and system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data, Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data and host data.
0	0	1	1	Checks for odd parity on both SCSI data received and system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data, and odd parity when sending host data.
0	1	0	0	Will not check for parity errors. Parity on DP(2-0) is ignored and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	0	1	Will not check for parity errors. Parity on DP(2-0) is ignored, and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
0	1	1	0	Checks for odd parity on SCSI data received. Parity on DP(2-0) is ignored, and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	1	1	1	Checks for odd parity on SCSI data received. Parity on DP(2-0) is ignored, and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.

Table 2-1. Parity Control (Continued)

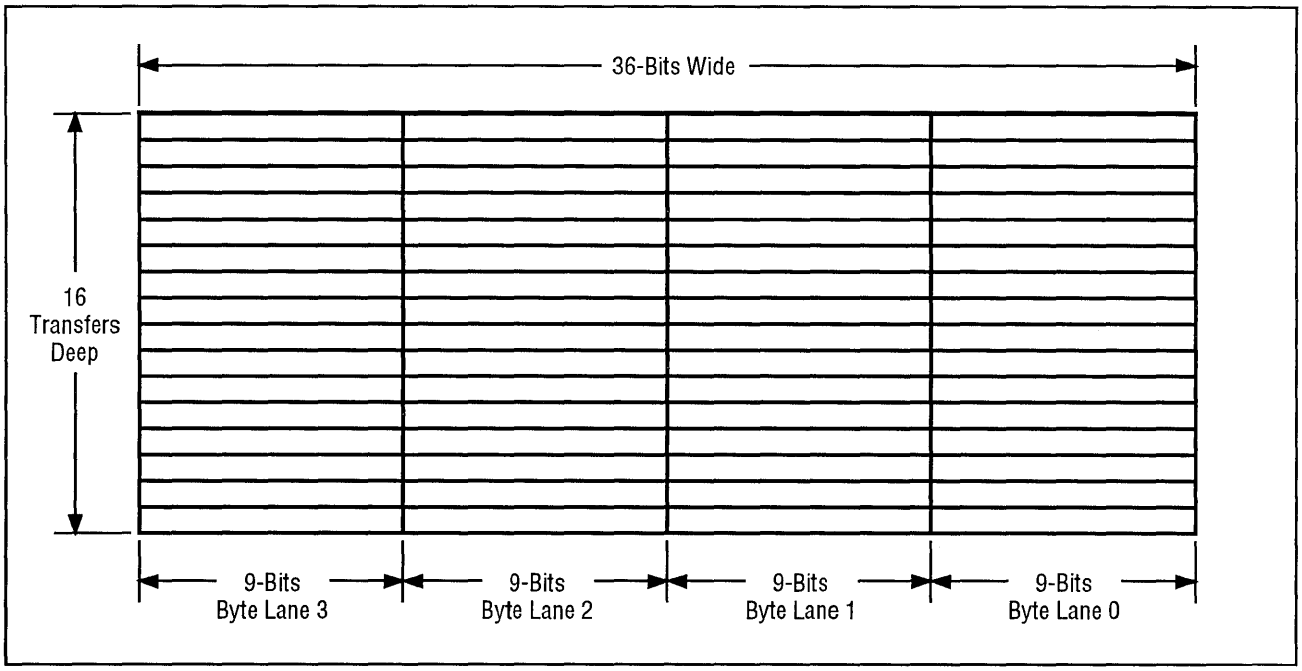
EVP	EPG	EPC	ASEP	Description
1	0	0	0	Will not check for parity errors. Parity flows from DP(2-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data, and even parity when sending host data.
1	0	0	1	Will not check for parity errors. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data and host data.
1	0	1	0	Checks for odd parity on SCSI data received and even parity on system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data, Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data, and even parity when sending host data.
1	0	1	1	Checks for odd parity on SCSI data received and even parity on system data when sending. Parity flows from DP(3-0) through the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data and host data.
1	1	0	0	Will not check for parity errors. Parity on DP(2-0) is ignored, and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	0	1	Will not check for parity errors. Parity on DP(2-0) is ignored, and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	1	1	0	Checks for odd parity on SCSI data received. Parity on DP(2-0) is ignored, and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	1	1	Checks for odd parity on SCSI data received. Parity on DP(2-0) is ignored, and DP(3) becomes ABORT/. Parity is generated when sending SCSI data. Parity flows from the SCSI bus to the chip, but is not asserted on DP(3-0) when receiving SCSI data. Asserts even parity when sending SCSI data.

Key: *EPG = Enable Parity Generation; EPC = Enable Parity Checking; ASEP = Assert SCSI Even Parity; EVP = Even Parity*

DMA FIFO

The DMA FIFO is a 64 x 9 bit FIFO. It can be divided into four sections, each nine bits wide and 16 transfers deep. Each of these four sections are called byte lanes. Each byte lane can be individually tested by writing known data into the FIFO and reading that same data back out of the FIFO. See the *53C710 Programmer's Guide* for detailed FIFO diagnostic examples.

Figure 2-1. DMA FIFO Sections



Interrupted Transfer Cleanup

The data path through the 53C710 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

Figure 2-2 shows how data is moved to or from the SCSI bus in each of the different modes.

The following steps will determine if any bytes remain in the data path when the chip halts an operation:

Asynchronous SCSI Send:

1) Use the algorithm described in the DFIFO register description (Chapter 4) to determine if any bytes are left in the DMA FIFO.
2) Read the SSTAT1 register and examine bit 6 to determine if any bytes are left in the SODL register. If bit 6 is set, then there is a byte in the SODL register.

Synchronous SCSI Send:

1) Use the algorithm described in the DFIFO register description to determine if any bytes are left in the DMA FIFO.
2) Read the SSTAT1 register and examine bit 6 to determine if any bytes are left in the SODL register. If bit 6 is set, then there is a byte in the SODL register.
3) Read the SSTAT1 register and examine bit 5 to determine if any bytes are remaining in the SODR register. If bit 5 is set, then there is a byte in the SODR register.

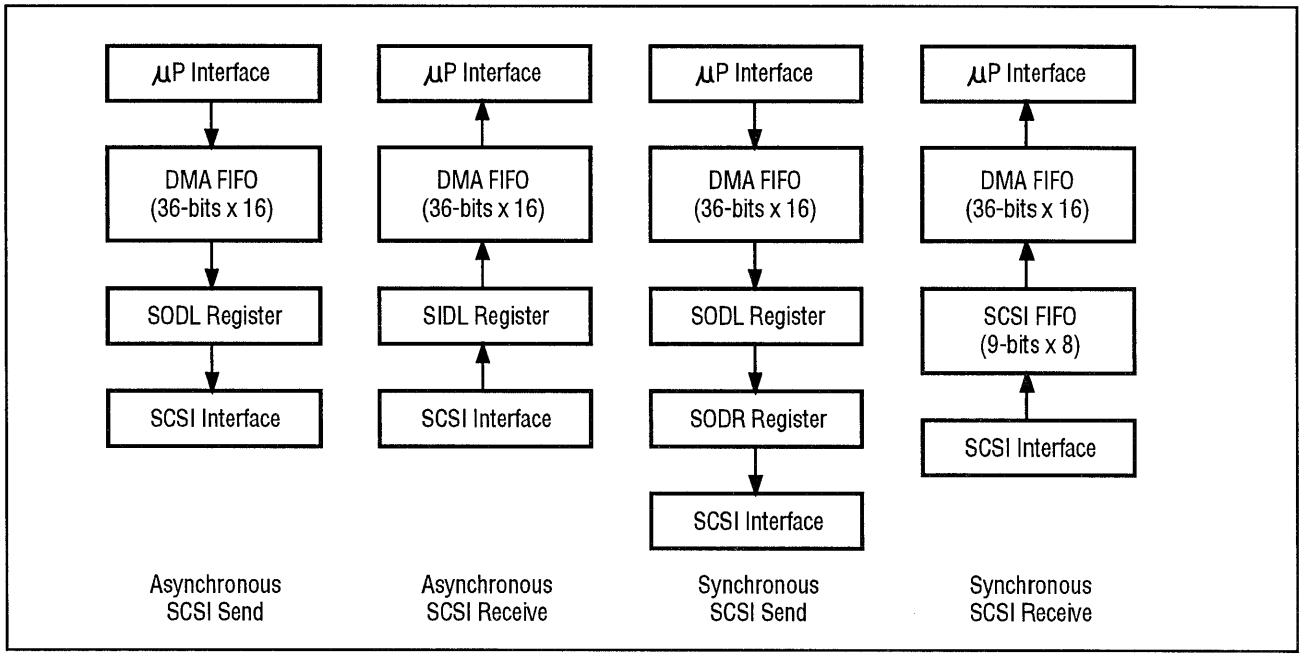
Asynchronous SCSI Receive:

1) Use the algorithm described in the DFIFO register description to determine if any bytes are left in the DMA FIFO.
2) Read the SSTAT1 register and examine bit 7 to determine if any bytes are left in the SIDL register. If bit 7 is set, then there is a byte in the SIDL register.

Synchronous SCSI Receive:

1) Use the algorithm described in the DFIFO register description to determine if any bytes are left in the DMA FIFO.
2) Read the SSTAT2 register and examine bits 7-4, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

Figure 2-2. 53C710 Data Paths



Host Interface

Big/Little Endian Support

The Big/Little Endian mode select pin gives the 53C710 the flexibility of operating with either byte orientation. Internally, in either mode, the byte lanes of the DMA FIFO and registers are not modified.

When a longword is accessed, no repositioning of the individual bytes is necessary, since longwords are addressed identically in either mode. Since longwords are always used by SCRIPTS, compatibility is maintained.

Big/Little Endian mode selection has the most effect on individual byte access. Internally, the 53C710 adjusts the byte control logic of the DMA FIFO and register decodes to access the appropriate byte lane. The registers will always appear on the same byte lane, but the address of the register will be repositioned.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address 'n' - there is no byte ordering in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address 0 is the first byte out on the SCSI bus, address 1 is the second byte, etc.

Correct SCRIPTS will be generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPTS patching in memory must patch the instructions in the order that the SCRIPTS processor expects it.

Software drivers for the 53C710 should access registers by their logical name (i.e., "SCNTL0) rather than by their address. The logical name should be equated to the register's Big Endian address in Big Endian mode (SCNTL0 = 03h), and its Little Endian address in Little Endian Mode (SCNTL0 = 00h). This way, there is no change to the software when moving from one mode to the other; only the equate file needs to be changed.

Addressing of registers from within a SCRIPT is independent of bus mode. Internally, the 53C710 always operates in Little Endian mode.

Big Endian Mode

Big Endian is used primarily in designs based on Motorola processors. The 53C710 treats D(31-24) as the lowest physical memory address. The register map is left-justified (Address 03h = SCNTL0).

Little Endian Mode

Little Endian is used primarily in designs based on Intel processors. This mode treats D(7-0) as the lowest physical memory address. The register map is right-justified (Address 00h = SCNTL0).

System data bus	(31-24)	(23-16)	(15-8)	(7-0)
53C710 pins	(31-24)	(23-16)	(15-8)	(7-0)
Register	SIEN	SDID	SCNTL1	SCNTL0
Little Endian addr	03h	02h	01h	00h
Big Endian addr	00h	01h	02h	03h

Misaligned Transfers

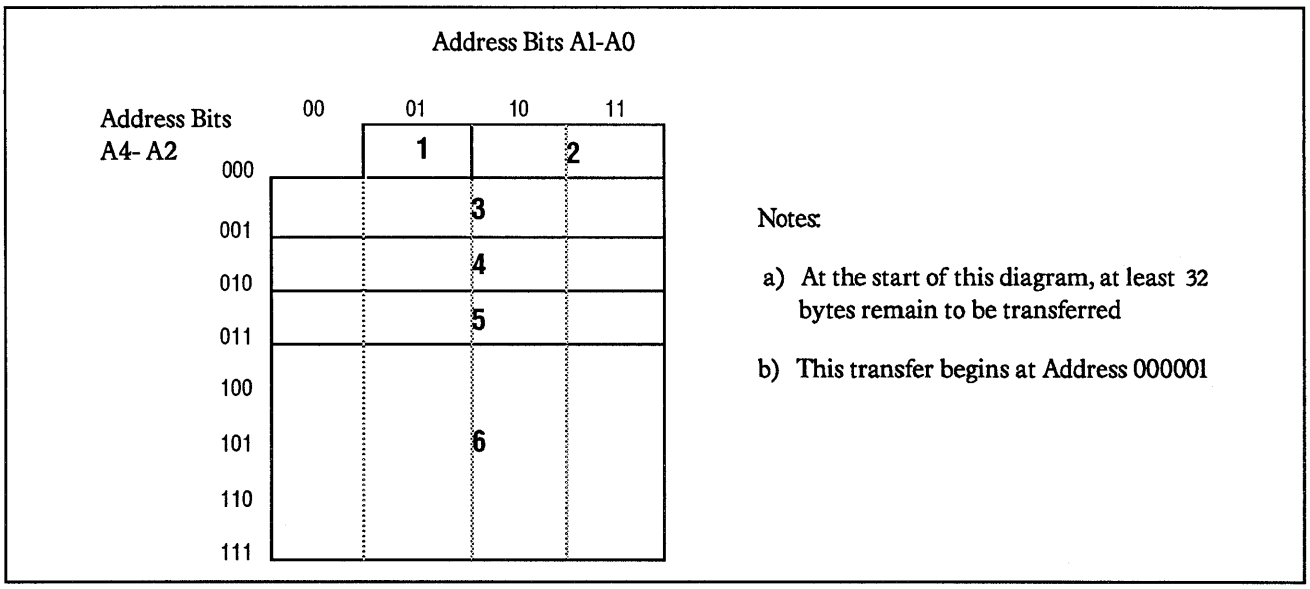
The 53C710 accommodates block data transfers beginning or ending on odd byte or odd word addresses in system memory. Such transfers are termed "misaligned." An odd byte is defined as one in which the address contains A0 = 1; an odd word is defined as one in which the address contains A1 = 1. Misaligned transfers differ depending on the type of transfer (cache-line or programmable bursting) and whether they occur at the start or end of the transfer. The 53C710 does not perform 3-byte transfers.

Cache-Line Bursting

Start of Transfer

At the start of the transfer, if the address starts at an odd byte boundary (bit A0 = 1), the 53C710 will line up to a word boundary by performing a single-byte (8-bit) transfer in a single bus ownership. Then, if the address is at an odd word boundary (bit A1 = 1), the 53C710 will line up to a longword boundary by performing a single-word (2-byte) transfer in a single bus ownership. At this point, longword (4-byte) transfers will be performed, one per bus ownership, until the address bits line up to a cache-line boundary (A(3-0) = 0). Once aligned, cache-line bursts of four longwords per bus ownership will be performed until the byte count decreases to 31 or less. The worst case example of five bus ownerships before cache line bursting can begin is depicted in Little Endian mode in Figure 2-3.

Figure 2-3. Cache Line Bursting, Start of Transfer (Little Endian Mode)

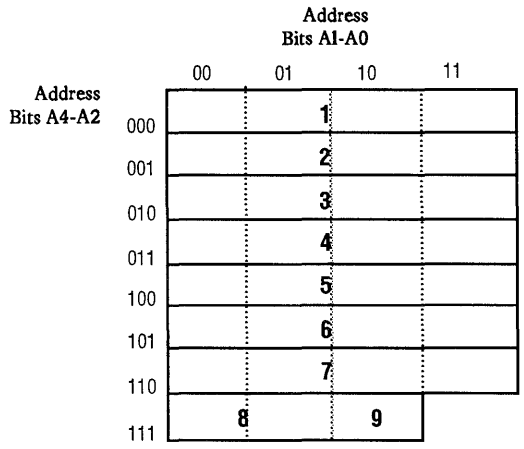


End of Transfer
When the byte count decreases to 31 or fewer bytes, the 53C710 drops out of cache burst mode and transfers the remaining longwords, words, and/or bytes in one or two bus ownerships until the transfer is complete. The 53C710 transfers longwords until the byte count decreases to 3 or less. If the byte count is 3 or 2, one word is transferred. If the byte count is 1, one byte is transferred. An example depicting the remaining transfers when the byte count is 31 is shown in Figure 2-4. ***Note:*** *When doing Cache line bursting and using Memory-to-Memory Move, A3-A0 on the source and destination addresses must be the same. The burst will not actually start until A3-A0 are zero.*

Programmable Bursting
When not in cache-line burst mode, the 53C710 is able to do 1, 2, 4 or 8 transfers per bus ownership. The transfers can be either byte, word, or longword transfers.

Start of Transfer
The 53C710 transfers the programmable burst length number of transfers during each bus ownership. If the address starts at an odd byte boundary (bit A0 = 1), the 53C710 will line up to a word boundary by performing a single-byte transfer. If A1=1, the 53C710 will perform a word transfer. At this point, the 53C710 will transfer longwords until the byte count decreases to 3 or less. The chip will transfer the programmable-burst-length number of transfers per bus ownership regardless of the width (byte, word or longword). An example of a transfer in which the programmable burst length is 8 is depicted in Figure 2-5.

Figure 2-4. Cache Line Bursting, End of Transfer (Little Endian Mode)

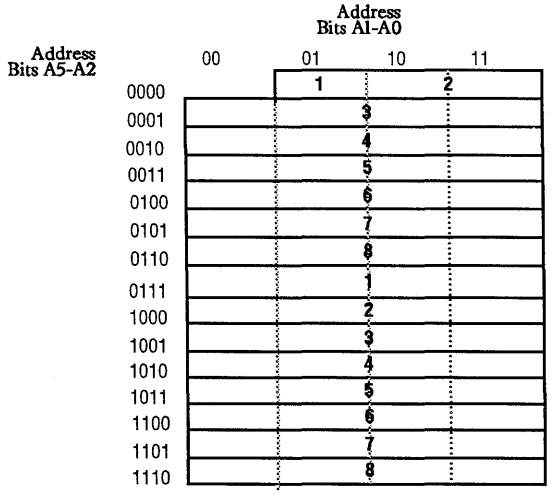


Notes:

a) This transfer assumes that the remaining byte count equals 31.

b) The 53C710 transfers each longword, word, and/or byte separately during the same bus ownership.

Figure 2-5. Programmable Bursting, Start of Transfer (Little Endian Mode)



Notes:

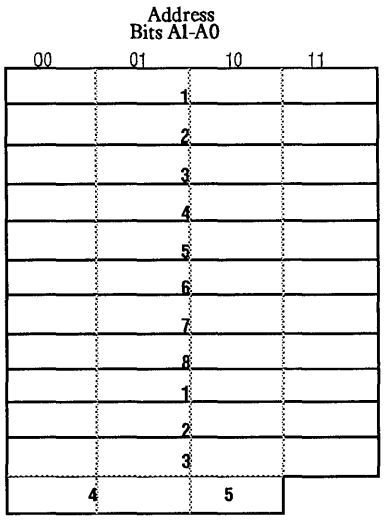
a) This transfer begins at Address 000001

b) The programmable burst length is 8

c) The 53C710 transfers each byte, word and longword separately during the same bus ownership.

End of Transfer
The 53C710 transfers longwords until the byte count decreases to 3 or less. If the byte count is 3 or 2, one word is transferred. If the byte count is 1, one byte is transferred. The 53C710 will transfer the programmable-burst-length number of transfers per bus ownership. At the end of a block transfer, if the byte count is less than the programmable-burst-length, the remaining bytes will be transferred during the bus ownership. It is possible to transfer less but not more than the programmable-burst-length number of transfers per bus ownership. An example of a transfer in which the programmable burst length is 8 is depicted in Figure 2-6. **Note:** Each bus ownership requires the 53C710 to arbitrate for the host bus. There is a fairness delay of 5-8 clocks between each bus ownership.

Figure 2-6. Programmable Bursting, End-of-Transfer (Little Endian Mode)



Notes:

a) At the start of this diagram, 47 bytes remain to be transferred

b) The programmable burst length is 8

c) Only three longwords, one word, and one byte are transferred in the last bus ownership.

Host Bus Retry

Host Bus Retry allows the 53C710 to retry the previous cycle using the same address, size, etc. The bus retry signals are asserted by an external device using the HALT/ (halt) and BERR/ (bus error) signals in Bus Mode 1, and TA/ (transfer acknowledge) and TEA/ (transfer error acknowledge) in Bus Mode 2. During a non-cache line burst, a bus retry can be executed in any cycle. During a cache line burst, however, the bus retry should be executed during the ACK portion of the first transfer in the first cycle. In both bus modes, the 53C710 will retry the bus cycle and assert the CBREQ/ (Cache Burst Request) again. If a bus retry is attempted during one of the subsequent cycles, the 53C710 will halt with a bus error status

Bidirectional STERM/TA

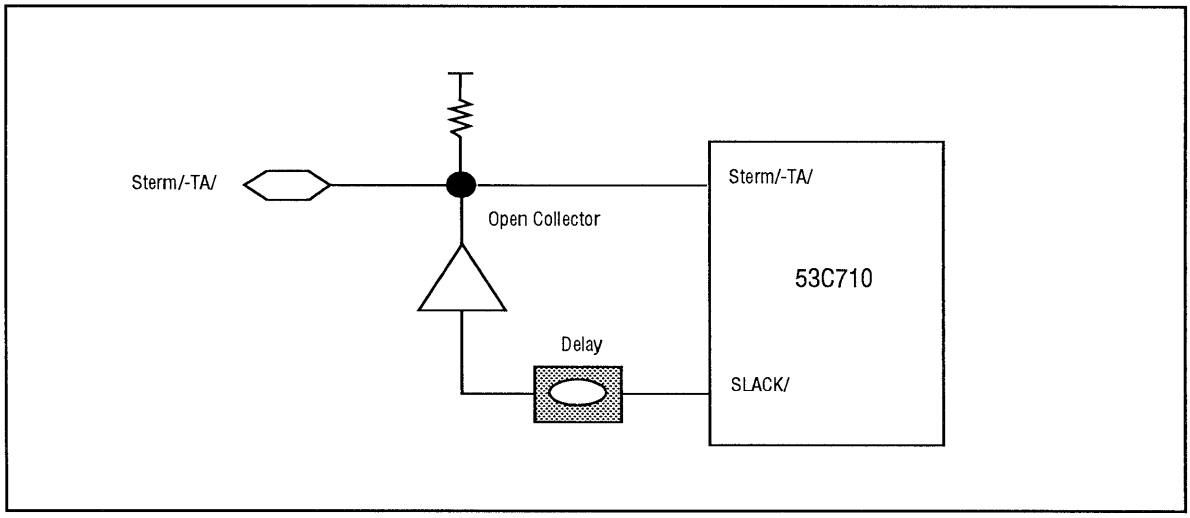
The STERM/TA signal terminates a read or write cycle. In a typical system, STERM/TA is a wire-OR signal driven by slave devices and monitored by bus masters. When the system CPU is faster than the slave device being accessed, a cycle may be terminated as soon as the slave is ready. Slave devices which are faster than the CPU are required to insert wait states to allow the CPU to catch up. The 53C710 is able to accommodate both situations.

During slave accesses, the SLACK output provides an indication that the 53C710 is ready to terminate a read or write cycle (similar to READYO on the 53C700). After asserting SLACK, the 53C710 will sample STERM/TA on every subsequent rising BCLK edge until it is sampled active, at which time the read/write cycle will be terminated (STERM/TA is analogous to READYI on the 53C700). Any time between SLACK and STERM/TA is treated as a wait state; a read/write cycle may be stretched indefinitely, but write data must be valid by the second clock cycle after Chip Select is sampled true.

Typically, SLACK is tied back to STERM/TA as in Figure 2-7. If the system CPU is not capable of completing a slave cycle in the minimum time required by the 53C710, SLACK must be delayed before asserting STERM/TA. If the system CPU is capable of running slave read/write cycles with zero additional wait states, no delay is necessary.

In systems where the CPU is faster than the 53C710, SLACK may be connected to STERM/TA with external logic, but the best solution is to set the Enable Acknowledge (EA) bit in the DCNTL register to internally connect SLACK to STERM/TA. When the EA bit is set, the STERM/TA pin changes from being an input in both master and slave modes, and becomes bidirectional: input in master mode, and output in slave mode. This way, no external logic is required and proper timing is guaranteed.

Figure 2-7. Bidirectional STERM/TA



SCSI Bus Interface

The 53C710 can be used in both single-ended and differential applications.

In single-ended mode, all SCSI signals are active low. The 53C710 contains the open-drain output drivers and can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down 53C710 has no effect on an active SCSI bus (CMOS "voltage feed-through" phenomenon). Additionally, signal filtering is present at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

In Differential Mode, the SDIR (7-0), SDIRP, IGS, TGS, RSTDIR, BSYDIR, and SELDIR signals control the direction of external differential-pair transceivers. See Figure 2-8 for the suggested differential wiring diagram. The wiring diagram shows five 75ALS170 3-channel transceivers and one 75ALS171 3-channel transceiver, though other single and multi-channel devices may be used (DS36954 4-channel transceiver, for instance). The suggested value for the 15 pull-up resistors in the diagram is 680Ω. If Active Negation is enabled and the chip is operating in differential mode, the value of the pull-up resistors should be 15KΩ. Pull-up resistors are not necessary on SCSI REQ, ACK, Data and Parity signals if Active Negation is enabled.

Terminator Networks

The terminator networks provide the biasing needed to pull inactive signals to an inactive voltage level, and are required for both single-ended and differential applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than 2 sets of terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed.

Single-ended cables are terminated differently from differential cables. Single-ended cables use a 220 ohm pull-up to the termination power supply (Term-Power) line and a 330 ohm pull-down to Ground. Differential cables use a 330 ohm pull-up from "– SIG" to Term-Power, a 330 ohm pull-down from "+ SIG" to Ground, and a 150 ohm resistor from "– SIG" to "+ SIG".

Because of the high performance nature of the 53C710, Alternative Two single-ended termination is recommended. This method employs a 2.85 Volt regulator and 110 Ohm pull-up resistors (no pull-down). Figure 2-9 shows the schematics for Alternative Two termination. For more information on Alternative Two termination, refer to the SCSI-2 specification.

(Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection or reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select one target and is reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection.

The 53C710 can handle this condition in a manner identical to the 53C700, that is, auto-switching between initiator and target modes, but the recommended method is to disable the auto-switching utility.

When auto-switching is enabled, regardless of the current operating mode (initiator or target), if the 53C710 becomes reselected while executing a (Re)Select instruction, then it will auto-switch to initiator mode. Similarly, if the 53C710 becomes selected while executing a (Re)Select instruction, it will auto-switch to target mode.

After the automatic mode switch, the 53C710 fetches the next instruction from the alternate address, pointed to by the DNAD register (the second 32-bit word of the (Re)Select instruction).

The recommended method of handling (re)selection during (re)selection is to disable auto-switching and put a Set Target instruction at the start of the target SCRIPT (before the Wait Select code).

Synchronous Operation

The 53C710 can transfer synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPT execution begins or from within a SCRIPT via a table indirect I/O instruction.

The 53C710 can always receive data at a synchronous transfer period of 100/200 ns (SCSI-2/SCSI-1), regardless of the transfer period used to send data. Therefore, when negotiating for synchronous data transfers, the suggested transfer period is 100/200 ns. Depending on the SCLK frequency, the 53C710 can send synchronous data at intervals as short as 100/200 ns.

Figure 2-8. Differential Wiring Diagram

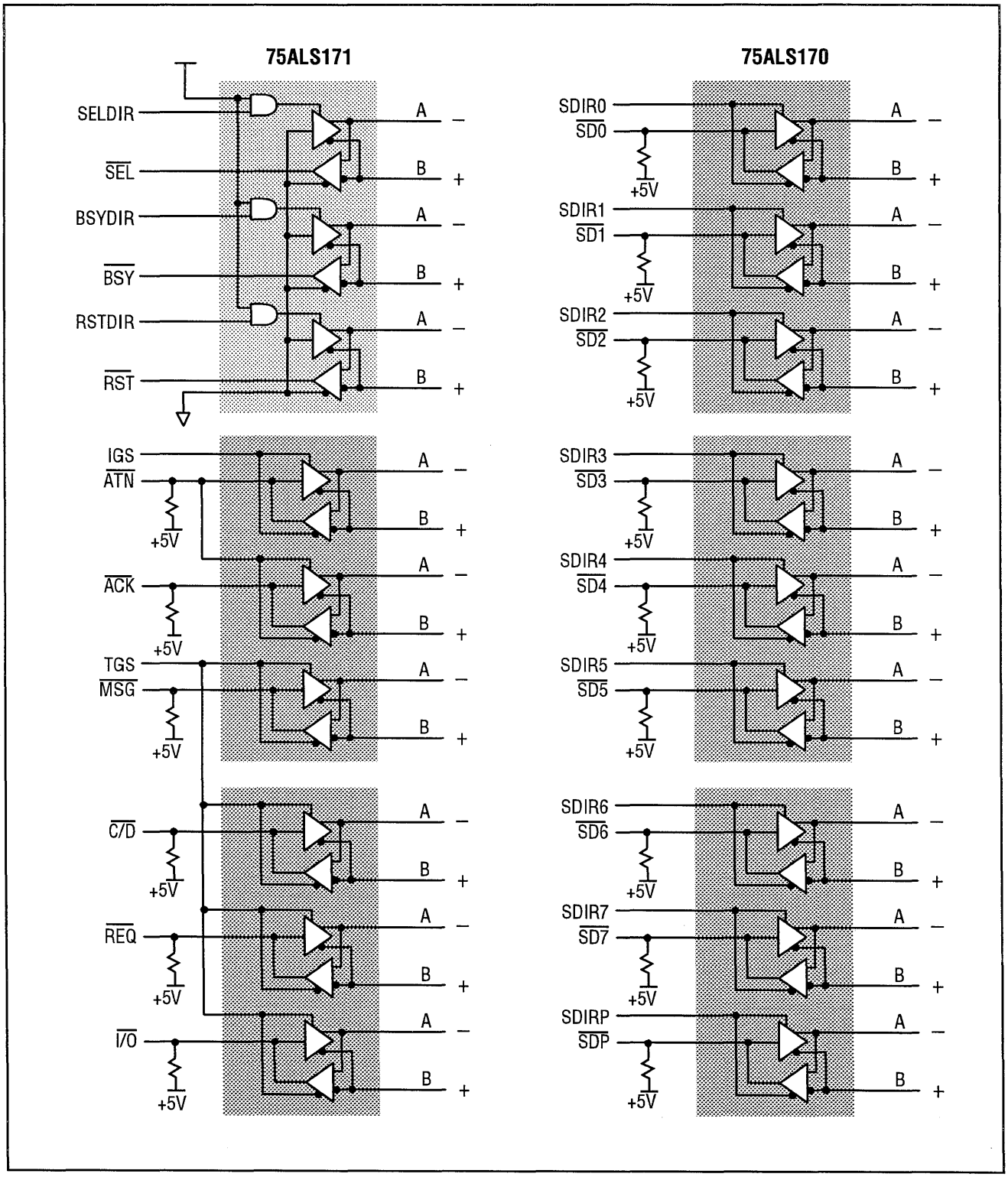
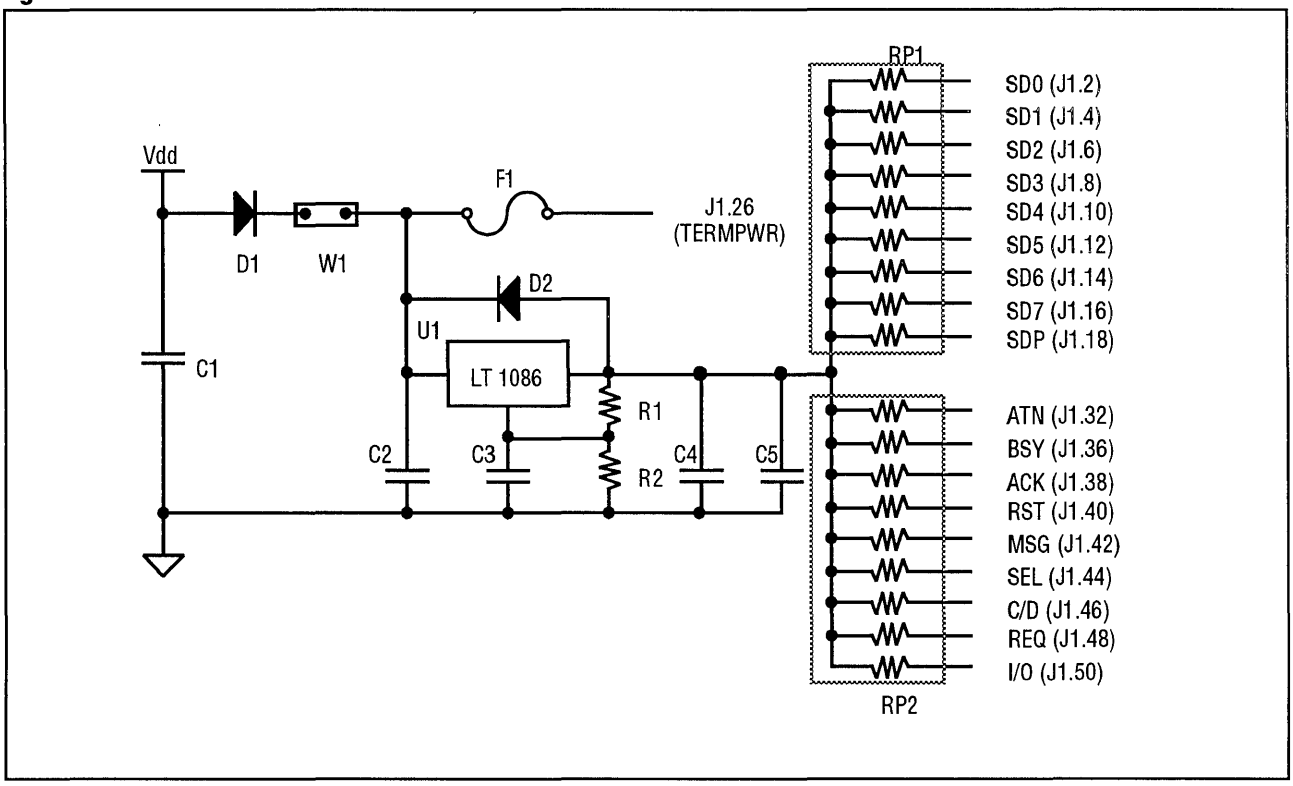


Figure 2-9. Alternative Two Termination



Key:

C1	4.7 µF tantalum, SMT
C2, C3	1.0 µF tantalum, SMT
C4	2.2 µF tantalum, SMT
C5	0.1 µF ceramic, SMT
D1-D2	Schottkey diode, 1NS817
F1	1.5 Amp fuse, socketed, 2AG
J1	50-pin dual row header, male SCSI connector
RP1-RP2	110 x 9 pull-ups, 1% SIP-10
U1	Voltage Regulator LT 1086, TO-39
W1	2-position jumper

Chapter 3

Signal Descriptions

The 53C710 host bus can operate in one of two modes: Bus Mode 1 (asynchronous) and Bus Mode 2 (synchronous). The bus mode is selected with the Bus Select pin. The signal types are abbreviated as follows: "I" for input, "O" for output, and "Z" for high-impedance. A slash ("/") indicates an active-low signal. Refer to the *DC Electrical Characteristics* section in Chapter 6 for specific pin type (tristate, open drain, etc.) and current drive capabilities.

Table 3-1. Interface Signals

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description
D(31-0)	D(31-0)	I/O	I/O	*Host Data Bus* – Main 32-bit data path into host memory.
DP(3-0)	DP(3-0)	I/O	I/O	*Host Bus Data Parity* – DP0 provides parity for D(7-0), DP1 for D(15-8), etc. Parity is valid on all byte lanes, including unused lanes. When the parity through mode is disabled, DP3 becomes a hardware abort input (ABRT/).
DS/	DLE			*Data Strobe, Data Latch Enable*
		Z	O	DS/ Indicates that valid data has been or should be placed on the data lines
		I	I	DLE Latches read data into the 53C710 when operating in Bus Mode 2. Data latches are transparent when DLE is high. This signal is used to address host memory and internal registers
A(31-0)	A(31-0)	I	O	*Address Bus*
AS/	TS/	I	O	*Address Strobe, Transfer Start*
				AS/ Indicates that a valid address is on A(31-0).
				TS/ Transfer start indicates that a bus cycle is starting and all of the status and address lines are valid.
R_W/	R_W/	I	O	*Read/Write* – Indicates the direction of the data transfer relative to the current master.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description
SIZ(1-0)	SIZ(1-0)	I	O	*Transfer Size* – Indicates the current transfer width. 00 Longword (4-bytes) 01 Byte (1-byte) 10 Word 11 Bus Mode 1: Illegal in slave mode, will not occur in master Bus Mode 2: Cache-line burst
STERM/	TA/	I(O)	I	*Synchronous Cycle Termination, Transfer Acknowledge* STERM/ Acknowledges transfer to a 32-bit wide port. When the EA bit in the DCNTL register is set, this signal becomes bidirectional: input in master mode and output in slave mode. TA/ Acknowledges transfer to a 32-bit wide port. When the EA bit in the DCNTL register is set, this signal becomes bidirectional: input in master mode and output in slave mode.
BERR/	TEA/	O	I	*Bus Error Acknowledge, Transfer Error Acknowledge* BERR/ Indicates that a bus fault has occurred. May be used with HALT/ to force a bus retry. TEA/ Indicates that a bus fault has occurred.
HALT/	TIP/	Z		*Halt, Transfer in Progress*
			I	HALT/ Input ONLY, used with BERR/ to indicate a bus retry cycle.
			O	TIP/ Bidirectional, indicates that bus activity is in progress.
SLACK/	SLACK/	O	O	*Slave Acknowledge* – When asserted, indicates the internal end of a slave mode cycle. The external slave cycle ends when the 53C710 observes either STERM/-TA/ or BERR/ -TEA/.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description
FC(2-0)	TM(2-0)	Z	O	*Function Codes, Transfer Modifiers* – Indicates the status of the current bus cycle. FC0, TM0 = 1 Indicates data space; it is the default for all transfers FC0, TM0 = 0 Indicates program space. It may be optionally selected when setting the PD bit in the DMODE register. FC1, TM1 User definable from the DMODE register bits. FC2, TM2 User definable from the DMODE register bits.
SC(1-0)	SC(1-0)	Z (O)	O	*Snoop Control* – Indicates the bus snooping level. The bits are user programmable through bits in the CTEST7 register. They are asserted when the 53C710 is the bus master. (SC(1-0) may optionally be used as pure outputs, active in both master and slave modes. See the CTEST8 register description for use of SC(1-0) as pure outputs.)
MASTER/	MASTER/	O	O	*Master Status* – Driven low when the 53C710 becomes bus master.
FETCH/	FETCH/	O	O	*Fetching Op Code* – Indicates that the next bus request will be for an op code fetch.
BR/	BR/	O	O	*Bus Request* – Indicates that there is a request to use the host bus.
BG/	BG/	I	I	*Bus Grant* – Indicates that the host bus has been granted to the 53C710.
BGACK/	BB/	Z	I/O	*Bus Grant Acknowledge, Bus Busy (can be wire-OR'd)* BGACK/ Indicates that the 53C710 or another device has taken control of the host bus signals. BB/ Indicates that the 53C710 or another device has taken control of the host bus signals.
BOFF/	BOFF/	I	I	*Back Off* – Forces the 53C710 to relinquish bus mastership at the end of the current cycle, if the proper setup timing requirements are met. When BOFF is deasserted, a new arbitration cycle will occur and bus cycles will resume.
BCLK	BCLK	I	I	*Bus Clock* – This clock controls all host related activity.
RESET/	RESET/	I	I	*Chip Reset* – Forces a full chip reset.
CS/	CS/	I	I	*Chip Select* – Selects the 53C710 as a slave I/O device. When CS/ is detected: Bus Mode 1: CBACK/ is deasserted Bus Mode 2: TBI/ is asserted.

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description
IRQ/	IRQ/	O	O	*Interrupt* – Indicates that service is required from the host CPU.
UPSO	TT0	Z	O	*User Programmable Status, Transfer Type Zero* UPSO – General purpose line. The value in a DMODE register bit is asserted while the chip is a bus master. TT0 – Indicates the current bus transfer type. This bit can be programmed from a register bit (default = 0). It is asserted only when the 53C710 is bus master.
CBREQ/	TT1/	Z	O	*Cache Burst Request, Transfer Type Bit 1* CBREQ/ – Cache burst request indicates an attempt to execute a line transfer of four long words TT1/ – Transfer type bit 1, output line indicating the current bus transfer type. This bit can be programmed from a CTEST7 register bit (default = 1). It is only asserted when the 53C710 is bus master.
CBACK/	TBI/	O	I	*Cache Burst Acknowledge, Transfer Burst Inhibit* CBACK/ – Indicates that the memory can handle a burst request. In slave mode this signal is deasserted in response to CS/. TBI/ – Transfer burst inhibit indicates that the memory can not currently handle a burst request. In slave mode this signal is asserted in response to CS/.
BS	BS	I	I	*Bus Mode Select* – Selects between asynchronous and synchronous host bus modes. BS = 0 – Bus Mode 2 (68040-like) host bus mode BS = 1 – Bus Mode 1 (68030-like) host bus mode
BIG_LIT/	BIG_LIT/	I	I	*Big/Little Endian Select* – Selects the byte order interpretation of data transferred between the HOST and SCSI bus. It also affects how the register set is addressed. BIG_LIT/ = 0 – Little Endian byte order BIG_LIT/ = 1 – Big Endian byte order

Table 3-1. Interface Signals (Continued)

Bus Mode 1	Bus Mode 2	Slave Type	Master Type	Description
SCLK	SCLK	I	I	*SCSI Clock* – SCLK is used to derive all SCSI related timings. The speed of this clock will be determined by the application's requirements; in some applications SCLK and BCLK may be tied to the same source.
SD(7-0)	SDP/	I/O	I/O	*SCSI Data* SD/(7-0) 8-bit SCSI data bus SDP/ SCSI data parity bit
SCTRL/	SCTRL/	I/O	I/O	*SCSI Control* CD/ SCSI phase line, command/data IO/ SCSI phase line, input/output MSG/ SCSI phase line, message REQ/ Data handshake signal from target device ACK/ Data handshake signal from initiator device ATN/ SCSI bus attention signal. BSY/* SCSI bus arbitration signal, signal busy SEL/* SCSI bus arbitration signal, select device RST/* SCSI bus reset. *(BSY/, SEL/, and RST/ are input only in Differential Mode.)
SDIR(7-0)	SDIR(7-0)	O	O	*Differential Support Lines* – Driver direction control for SCSI data lines.
SDIRP	SDIRP	O	O	*Differential Support Line* – Driver direction control for SCSI parity signal.
BSYDIR	BSYDIR	O	O	*Differential Support Line* – Driver enable control for SCSI BSY/ signal.
SELDIR	SELDIR	O	O	*Differential Support Line* – Driver enable control for SCSI SEL/ signal.
RSTDIR	RSTDIR	O	O	*Differential Support Line* – Driver enable control for SCSI RST/ signal.
IGS	IGS	O	O	*Differential Support Line* – Direction control for initiator driver group.
TGS	TGS	O	O	*Differential Support Line* – Direction control for target driver group.

Chapter 4

Registers

This chapter contains descriptions of all 53C710 registers. Table 4-1 summarizes the 53C710 register set. Figure 4-1 shows a more graphical representation of the register set and lists registers by both their Big and Little Endian addresses. Figure 4-1, the register map, is left-justified for Big Endian addresses and right-justified for Little Endian addresses.

Table 4-1. Register Addresses and Descriptions

Little Endian Address	Big Endian Address	Read/ Write	Label	Description
00	03	R/W	SCNTL0	SCSI control 0
01	02	R/W	SCNTL1	SCSI control 1
02	01	R/W	SDID	SCSI destination ID
03	00	R/W	SIEN	SCSI interrupt enable
04	07	R/W	SCID	SCSI chip ID
05	06	R/W	SXFER	SCSI transfer
06	05	R/W	SODL	SCSI output data latch
07	04	R/W	SOCL	SCSI output control latch
08	0B	R/W*	SFBR	SCSI first byte received *(Write restrictions apply; refer to register description.)
09	0A	R	SIDL	SCSI input data latch
0A	09	R	SBDL	SCSI bus data lines
0B	08	R/W	SBCL	SCSI bus control lines
0C	0F	R	DSTAT	DMA status
0D	0E	R	SSTAT0	SCSI status 0
0E	0D	R	SSTAT1	SCSI status 1
0F	0C	R	SSTAT2	SCSI status 2
10-13	10-13	R/W	DSA	Data structure address
14	17	R/W	CTEST0	Chip test 0
15	16	R	CTEST1	Chip test 1
16	15	R	CTEST2	Chip test 2
17	14	R	CTEST3	Chip test 3

Table 4-1. Register Addresses and Descriptions (Continued)

Little Endian Address	Big Endian Address	Read/ Write	Label	Description
18	1B	R/W	CTEST4	Chip test 4
19	1A	R/W	CTEST5	Chip test 5
1A	19	R/W	CTEST6	Chip test 6
1B	18	R/W	CTEST7	Chip test 7
1C-1F	1C-1F	R/W	TEMP	Temporary stack
20	23	R/W	DFIFO	DMA FIFO
21	22	R/W	ISTAT	Interrupt status
22	21	R/W	CTEST8	Chip test 8
23	20	R/W	LCRC	Longitudinal parity
24-26	25-27	R/W	DBC	DMA byte counter
27	24	R/W	DCMD	DMA command
28-2B	28-2B	R/W	DNAD	DMA next address for data
2C-2F	2C-2F	R/W	DSP	DMA SCRIPTS pointer
30-33	30-33	R/W	DSPS	DMA SCRIPTS pointer save
34-37	34-37	R/W	SCRATCH	General purpose scratch pad
38	3B	R/W	DMODE	DMA mode
39	3A	R/W	DIEN	DMA interrupt enable
3A	39	R/W	DWT	DMA watchdog timer
3B	38	R/W	DCNTL	DMA control
3C-3F	3C-3F	R	ADDER	Sum output of internal adder

Figure 4-1. Register Address Map

Big Endian Mode (Left-justified) →

SCRIPTS and Little Endian Mode ← (Right-justified)

00	SIEN	SDID	SCNTL1	SCNTL0	00
04	SOCL	SODL	SXFER	SCID	04
08	SBCL	SBDL	SIDL	SFBR	08
0C	SSTAT2	SSTAT1	SSTAT0	DSTAT	0C
10	DSA				10
14	CTEST3	CTEST2	CTEST1	CTEST0	14
18	CTEST7	CTEST6	CTEST5	CTEST4	18
1C	TEMP				1C
20	LCRC	CTEST8	ISTAT	DFIFO	20
24	DCMD	DBC			24
28	DNAD				28
2C	DSP				2C
30	DSPS				30
34	SCRATCH				34
38	DCNTL	DWT	DIEN	DMODE	38
3C	ADDER				3C

Register Descriptions

Throughout this chapter, registers are referenced by their Little Endian addresses, with Big Endian addresses in parentheses.

The term "set" is used to refer to bits that are programmed to a binary one. Similarly, the terms "clear" and "reset" are used to refer to bits that are programmed to a binary zero.

Reserved bits are designated as "RES" in each register diagram. These bits should always be written to zero; mask all information read from them.

Unless otherwise indicated, all bits in registers are active high, i.e., the feature is enabled by setting the bit.

The bottom line of every register diagram shows the default register values after the chip is powered-up or reset. In the default lines below each diagram, a value of 1 indicates that the register is set; a value of 0 indicates that the bit is clear; and a value of X indicates that the default is indeterminate or is a don't care.

WARNING: *The only register that the host CPU can access while the 53C710 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere with the operation of the chip. All registers are accessible via SCRIPTS.*

Register 00 (03) SCSI Control 0 (SCNTL0)

Read/Write

ARB1	ARB0	START	WATN/	EPC	EPG	AAP	TRG
7	6	5	4	3	2	1	0

Default >>>

1	1	0	0	0	0	0	0

Bit 7 ARB1 (Arbitration mode bit 1)

Bit 6 ARB0 (Arbitration mode bit 0)

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection or reselection

Simple Arbitration

1) The 53C710 waits for a bus free condition to occur.
2) It asserts BSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus

   If the SEL/ signal is asserted by another SCSI device, the 53C710 will deassert BSY/, deassert its ID and set the Lost Arbitration bit in the SSTAT1 register.
3) After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the 53C710 has won arbitration.
4) Once the 53C710 has won arbitration, SEL must be asserted via the SOCL for a bus clear plus a bus settle delay (1.2 µs) before a low-level selection can be performed.

Full Arbitration, Selection/Reselection

1) The 53C710 waits for a bus free condition.
2) It asserts BSY/ and its SCSI ID (the highest priority ID stored in the SCID register) onto the SCSI bus.
3) If the SEL/ signal is asserted by another SCSI device or if the 53C710 detects a higher priority ID, the 53C710 will deassert BSY/, deassert its ID, and wait until the next bus free state to try arbitration again.
4) The 53C710 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT1 register.
5) The 53C710 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SDID register) and the 53C710's ID (the highest priority ID stored in the SCID register).
6) After a selection is complete, the Function Complete bit is set in the SSTAT0 register.
7) If a selection timeout occurs, the Selection Timeout bit is set in the SSTAT0 register.

Bit 5 START (Start sequence)
When this bit is set, the 53C710 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is used in low-level mode; when executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the connected bit in the SCNTL1 register indicates that 53C710 is already connected to the SCSI bus.

This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, the connected bit in the SCNTL1 register should be checked to verify that the 53C710 did not connect to the SCSI bus.

Bit 4 WATN (Select with ATN/ on a start sequence)
When this bit is set, the SCSI ATN/ signal will be asserted during the selection phase (ATN/ is asserted at the same time BSY/ is deasserted while selecting a target). If a selection timeout occurs during an attempt to select a target device, ATN/ will be deasserted at the same time SEL/ is deasserted.

When this bit is clear, the ATN/ signal will not be asserted during selection.

When executing SCSI SCRIPTS this bit is controlled by the SCRIPTS processor, but it may be set manually in low-level mode.

Bit 3 EPC (Enable parity checking)
When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. The host data bus is checked for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SODL register when sending SCSI data in either initiator or target mode. If a parity error is detected, bit 0 of the SSTAT0 register is set and an interrupt may be generated.

If the 53C710 is operating in initiator mode and a parity error is detected, ATN/ can optionally be asserted, but the transfer continues until the target changes phase to Message Out.

When this bit is cleared, parity errors are not reported.

Bit 2 EPG (Enable parity generation/parity through)
When this bit is set, the SCSI parity bit will be generated by the 53C710. The host data bus parity lines DP(3-0) are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines will flow through the 53C710's internal FIFOs and be driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus).

This bit is set to enable the DP3_ABRT/ pin to function as an abort input (ABRT/).

Bit 1 AAP (Assert ATN/ on parity error)
When this bit is set, the 53C710 automatically asserts the SCSI ATN/ signal upon detection of a parity error. ATN/ is only asserted in initiator mode. The ATN/ signal is asserted before deasserting ACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the 53C710 to assert ATN/ in this manner. The following parity errors can occur:

1) A parity error detected on data received from the SCSI bus.
2) A parity error detected on data transferred to the 53C710 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

Bit 0 TRG (Target mode)
This bit determines the default operating mode of the 53C710, though there are instances when the chip may act in a role other than the default. For example, a mostly-initiator device may be selected as a target. An automatic mode change does not affect the state of this bit. After completion of a mode change I/O operation, the 53C710 returns to the role defined by this bit.

When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the 53C710 is an initiator device by default.

Register 01 (02) SCSI Control One (SCNTL1)

Read/Write

EXC 7	ADB 6	ESR 5	CON 4	RST 3	AESP 2	RES 1	RES 0

Default >>>

0 0 0 0 0 0 0 0

Bit 7 EXC (Extra clock cycle of data setup)
When this bit is set, an extra clock period of data setup is added to each SCSI data transfer. The extra data setup time can provide additional system design flexibility, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

Bit 6 ADB (Assert SCSI data bus)
When this bit is set, the 53C710 drives the contents of the SCSI Output Data Latch (SODL) register onto the SCSI data bus. When the 53C710 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. When the 53C710 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the 53C710 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low-level mode.

Bit 5 ESR (Enable selection & reselection)
When this bit is set, the 53C710 will respond to bus-initiated selections and reselections. The 53C710 can respond to selections and reselections in both initiator and target roles. If SCSI Disconnect/Reconnect is to be supported, this bit should be set as part of the initialization routine.

Bit 4 CON (Connected)
This bit is automatically set any time the 53C710 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C710 has responded to a bus initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low-level mode. When this bit is clear, the 53C710 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

Bit 3 RST (Assert SCSI RST/ signal)
Setting this bit asserts the SCSI RST/ signal. The RST/ signal remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor ora SCRIPTS delay routine.

Bit 2 AESP (Assert even SCSI parity (force bad parity))
When this bit is set and the Enable Parity Generation bit is set in the SCNTL0 register, the 53C710 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the 53C710. If parity checking is enabled, then the 53C710 checks data received for odd parity. This bit is used for diagnostic testing and should be clear during normal operation. It can be used to generate parity errors, to test error handling functions.

Bit 1 Reserved
Bit 0 Reserved

Register 02 (01) SCSI Destination ID (SDID)

Read/Write

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-0 ID7-ID0 (SCSI ID 7-0)
This register sets the SCSI ID of the device to be selected when executing a select or reselect command. Only one of these bits should be set for proper selection or reselection. When executing SCSI SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTS Select or Reselect instruction.

Note: When using Table Indirect I/O commands, the destination ID will be loaded from the data structure.

Register 03 (00) SCSI Interrupt Enable (SIEN)

Read/Write

M/A	FCMP	STO	SEL	SGE	UDC	RST/	PAR
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bit 7 M/A (Initiator: phase mismatch, or Target: ATN/ active)

Bit 6 FCMP (Function complete)

Bit 5 STO (SCSI bus timeout)

Bit 4 SEL (Selected or reselected)

Bit 3 SGE (SCSI gross error)

Bit 2 UDC (Unexpected disconnect)

Bit 1 RST/ (SCSI RST/ received)

Bit 0 PAR (Parity error)

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SSTAT0 register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the SSTAT0 register. Masking an interrupt will not prevent the ISTAT SIP bit from being set, except in the case of non-fatal interrupts (SEL and FCMP). Setting a mask bit unmasks the corresponding interrupt, enabling the assertion of IRQ/ for that interrupt.

A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT SIP or DIP bit is set.

The 53C710 IRQ/output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted. In the case of non-fatal interrupts, masking an interrupt after it occurs will cause the ISTAT SIP bit to clear and allow pending interrupts to fall through (interrupt stacking will be disabled).

Register 04 (07) SCSI Chip ID (SCID)

Read/Write

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-0 ID7-ID0 (SCSI ID 7-0)

This register sets up the 53C710's SCSI ID. If more than one bit is set, the 53C710 will respond to each corresponding SCSI ID. The 53C710 always uses the highest priority SCSI ID during arbitration. For example, if 84h were written to this register, the 53C710 would respond when another device selects ID 7 or ID 2. When arbitrating for the SCSI bus, ID 7 would be used as the 53C710's SCSI ID.

Register 05 (06) SCSI Transfer (SXFER)

Read/Write

DHP	TP2	TP1	TP0	MO3	MO2	MO1	MO0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

***Note:** When using Table Indirect I/O commands, bits 6-0 of this register will be loaded from the I/O data structure.*

Bit 7 DHP (Disable halt on parity error or ATN/)
When this bit is cleared, the 53C710 immediately halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the 53C710 may transfer up to 3 additional bytes before halting to synchronize between internal core cells. During synchronous operation, the 53C710 transfers data until there are no outstanding synchronous offsets. If the 53C710 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. While sending data in target mode with pass parity enabled, the byte with the parity error will not be sent across the SCSI bus.

When this bit is set, the 53C710 does not halt the SCSI transfer when a parity error is received until the end of a Block Move operation. When this bit is set and the initiator asserts ATN/, the 53C710 will complete the Block Move and then, depending on whether or not the ATN/ interrupt is enabled, either generate an interrupt or continue fetching instructions (the instruction following the should be a MOVE address, IF ATN).

Bit 6 TP2 (SCSI synchronous transfer period bit 2)
Bit 5 TP1 (SCSI synchronous transfer period bit 1)
Bit 4 TP0 (SCSI synchronous transfer period bit 0)
These bits determine the SCSI synchronous transfer period used by the 53C710 when sending synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data transfer period used by the 53C710.

TP2	TP1	TP0	XFERP
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The actual synchronous transfer period used by the 53C710 when transferring SCSI data is defined by the following equations:

The minimum synchronous transfer period when sending SCSI data:

Period = TCP * (4 + XFERP + 1)

If Bit 7 in the SCNTL1 register is set
(one extra clock cycle of data setup)

Period = TCP * (4 + XFERP)

If Bit 7 in the SCNTL1 register is clear
(no extra clock cycle of data setup)

The minimum synchronous transfer period when receiving SCSI data:

Period = TCP * (4 + XFERP)

Whether sending or receiving, TCP = 1 / SCSI core clock frequency. The SCSI core clock frequency is determined by the CF(1-0) bits in the DCNTL register and SSCF(1-0) bits in SBCL.

The following table gives examples of synchronous transfer periods for SCSI-1 transfer rates.

CLK (MHz)	SCSI CLK / DCNTL bits 7, 6	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	/3	0	180	5.55
66.67	/3	1	225	4.44
50	/2	0	160	6.25
50	/2	1	200	5
40	/2	0	200	5
37.50	/1.5	0	160	6.25
33.33	/1.5	0	180	5.55
25	/1	0	160	6.25
20	/1	0	200	5
16.67	/1	0	240	4.17

The following table gives example transfer periods for fast SCSI-2 transfer rates.

CLK (MHz)	SCSI CLK / SBCL bits 1, 0	XFERP	Synch Transfer Period (ns)	Synch Transfer Rate (MB/S)
66.67	/1.5	0	90	11.11*
66.67	/1.5	1	112.5	8.88
50	/1	0	80	12.5*
50	/1	1	100	10.0
40	/1	0	100	10.0
37.50	/1	0	106.67	9.375
33	/1	0	120	8.33
25	/1	0	160	6.25
20	/1	0	200	5
16.67	/1	0	240	4.17

* *Violates SCSI specifications.*

Bits 3-0 MO3-MO0 (Max SCSI synchronous offset)
These bits describe the maximum SCSI synchronous offset used by the 53C710 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the 53C710. These bits determine the 53C710's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0 – Asynchronous operation
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	X	X	1	Reserved
1	X	1	X	Reserved
1	1	X	X	Reserved

Register 06 (05) SCSI Output Data Latch (SODL)

Read/Write

SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-0 SD7-SD0 (SCSI output data latch)

This register is used primarily for diagnostics testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register is used to send data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip.

Register 07 (04) SCSI Output Control Latch (SOCL)

Read/Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bit 7 REQ (Assert SCSI REQ/ signal)

Bit 6 ACK (Assert SCSI ACK/ signal)

Bit 5 BSY (Assert SCSI BSY/ signal)

Bit 4 SEL (Assert SCSI SEL/ signal)

Bit 3 ATN (Assert SCSI ATN/ signal)

Bit 2 MSG (Assert SCSI MSG/ signal)

Bit 1 C/D (Assert SCSI C/D signal)

Bit 0 I/O (Assert SCSI I/O signal)

This register is used primarily for diagnostics testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set or reset when executing SCSI SCRIPTS. Do not write to the register once the 53C710 becomes connected and starts executing SCSI SCRIPTS.

Register 08 (0B) SCSI First Byte Received (SFBR)

Read/Write

1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0
7	6	5	4	3	2	1	0

Default >>>

0 0 0 0 0 0 0 0

Bits 7-0 1B7-IB0 (First byte received)

This register contains the first byte received in any asynchronous information transfer phase. For example, when the 53C710 is operating in initiator mode, this register contains the first byte received in Message In, Status Phase, Reserved In and Data In.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register even if the present phase is the same as the last phase. The first-byte-received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

Additionally, the SFBR register may be used to contain the device ID after a selection or reselection, if the COM bit is clear in the DCNTL register. However, for maximum flexibility it is strongly recommended that the ID byte be directed only to the LCRC register (COM bit set).

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate 53C710 register (such as the SCRATCH register), and then to the SFBR.

Register 09 (0A) SCSI Input Data Latch (SIDL)

Read Only

SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
7	6	5	4	3	2	1	0

Default >>>

0 0 0 0 0 0 0 0

Bits 7-0 SD7-SD0 (SCSI input data latch)

This register is used primarily for diagnostics testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the 53C710 by reading this register to provide loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register, this register contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid.

Register 0A SCSI Bus Data Lines (SBDL)

Read Only

DB7 7	DB6 6	DB5 5	DB4 4	DB3 3	DB2 2	DB1 1	DB0 0
Default >>>							
X	X	X	X	X	X	X	X

Bits 7-0 SD7-SD0 (SCSI bus data)

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time that the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostics testing or in low-level mode.

Register 0B (08) SCSI Bus Control Lines (SBCL)

Read/Write

REQ 7	ACK 6	BSY 5	SEL 4	ATN 3	MSG 2	C/D 1	I/O 0
Default >>>							
X	X	X	X	X	X	X	X

Bit 7 REQ (REQ/ status)

Bit 6 ACK (ACK/ status)

Bit 5 BSY (BSY/ status)

Bit 4 SEL (SEL/ status)

Bit 3 ATN (ATN/ status)

Bit 2 MSG (MSG/ status)

Bit 1 C/D (C/D status)

Bit 0 I/O (I/O status)

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read. This register can be used for diagnostics testing or operation in low-level mode.

Writing to bits 7-2 has no effect.

Bits 1-0 SSCF1-SSCF0 (Synchronous SCSI Clock Control bits)

SSCF1	SSCF0	Synchronous CLK
0	0	Set by DCNTL
0	1	SCLK / 1.0
1	0	SCLK / 1.5
1	1	SCLK / 2.0

When written, these bits determine the clock prescale factor used by the synchronous portion of the SCSI core. The default is to use the same clock prescale factor as the asynchronous logic (set by CF(1-0) in DCNTL). Setting one or both of these bits allows the synchronous logic to run at a different speed than the asynchronous logic; this is necessary for fast SCSI-2.

Register 0C (0F) DMA Status (DSTAT)

Read Only

DFE	RES	BF	ABRT	SSI	SIR	WTD	IID
7	6	5	4	3	2	1	0
Default >>>							
1	0	0	0	0	0	0	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C710 stacks interrupts). DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of both the DSTAT and SSTAT0 registers (in either order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading both registers when both the ISTAT SIP and DIP bits may not be set, the SSTAT0 register should be read before the DSTAT register to avoid missing a SCSI interrupt. Both concerns are avoided if the registers are read together as a 32-bit longword.

Bit 7 DFE (DMA FIFO empty)
This status bit is set when the DMA FIFO is empty. This bit may be changing at the time this register is read. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and reading it will not cause an interrupt.

Bit 6 RES (Reserved)

Bit 5 BF (Bus fault)
This bit is set when a host bus fault condition is detected. A host bus fault occurs when the 53C710 is bus master, and is defined as a memory cycle that is ended by the assertion of BERR/ (without HALT/) or TEA/ (without TA/). A bus fault will also occur if Retry is attempted after the first transfer of a cache line burst.

Bit 4 ABRT (Aborted)
This bit is set when an abort condition occurs. An abort condition occurs because of the following: the DP3_ABRT/ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting bit 7 of the ISTAT register.

Bit 3 SSI (SCRIPT step interrupt)
If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after executing each SCRIPTS instruction.

Bit 2 SIR (SCRIPT interrupt instruction received)
This status bit is set whenever an Interrupt instruction is evaluated as true.

Bit 1 WTD (Watchdog timeout detected)
This status bit is set when the watchdog timer decrements to zero. The watchdog timer is only used for the host memory interface. When the timer decrements to zero, it indicates that the memory system did not assert the acknowledge signal within the specified timeout period.

Bit 0 IID (Illegal instruction detected)
This status bit will be set any time an illegal instruction is decoded, whether the 53C710 is operating in single-step mode or automatically executing SCSI SCRIPTS.

This bit will also be set if the 53C710 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

Register 0D (0E) SCSI Status Zero (SSTAT0)

Read Only

M/A	FCMP	STO	SEL	SGE	UDC	RST/	PAR
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C710 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN register.

When performing consecutive 8-bit reads of both the DSTAT and SSTAT0 registers (in either order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading both registers when both the ISTAT SIP and DIP bits may not be set, read the SSTAT0 register before the DSTAT register to avoid missing a SCSI interrupt. To clear the interrupts and avoid missing a SCSI interrupt, read both registers together as a 32-bit longword.

Bit 7 M/A (Initiator: phase mismatch, or Target: ATN/ active)
In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the SCSI phase defined in a Block Move instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator.

Bit 6 FCMP (Function complete)
This bit is set when an arbitration only or full arbitration sequence has completed.

Bit 5 STO (SCSI bus timeout)
This bit is set if one of the following conditions occurs:

1) There is a selection or reselection timeout. A selection/reselection timeout occurs if the device being selected or reselected does not respond within the 250 ms timeout period.
2) The Wait for Disconnect takes longer than 250 ms. The Wait for Disconnect instruction has a bus activity timer that is reset by the physical disconnect.
3) No SCSI activity occurs for 250 ms while the 53C710 is connected to the bus. There is a timer on all bytes (in all phases) sent or received on the SCSI bus. The timer is a bus activity timer that is reset by a byte going over the SCSI bus. If 250 ms pass without a byte being moved, then a timeout will occur.

Bit 4 SEL (Selected or reselected)
This bit is set when the 53C710 is selected or reselected by another SCSI device. The Enable Selection and Reselection bit must be set in the SCNTL1 register for the 53C710 to respond to selection and reselection attempts.

Bit 3 SGE (SCSI gross error)
This bit is set when the 53C710 encounters a SCSI Gross Error condition. The following conditions can cause a SCSI Gross Error condition.

1) *Data underflow* – The SCSI FIFO register was read when no data was present.
2) *Data overflow* – Too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.
3) *Offset underflow* – When the 53C710 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.
4) *Offset overflow* – The other SCSI device sent a REQ/ or ACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.
5) *Residual data in the synchronous data FIFO* – A transfer other than synchronous data receive was started with data left in the synchronous data FIFO.
6) A phase change occurred with an outstanding synchronous offset when the 53C710 was operating as an initiator.

Bit 2 UDC (Unexpected disconnect)
This bit is only valid when the 53C710 is in initiator mode. It is set when the 53C710 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. When the 53C710 is executing SCSI SCRIPTS, an unexpected disconnect is defined to be a disconnect that does not occur after receiving either a Disconnect Message (04h) or a Command Complete Message (00h). When the 53C710 operates in low-level mode, any disconnect can cause an interrupt, even a valid SCSI disconnect.

Bit 1 RST/ (SCSI RST/ received)
This bit is set when the 53C710 detects an active RST/ signal, whether the reset was generated outside the chip or caused by the Assert RST/ bit in the SCNTL1 register. The 53C710 SCSI reset detection logic is edge-sensitive, so that multiple interrupts will not be generated for a single assertion of the SCSI RST/ signal.

Bit 0 PAR (Parity error)
This bit is set when the 53C710 detects a parity error while sending or receiving SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register. A parity error can occur from the host bus only if pass through parity is enabled (bit 3 in the SCNTL0 register = 1, bit 2 in the SCNTL0 register = 0).

Register 0E (0D) SCSI Status One (SSTAT1)

Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
7	6	5	4	3	2	1	0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7 ILF (SIDL register full)
This bit is set when the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6 ORF (SODR register full)
This bit is set when the SCSI Output Data Register (SODR), a hidden buffer register which is not directly accessible, contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is a not accessible to the user (cannot be read or written). This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5 OLF (SODL register full)
This bit is set when the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output Data Register (SODR), a hidden buffer register

which is not accessible, and then to the SODL register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 4 AIP (Arbitration in progress)
Arbitration in Progress (AIP = 1) indicates that the 53C710 has detected a bus free condition, asserted BSY and asserted its SCSI ID onto the SCSI bus.

Bit 3 LOA (Lost arbitration)
When set, LOA indicates that the 53C710 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

Bit 2 WOA (Won arbitration)
When set, WOA indicates that the 53C710 has detected a bus free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration and selection for this bit to be set.

Bit 1 RST/ (SCSI RST/ signal)
This bit represents the current status of the SCSI RST/ signal. This signal is not latched and may be changing when read.

Bit 0 SDP/ (SCSI SDP/ parity signal)
This bit represents the current status of the SCSI SDP/ parity signal. This signal is not latched and may be changing when read.

Register 0F (0C) SCSI Status Two (SSTAT2)

Read Only

FF3	FF2	FF1	FF0	SDP	MSG	C/D	I/O
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-4 FF3-FF0 (FIFO flags)

FF3	FF2	FF1	FF0	Bytes in the SCSI FIFO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

These four bits define the number of bytes that currently reside in the 53C710's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO. Because the FIFO is only 8 bytes deep, values over 8 will not occur.

Bit 3 SDP (Latched SCSI parity)
This bit reflects the SCSI parity signal (SDP/) corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the SIDL register. This bit is active high: it is set when the parity signal is active.

Bit 2 MSG (SCSI MSG/ signal)
Bit 1 C/D (SCSI C/D signal)
Bit 0 I/O (SCSI I/O signal)
These SCSI phase status bits are latched on the asserting edge of REQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low-level mode.

Registers 10-13 (10-13) Data Structure Address (DSA)

Read/Write

This register contains the base address used for all table indirect calculations. It is 32 bits wide and defaults to all zeros.

During any Memory Move operation, the contents of this register are overwritten. If the DSA value is needed for a subsequent SCSI SCRIPT, save and later restore it. Note that it is possible to perform a Memory-to-DSA Move, but not a DSA-to-Memory Move.

The Table Indirect SCRIPTS addressing mode is described in detail in the 53C710 *Programmer's Guide.*

Register 14 (17) Chip Test Zero (CTEST0)

Read/Write

RES 7	BTD 6	GRP 5	EAN 4	HSC 3	ERF 2	RES 1	DDIR 0

Default >>>

0 0 0 0 0 0 0 0

Bit 7 Reserved

This bit must always be written to zero.

Bit 6 BTD (Byte-to-Byte Timer Disable)

This bit, in conjunction with the Notime bit in CTEST4, provides the following selection/byte-to-byte timer options: at power-up or if both bits are not set, the selection and byte-to-byte timer are enabled; if Notime is set, both functions are disabled; if Notime is not set and the byte-to-byte disable is set, the selection timer will function but the byte-to-byte timer will be disabled.

Bit 5 GRP (Generate Receive Parity for Pass-Through)

When this bit is set, and the 53C710 is in parity pass-through mode, the parity received on the SCSI bus will not pass through to the DMA FIFO. Parity will be generated as data enters the DMA FIFO, eliminating the possibility of bad SCSI parity passing through to the host bus. A SCSI parity error interrupt will be generated, but a system parity problem will not be created. After reset or when the bit is cleared, while parity pass-through mode is enabled, parity received on the SCSI bus will pass through the 53C710 unmodified.

Bit 4 EAN (Enable Active Negation)

Asserting this bit will cause SCSI Request, Acknowledge, Data and Parity to be actively deasserted, instead of relying on external pull-ups, when the 53C710 is driving these signals. Active deassertion of these signals will occur only when the 53C710 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, Active Negation should be enabled to improve setup and hold times. After reset or when the bit is cleared, Active Negation is disabled.

Bit 3 HSC (Halt SCSI Clock)

Asserting this bit causes the internal divided SCSI clock to stop in a glitchless manner. This bit may be used for test purposes or to lower I_{dd} during a power-down mode.
Note: *SCSI registers must be reinitialized at power-up.*

Bit 2 ERF (Extend REQ/ACK Filtering)

The SCSI core contains a special digital filter on the REQ/ and ACK/ pins which will cause glitches on deasserting edges to be disregarded. Asserting this bit will extend the filter delay from 30 ns to 60 ns on the deasserting edge of the REQ/ and ACK/ signals. The 30 ns delay should be used for fast SCSI. ***Note:*** *This bit must never be set during fast SCSI operations (>5M transfers per second), because a valid assertion could be treated as a glitch. This bit does not affect transfer rates.*

Bit 1 Reserved

Bit 0 DDIR (Data transfer direction)

This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus. This bit cannot be written.

Register 15 (16) Chip Test One (CTEST1)

Read Only

FMT3 7	FMT2 6	FMT1 5	FMT0 4	FFL3 3	FFL2 2	FFL1 1	FFL0 0
Default >>>							
1	1	1	1	0	0	0	0

Bits 7-4 FMT3-FMT0 (Byte empty in DMA FIFO)

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane 3 is empty, then FMT3 will be 1. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

Bits 3-0 FFL3-FFL0 (Byte full in DMA FIFO)

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane 3 is full, then FFL3 will be 1. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register 16 (15) Chip Test Two (CTEST2)

Read Only

RES	SIGP	SOFF	SFP	DFP	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0

Default >>>

0	0	1	0	0	0	0	1

Bit 7 RES (Reserved)

Bit 6 SIGP (Signal process)
This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is a flag which may be passed to or from a running SCRIPT. The only SCRIPTS instruction directly affected by the SIGP bit is Wait for Selection/ Reselection. When this bit is read, the SIGP bit in the ISTAT register is cleared.

Bit 5 SOFF (SCSI offset compare)
This bit operates differently, depending on whether the chip is an initiator or target. If the 53C710 is an initiator, this bit will be set whenever the SCSI synchronous offset counter is equal to zero. If the 53C710 is a target, this bit will be set whenever the SCSI synchronous offset counter is equal to the maximum synchronous offset defined in the SXFER register.

Bit 4 SFP (SCSI FIFO parity)
This bit represents the parity bit of the SCSI synchronous FIFO corresponding to data read out of the FIFO. Reading the CTEST3 register unloads a data byte from the bottom of the SCSI synchronous FIFO. When the CTEST3 register is read, the data parity bit is latched into this bit location.

Bit 3 DFP (DMA FIFO parity)
This bit represents the parity bit of the DMA FIFO when the CTEST6 register reads data out of the FIFO. Reading the CTEST6 register unloads one data byte from the bottom of the DMA FIFO. When the CTEST6 register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

Bit 2 TEOP (SCSI true end of process)
This bit indicates the status of the 53C710's internal TEOP signal. The TEOP signal acknowledges the completion of a block move through the SCSI portion of the 53C710. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

Bit 1 DREQ (Data request status)
This bit indicates the status of the 53C710's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

Bit 0 DACK (Data acknowledge status)
This bit indicates the status of the 53C710's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register 17 (14) Chip Test Three (CTEST3)

Read Only

SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-0 SF7-SF0 (SCSI FIFO)

Reading this register unloads the bottom byte of the 8-byte SCSI synchronous FIFO. Reading this register also latches the parity bit for the FIFO into the SCSI FIFO Parity bit in the CTEST2 register. The FIFO Full bits in the SSTAT2 register can be read to determine how many bytes currently reside in the SCSI synchronous FIFO. Reading this register when the SCSI FIFO is empty causes a SCSI Gross Error (FIFO underflow).

Register 18 (1B) Chip Test Four (CTEST4)

Read Only

MUX	ZMOD	SZM	SLBE	SFWR	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bit 7 MUX (Host bus multiplex mode)
When set, the MUX bit puts the 53C710 into host bus MUX mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is tristated), and then tristates the address bus and drives the data bus (if a write). This allows the address and data buses to be tied together. It should be written prior to acquiring bus mastership. The Mux mode bit allows the 53C710 to operate without external hardware on those host buses on which data and addresses share a common 32 bits.

Bit 6 ZMOD (High impedance mode)
Setting this bit causes the 53C710 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the 53C710, this bit must be cleared.

This bit is intended for board-level testing only. Setting this bit during system operation will likely result in a system crash.

Bit 5 SZM (SCSI high-impedance mode)
Setting this bit causes the 53C710 to place certain SCSI outputs in a high-impedance state. The following outputs will be in a high-impedance state: SD(7-0), SDP, BSY/, SEL/, RST/, REQ/, C/D, I/O, MSG/, ACK/, ATN/. The direction control lines (SDIR(7-0), SDIRP, BSYDIR, RSTDIR, and SELDIR) are driven low and will not be in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

Bit 4 SLBE (SCSI loopback enable)
Setting this bit enables loopback mode. Loopback allows

any SCSI signal to be asserted. 53C710 may be an initiator or a target. It also allows the 53C710 to transfer data from the SODL register back into the SIDL register. For a complete description of the tests that can be performed in loopback mode, please refer to the *53C710 Programmer's Guide.*

Bit 3 SFWR (SCSI FIFO write enable)
Setting this bit redirects data from the SODL to the SCSI FIFO. A write to the SODL register loads a byte into the SCSI FIFO. The parity bit loaded into the FIFO will be odd or even parity depending on the status of the Assert SCSI Even Parity bit in the SCNTL1 register. Clearing this bit will disable this feature.

Bits 2-0 FBL2-FBL0 (FIFO byte control)

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24-16)

These bits send the contents of the CTEST6 register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 & FBL0 determine which of four byte lanes can be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set to this value before executing SCSI SCRIPTS).

Register 19 (1A) Chip Test Five (CTEST5)

Read/Write

ADCK 7	BBCK 6	ROFF 5	MASR 4	DDIR 3	EOP 2	DREQ 1	DACK 0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7 ADCK (Clock address incrementer)
Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

Bit 6 BBCK (Clock byte counter)
Setting this bit decrements the byte count contained in the DBC register. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

Bit 5 ROFF (Reset SCSI offset)
Setting this bit resets the current offset pointer in the SCSI synchronous offset counter. This bit is set when a SCSI Gross Error condition occurs. The offset should be reset when a synchronous transfer does not complete successfully. This bit automatically resets itself after clearing the synchronous offset.

Bit 4 MASR (Master control for set or reset pulses)
This bit controls the operation of bits 3-0. When this bit is set, bits 3-0 assert the corresponding signals. When this bit is reset, bits 3-0 deassert the corresponding signals. This bit and bits 3-0 should not be changed in the same write cycle.

Bit 3 DDIR (DMA direction)
Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

Bit 2 EOP (End of process)
Setting this bit either asserts or deasserts the internal EOP control signal depending on the current status of the MASR bit in this register. The internal EOP signal is an output from the DMA portion of the 53C710 to the SCSI portion of the 53C710. Asserting the EOP signal indicates that the last data byte has been transferred between the two portions of the chip. Deasserting the EOP signal indicates that the last data byte has not been transferred between the two portions of the chip. If the MASR bit is configured to assert this signal, this bit automatically clears itself after pulsing the EOP signal.

Bit 1 DREQ (Data request)
Setting this bit either asserts or deasserts the internal DREQ (data request signal) depending on the current status of the MASR bit in this register. Asserting the DREQ signal indicates that the SCSI portion of the 53C710 requests a data transfer with the DMA portion of the chip. Deasserting the DREQ signal indicates that data should not be transferred between the SCSI portion of the 53C710 and the DMA portion. If the MASR bit is configured to assert this signal, this bit automatically clears after asserting the DREQ signal.

Bit 0 DACK (Data acknowledge)
Setting this bit either asserts or deasserts the internal DACK/ data request signal dependent on the current status of the MASR bit in this register. Asserting the DACK/ signal indicates that the DMA portion of the 53C710 acknowledges a data transfer with the SCSI portion of the chip. Deasserting the DACK/ signal indicates that data should not be transferred between the DMA portion of the 53C710 and the SCSI portion. If the MASR bit is configured to assert this signal, this bit automatically clears itself after asserting the DACK/ signal.

Register 1A (19) Chip Test Six (CTEST6)

Read/Write

DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
7	6	5	4	3	2	1	0

Default >>>

0	0	0	0	0	0	0	0

Bits 7-0 DF7-DF0 (DMA FIFO)

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the CTEST2 register.

To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting a SCRIPT.

Register 1B (18) Chip Test Seven (CTEST7)

Read/Write

CDIS 7	SCI 6	SC0 5	Notime 4	DFP 3	EVP 2	TTI 1	DIFF 0

Default >>>

0 0 0 0 0 0 0 0

Bit 7 CDIS (Cache burst disable)
When this bit is set, the 53C710 will not request a cache-line burst. When this bit is clear, the chip will attempt cache-line bursts when two conditions are met. The first condition is that the address must be lined up to a cache line boundary (A3-A0 must be zero). The second condition is that the transfer counter must be at least 32. Cache line burst mode eliminates the need for a full handshake between the bus master and the memory device when transferring data.

Bits 6-5 SC1-SC0 (Snoop control)
The SC0 and SC1 bits control the two Snoop Control pins. The SC1 bit controls the Snoop Control 1 pin all of the time. The SC0 bit controls the Snoop Control 0 pin only when the Snoop Mode bit is not set. Monitoring the SC0 bit gives advance notice of a pending 53C710 bus request. Bus snooping allows for transmission of additional information to other devices on the host bus about the current type of transfer. In Bus Mode 2, the host processor can snoop an alternate master Read/Write transfer, ensuring access to valid data. In other operating modes, these bits and pins provide additional user-defined functionality.

Bit 4 Notime (Selection timeout disable)
Setting this bit disables the 250 ms timer for all modes, including byte to byte.

Bit 3 DFP (DMA FIFO parity)
This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO via programmed I/O. In order to transfer data to or from the DMA FIFO, perform a read or a write to the CTEST6 register. When loading data into the FIFO via programmed I/O, write this bit to the FIFO as the parity bit for each byte loaded. When writing data to the DMA FIFO, set this bit with the status of the parity bit to be written to the FIFO before writing the byte to the FIFO. For the details of performing a diagnostic test of the DMA FIFO, please refer to the 53C710 *Programmer's Guide*.

Bit 2 EVP (Even parity)
Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense.

Setting this bit causes the 53C710 to generate even parity when driving data on the host data bus. The 53C710 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the 53C710 checks parity and sends the data to the SCSI bus. Clearing this bit causes the 53C710 to maintain odd parity throughout the chip.

Bit 1 TTI (Transfer type bit)
The inverted value of this bit is asserted on the TTI pin during bus mastership in Bus Mode 2 only. This bit is not used in Bus Mode 1.

Bit 0 DIFF (Differential mode)
Setting this bit enables the 53C710 to interface with external differential pair transceivers. The SCSI BSY/, SEL/, and RST/ are input only in differential mode. For more information on differences between the two modes, refer to the pin descriptions for these signals. Resetting this bit enables single-ended mode. This bit should be set in the initialization routine if the differential pair interface is to be used.

Registers 1C-1F (1C-1F) Temporary Stack (TEMP)

Read/Write

Default >>> all zeros

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction. The address pointer stored in this register is loaded into the DSP register. This address points to the next instruction to be executed. Do not write to TEMP while the 53C710 is executing SCSI SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are destroyed. If the TEMP value is needed for a subsequent SCSI SCRIPT, save and then later restore it.

Register 20 (23) DMA FIFO (DFIFO)

Read/Write

RES	B06	BO5	BO4	BO3	BO2	BO1	BO0
7	6	5	4	3	2	1	0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7 RES (Reserved)

Bits 6-0 BO6-BO0 (Byte offset counter)
These six bits indicate the amount of data transferred between the SCSI core and the DMA core. They may be used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

The following steps will determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

1) Subtract the seven least-significant bits of the DBC register from the 7-bit value of the DFIFO register
2) AND the result with 7Fh for a byte count between zero and 64.

Register 21 (22) Interrupt Status (ISTAT)

Read/Write

ABRT 7	RST 6	SIGP 5	RES 4	CON 3	RES 2	SIP 1	DIP 0

Default >>>

0 0 0 0 0 0 0 0

This is the only register that can be accessed by the host CPU while the 53C710 is executing SCRIPTS without interfering in the operation of the 53C710. It may be used to poll for interrupts if interrupts are masked. When either the SIP or DIP bit is set, the DSTAT and SSTAT0 latches will close and subsequent interrupts will be stacked (held in a pending register "behind" the status register). When the current interrupt is cleared by reading the appropriate status register, the stacked interrupts will be transferred to the status register and cause another interrupt.

When an interrupting event occurs, the 53C710 will halt in an orderly fashion before asserting IRQ. If in the middle of an instruction fetch, the fetch will be completed (except in the case of a Bus Fault or Watchdog Timeout), though execution will not begin. If possible, DMA write operations will empty the FIFO before halting. All other DMA operations will finish only the current cycle (or burst if a cache line) before halting. SCSI handshakes that have begun will be completed before halting. The 53C710 will attempt to clean up any outstanding synchronous offset. In the case of Transfer Control Instructions, once execution begins it will continue to completion before halting. If the instruction is a JUMP/CALL WHEN, the wait will abort and the DSP will be updated to the transfer address before halting. All other instructions may halt before completing execution.

Bit 7 ABRT (Abort operation)

Setting this bit aborts the current operation being executed by the 53C710. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1) Set this bit.
2) Wait for an interrupt.
3) Read the ISTAT register.
4) If the SCSI Interrupt Pending bit is set, read the SSTAT0 register to determine the cause of the SCSI Interrupt and go back to step 2.
5) If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, write 00h value to this register.
6) Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Bit 6 RST (Software reset)

Setting this bit resets the 53C710. All registers except the DCNTL EA bit are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This bit is not self-clearing; it must be cleared to remove the reset condition (a hardware reset will also clear this bit). This reset will not clear the Enable Acknowledge (EA) or Function Control One (FC1) bits.

Bit 5 SIGP (Signal process)

SIGP is a Read/Write bit that can be written at any time, and polled and reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPT.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that opcode to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the Wait for Selection/Reselection condition. **Note:** If the SIGP bit is active when a selection/reselection occurs, the auto-switching from/to target mode will be disabled and must be manually set by either the host or a SCRIPT.

Bit 4 RES (Reserved)

Bit 3 CON (Connected)
This bit is automatically set any time the 53C710 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C710 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low-level mode. When this bit is clear, the 53C710 is not connected to the SCSI bus.

Bit 2 RES (Reserved)

Bit 1 SIP (SCSI interrupt pending)
This status bit is set when an interrupt condition is detected in the SCSI portion of the 53C710. The following conditions will cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)
- An arbitration sequence is completed
- A selection or reselection timeout occurs
- The 53C710 was selected or reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected

To determine exactly which condition(s) caused the interrupt, read the SSTAT0 register.

Bit 0 DIP (DMA interrupt pending)
This status bit is set when an interrupt condition is detected in the DMA portion of the 53C710. The following conditions will cause a DMA interrupt to occur:

- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- The Watchdog Timer decrements to zero
- An illegal instruction is detected

To determine exactly which condition(s) caused the interrupt, read the DSTAT register.

Register 22 (21) Chip Test Eight (CTEST8)

Read/Write

V3	V2	V1	V0	FLF	CLF	FM	SM
7	6	5	4	3	2	1	0

Default >>>

V	V	V	V	0	0	0	0

Bits 7-4 V3-V0 (Chip revision level)
These bits identify the chip revision level for software purposes. This data manual applies to devices with revision level 1.

Bit 3 FLF (Flush DMA FIFO)
When this bit is set, data residing in the DMA FIFO is transferred to memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the 53C710 has successfully transferred the data, this bit should be reset. ***Note:*** ***All chip registers may be read during flush operations.***

Bit 2 CLF (Clear DMA and SCSI FIFOs)
When this bit is set, all data pointers for the SCSI and DMA FIFOs are cleared. In addition to the SCSI and DMA FIFO pointers, the SIDL, SODL, and SODR full bits in the SSTAT1 register are cleared. Any data in either of the FIFOs is lost. This bit automatically resets after the 53C710 has successfully cleared the appropriate FIFO pointers and registers.

Bit 1 FM (Fetch pin mode)
When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the opcode portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM, reducing the long delay associated with arbitrating for the host bus in order to fetch SCRIPTS instructions from system memory.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

Bit 0 SM (Snoop pins mode)
When set, the two snoop pins change functions and become pure outputs that are always driven, except when in ZMODE.

Pin	Function
SC0	Becomes a copy of the internal bus request signal. Signal will assert prior to BR/ and will be negated during the AS/ (Asynchronous, or TS/, Synchronous) of the last bus cycle.
SC1	Drives the value in the SC1 register bit.

When clear, the snoop pins are driven during host bus ownership with the values of the CTEST7 SC(1-0) bits.

Register 23 (20) Longitudinal Parity (LCRC)

Read/Write

7	6	5	4	3	2	1	0

Default >>>

0 0 0 0 0 0 0 0

Bits 7-0 Longitudinal Parity

This register contains the longitudinal parity for all data crossing from the DMA FIFO to or from the SCSI core. The parity will consist of an exclusive OR of all data bytes.

Writing to this register will clear its contents to 00h regardless of the value written.

Like the SFBR register in the 53C700, this register is used by the SCSI core to hold the SCSI ID value during selection and reselection. The LCRC register should be used instead of the SFBR because the SFBR is used as an accumulator during many SCRIPTS operations, and may be overwritten at any time by a selection or reselection.

Registers 24-26 (25-27) DMA Byte Counter (DBC)

Read/Write

Default >>> all zeros

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the 53C710. The DBC counter is decremented each time that the AS/ signal is pulsed by the 53C710. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if the chip is not operating in a target mode command phase.

The DBC register is also used during table indirect I/O SCRIPTS to hold the offset value.

Register 27 (24) DMA Command (DCMD)

Read/Write

7	6	5	4	3	2	1	0
Default >>>							
0	0	0	0	0	0	0	0

Bits 7-0 DMA Command

This 8-bit register determines the instruction for the 53C710 to execute. This register has a different function for each instruction. For a complete description, refer to the 53C710 instruction set.

Registers 28-2B (28-2B) DMA Next Data Address (DNAD)

Read/Write

Default >>> all zeros

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions.

To maintain software compatibility with the 53C700, interrupt vectors should be read from the DSPS register.

Registers 2C-2F (2C-2F) DMA SCRIPTS Pointer (DSP)

Read/Write

Default >>> all zeros

To execute SCSI SCRIPTS, the address of the first SCSI SCRIPT must be written to this register. In normal SCRIPTS operation, once the starting address of the SCSI SCRIPTS is written to this register, the SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a SCRIPTS step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPT. When writing this register 8 bits at a time, writing the upper 8 bits , 2F (2C), begins execution of SCSI SCRIPTS.

Registers 30-33 (30-33) DMA Scripts Pointer Save (DSPS)

Read/Write

Default >>> all zeros

This register contains the second longword of Read/Write or Transfer Control SCRIPTS instructions. It is overwritten each time a SCRIPTS instruction is executed. When a SCRIPTS interrupt is fetched, this register holds the interrupt vector.

Registers 34-37 (34-37) Scratch Register (SCRATCH)

Read/Write

Default >>> all zeros

This is a general purpose, user defined scratch pad register. Most SCRIPTS operations will not destroy the contents of this register; only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents.

The SCRATCH register combined with Register-to-Register Move, AND, OR, and ADD operations provides the capability to write a complete SCSI interface program in SCRIPTS.

Register 38 (3B) DMA Mode (DMODE)

Read/Write

BL1	BL0	FC2	FC1	PD	FAM	U0	MAN
7	6	5	4	3	2	1	0

Default >>>

0 0 0 0 0 0 0 0

Bit 7-6 BL1-BL0 (Burst length)

BL1	BL0	Burst Length
0	0	1 - transfer burst
0	1	2 - transfer burst
1	0	4 - transfer burst
1	1	8 - transfer burst

These bits control the number of bus cycles performed per bus ownership. The 53C710 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request is also asserted during start-of-transfer/end-of-transfer cleanup & alignment, even though less than a full burst of transfers may be performed.

To perform cache line bursts, these bits must be set to 4 or 8 transfers and cache bursting must be enabled (CTEST7). Cache bursts are always four longword transfers, regardless of the setting of these bits.

The 53C710 inserts a "fairness delay" of approximately 5 to 8 BCLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

Bit 5-4 FC2-FC1 (Function code)
These bits are user defined. Their values are asserted onto the corresponding device pins during bus mastership. These bits/pins are active in both bus modes.

Bit 3 PD (Program/data)
This bit affects the function of the FC0/ pin. Setting this bit causes the 53C710 to drive the FC0/ signal low when fetching instructions from memory. Clearing this bit causes the 53C710 to drive the FC0/ signal high when fetching instructions from memory.

The FC0/ signal is always driven high when moving data to or from memory and can only be driven low during instruction fetch cycles. This feature can be used to allow SCRIPTS and data to be stored in separate memory banks.

Bit 2 FAM (Fixed address mode)
Setting this bit disables the address pointer (DNAD register) so that it will not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. This bit is used to transfer data to or from a fixed port address. The port width must equal 32 bits.

Bit 1 U0/TT0 (User programmable transfer type)
In both bus modes, UPSO-TT0/ is a general purpose output pin. The value of this bit is asserted onto the UPSO-TT0/ pin while the 53C710 is a bus master, to indicate the type of access for the current bus transfer.

Bit 0 MAN (Manual start mode)
Clearing this bit causes the 53C710 to automatically fetch and execute SCSI SCRIPTS after the DSP register is written. Setting this bit disables the 53C710 from automatically fetching and executing SCSI SCRIPTS after the DSP register is written. When the Start DMA bit in the DCNTL register is cleared, it controls the start time of the operation. Once the Start DMA bit in the DCNTL register is set, the 53C710 automatically fetches and executes each instruction.

Register 39 DMA Interrupt Enable (DIEN)

Read/Write

RES 7	RES 6	BF 5	ABRT 4	SSI 3	SIR 2	WTD 1	IID 0

Default >>>

0 0 0 0 0 0 0 0

Bit 7 RES (Reserved)

Bit 6 RES (Reserved)

Bit 5 BF (Bus fault)

Bit 4 ABRT (Aborted)

Bit 3 SSI (SCRIPT step interrupt)

Bit 2 SIR (SCRIPT interrupt instruction received)

Bit 1 WTD (Watchdog timeout detected)

Bit 0 IID (Illegal instruction detected)

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DSTAT register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the ISTAT DIP from being set; all DMA interrupts are considered fatal. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

A masked non-fatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking does not begin until either the ISTAT SIP or DIP bit is set.

The 53C710 IRQ/output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

Register 3A (39) DMA Watchdog Timer (DWT)

Read/Write

7	6	5	4	3	2	1	0

Default >>>

0 0 0 0 0 0 0 0

Bits 7-6 DMA Watchdog Timer

The DMA watchdog timer register provides a timeout mechanism during data transfers between the 53C710 and memory. This register determines the amount of time that the 53C710 will wait for the assertion of the transfer acknowledge (TA/) signal after starting a bus cycle. Write the timeout value to this register during initialization. Every time that the 53C710 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the timeout feature by writing 00h to this register.

The unit time base for this register is 16* BCLK input period. For example, at 50 MHz the time base for this register is 16 x 20 ns = 320 ns. If a timeout of 50 µs is desired, then this register should be loaded with a value of 9Dh.

The minimum timeout value that should be loaded into this register is 02h; the value 01h will not provide a reliable timeout period.

Register 3B (38) DMA Control Register (DCNTL)

Read/Write

CF1 7	CF0 6	EA 5	SSM 4	LLM 3	STD 2	FA 1	COM 0
Default >>>							
0	0	0	0	0	0	0	0

Bit 7-6 CF1-CF0 (Clock frequency)

CF1	CF0	SCSI Core Clock	SCLK Frequency
1	1	SCLK / 3	50.01 - 66.67MHz
0	0	SCLK / 2	37.51 - 50.00 MHz
0	1	SCLK / 1.5	25.01 - 37.50 MHz
1	0	SCLK / 1	16.67 - 25.00 MHz

These two bits determine the SCLK prescale factor used by the 53C710 SCSI core; the internal SCSI clock is derived from the externally applied SCLK. The above table describes how to program these two bits.

***Note:** It is important that these bits be set to the proper values to guarantee that the 53C710 meets the SCSI timings as defined by the ANSI specification. These bits affect both asynchronous and synchronous timings (unless the synchronous clock is decoupled via the SBCL register).*

Bit 5 EA (Enable ack)
Setting this bit will cause the STERM/-TA pin to become bidirectional. As a result, the 53C710 will generate STERM/-TA/ during slave accesses. When this bit is clear, the 53C710 will monitor STERM/-TA/ to determine the end of a cycle. This bit takes effect during the cycle in which it is set; setting this bit must be the first I/O performed to the 53C710 if this feature is desired. See Chapter 2 for information on bidirectional STERM/-TA/.

Bit 4 SSM (Single-step mode)
Setting this bit causes the 53C710 to stop after executing each SCRIPTS instruction, and generate a SCRIPTS step interrupt. When this bit is clear, the 53C710 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the 53C710 after it generates a SCRIPTS Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

Bit 3 LLM (Enable SCSI low-level mode)
Setting this bit places the 53C710 in low-level mode. In this mode, no DMA operations can occur, and no SCRIPTS instructions can be executed. Arbitration and selection may be performed by setting the Start Sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Bit 2 STD (Start DMA operation)
The 53C710 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the 53C710 is in one of the following modes:

1) *Manual start mode* – Bit 0 in the DMODE register is set
2) *Single-step mode* – Bit 4 in the DCNTL register is set

When the 53C710 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the 53C710 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after each single-step interrupt.

Bit 1 FA (Fast arbitration)
When this bit is set, the 53C710 will immediately become bus master after receiving a bus grant, saving one clock cycle of arbitration time. When this bit is clear, the 53C710 will follow the normal arbitration sequence.

Bit 0 COM (53C700 compatibility)
When this bit is clear, the 53C710 will behave in a manner compatible with the 53C700; selection/reselection IDs will be stored in both the LCRC and SFBR registers, and auto switching is enabled. The default condition of this bit (clear) causes the 53C710 to act the same as the 53C700.

When this bit is set, the ID will be stored only in the LCRC register, protecting the SFBR from being overwritten if a selection/reselection occurs during DMA register-to-register operations. When this bit is set, auto switching is disabled.

Register 3C-3F (3C-3F) Adder Sum Output (ADDER)

Read Only

Default >>> all zeros

This 32-bit register contains the output of the internal adder, and is used primarily for test purposes.

Chapter 5

Instruction Set of the I/O Processor

After power up and initialization of the 53C710, the chip may be operated in one of two modes:

1) Low-level register interface; or

2) SCSI SCRIPTS mode

In the low-level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip may be operated much like an NCR 53C80. An external processor has access to the SCSI bus signals and the low-level DMA signals, to allow creation of complicated board level test algorithms. The low-level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low-level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

To operate in the SCSI SCRIPTS mode, the 53C710 requires only a SCRIPTS start address. All commands are fetched from external memory. The 53C710 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (such as detection of a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the 53C710 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DSP register to restart the automatic fetch and execution of instructions.

The SCSI SCRIPTS mode of execution allows the 53C710 to make decisions based on the status of the SCSI bus. This reduces the need for interrupt servicing by the microprocessor.

Given the rich set of SCSI oriented features included in the command set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Switching to low-level mode for error recovery should never be required.

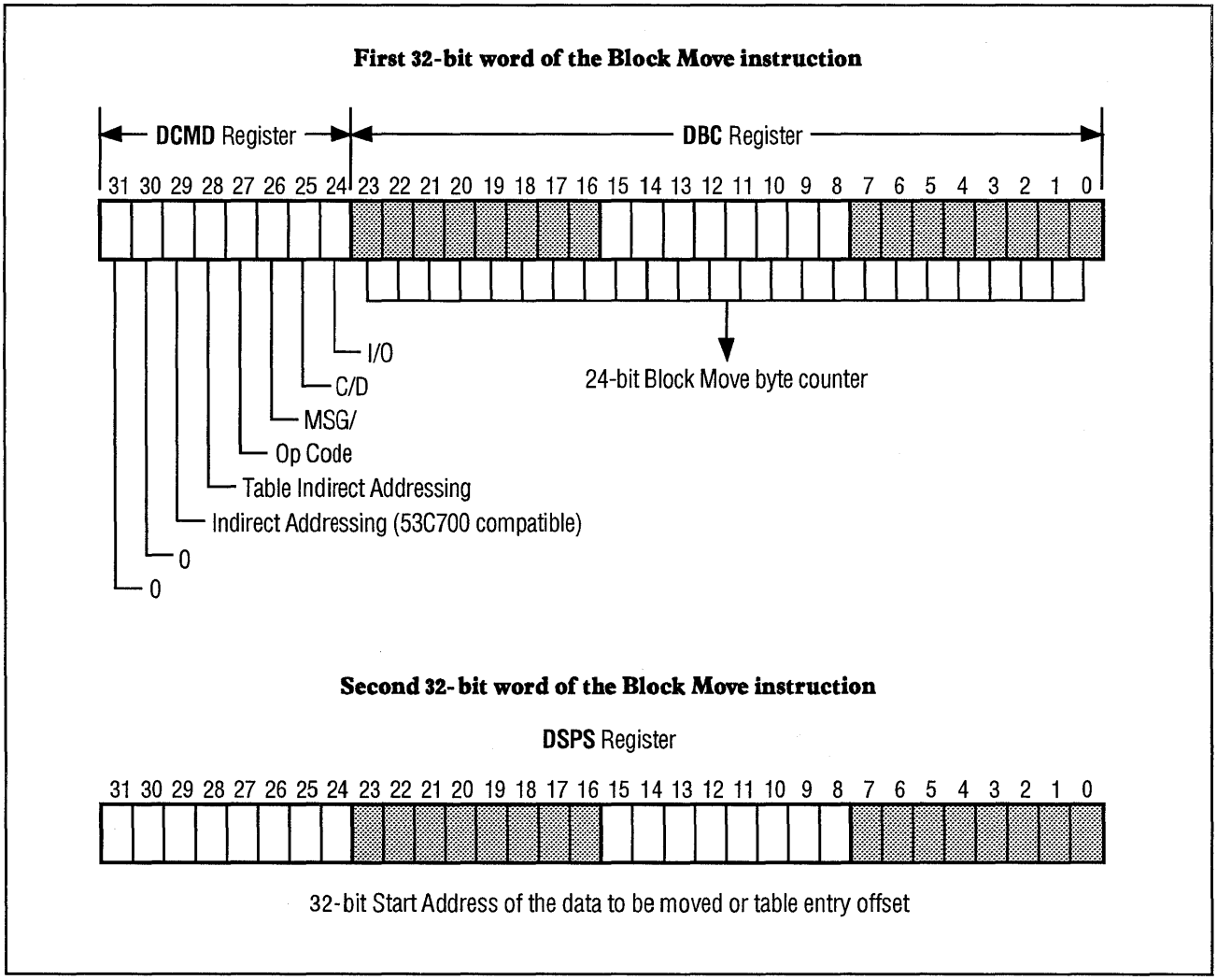
Five types of instructions are implemented in the 53C710:

- Block Move
- I/O or Read/Write
- Transfer Control
- Memory Move

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, only used by Memory Move instructions, is loaded into the TEMP register.

Block Move Instructions

Figure 5-1. Block Move Instruction Register



Bits 31-30 Instruction Type Block Move

Bit 29 Indirect Addressing

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred.

When set, the 32-bit data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third longword fetch (4-byte transfer across the host computer bus).

Direct – The byte count and absolute address are as follows:

Command	Byte Count
Address of Data	

Indirect – Use the byte count and fetch the data address from the address in the command. The byte count is contained in the DBC register and the data address is fetched from the DSPS register.

Command	Byte Count
Address of Data	

Once the data buffer address is loaded, it is executed as if the chip were operating in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the NCR SCSI SCRIPTS compiler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Bit 28 Table Indirect

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA register. Both the transfer count and the source/destination address are fetched from this address.

Table Indirect – Use the signed integer offset, in bits 23-0 of the second 4 bytes of the instruction, to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but ignored.

Command	Not Used
xx	Table Offset

Prior to the start of an I/O, the Data Structure Base Address register (DSA) must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

For a MOVE command, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the 53C710. Execution begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory: the eight bytes of data in the MOVE command must be contiguous, as shown below; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

(00)	Byte Count
	Physical Data Address

Bit 27 Opcode

This 1-bit field defines the instruction to be executed. The Opcode Field bit has different meaning depending on whether the 53C710 is operating in initiator or target mode. Entering a reserved value for the current operating mode will cause an illegal instruction interrupt.

Target Mode

OPC	Instruction Defined
0	MOVE
1	Reserved

1) The 53C710 verifies that it is connected to the SCSI bus as a target before executing this instruction.
2) The 53C710 asserts the SCSI phase signals (MSG/, C/D, & I/O) as defined by the Phase Field bits in the instruction.
3) If the instruction is for the command phase, the 53C710 receives the first command byte and decodes its SCSI Group Code.

   If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the 53C710 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.

   If any other Group Code is received, the DBC register is not modified and the 53C710 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h, an illegal instruction interrupt is generated.
4) The 53C710 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register.
5) If the SCSI ATN/ signal is asserted by the initiator or if a parity error occurs during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SXFER register controls whether an interrupt will be generated.

Initiator Mode

OPC	Instruction Defined
0	Reserved
1	MOVE

1) The 53C710 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.
2) The 53C710 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the 53C710 has not yet transferred data by responding with an ACK/.
3) The 53C710 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT2 register. These phase lines are latched when REQ/ is asserted.
4) If the SCSI phase bits match the value stored in the SSTAT2 register, the 53C710 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register.
5) If the SCSI phase bits do not match the value stored in the SSTAT2 register, the 53C710 generates a phase mismatch interrupt and the command is not executed.

Bits 26-24 SCSI Phase

This 3-bit field defines the desired SCSI information transfer phase. When the 53C710 operates in initiator mode, these bits are compared with the latched SCSI phase bits in the SSTAT2 register. When the 53C710 operates in target mode, the 53C710 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bits 23-0 Transfer Counter

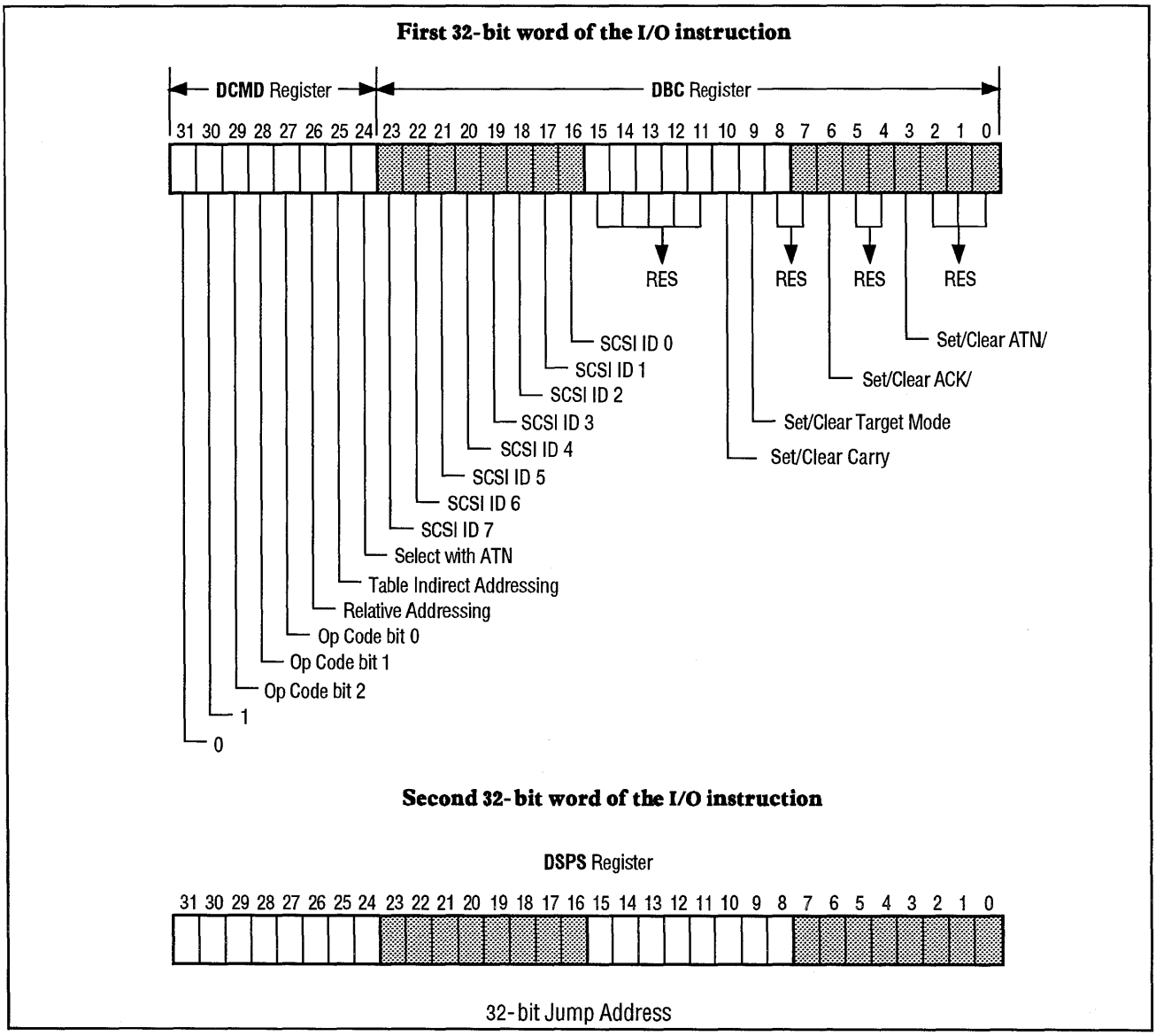
This 24-bit field specifies the number of data bytes to be moved between the 53C710 and system memory. The field is stored in the DBC register. When the 53C710 transfers data to or from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the 53C710 fetches the next instruction.

Bits 31-0 Start Address

This 32-bit field specifies the starting address of the data to be moved to or from memory. This field is copied to the DNAD register. When the 53C710 transfers data to or from memory, the DNAD register is incremented by the number of bytes transferred.

I/O Instructions

Figure 5-2. I/O Instruction Register



Bits 31-30 Instruction Type - I/O Instruction

Bits 29-27 Opcode

The Opcode bits have different meanings, depending on whether the 53C710 is operating in initiator or target mode. Opcode values 101 through 111 are not reserved, but are considered Read/Write instructions rather than I/O, and are discussed in the *Read/Write Instructions* section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1) The 53C710 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C710 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2) If the 53C710 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the 53C710 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register.
3) If the 53C710 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically configures itself to be in the initiator mode if it is reselected, or the target mode if it is selected.

Disconnect Instruction

The 53C710 disconnects from the SCSI bus by deasserting all SCSI signal outputs. The SCSI direction control signals are deasserted, which disables the differential pair output drivers.

Wait Select Instruction

1) If the 53C710 is selected, it fetches the next instruction from the address pointed to by the DSP register.
2) If reselected, the 53C710 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically configures into initiator mode when reselected.
3) If the CPU sets the SIGP bit in the ISTAT register, the 53C710 will abort the WAIT SELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set, the corresponding bit in the ALU is set. ***Note:*** *None of the signals are affected on the SCSI bus in target mode.*

Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ATN/ should not be cleared except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is also cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared. ***Note:*** *None of the signals are affected on the SCSI bus in target mode.*

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1) The 53C710 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C710 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2) If the 53C710 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. It then fetches the next instruction from the address pointed to by the DSP register.
3) If the 53C710 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically configures itself to initiator mode if it is reselected, or to target mode if it is selected.
4) If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

1) The 53C710 waits for the target to perform a "legal" disconnect from the SCSI bus. A "legal" disconnect occurs when BSY/ and SEL/ are inactive for a minimum of one Bus Free Delay (400 ns), after the 53C710 has received a Disconnect Message or a Command Complete Message.

Wait Reselect Instruction

1) If the 53C710 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically configures itself to be in target mode when selected.
2) If the 53C710 is reselected, it fetches the next instruction from the address pointed to by the DSP register.
3) If the CPU sets the SIGP bit in the ISTAT register, the 53C710 will abort the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits in the SOCL register are set. ACK/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set, the corresponding bit in the ALU is set. ***Note:*** *None of the signals are affected on the SCSI bus in target mode.*

Clear Instruction

When the ACK/ or ATN/ bits are set, the corresponding bits are cleared in the SOCL register. ATN/ should not be cleared except for testing purposes. When the target bit is cleared, the corresponding bit in the SCNTL0 register is also cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared. ***Note:*** *None of the signals are affected on the SCSI bus in target mode.*

Bit 26 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DNAD register is used as a relative displacement from the current DSP address.

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Bit 25 Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC register is used as an offset relative to the value in the DSA register. The SCSI ID, synchronous offset and synchronous period are loaded from this address.

Prior to the start of an I/O, the Data Structure Base Address register (DSA) must be loaded with the base address of the I/O data structure. The address may be any longword on a longword boundary.

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory:

1) The I/O data structure must lie within the 8 MB above or below the base address.
2) An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register.

(00)	ID	offset/period	(00)

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	1
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

Direct – Uses the device ID and physical address in the command.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect – Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative – Uses the device ID in the command, but treats the alternate address as a relative jump

Command	ID	Not Used	Not Used
xx	Alternate Jump Offset		

Table Relative – Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits 23-0 of the first four bytes of the SCRIPT to the data structure base address to form the fetch address.

Command	Table Offset
xx	Alternate Jump Offset

Bit 24 Select with ATN/

This bit specifies whether ATN/ will be asserted during the selection phase when the 53C710 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Bits 23-16 SCSI Destination ID

This 8-bit field specifies the destination SCSI ID for an I/O instruction. Only one bit may be set in this field.

Bit 10 Set/Clear Carry

This bit is used in conjunction with a Set or Clear command to set or clear the Carry bit. Setting this bit with a Set command asserts the Carry bit in the ALU. Clearing this bit with a set command deasserts the Carry bit in the ALU.

Bit 9 Set/Clear Target Mode

This bit is used in conjunction with a Set or Clear command to set or clear target mode. Setting this bit with a Set command configures the 53C710 as a target device (this sets bit 0 of the SCNTL0 register). Setting this bit with a Clear command configures the 53C710 as an initiator device (this clears bit 0 of the SCNTL0 register).

Bit 6 Set/Clear ACK/

Bit 3 Set/Clear ATN/

These two bits are used in conjunction with a Set or Clear command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal; bit 3 controls the SCSI ATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the command used. The Set command is used to assert ACK/ and/or ATN/ on the SCSI bus. The Clear command is used to deassert ACK/ and/or ATN/ on the SCSI bus.

Since ACK/ and ATN/ are initiator signals, they will not be asserted on the SCSI bus unless the 53C710 is operating as an initiator or the SCSI Loopback Enable bit is set in the CTEST4 register.

The Set/Clear SCSI ACK/ATN instruction is used after message phase Block Move operations, to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction. After the target has serviced the request for a message-out phase, ATN is deasserted with a Clear SCSI ATN instruction.

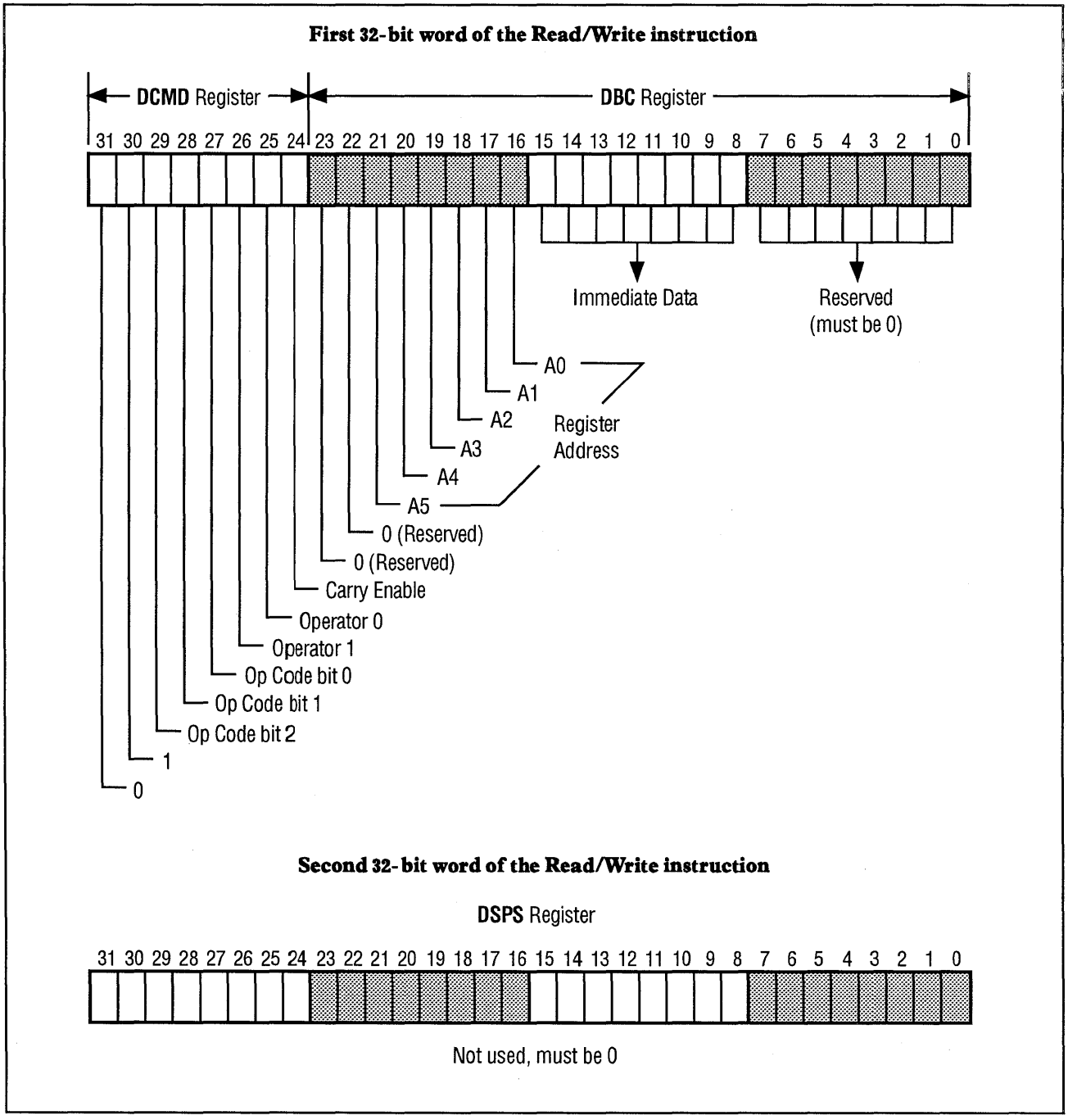
Bits 31-0 Jump Address

This 32-bit field specifies the address of the instruction to fetch when the 53C710 encounters a jump condition. The 53C710 fetches instructions from the address pointed to by this field whenever the 53C710 encounters a SCSI condition that is different from the condition specified in the instruction.

For example, during the execution of a Select instruction in initiator mode, if the 53C710 is reselected, then the next instruction is fetched from the address pointed to by the jump address field. For a complete description of the different jump conditions, refer to the description of each instruction.

Read/Write Instructions

Figure 5-3. Read/Write Instruction Register



Operator	Opcode 111 Read Modify Write	Opcode 110 Move to SFBR	Opcode 101 Move from SFBR
00	Immediate data to destination register	Immediate data to SFBR	Immediate data to destination register
01	Immediate data OR'ed with destination register	Immediate data OR register to SFBR	Immediate data OR'ed with SFBR to destination register
10	Immediate data AND'ed with destination register	Immediate data AND register to SFBR	Immediate data AND'ed with SFBR to destination register
11	Immediate data added to destination register	Immediate data added with register to SFBR	Immediate data added with SFBR to destination register

Bits 31-30 Instruction Type - Read/Write Instruction

Bit 24 Carry Enable

When this bit is set, it will allow the previous carry value to be used by the present Add instruction. The carry value will remain intact unless it is modified by an Add, Set Carry or Clear Carry instruction. All other instructions do not affect Carry. If Carry Enable is not set, no carry will be used during the present Add instruction.

Bits 21-16 Register Address - A(5-0)

Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A(5-0) selects an 8-bit source/destination register within the 53C710. Register addresses are always written using Little Endian byte orientation.

Read-Modify-Write Cycles

In this cycle, the register is read, the selected operation is performed, and the result is written back to the source register.

The add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

Move to / from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this command are:

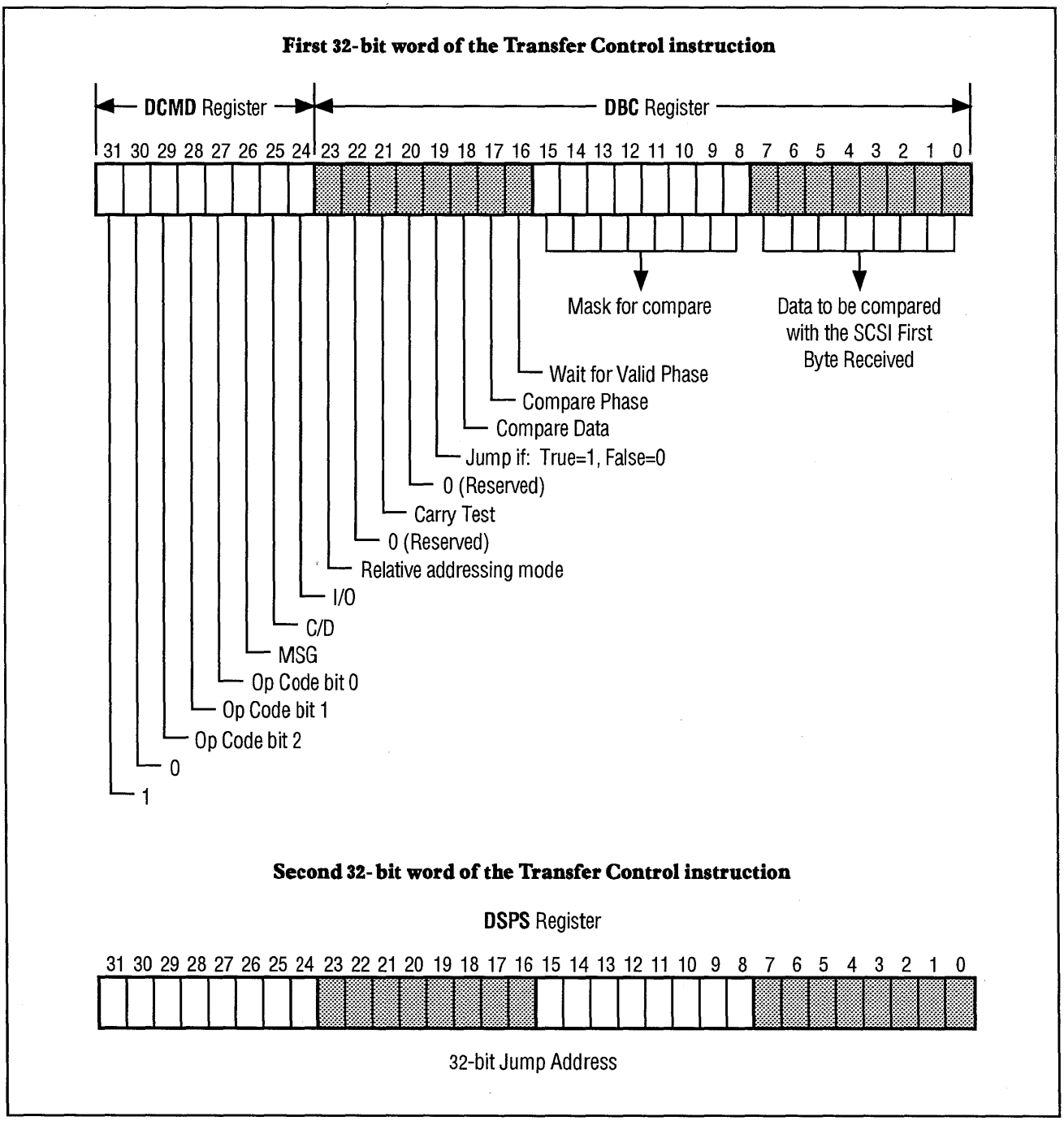
- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SFBR from/to any other register.
- Alter the value of a register with AND/OR/ADD operators.
- After moving values to SFBR, the compare and jump, call, or similar commands may be used to check the value.

A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

The ISTAT register cannot be accessed using the Read/Write Instruction. To move the ISTAT register to the SFBR, use a Memory Move to transfer the ISTAT to SCRATCH1, then perform a SCRATCH1-to-SFBR Move.

Transfer Control Instructions

Figure 5-4. Transfer Control Instruction Register



Bits 31-30 Instruction Type - Transfer Control Instruction

Bits 29-27 Opcode

This three-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be dependent on a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	X	X	Reserved

Jump Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the 53C710 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.
2) If the comparisons are false, the 53C710 fetches the next instruction from the address pointed to by the DSP register, leaving the instruction pointer unchanged.

Call Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the 53C710 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

   When the 53C710 executes a Call instruction, the instruction pointer contained in the DSP register is stored in the TEMP register.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.
2) If the comparisons are false, the 53C710 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

Note: *The Memory Move instruction destroys the return address stored in the TEMP register.*

Return Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C710 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

   When the 53C710 executes a CALL instruction, the current instruction pointer contained in the DSP register is stored in the TEMP register.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register.

   The 53C710 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.
2) If the comparisons are false, then the 53C710 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

Note: *The Memory Move instruction destroys the return address stored in the TEMP register.*

Interrupt Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C710 generates an interrupt by asserting the IRQ/ signal.
2) The 32-bit address field stored in the DSPS register can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.
3) The 53C710 halts and the DSP register must be written to start any further operation.

Bits 26-24 SCSI Phase

This three-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the 53C710 is operating in initiator mode; when the 53C710 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bit 23 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DSPS register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative addressing does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address – Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address – Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
xx	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPT currently being executed by the 53C710. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (twos compliment), the jump can be forward or backward.

A relative transfer can be made to any address within a 16-MB segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

Bits 22-20 Reserved

Bit 21 Carry Test

When this bit is set, decisions based on the ALU Carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Bit 19 Jump If True/False

This bit determines whether the 53C710 should branch when a comparison is true or when a comparison is false. This bit applies to both Phase Compares and Data Compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Bit 18 Compare Data

When this bit is set, then the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Bit 17 Compare Phase

While the 53C710 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ/) are compared to the Phase Field in the Transfer Control instruction; if they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur.

When the 53C710 is operating in target mode this bit, when set, tests for an active SCSI ATN/ signal.

Bit 16 Wait For Valid Phase

If the Wait for Valid Phase bit is set, then the 53C710 waits for a previously unserviced phase before comparing the SCSI phase & data.

If the Wait for Valid Phase bit is clear, then the 53C710 compares the SCSI phase & data immediately.

Bits 15-8 Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored.

For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is on while ignoring the remaining bits.

Bits 7-0 Data Compare Value

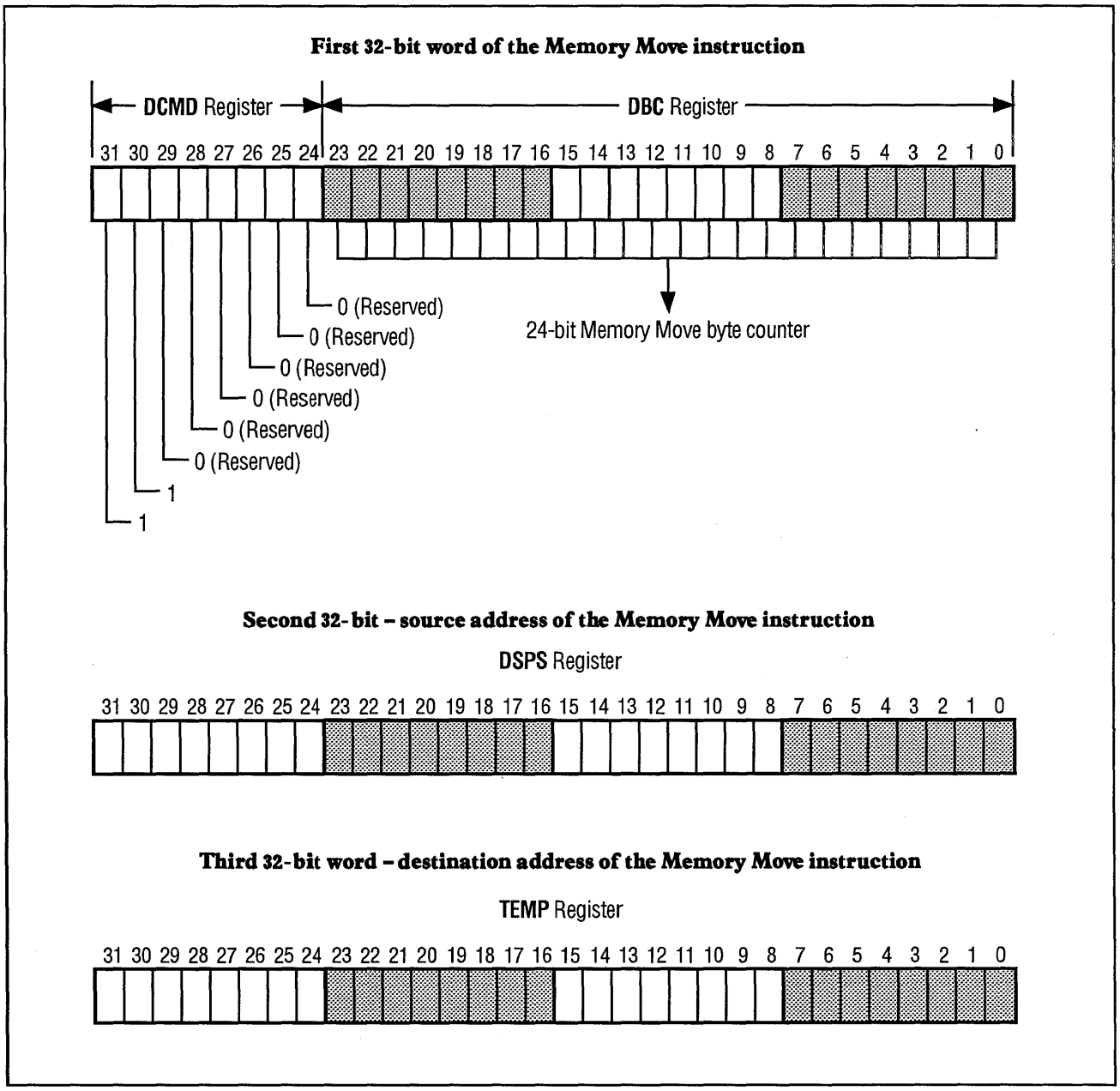
This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

Bits 31-0 Jump Address

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the 53C710 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by four, loaded into the DSP register and becomes the current instruction pointer.

Memory Move Instructions

Figure 5-5. Memory Move Instruction Register



The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the 53C710 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than current DMA controllers. Up to 16 MB may be transferred with one instruction. There are three restrictions:

1) Both the source and destination addresses must start with the same address alignment (A(1-0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur.
2) During execution of this opcode, TEMP and DSA are destroyed. Therefore, if the contents of either register are required for additional SCRIPTS, save them before any Memory Move is executed. Before resuming a SCSI SCRIPT, restore the contents to the appropriate register.
3) Indirect addresses are not allowed.

The Memory-to-Memory Move instruction passes the source and destination addresses and the byte count to the 53C710. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

The DSPS and DSA registers are additional holding registers used during the Memory Move.

Bits 31-30 Instruction Type - Memory Move Instruction

Bits 29-24 Reserved

These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

Bits 23-0 Transfer Count

The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

Read/Write System Memory from a Script

By using the Memory Move instruction, single or multiple register values may be transferred to or from system memory.

Because the Chip Select (CS/) input is derived from an address decode, it could activate during a Memory Move operation if the source/destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower 6 bits of the memory address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate 53C710 register (for example, the SCRATCH register), and then to the SFBR.

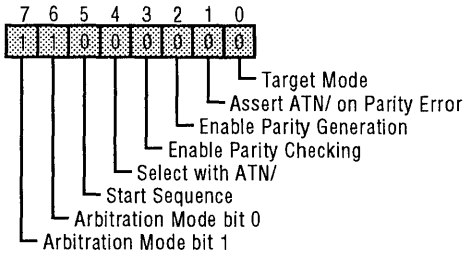
The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

Appendix A

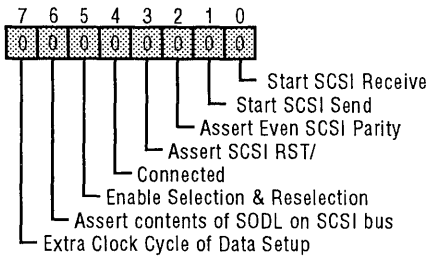
53C710 Register Summary

Default values for each bit are shown in the shaded areas.

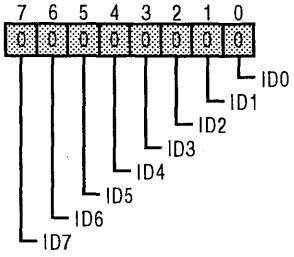
SCNTL0 Register R/W (00h)



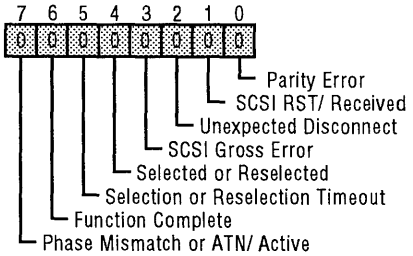
SCNTL1 Register R/W (01h)



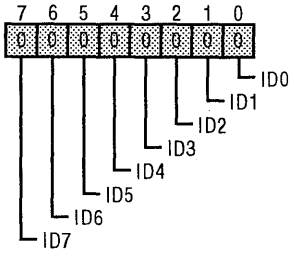
SDID Register R/W (02h)



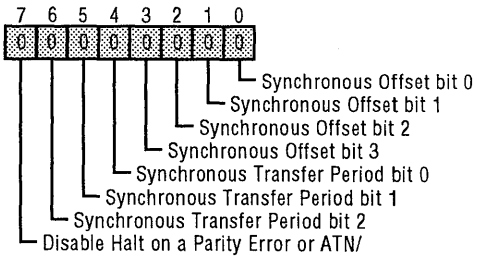
SIEN Register R/W (03h)



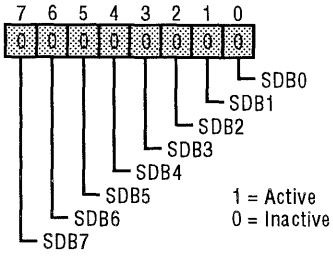
SCID Register R/W (04h)



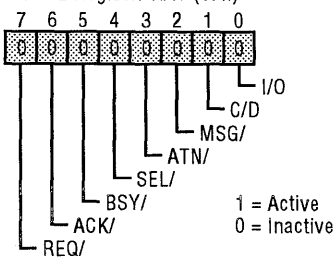
SXFER Register R/W (05h)



SODL Register R/W (06h)

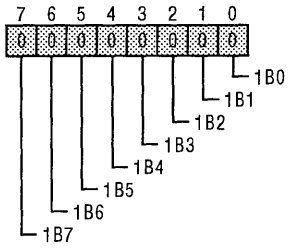


SOCL Register R/W (07h)

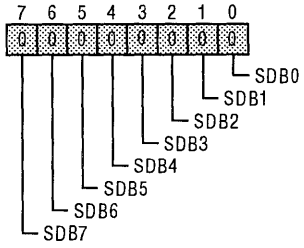


53C710 Register Summary (Continued)

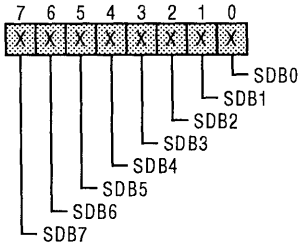
SFBR Register R (08h)



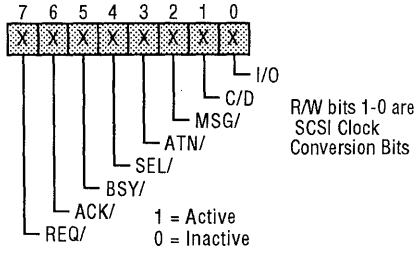
SIDL Register R (09h)



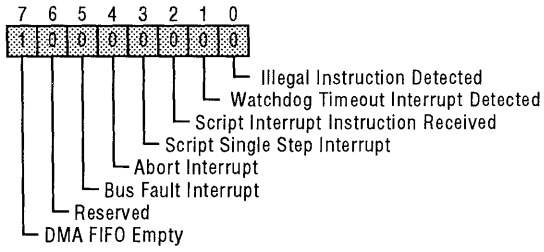
SBDL Register R (0Ah)



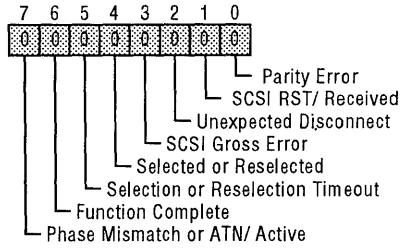
SBCL Register R (0Bh)



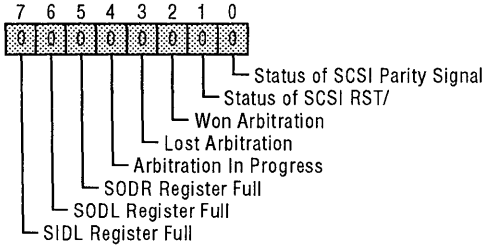
DSTAT Register R (0Ch)



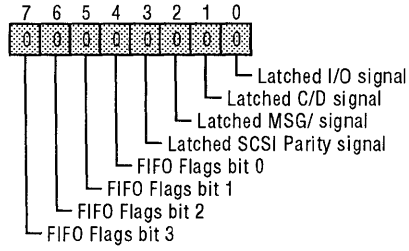
SSTAT0 Register R (0Dh)



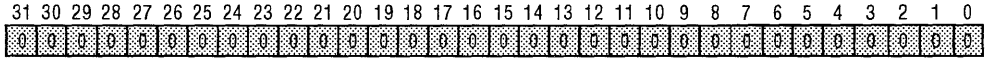
SSTAT1 Register R (0Eh)



SSTAT2 Register R (0Fh)

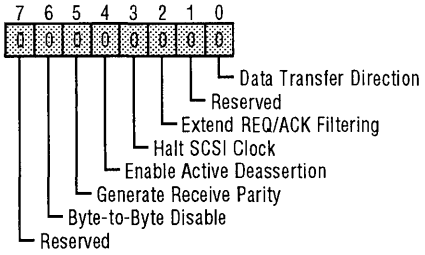


DSA Register (10-13h)

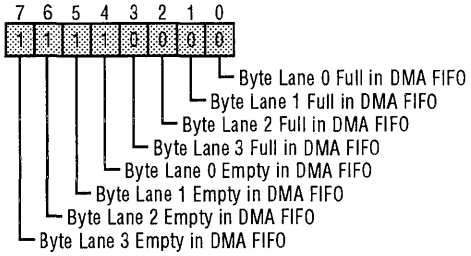


53C710 Register Summary (Continued)

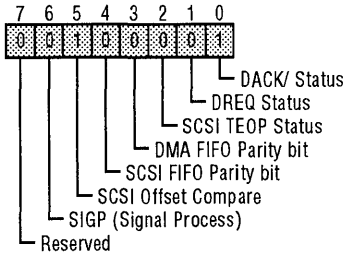
CTEST0 Register R/W (14h)



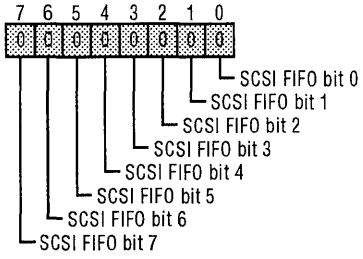
CTEST1 Register R (15h)



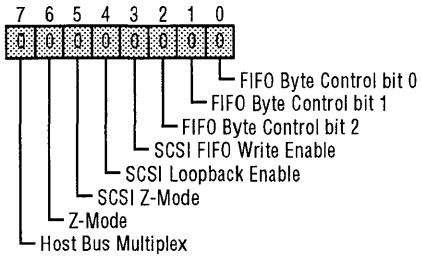
CTEST2 Register R (16h)



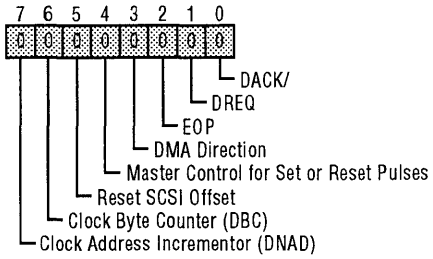
CTEST3 Register R (17h)



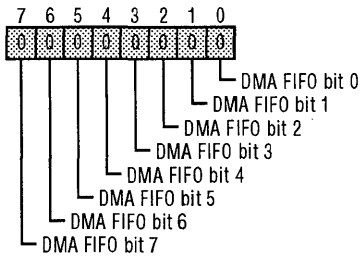
CTEST4 Register R/W (18h)



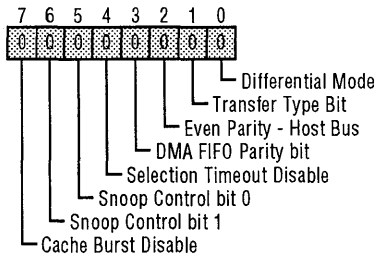
CTEST5 Register R/W (19h)



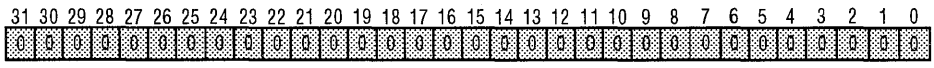
CTEST6 Register R/W (1Ah)



CTEST7 Register R/W (1Bh)

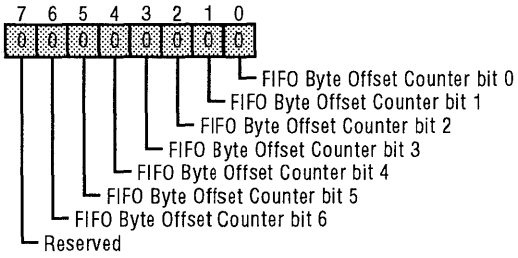


TEMP Register R/W (1C-1Fh)

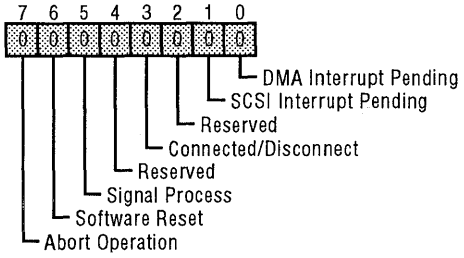


53C710 Register Summary (Continued)

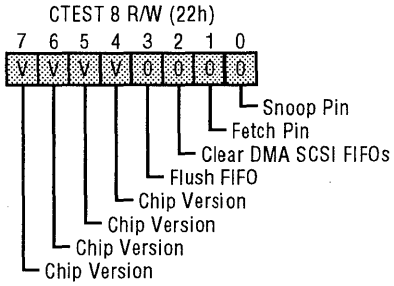
DFIFO Register R/W (20h)



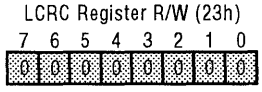
ISTAT Register R/W (21h)



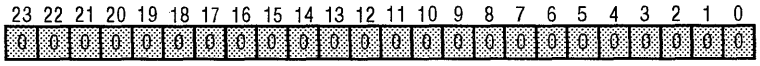
CTEST 8 R/W (22h)



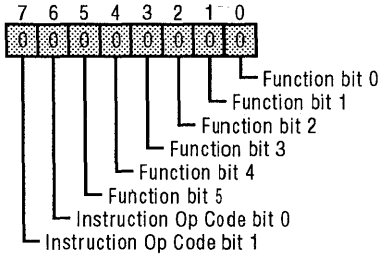
LCRC Register R/W (23h)



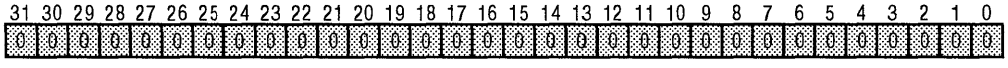
DBC Register R/W (24-26h)



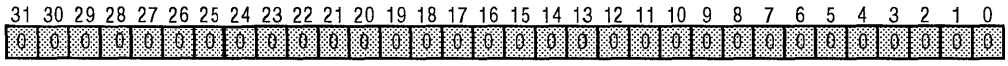
DCMD Register R/W (27h)



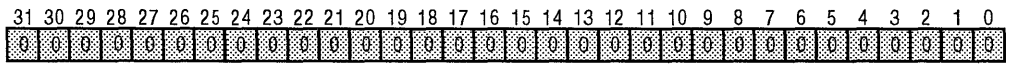
DNAD Register R/W (28-2Bh)



DSP Register R/W (2C-2Fh)

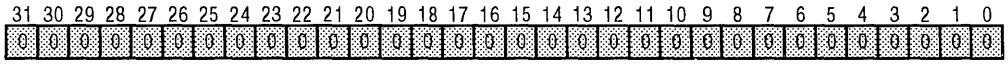


DSPS Register R/W (30-33h)

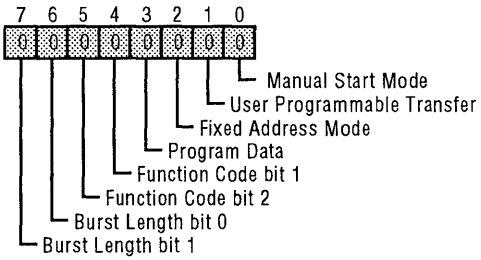


53C710 Register Summary (Continued)

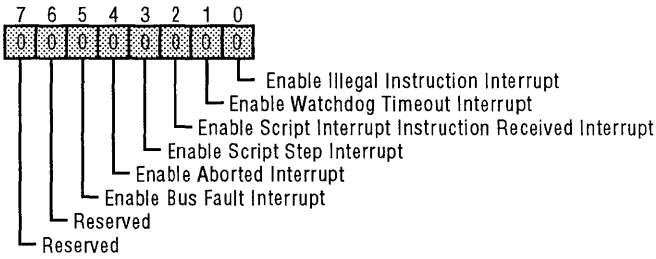
SCRATCH Register R/W (34-37h)



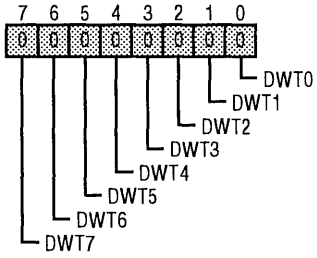
DMODE Register R/W (38h)



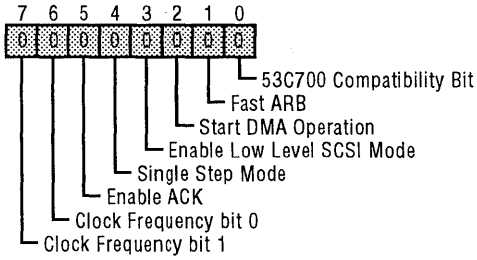
DIEN Register R/W (39h)



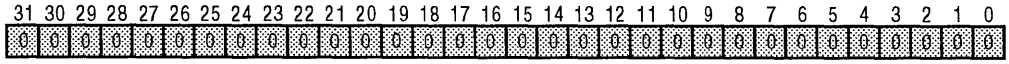
DWT Register R/W (3Ah)



DCNTL Register R/W (3Bh)



ADDER Register R (3C-3Fh)



Appendix B

Bit and Register Differences Between the 53C710 and the 53C700

The 53C710 can execute all 53C700 SCRIPTs without recompilation. However, because there are new registers and bits, and some registers and bits have been relocated or deleted, firmware drivers will need to be modified. The following table summarizes the differences between the 53C700 and 53C710 register sets. The byte addresses are referenced using little Endian byte orientation.

New

Item	53C700	53C710
Synchronous SCSI clock control bits	n/a	SBCL, bits 1-0
Bus fault bit	n/a	DSTAT, bit 5
Data structure address register	n/a	DSA
SIGnal process test & reset bit	n/a	CTEST2, bit 6
MUX mode bit	n/a	CTEST4, bit 7
Cache burst disable bit	n/a	CTEST7, bit 7
Snoop control bits 1-0	n/a	CTEST7, bits 6-5
Transfer type one bit	n/a	CTEST7, bit 1
Byte offset six bit	n/a	DFIFO, bit 6
SIGnal process set bit	n/a	ISTAT, bit 5
CTEST8 register	n/a	CTEST8
FETCH/ pin control bit	n/a	CTEST8, bit 1
Snoop mode bit	n/a	CTEST8, bit 0
LCRC register	n/a	LCRC
Scratch register	n/a	SCRATCH
Function code bits 2-1	n/a	DMODE, bits 5-4
Program/data function code 0 control bit	n/a	DMODE, bit 3
UPSO-TT0/ bit	n/a	DMODE, bit 1
Bus fault interrupt enable bit	n/a	DIEN, bit 5
Enable acknowledge control bit	n/a	DCNTL, bit 5
Fast arbitration mode bit	n/a	DCNTL, bit 1
53C700 compatibility bit	n/a	DCNTL, bit 0
Adder output register	n/a	ADDER

New (Continued)

Item	53C700	53C710
Filter Delay Select bit	n/a	CTEST0, bit 2
Halt SCSI Clock bit	n/a	CTEST0, bit 3
Enable Active Deassertion bit	n/a	CTEST0, bit 4
Generate Receive Parity bit	n/a	CTEST0, bit 5
Byte-to-Byte Disable bit	n/a	CTEST0, bit 6

Deleted

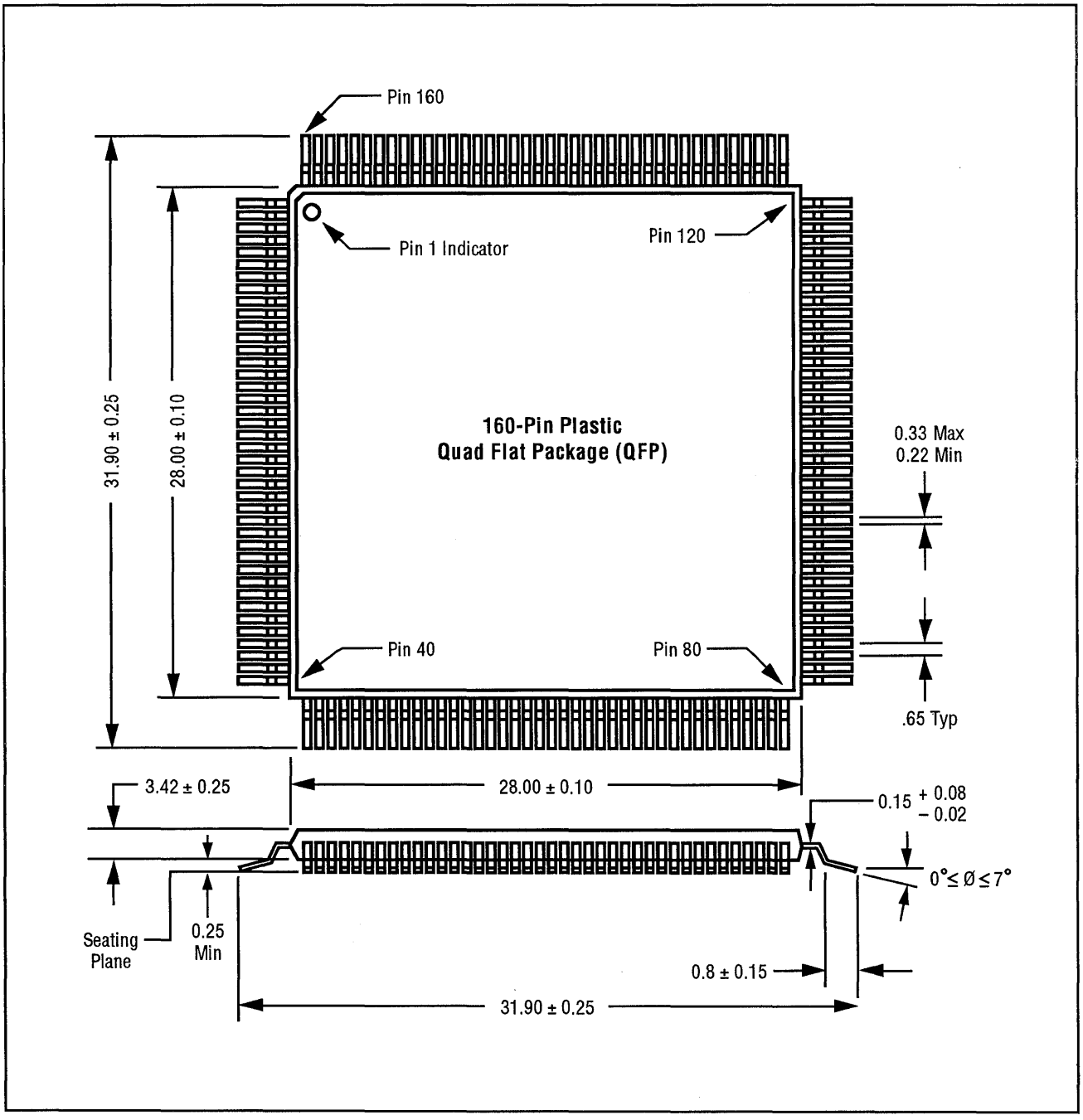
Item	53C700	53C710
DC/ pin control bit	CTEST7, bit 1	n/a
DSPS and DSP empty bit	ISTAT, bit 2	n/a
16-bit DMA, '286-mode bits	DMODE, bits 5-4	n/a
I/O-memory mapped DMA bit	DMODE, bit 3	n/a
Pipeline mode bit	DMODE, bit 1	n/a
16-bit SCSI scripts mode bit	DCNTL, bit 5	n/a
Real target mode bit	CTEST0, bit 1	n/a
Start SCSI Send	SCNTL1, bit 1	n/a
Start SCSI Receive	SCNTL1, bit 0	n/a

Moved

Item	53C700	53C710
Flush FIFO bit	DFIFO, bit 7	CTEST8, bit 3
Clear FIFO bit	DFIFO, bit 6	CTEST8, bit 2
Software reset bit	DCNTL, bit 0	ISTAT, bit 6
Chip revision level bits	CTEST7, bits 7-4	CTEST8, bits 7-4
DMODE register	Address 34h	Address 38h

Appendix C

Mechanical Data



Note: *All dimensions are in millimeters. This package is known as a Metric QFP, and should not be confused with the similiar JEDEC QFP.*

Index

S

T

Index

S

T

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Device Errata Listing 139

NCR 53C710-1
NCR Part Number: 609-3400563

List of Items Included In This Errata:

ITEM 1: Fixed Address Mode
ITEM 2: Byte to Byte Timer
ITEM 3: Bus Retry with BOFF/
ITEM 4: Snooping Using SC0
ITEM 5: Read/Write followed by ISTAT register read

Item 1: Fixed Address Mode

CONDITION:

A SCSI interrupt is generated during a block move instruction when receiving data and fixed address mode is enabled.

DESCRIPTION:

The 53C710-1 is receiving SCSI data and transferring it to memory. A SCSI interrupting condition occurs and there is data remaining in the FIFO. At this point, the 53C710-1 will automatically begin to flush the remaining bytes. Under certain conditions, described below, the chip will continually attempt to empty the DMA FIFO and not assert the IRQ/ pin. The chip acts in this way because the fixed address mode function does not allow the internal address pointer to increment, thereby making the bytes in byte lanes 1 and 2 inaccessible.

When flushing after an interrupting condition, the chip will continue to transfer the remaining bytes until there are less than 4 bytes in the FIFO. At this point the chip goes into byte mode operation and attempts to flush the remaining 1, 2, or 3 bytes. Because the address pointer can not increment beyond byte lane 0, bytes remaining in byte lanes 1 and 2 cannot be transferred. The chip will continue to attempt to flush these bytes unsuccessfully, and no interrupting condition will occur. If the remaining bytes in the FIFO are in byte lanes 0 or 3, the transfer will complete properly and the interrupt will be generated.

WORK-AROUND:

No work around is available. The fixed address mode function should not be enabled. A SCSI interrupting condition may occur at any time which may cause

a hang condition. This function will be de-featured in future printings of the NCR 53C710-1 Data Manual and the Programmers Guide.

Item 2: Byte to Byte Timer

CONDITIONS:

When using the Byte to Byte Timer for other than catastrophic bus failures, time-outs could occur within every 1 ms.

DESCRIPTION:

The 53C710-1 has experienced an unrecoverable failure. If a SCSI Reset is executed following the time out, the chip will continue to operate correctly. However, if a SCSI Reset is not executed after the failure, the timer will time-out again as early as 1 ms later.

WORK-AROUND:

The byte to byte Timer should only be used to time-out unrecoverable bus failures. When the time-out occurs, it must be followed by a SCSI Reset.

Item 3: Bus Retry with BOFF/

CONDITIONS:

Simultaneous assertion of Bus Retry and BOFF signals.

DESCRIPTION:

A Bus Retry condition occurs as the host is asserting BOFF/. (If running in 030 Mode, BERR/, TA/, and HALT/ are asserted at the same time as BOFF/. In 040 Mode, TEA/, and TA/ are asserted at the same time as BOFF/.) The chip relinquishes bus ownership at the end of the current cycle, and immediately rearbitrates for the bus, attempting a Bus Retry while BOFF/ is still asserted.

WORK-AROUND:

A Backoff_Retry condition can be successfully generated by externally gating bus while BOFF/ is asserted, thereby generating a Backoff_Retry condition.

NOTE: A Bus Retry will work correctly when the associated signals are asserted alone, not with the BOFF/. Alternately, the BOFF/ will work correctly if not asserted when a Bus Retry condition occurs.

Item 4: Snooping Using SC0

CONDITIONS:

Setting Snoop Mode, Bit 0, in CTEST8 to use the SC0 for an early bus request.

DESCRIPTION:

In high-latency systems where more than two bursts of data may be available in the NCR 53C710-1 chip, SC0 may or may not be deasserted between the first and second burst of data.

The SCO pin is not affected by the fairness timer and may therefore not go off between bursts; BR/ will always go off between bursts.

While a data transfer is occuring the SC0 pin is stable. Between transfers, while data is falling through the DMA fall-through FIFO, the SC0 is a live decode of the FIFO full flags and will not be a stable signal.

WORK-AROUND:

There is no work-around for this problem. NCR recommends that SC0 not be used to generate an early bus request.

Item 5: Read/Write followed by ISTAT register read

CONDITIONS:

The 53C710-1 executes a read/write instruction (MOVE {register | data8 | register operator data8} to register [WITH CARRY]) in SCRIPTS while the CPU is polling the ISTAT register.

DESCRIPTION:

When the 53C710-1 SCRIPTS processor is executing a read/write command and the CPU reads the ISTAT register during the write portion of the SCRIPTS command, the parity may be corrupted. Since there is no parity in the internal registers, the parity is disabled during the read/write command. The parity bit will be pulled high.

WORK-AROUND:

One possible work-around for this is not to check parity when reading the ISTAT register.

Another possible work-around is to not poll the ISTAT register. Use the IRQ pin to determine when an interrupt has occurred. Once the interrupt has occurred, the ISTAT register can be read without any parity corruption because at this time the SCRIPTS are not running.