45CF8 FINITE IMPULSE RESPONSE FILTER

Introduction

The NCR45CF8 Finite Impulse Response Filter is a directly cascadable device which is designed for the implementation of video speed FIR filters with either linear or non-linear phase characteristics. Each chip contains four 9×8 parallel multipliers, along with adders and delays to implement a four-stage general FIR filter.

A unique architecture allows the NCR45CF8 to be cascaded to any number of stages in either the linear or nonlinear phase modes. For example, a 24-tap filter requires only three NCR45CF8 devices.

Multiple coefficients of each chip can be changed during each clock cycle. Two's complement or unsigned magnitude format is selected independently for each coefficient and each data input. Input data is nine bits and the coefficients are eight bits, with multiplication results rounded to 14 bits. The output is summed to 18 bits.

Two versions of the NCR45CF8 have been designed to allow implementation of FIR digital filters with both even and odd numbers of taps. In the linear phase mode, port B is connected to port C, which wraps around the partial sums. The NCR45CF8E (even) repeats the center coefficient while the NCR45CF8O (odd) does not repeat the center coefficient.

General Description

The NCR45CF8 is a directly cascadable finite impulse response (FIR) filter chip designed for the implementation of video speed FIR filters with either linear or non-linear phase characteristics. Each chip contains four 9×8 parallel multipliers, along with adders and delays, to implement either a four stage general FIR filter (with non-symmetric coefficients) or an eight stage linear phase FIR filter (with symmetric coefficients). A unique architecture allows the NCR45CF8 to be cascaded to any number of stages in either the linear or nonlinear phase modes. For example, a 24-tap linear phase FIR filter requirs only three NCR45CF8 devices.

For maximum versatility, one coefficient of each chip can be changed during each clock cycle. Two's complement or unsigned magnitude format is selected independently for each coefficient and each data input. Data inputs are nine bits and coefficients are eight bits. Multiplication results are rounded to fourteen bits and the output is summed to eighteen bits.

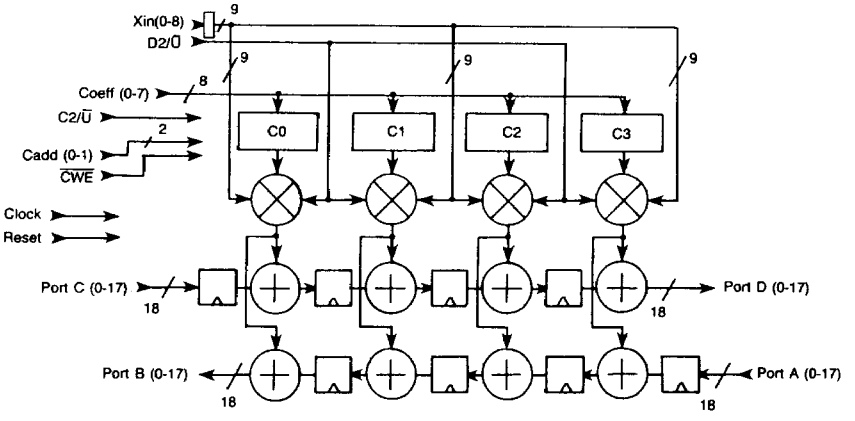
Features

- Directly cascadable with no external components
- 14.5 Mhz throughput rate
- Linear or non-linear phase operation
- 4 stages per chip in non-linear phase mode
- 8 stages per chip in linear phase mode
- TTL compatible
- Low power CMOS

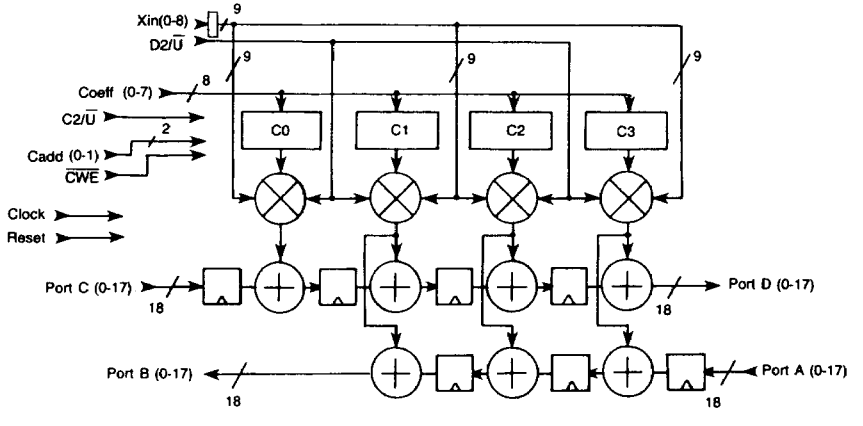
Applications

- Digital Video Filters
- 2-D Filtering
- Multi-bit Correlation
- Adaptive Filters

NCR45CF8E Block Diagram

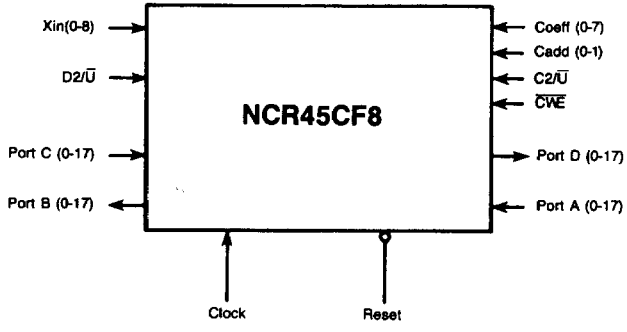


NCR45CF8O Block Diagram



Two versions of the NCR45CF8 are available. This is to allow linear phase digital filters with either an even or an odd number of taps to be implemented. In the linear phase mode, port B is connected to port C to wrap around the partial sums. The NCR45CF8E (even) repeats the center coefficient while the NCR45CF8O (odd) does not repeat the center coefficient.

Logic Diagram



PIN NAME	FUNCTION
Data	Data Input
D2/U	Data Format Select
Coeff	Coefficient Input
Cadd	Coefficient Tap Address
C2/U	Coefficient Format Select
CWE	Coefficient Write Enable
Port A, C	Input Ports
Port B, D	Output Ports

NOTE: BIT 0 of the Input Ports, Output Ports, Data Input Bus and Coefficient Input Bus is the Least Significant bit.

The individual coefficients and data values can be input to the NCR45CF8 in either unsigned magnitude or two's complement format. For coefficient input, the C2/$\overline{U}$ input is held high for two's complement and low for unsigned magnitude format. For data value input, the D2/$\overline{U}$ input is held high for two's complement and low for unsigned magnitude format. These control lines may be changed independently for every clock cycle as a data value or a coefficient is input. Coefficients are updated by placing the new value on the coefficient input lines with the appropriate tap address on the Cadd lines and taking the $\overline{CWE}$ line low. One coefficient may be updated during each cycle. Coefficient storage is fully static, so the coefficients can be loaded once and will remain stable as long as the power is on. A reset line is provided to insure complete device initialization in a known state. When the reset line is pulled low, all internal registers, including data and coefficient registers, are initialized to zero. This assures proper filter output during the first few cycles of operation when data has not yet propagated the full length of the filter. A four cycle latency exists from data input to sum output due to internal pipelining.

The canonical FIR filter structure shown in figure 1a is equivalent to the structure of figure 1b. The second structure has the advantage of regularity and is easily cascaded. When used with non-symmetric coefficients, two NCR45CF8 chips will implement the structure shown in figure 1b. Four taps, or stages, of such a filter are implemented in each chip. In many instances, a linear phase FIR filter is desired. Linear phase is achieved by using coefficients which are symmetric about the center tap, or taps, of the filter. Figure 2 shows a linear phase filter.

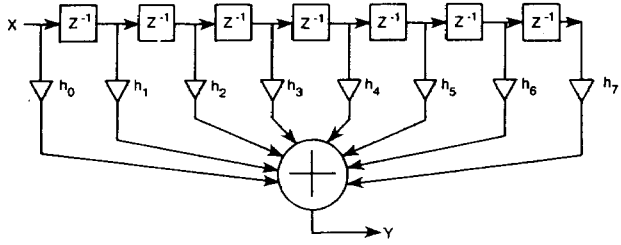


Figure 1a. Direct form (canonical) FIR filter structure.

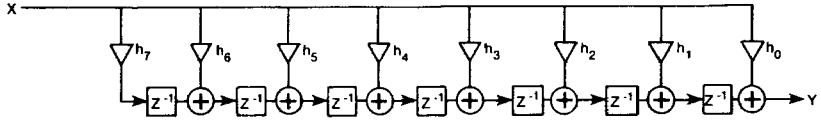


Figure 1b. Equivalent FIR filter structure.

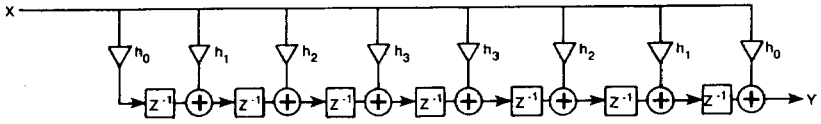


Figure 2. Linear phase FIR filter.

A significant savings in hardware can be realized by sharing the multipliers with the same coefficients. This reduces the number of multipliers required for a length-N filter from N to N/2. A structure that takes advantage of the symmetric coefficient characteristic of the linear phase mode, while maintaining cascadeability, is shown in figure 3.

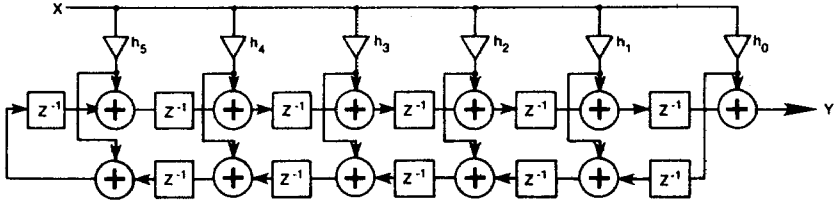


Figure 3. Linear phase FIR architecture using N/2 multipliers.

The NCR45CF8 device can be used as a four stage or tap, section of a FIR filter with arbitrary coefficients, such as previously shown in figure 1b. It can also be used to implement eight stages, or taps, of a linear phase FIR filter by externally connecting port B to port C. Multiple NCR45CF8 devices can be cascaded in either the linear or non-linear phase mode to create longer filters. This is shown in figure 4. Any number of NCR45CF8 devices can be cascaded electrically, but caution must be exercised to scale the coefficients so that overflow does not occur in the adder strings.

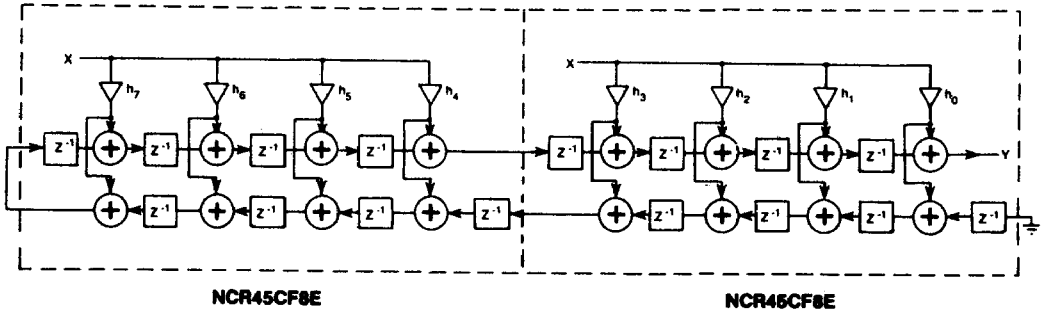


Figure 4. Cascading two NCR45CF8 chips to form a length-16 linear phase FIR filter.

System requirements can dictate a filter design to have either an odd or an even number of taps. For an odd tap filter with non-symmetric coefficients, the NCR45CF8E can be used with the coefficient of the first (leftmost) tap of the first (leftmost) chip set to zero. This neutralizes the effect of that tap since it will produce a zero product that will have no impact on the overall filter output. Doing this effectively cuts one tap off the filter, resulting in a filter with an odd number of taps.

Odd tap FIR filters with symmetric coefficients are implemented with a unique (non-repeated) center coefficient. This structure is shown in figure 5. The NCR45CF8E (even) is used for even tap filters and for cascaded sections of odd tap filters, while the NCR45CF8O (odd) is used for the leftmost device in an odd tap linear phase filter. Figure 6 shows both devices cascaded to form a 15-tap linear phase FIR filter. Note that the leftmost device must be the odd tap version since the center coefficient is not repeated in this filter.

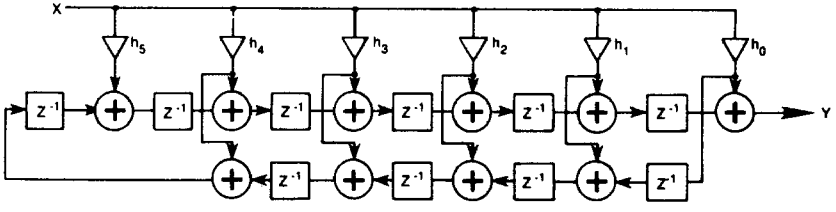


Figure 5. Odd tap linear phase FIR structure.

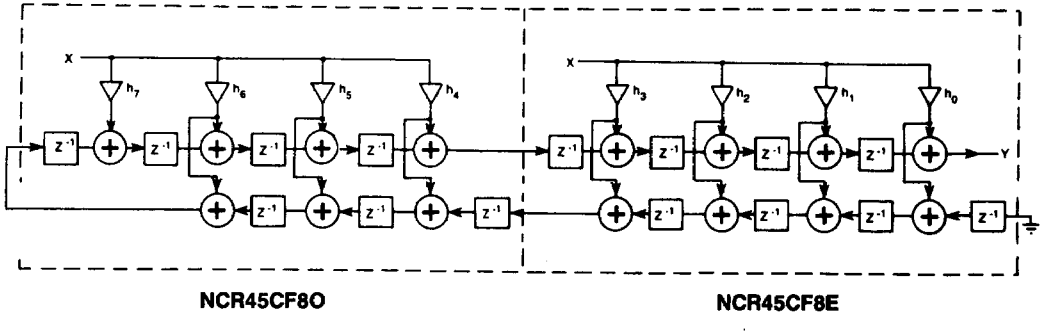


Figure 6. Cascading two NCR45CF8 chips to form a length-15 linear phase FIR filter.

Interleaving for Higher Speed Operation

By interleaving two (or more) filters the effective data rate can be doubled. The 8-tap FIR filter of figure 7 is limited to 14.5 Mhz operation. The same filter, implemented in four sections using twice the hardware, is shown in figure 8. The proper addition of the output of the four sections will cause a filter with 29 Mhz throughput to result. Figure 9 shows the interleave operation. Essentially, this scheme doubles the filter throughput by distributing computation between two sets of hardware.

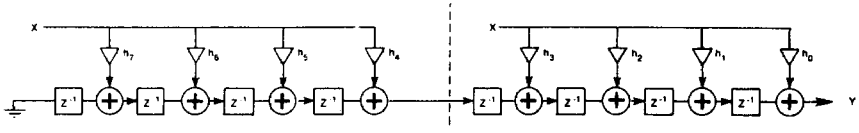


Figure 7. Eight tap filter using two NCR45CF8 devices (non-linear phase mode 14.5 MHz data rate).

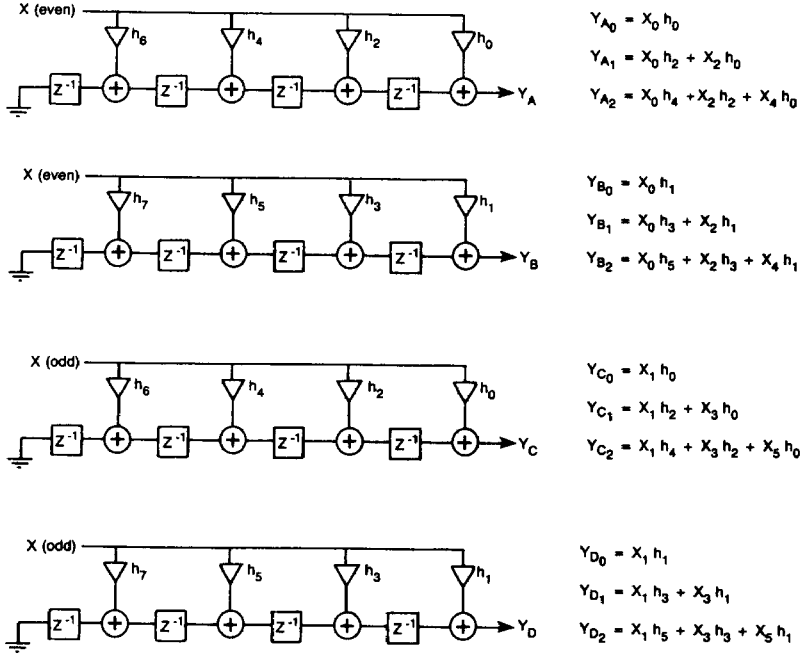


Figure 8. Four section equivalent FIR filter showing distribution of data and coefficients (14.5 MHz operation within sections).

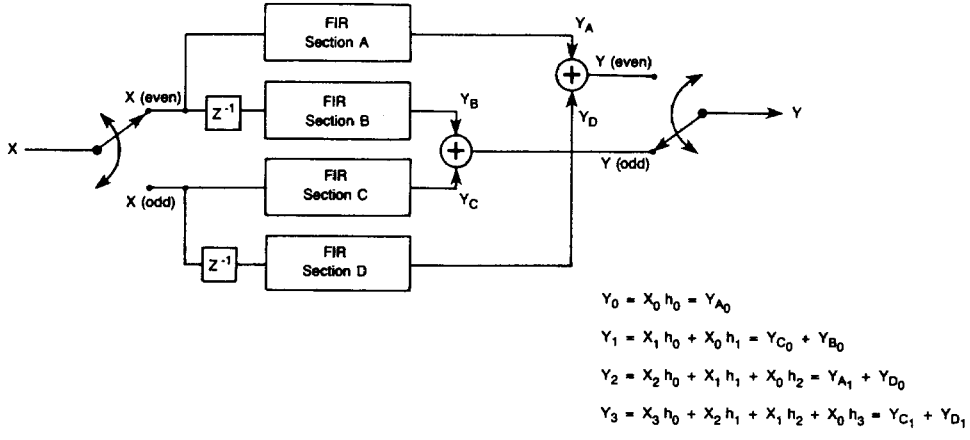


Figure 9. 29 MHz throughput interleaved FIR filter (14.5 MHz components).

Another application of the double throughput system is for interpolating FIR filters. A filter like the one shown in figure 10, where every other coefficient is zero, is often desired. By distributing the computation between two NCR45CF8 filter sections, a 29 Mhz interpolating FIR filter can be constructed. Figure 11 shows such a system.

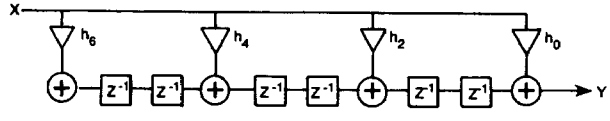


Figure 10. Interpolating FIR filter.

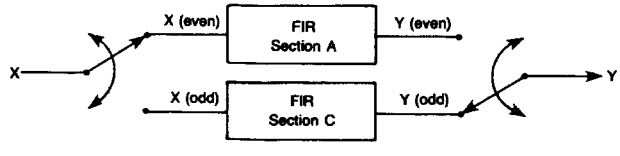
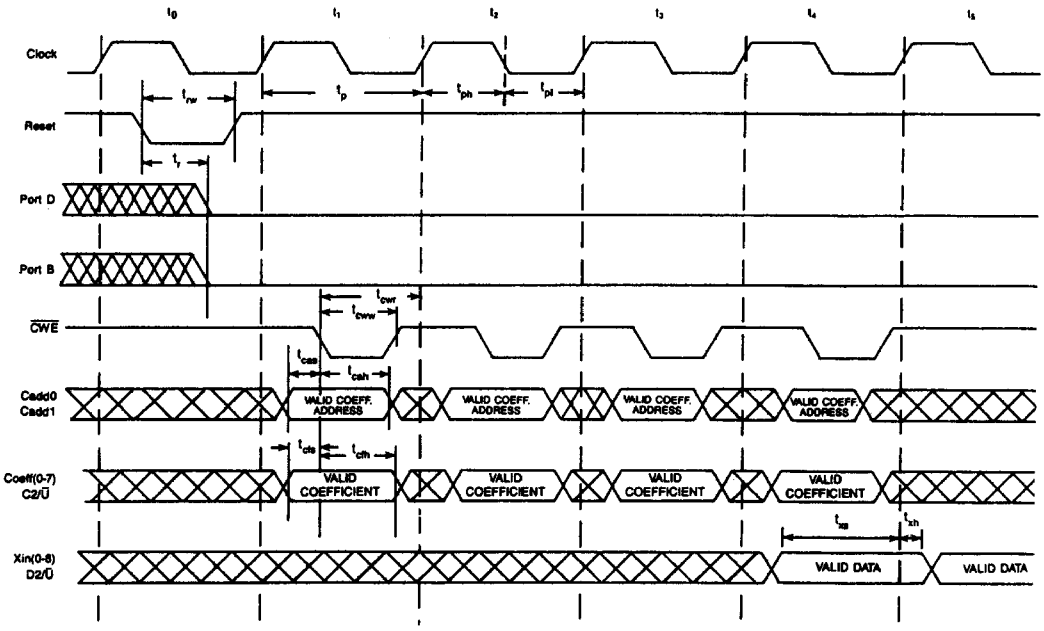


Figure 11. 29 MHz interpolating FIR filter using interleaved filter sections (14.5 MHz components).

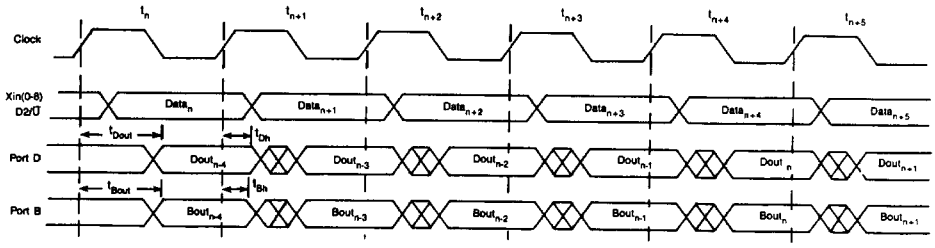
AC Characteristics over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
t_p	clock period	69		ns
t_{ph}	clock high time	29		ns
t_{pl}	clock lot time	29		ns
t_r	reset time		50	ns
t_{rw}	reset pulse width	30		ns
t_{xh}	data hold time	12.5		ns
t_{xs}	data setup time	5		ns
t_{cww}	coefficient write pulse width	12.5		ns
t_{cas}	coefficient address setup time	0		ns
t_{cah}	coefficient address hold time	15		ns
t_{cfs}	coefficient setup time	5		ns
t_{cfh}	coefficient hold time	12.5		ns
t_{cwr}	coefficient write recovery time	25		ns
t_{Dout}	clock to Port D valid		55	ns
t_{Dh}	clock to Port D invalid	20		ns
t_{Bout}	clock to Port B valid		55	ns
t_{Bh}	clock to Port B invalid	20		ns
t_{As}	Port A setup time	0		ns
t_{Ah}	Port A hold time	15		ns
t_{Cs}	Port C setup time	0		ns
t_{Ch}	Port C hold time	15		ns

Timing Diagram I - Coefficient Initialization Sequence

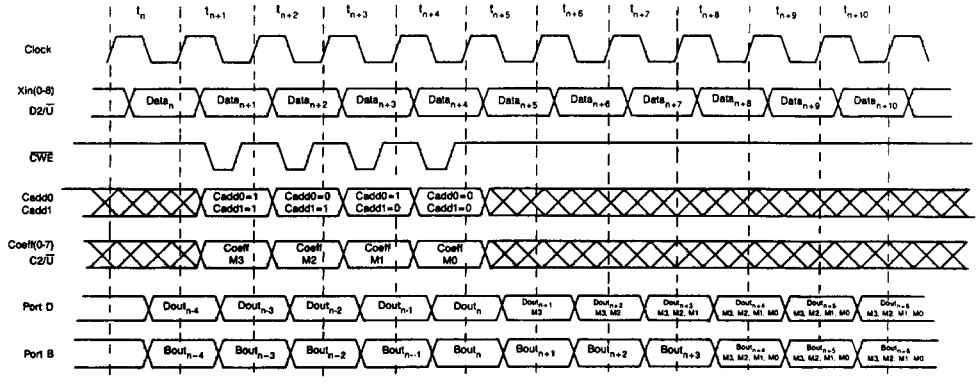


Timing Diagram II - Free Running Mode with Stable Coefficients



This shows the filter in a free-running mode with coefficients already loaded and stable. $Dout_n$ and $Bout_n$ are the first outputs using the $Data_n$. Thus, a latency of four cycles is present in this filter. Both CWE and RESET are assumed to be held high (inactive) in this mode. The C2/U and Coeff (0-7) inputs are don't cares.

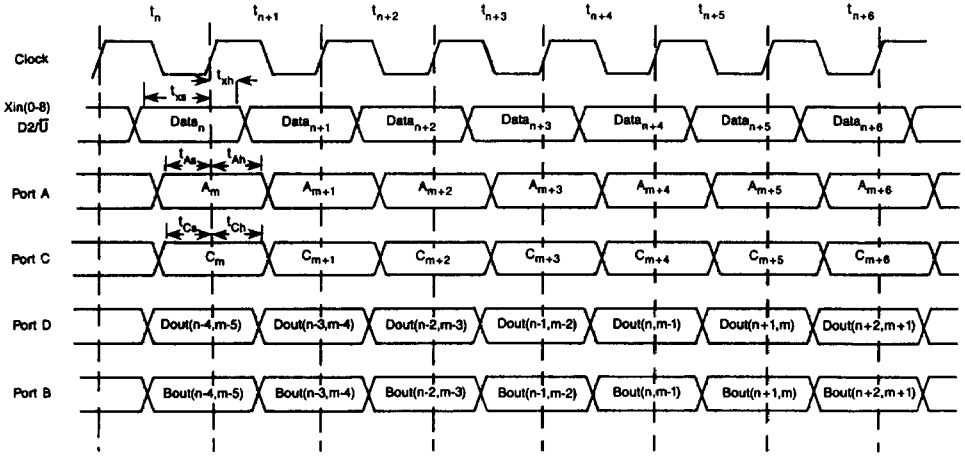
Timing Diagram III - Free Running Mode with Changing Coefficients



Timing diagram III shows the latency effects on filter output from changing the coefficients while the filter is running. One coefficient can be changed during each cycle. It should be noted that a four cycle latency exists between a coefficient update and output data effected by the update. This latency is due to internal delays in the multipliers. The sequence of the coefficient update is arbitrary and is controlled by the Cadd0 and Cadd1 lines. The M3, M2, M1, M0 notation on the Coeff(0-7) inputs and the Port B and Port D outputs shows how the output data is effected by this particular sequence of coefficient updates. It should also be noted that with this sequence of coefficient updates (M3, M2, M1, M0), Port D sees the effect on output one at a time, while Port B sees the effect all at once.

Timing Diagram IV - Input Port Timing

Timing diagram IV shows the relationship of the Port B and Port D outputs to the filter inputs: Xin, Port A, and Port C. At time t_n, Datan is input through Xin, while A_m and C_m are input through Ports A anc C, respectively. The four cycle latency discussed previously is evident since the Port B and D outputs do not depend on $Data_n$ until t_{n+4}. A_m and C_m both experience a five cycle latency before contributing to the Port B and D outputs, respectively, at t_{n+5}. This diagram shows a FIR filter used as a "non-end" chip in a cascaded, multi-chip linear phase configuration. If it was the lead chip, Port A would be grounded. If it was the left end chip (Port B tied to Port C of the same NCR45CF8E), then an input A_m at t_n would not contribute to the Port D output unitl t_{n+9}.



Absolute Maximum Ratings

Supply Voltage, V_{DD} ..... +7V

Voltage on any pin with respect to ground ..... −0.3 to VDD + 0.3V

Storage temperature ..... −65 °C to 150 °C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operation conditions stipulated elsewhere in this specification is not implied.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	4.75	5.25	Volts
V_{IH}	Input high level voltage (All inputs except Input Ports)	2.0	V_{DD}	Volts
V_{IHC}*	Input high level voltage, Parts A and C.	.7 V_{DD}	V_{DD}	Volts
V_{IL}	Input low level voltage	0	0.8	Volts
T_A	Operating ambient temperature	0	70	°C

*Port A and Port C use CMOS Input levels, all other pins use TTL levels.

Static Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Max.	Units
I_{IN}	Input leakage current	V_{IN} =0V to V_{DD}max		±10	μA
I_O	Output leakage current	V_O =0.4 to V_{DD}max		±10	μA
V_{OH}	Output high voltage	I_{OH} =4.0mA	2.4		Volts
V_{OL}	Output low voltage	I_{OL} =4.0mA		0.8	Volts
I_{DD}	Supply current — Active	Outputs Loaded		130	mA
	Supply current — Standby	Clock Inactive		10	mA
I_{SC}	Short circuit Output current †	One Output Shorted to ground or power		75	mA

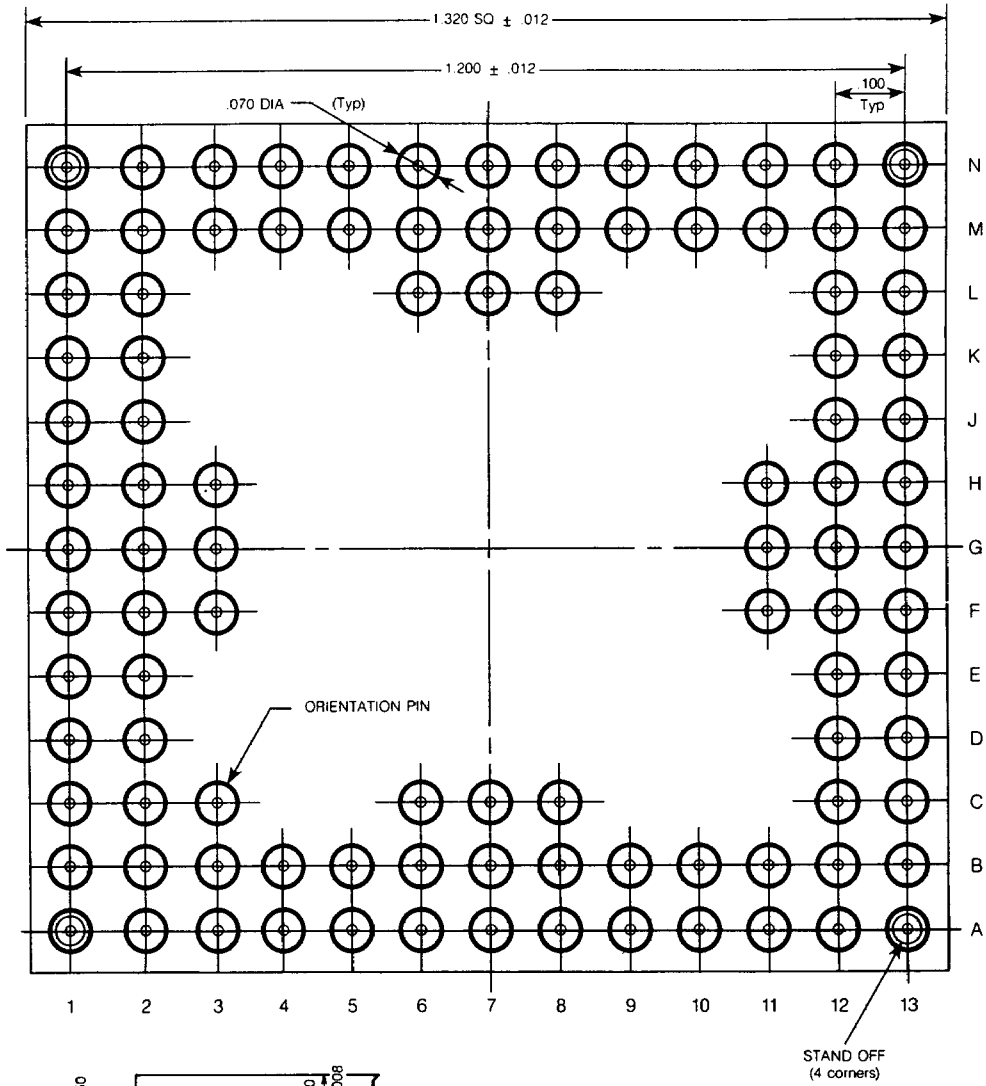
† Operating the device with Outputs Shorted to power or ground may result in permanent damage to the chip.

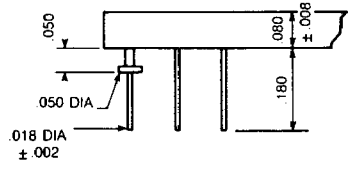
Capacitance TA = 25°C, f = 1 MHz

Symbol	Parameter	Condition	Min.	Max.	Units
C_{IN}	Input capacitance	All pins except pin under test are tied to ground		5	pF
C_O	Output capacitance			10	pF

Plastic Pin Grid Array Package

Bottom View





Side View

NOTE: ALL DIMENSIONS ARE IN INCHES

Table of Pin Numbers vs. Signal Labels for Plastic Pin Grid Array Package

PIN #	LABEL	PIN #	LABEL	PIN #	LABEL
A1	C11	E1	C3	M1	B8
A2	C13	E2	C4	M2	B5
A3	C14	E12	D13	M3	B3
A4	C16	E13	D14	M4	B1
A5	Xin5	F1	C0	M5	$\overline{CWE}$
A6	Xin8	F2	C1	M6	C2/$\overline{U}$
A7	D2/$\overline{U}$	F3	C2	M7	Coeff6
A8	Xin3	F11	D15	M8	Coeff3
A9	Xin0	F12	D16	M9	Coeff0
A10	D1	F13	D17	M10	A16
A11	D3	G1	B17	M11	A13
A12	D5	G2	Reset	M12	A11
A13	D7	G3	Vss	M13	A10
B1	C9	G11	Vss	N1	B6
B2	C10	G12	A0	N2	B4
B3	C12	G13	Clock	N3	B2
B4	C15	H1	B16	N4	B0
B5	C17	H2	B15	N5	Cadd0
B6	Xin7	H3	B14	N6	Coeff7
B7	Xin4	H11	A3	N7	Coeff5
B8	Xin2	H12	A2	N8	Coeff4
B9	D0	H13	A1	N9	Coeff1
B10	D2	J1	B13	N10	A17
B11	D4	J2	B12	N11	A15
B12	D6	J12	A5	N12	A14
B13	D9	J13	A4	N13	A12
C1	C7	K1	B11		
C2	C8	K2	B10		
C3	***	K12	A7		
C6	Xin6	K13	A6		
C7	Vdd	L1	B9		
C8	Xin1	L2	B7		
C12	D8	L6	Cadd1		
C13	D10	L7	Vdd		
D1	C5	L8	Coeff2		
D2	C6	L12	A9		
D12	D11	L13	A8		
D13	D12				

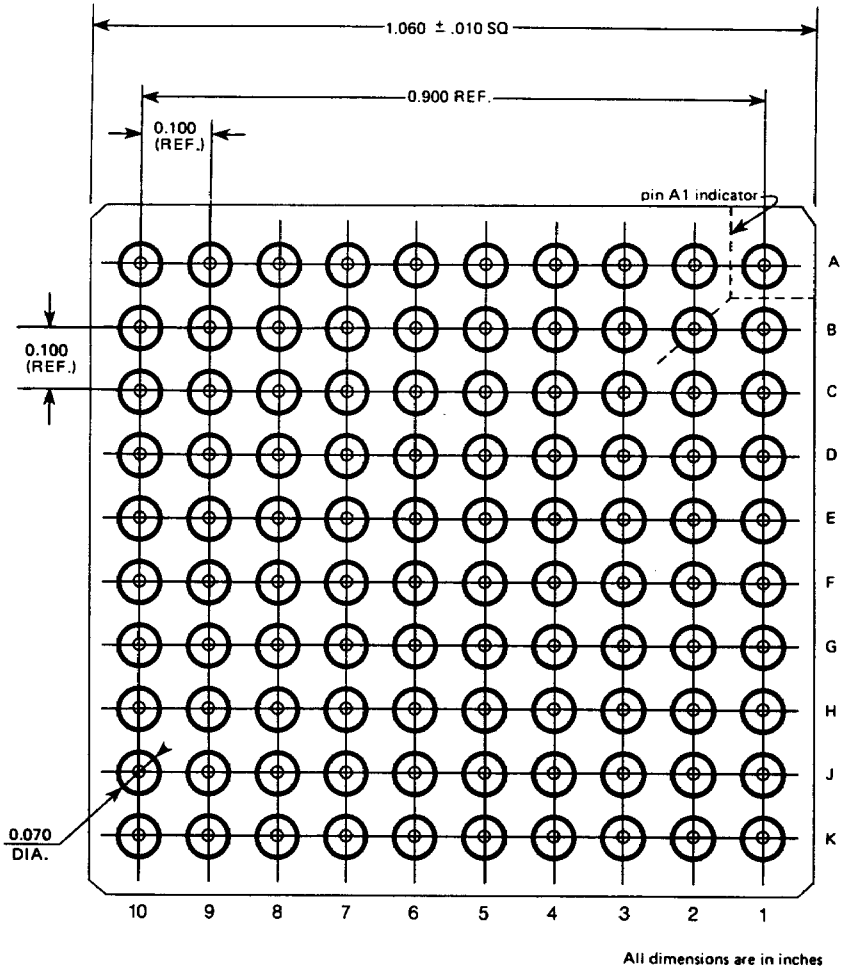
*** PIN NUMBER C3 is for ORIENTATION PURPOSES ONLY. This PIN is electrically floating.

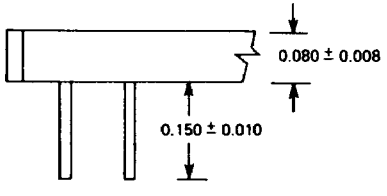
Table of Signal Names vs. Pin Numbers for Plastic Pin Grid Array Package

SIGNAL LABEL	PIN #	SIGNAL LABEL	PIN #	SIGNAL LABEL	PIN #	SIGNAL LABEL	PIN #
A0	G12	B7	L2	C14	A3	Coeff3	M8
A1	H13	B8	M1	C15	B4	Coeff4	N8
A2	H12	B9	L1	C16	A4	Coeff5	N7
A3	H11	B10	K2	C17	B5	Coeff6	M7
A4	J13	B11	K1	D0	B9	Coeff7	N6
A5	J12	B12	J2	D1	A10	Xin0	A9
A6	K13	B13	J1	D2	B10	Xin1	C8
A7	K12	B14	H3	D3	A11	Xin2	B8
A8	L13	B15	H2	D4	B11	Xin3	A8
A9	L12	B16	H1	D5	A12	Xin4	B7
A10	M13	B17	G1	D6	B12	Xin5	A5
A11	M12	C0	F1	D7	A13	Xin6	C6
A12	N13	C1	F2	D8	C12	Xin7	B6
A13	M11	C2	F3	D9	B13	Xin8	A6
A14	N12	C3	E1	D10	C13	Cadd0	N5
A15	N11	C4	E2	D11	D12	Cadd1	L6
A16	M10	C5	D1	D12	D13	C2/$\overline{U}$	M6
A17	N10	C6	D2	D13	E12	D2/$\overline{U}$	A7
B0	N4	C7	C1	D14	E13	$\overline{CWE}$	M5
B1	M4	C8	C2	D15	F11	Clockin	G13
B2	N3	C9	B1	D16	F12	Reset	G2
B3	M3	C10	B2	D17	F13	Vdd	C7
B4	N2	C11	A1	Coeff0	M9	Vdd	L7
B5	M2	C12	B3	Coeff1	N9	Vss	G3
B6	N1	C13	A2	Coeff2	L8	Vss	G11

Ceramic Pin Grid Array Package

Bottom View





Side View

Table of Pin Numbers vs. Signal Labels for Ceramic Pin Grid Array Package

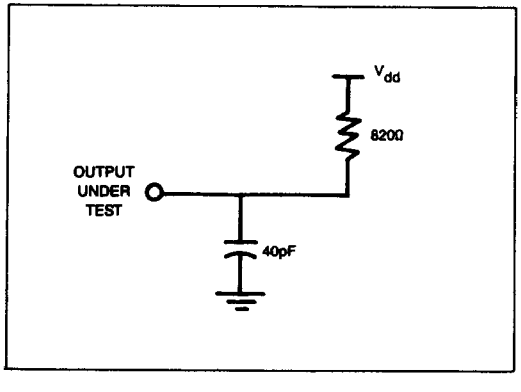
PIN #	LABEL	PIN #	LABEL	PIN #	LABEL
A1	D11	E1	Xin4	J1	Xin7
A2	D16	E2	Xin3	J2	C12
A3	D17	E3	Xin2	J3	C8
A4	Clock	E4	Xin1	J4	C5
A5	D14	E5	D0	J5	C0
A6	A0	E6	A5	J6	B14
A7	A4	E7	A14	J7	B12
A8	A8	E8	V_{dd}	J8	B11
A9	A12	E9	Coeff2	J9	B7
A10	A16	E10	Coeff1	J10	B6
B1	D7	F1	Xin5	K1	C15
B2	D8	F2	Xin6	K2	C11
B3	D12	F3	V_{dd}	K3	C7
B4	D13	F4	C13	K4	C3
B5	D15	F5	C4	K5	Reset
B6	A1	F6	$\overline{CWE}$	K6	B13
B7	A6	F7	Cadd1	K7	B17
B8	A9	F8	C2/$\overline{U}$	K8	B16
B9	A13	F9	Coeff7	K9	B15
B10	Coeff3	F10	Coeff6	K10	B10
C1	D3	G1	C2/$\overline{U}$		
C2	D4	G2	C17		
C3	D6	G3	C14		
C4	D10	G4	C9		
C5	V_{ss}	G5	C2		
C6	A2	G6	B8		
C7	A7	G7	B4		
C8	A11	G8	B1		
C9	A17	G9	B0		
C10	Coeff4	G10	Cadd0		
D1	Xin0	H1	Xin8		
D2	D1	H2	C16		
D3	D2	H3	C10		
D4	D5	H4	C6		
D5	D9	H5	C1		
D6	A3	H6	V_{ss}		
D7	A10	H7	B9		
D8	A15	H8	B5		
D9	Coeff0	H9	B3		
D10	Coeff5	H10	B2		

NCR45CF8 Finite Impulse Response Filter

Table of Pin Numbers vs. Signal Labels for Ceramic Pin Grid Array Package

SIGNAL LABEL	PIN #	SIGNAL LABEL	PIN #	SIGNAL LABEL	PIN #	SIGNAL LABEL	PIN #
A0	A6	B7	J9	C14	G3	Coeff3	B10
A1	B6	B8	G6	C15	K1	Coeff4	C10
A2	C6	B9	H7	C16	H2	Coeff5	D10
A3	D6	B10	K10	C17	G2	Coeff6	F10
A4	A7	B11	J8	D0	E5	Coeff7	F9
A5	E6	B12	J7	D1	D2	Xin0	D1
A6	B7	B13	K6	D2	D3	Xin1	E4
A7	C7	B14	J6	D3	C1	Xin2	E3
A8	A8	B15	K9	D4	C2	Xin3	E2
A9	B8	B16	K8	D5	D4	Xin4	E1
A10	D7	B17	K7	D6	C3	Xin5	F1
A11	C8	C0	J5	D7	B1	Xin6	F2
A12	A9	C1	H5	D8	B2	Xin7	J1
A13	B9	C2	G5	D9	D5	Xin8	H1
A14	E7	C3	K4	D10	C4	Cadd0	G10
A15	D8	C4	F5	D11	A1	Cadd1	F7
A16	A10	C5	J4	D12	B3	C2/$\overline{U}$	F8
A17	C9	C6	H4	D13	B4	D2/$\overline{U}$	G1
B0	G9	C7	K3	D14	A5	$\overline{CWE}$	F6
B1	G8	C8	J3	D15	B5	Clock	A4
B2	H10	C9	G4	D16	A2	Reset	K5
B3	H9	C10	H3	D17	A3	V_{dd}	E8
B4	G7	C11	K2	Coeff0	D9	V_{dd}	F3
B5	H8	C12	J2	Coeff1	E10	V_{ss}	C5
B6	J10	C13	F4	Coeff2	E9	V_{ss}	H6

AC Test Load Circuit



CAUTION

1. CMOS Devices are damaged by high energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted.
2. Remove power before insertion or removal of this device.

Application Notes

The ground pins (Vss) of the NCR45CF8 are not connected internally. In all applications, both ground pins must be connected externally to ground. We also recommend connecting both power pins (Vdd) externally to power in all applications. The NCR45CF8 device is a high speed CMOS integrated circuit, which will dissipate very little static power but will also consume significant dynamic current. We recommend the use of at least one 01.μf deglitching capacitor per NCR45CF8 chip to reduce switching noise on the system power buss. To prevent ringing, care should be taken to follow standard engineering practice for minimizing power and ground lead inductance.