

# ecoSWITCH™

## Advanced Load Management

### Controlled Load Switch with Low $R_{ON}$

## NCP45526

The NCP45526 load switch provides a component and area-reducing solution for efficient power domain switching with inrush current limit via soft start. This device is designed to integrate control and driver functionality with a high performance low on-resistance power MOSFET in a single package. This cost effective solution is ideal for power management and hot-swap applications requiring low power consumption in a small footprint.

### Features

- Advanced Controller with Charge Pump
- Integrated N-Channel MOSFET with Low  $R_{ON}$
- Input Voltage Range 0.5 V to 6 V
- Soft-Start via Controlled Slew Rate
- Power Good Signal
- Extremely Low Standby Current
- Load Bleed (Quick Discharge)
- This is a Pb-Free Device

### Typical Applications

- Portable Electronics and Systems
- Notebook and Tablet Computers
- Telecom, Networking, Medical, and Industrial Equipment
- Set-Top Boxes, Servers, and Gateways
- Hot-Swap Devices and Peripheral Ports

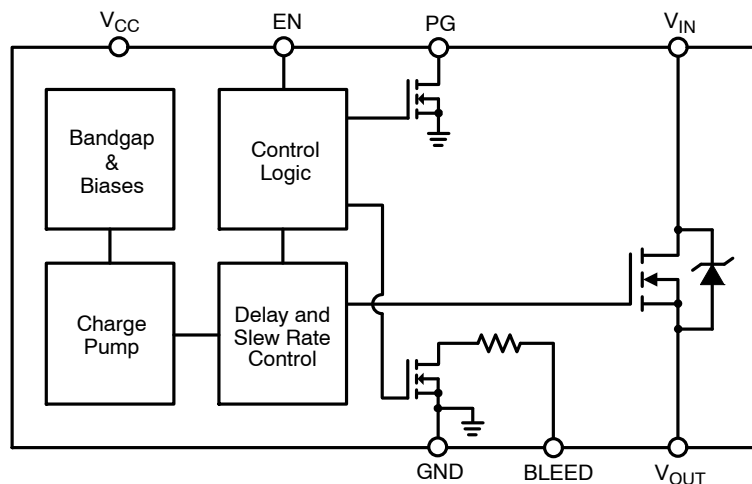


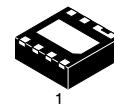
Figure 1. Block Diagram



ON Semiconductor®

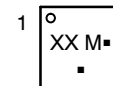
[www.onsemi.com](http://www.onsemi.com)

$R_{ON}$ TYP	$V_{CC}$	$V_{IN}$	$I_{MAX}$
18.0 mΩ	3.3 V	1.8 V	6 A
18.8 mΩ	3.3 V	5.0 V	



DFN8, 2x2  
CASE 506CC

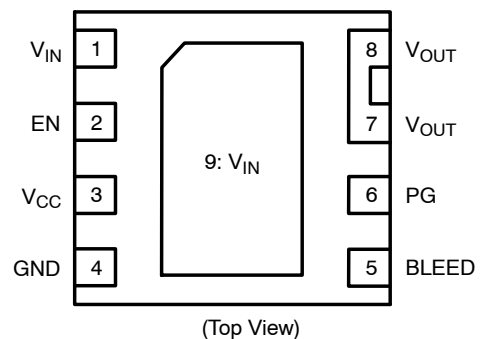
### MARKING DIAGRAM



XX = 4H for NCP45526-H  
= 4L for NCP45526-L  
M = Date Code  
■ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONFIGURATION



### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

# NCP45526

**Table 1. PIN DESCRIPTION**

Pin	Name	Function
1, 9	V <sub>IN</sub>	Drain of MOSFET (0.5 V – 6.0 V), Pin 1 must be connected to Pin 9
2	EN	NCP45526–H – Active–high digital input used to turn on the MOSFET, pin has an internal pull down resistor to GND
		NCP45526–L – Active–low digital input used to turn on the MOSFET, pin has an internal pull up resistor to V <sub>CC</sub>
3	V <sub>CC</sub>	Supply voltage to controller (3.0 V – 5.5 V)
4	GND	Controller ground
5	BLEED	Load bleed connection; must be tied to V <sub>OUT</sub> either directly or through a resistor ≤ 100 MΩ.
6	PG	NCP45526 – Active–high, open–drain output that indicates when the gate of the MOSFET is fully charged, external pull up resistor ≥ 1 kΩ to an external voltage source required; tie to GND if not used
7, 8	V <sub>OUT</sub>	Source of MOSFET connected to load

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Supply Voltage Range	V <sub>CC</sub>	–0.3 to 6	V
Input Voltage Range	V <sub>IN</sub>	–0.3 to 6	V
Output Voltage Range	V <sub>OUT</sub>	–0.3 to 6	V
EN Digital Input Range	V <sub>EN</sub>	–0.3 to (V <sub>CC</sub> + 0.3)	V
PG Output Voltage Range (Note 1)	V <sub>PG</sub>	–0.3 to 6	V
Thermal Resistance, Junction–to–Ambient, Steady State (Note 2)	R <sub>θJA</sub>	40.0	°C/W
Thermal Resistance, Junction–to–Ambient, Steady State (Note 3)	R <sub>θJA</sub>	72.7	°C/W
Thermal Resistance, Junction–to–Case (V <sub>IN</sub> Paddle)	R <sub>θJC</sub>	5.3	°C/W
Continuous MOSFET Current @ T <sub>A</sub> = 25°C	I <sub>MAX</sub>	6.0	A
Total Power Dissipation @ T <sub>A</sub> = 25°C (Notes 2 and 4) Derate above T <sub>A</sub> = 25°C	P <sub>D</sub>	2.50 24.9	W mW/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C (Notes 3 and 4) Derate above T <sub>A</sub> = 25°C	P <sub>D</sub>	1.37 13.8	W mW/°C
Storage Temperature Range	T <sub>STG</sub>	–40 to 150	°C
Lead Temperature, Soldering (10 sec.)	T <sub>SLD</sub>	260	°C
ESD Capability, Human Body Model (Notes 5 and 6)	ESD <sub>HBM</sub>	3.0	kV
ESD Capability, Machine Model (Note 5)	ESD <sub>MM</sub>	200	V
ESD Capability, Charged Device Model (Note 5)	ESD <sub>CDM</sub>	1.0	kV
Latch–up Current Immunity (Notes 5 and 6)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- PG is an open–drain output that requires an external pull up resistor ≥ 1 kΩ to an external voltage source.
- Surface–mounted on FR4 board using 1 sq–in pad, 1 oz Cu.
- Surface–mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
- Specified for derating purposes only, ensure that I<sub>MAX</sub> is never exceeded.
- Tested by the following methods @ T<sub>A</sub> = 25°C:  
 ESD Human Body Model tested per JESD22–A114  
 ESD Machine Model tested per JESD22–A115  
 ESD Charged Device Model tested per JESD22–C101  
 Latch–up Current tested per JESD78
- Rating is for all pins except for V<sub>IN</sub> and V<sub>OUT</sub> which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V<sub>IN</sub> and V<sub>OUT</sub> should be expected and these devices should be treated as ESD sensitive.

**Table 3. OPERATING RANGES**

Rating	Symbol	Min	Max	Unit
Supply Voltage	$V_{CC}$	3	5.5	V
Input Voltage	$V_{IN}$	0.5	6	V
Ground	GND		0	V
Ambient Temperature	$T_A$	-40	85	°C
Junction Temperature	$T_J$	-40	125	°C
OFF to ON Transition Energy Dissipation Limit (See application section)	$E_{TRANS}$	0	100	mJ

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Conditions (Note 7)	Symbol	Min	Typ	Max	Unit
<b>MOSFET</b>						
On-Resistance	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$	$R_{ON}$		18.0	24.0	m $\Omega$
	$V_{CC} = 3.3\text{ V}; V_{IN} = 5\text{ V}$			18.8	25.0	
Leakage Current (Note 8)	$V_{EN} = 0\text{ V}; V_{IN} = 6\text{ V}$	$I_{LEAK}$		0.1	1	$\mu\text{A}$
<b>CONTROLLER</b>						
Supply Standby Current (Note 9)	$V_{EN} = 0\text{ V}; V_{CC} = 3\text{ V}$	$I_{STBY}$		0.65	2	$\mu\text{A}$
	$V_{EN} = 0\text{ V}; V_{CC} = 5.5\text{ V}$			3.2	4.5	
Supply Dynamic Current (Note 10)	$V_{EN} = V_{CC} = 3\text{ V}; V_{IN} = 5\text{ V}$	$I_{DYN}$		150	250	$\mu\text{A}$
	$V_{EN} = V_{CC} = 5.5\text{ V}; V_{IN} = 1.8\text{ V}$			475	680	
Bleed Resistance	$V_{EN} = 0\text{ V}; V_{CC} = 3\text{ V}$	$R_{BLEED}$	86	115	144	$\Omega$
	$V_{EN} = 0\text{ V}; V_{CC} = 5.5\text{ V}$		72	97	121	
EN Input High Voltage	$V_{CC} = 3\text{ V} - 5.5\text{ V}$	$V_{IH}$	2			V
EN Input Low Voltage	$V_{CC} = 3\text{ V} - 5.5\text{ V}$	$V_{IL}$			0.8	V
EN Input Leakage Current	NCP45526-H; $V_{EN} = 0\text{ V}$	$I_{IL}$		90	500	nA
	NCP45526-L; $V_{EN} = 5.5\text{ V}$	$I_{IH}$		90	500	
EN Pull Down Resistance	NCP45526-H	$R_{PD}$	76	100	124	k $\Omega$
EN Pull Up Resistance	NCP45526-L	$R_{PU}$	76	100	124	k $\Omega$
PG Output Low Voltage (Note 11)	$V_{CC} = 3\text{ V}; I_{SINK} = 5\text{ mA}$	$V_{OL}$			0.2	V
PG Output Leakage Current (Note 12)	$V_{CC} = 3\text{ V}; V_{TERM} = 3.3\text{ V}$	$I_{OH}$		5	100	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7.  $V_{EN}$  shown only for NCP45526-H (EN Active-High) unless otherwise specified.

8. Average current from  $V_{IN}$  to  $V_{OUT}$  with MOSFET turned off.

9. Average current from  $V_{CC}$  to GND with MOSFET turned off.

10. Average current from  $V_{CC}$  to GND after charge up time of MOSFET.

11. PG is an open-drain output that is pulled low when the MOSFET is disabled.

12. PG is an open-drain output that is not driven when the gate of the MOSFET is fully charged, requires an external pull up resistor  $\geq 1\text{ k}\Omega$  to an external voltage source,  $V_{TERM}$ .

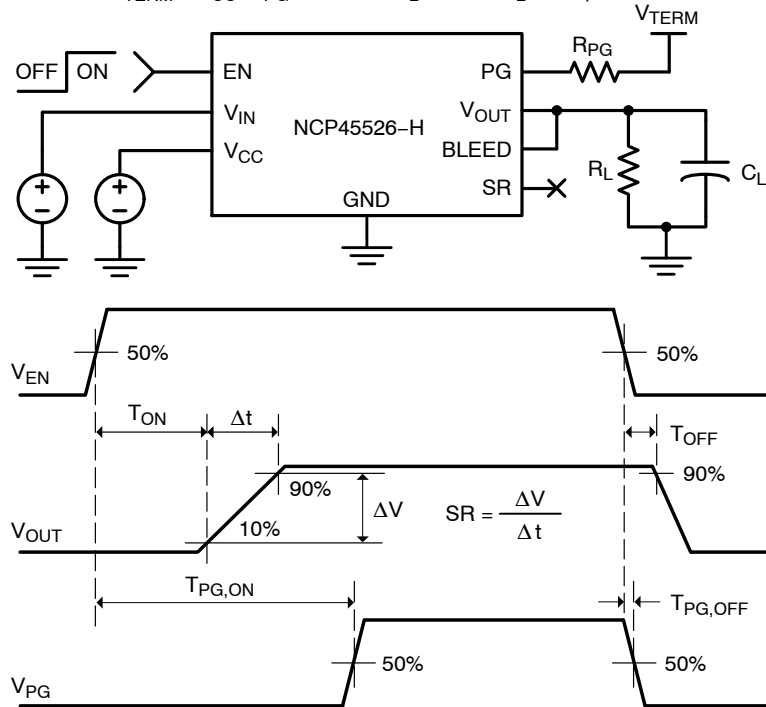
# NCP45526

**Table 5. SWITCHING CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified) (Notes 13 and 14)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Slew Rate	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$	SR		11.9		kV/s
	$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$			12.1		
	$V_{CC} = 3.3\text{ V}; V_{IN} = 5.0\text{ V}$			12.8		
	$V_{CC} = 5.0\text{ V}; V_{IN} = 5.0\text{ V}$			13.2		
Output Turn-on Delay	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$	$T_{ON}$		220		$\mu\text{s}$
	$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$			185		
	$V_{CC} = 3.3\text{ V}; V_{IN} = 5.0\text{ V}$			230		
	$V_{CC} = 5.0\text{ V}; V_{IN} = 5.0\text{ V}$			205		
Output Turn-off Delay	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$	$T_{OFF}$		1.2		$\mu\text{s}$
	$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$			0.9		
	$V_{CC} = 3.3\text{ V}; V_{IN} = 5.0\text{ V}$			0.8		
	$V_{CC} = 5.0\text{ V}; V_{IN} = 5.0\text{ V}$			0.5		
Power Good Turn-on Time	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$	$T_{PG,ON}$		0.91		ms
	$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$			0.93		
	$V_{CC} = 3.3\text{ V}; V_{IN} = 5.0\text{ V}$			0.96		
	$V_{CC} = 5.0\text{ V}; V_{IN} = 5.0\text{ V}$			0.93		
Power Good Turn-off Time	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$	$T_{PG,OFF}$		21		ns
	$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$			15		
	$V_{CC} = 3.3\text{ V}; V_{IN} = 5.0\text{ V}$			21		
	$V_{CC} = 5.0\text{ V}; V_{IN} = 5.0\text{ V}$			15		

13. See below figure for Test Circuit and Timing Diagram.

14. Tested with the following conditions:  $V_{TERM} = V_{CC}$ ;  $R_{PG} = 100\text{ k}\Omega$ ;  $R_L = 10\text{ }\Omega$ ;  $C_L = 0.1\text{ }\mu\text{F}$ .



**Figure 2. Switching Characteristics Test Circuit and Timing Diagram**

## APPLICATIONS INFORMATION

**Enable Control**

The NCP45526 has two part numbers, NCP45526-H and NCP45526-L, that only differ in the polarity of the enable control.

The NCP45526-H device allows for enabling the MOSFET in an active-high configuration. When the  $V_{CC}$  supply pin has an adequate voltage applied and the EN pin is at a logic high level, the MOSFET will be enabled. Similarly, when the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not being driven.

The NCP45526-L device allows for enabling the MOSFET in an active-low configuration. When the  $V_{CC}$  supply pin has an adequate voltage applied and the EN pin is at a logic low level, the MOSFET will be enabled. Similarly, when the EN pin is at a logic high level, the MOSFET will be disabled. An internal pull up resistor to  $V_{CC}$  on the EN pin ensures that the MOSFET will be disabled when not being driven.

**Power Sequencing**

The NCP45526 device will function with any power sequence, but the output turn-on delay performance may vary from what is specified. To achieve the specified performance, there are two recommended power sequences:

- 1)  $V_{CC} \rightarrow V_{IN} \rightarrow V_{EN}$
- 2)  $V_{IN} \rightarrow V_{CC} \rightarrow V_{EN}$

$V_{CC}$  must be at 2 V or higher when EN is asserted to ensure that the enable is latched properly for correct operation. If EN comes up before  $V_{CC}$  reaches 2 V, then the EN may not take effect.

**Load Bleed (Quick Discharge)**

The NCP45526 device has an internal bleed resistor,  $R_{BLEED}$ , which is used to bleed the charge off of the load to ground after the MOSFET has been disabled. In series with the bleed resistor is a bleed switch that is enabled whenever the MOSFET is disabled. The MOSFET and the bleed switch are never concurrently active.

Is it required that the BLEED pin be connected to  $V_{OUT}$  either directly (as shown in Figure 4) or through an external resistor,  $R_{EXT}$  (as shown in Figure 3).  $R_{EXT}$  should not exceed 100 M $\Omega$  and can be used to increase the total bleed resistance and decrease the load bleed rate.

Care must be taken to ensure that the power dissipated across  $R_{BLEED}$  is kept at a safe level. The maximum continuous power that can be dissipated across  $R_{BLEED}$  is 0.4 W.  $R_{EXT}$  can be used to decrease the amount of power dissipated across  $R_{BLEED}$ .

**Power Good**

The NCP45526 devices have a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active-high, open-drain output that requires an external pull up resistor,  $R_{PG}$ , greater than or equal to 1 k $\Omega$  to an external voltage source,  $V_{TERM}$ , that is compatible with input levels of all devices connected to this pin (as shown in Figures 3 and 4).

The power good output can be used as the enable signal for other active-high devices in the system (as shown in Figure 5). This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

**Slew Rate Control**

The NCP45526 devices are equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swap applications.

**Capacitive Load**

The peak in-rush current associated with the initial charging of the application load capacitance needs to stay below the specified  $I_{MAX}$ . CL (capacitive load) should be less than  $C_{max}$  as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}} \quad (\text{eq. 1})$$

Where  $I_{MAX}$  is the maximum load current, and  $SR_{typ}$  is the typical default slew rate when no external load capacitor is added to the SR pin.

**OFF to ON Transition Energy Dissipation**

The energy dissipation due to load current traveling from  $V_{IN}$  to  $V_{OUT}$  is very low during steady state operation due to the low  $R_{ON}$ . When the EN signal is asserted high, the load switch transitions from an OFF state to an ON state. During this time, the resistance from  $V_{IN}$  to  $V_{OUT}$  transitions from high impedance to  $R_{ON}$ , and additional energy is dissipated in the device for a short period of time. The worst case energy dissipated during the OFF to ON transition can be approximated by the following equation:

$$E = 0.5 \cdot V_{IN} \cdot (I_{INRUSH} + 0.8 \cdot I_{LOAD}) \cdot dt \quad (\text{eq. 2})$$

Where  $V_{IN}$  is the voltage on the  $V_{IN}$  pin,  $I_{INRUSH}$  is the inrush current caused by capacitive loading on  $V_{OUT}$ , and  $dt$  is the time it takes  $V_{OUT}$  to rise from 0 V to  $V_{IN}$ .  $I_{INRUSH}$  can be calculated using the following equation:

$$I_{INRUSH} = \frac{dv}{dt} \cdot C_L \quad (\text{eq. 3})$$

Where  $dv/dt$  is the programmed slew rate, and  $C_L$  is the capacitive loading on  $V_{OUT}$ . To prevent thermal lockout or damage to the device, the energy dissipated during the OFF to ON transition should be limited to  $E_{TRANS}$  listed in operating ranges table.

## ecoSWITCH LAYOUT GUIDELINES

### Electrical Layout Considerations

Correct physical PCB layout is important for proper low noise accurate operation of all ecoSWITCH products.

**Power Planes:** The ecoSWITCH is optimized for extremely low  $R_{on}$  resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to

the  $V_{IN}$  and  $V_{OUT}$  pins of the ecoSWITCH to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSWITCH requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. Direct coupling of  $V_{IN}$  to  $V_{OUT}$  should be avoided, as this will adversely affect slew rates. The figure below shows an example of correct power plane layout. The number and location of pins for specific ecoSWITCH products may vary. This demonstrates large planes for both  $V_{IN}$  and  $V_{OUT}$ , while avoiding capacitive coupling between the two planes.

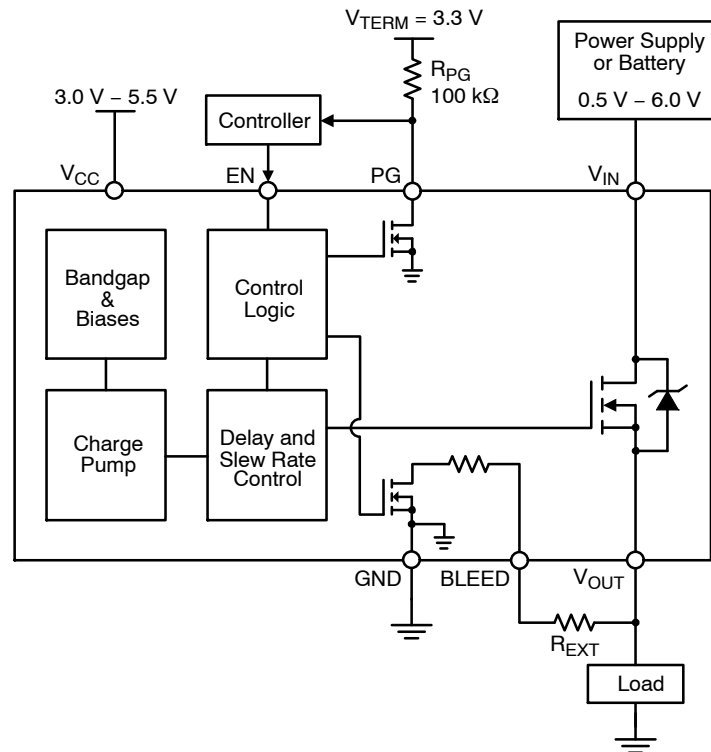


Figure 3. NCP45526 Typical Application Diagram – Load Switch

# NCP45526

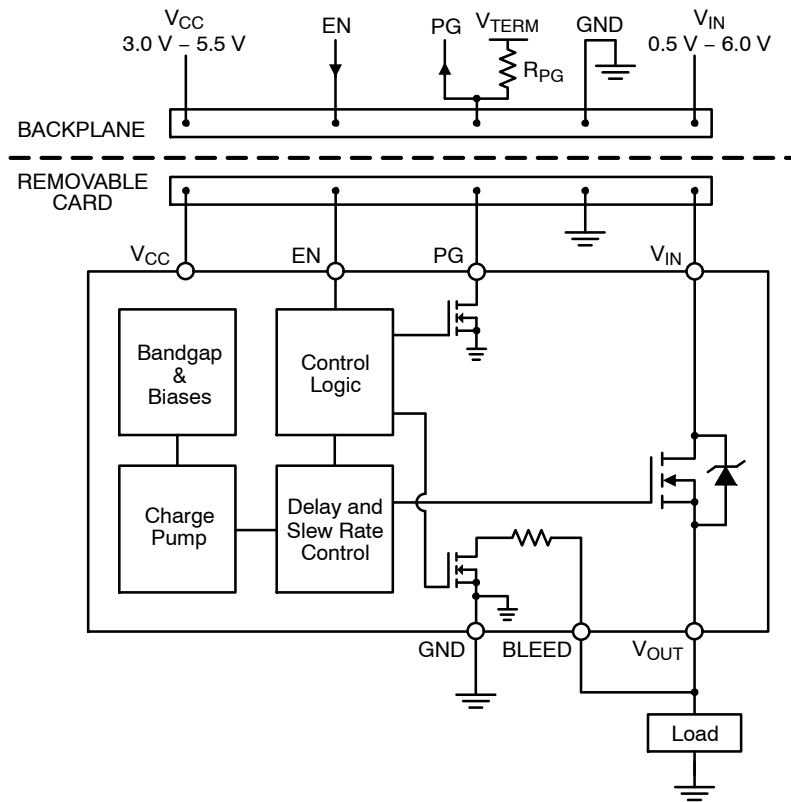


Figure 4. NCP45526 Typical Application Diagram – Hot Swap

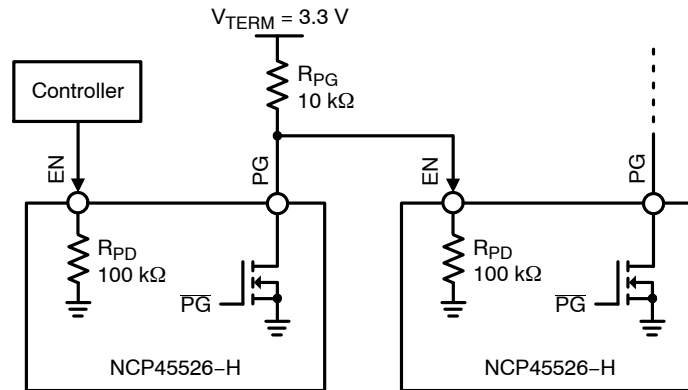


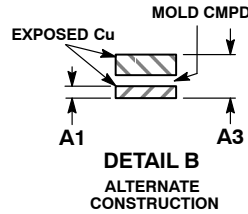
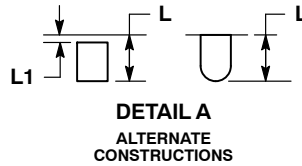
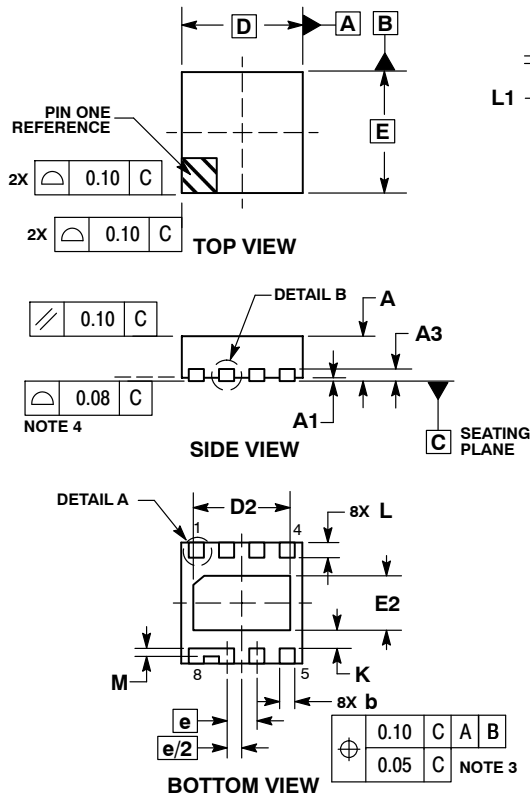
Figure 5. NCP45526 Simplified Application Diagram – Power Sequencing with PG Output

## ORDERING INFORMATION

Device	EN Polarity	Package	Shipping <sup>†</sup>
NCP45526IMNTWG-H	Active-High	DFN8 (Pb-Free)	3000 / Tape & Reel
NCP45526IMNTWG-L	Active-Low		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

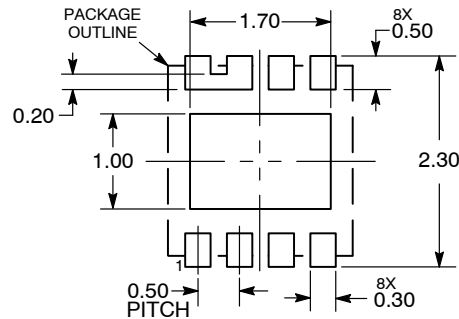
## PACKAGE DIMENSIONS

DFN8 2x2, 0.5P  
CASE 506CC  
ISSUE A

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.50	1.70
E	2.00	BSC
E2	0.80	1.00
e	0.50	BSC
K	0.20	REF
L	0.18	0.38
L1	---	0.15
M	0.14	REF

RECOMMENDED  
SOLDERING FOOTPRINT\*

DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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