

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

The NCE6005S uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

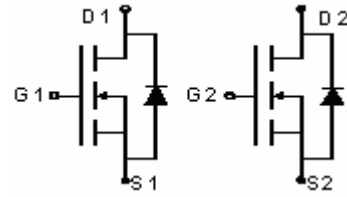
### General Features

- $V_{DS} = 60V, I_D = 4.5A$   
 $R_{DS(ON)} < 45m\Omega @ V_{GS} = 10V$  (Typ:  $38m\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

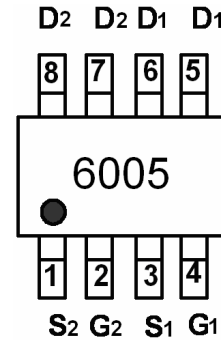
### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

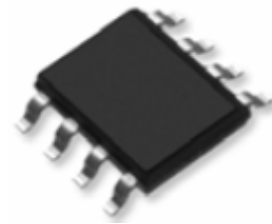
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment



SOP-8 top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
6005	NCE6005S	SOP-8	Ø330mm	12mm	2500 units

### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	4.5	A
Drain Current-Continuous ( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	3.0	A
Pulsed Drain Current	$I_{DM}$	20	A
Maximum Power Dissipation	$P_D$	2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$
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**Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

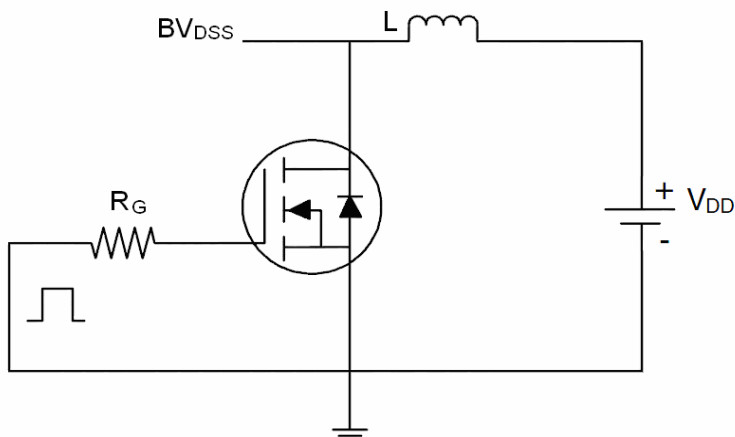
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	60	69	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =4.5A		38	45	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V,I <sub>D</sub> =4.5A	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V,V <sub>GS</sub> =0V, F=1.0MHz		450		PF
Output Capacitance	C <sub>OSS</sub>			60		PF
Reverse Transfer Capacitance	C <sub>RSS</sub>			25		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =30V,I <sub>D</sub> =4.5A V <sub>GS</sub> =10V,R <sub>GEN</sub> =3Ω	-	4.7	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	2.3	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	15.7	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	1.9	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V,I <sub>D</sub> =4.5A, V <sub>GS</sub> =10V	-	8.5	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.6	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	2.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =3.7A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	4	A

**Notes:**

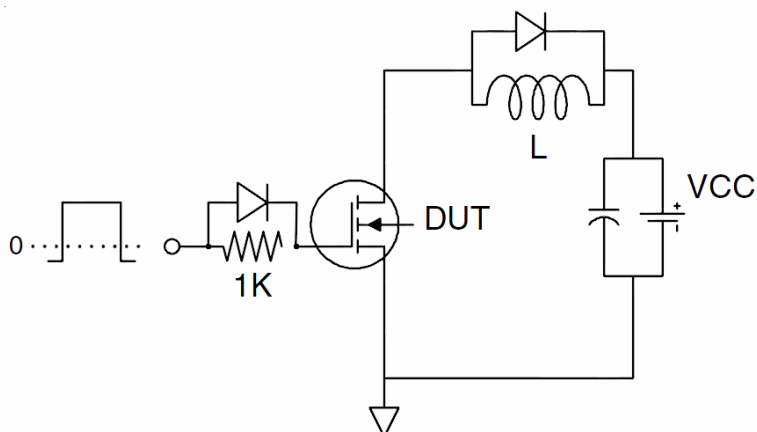
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Test Circuit

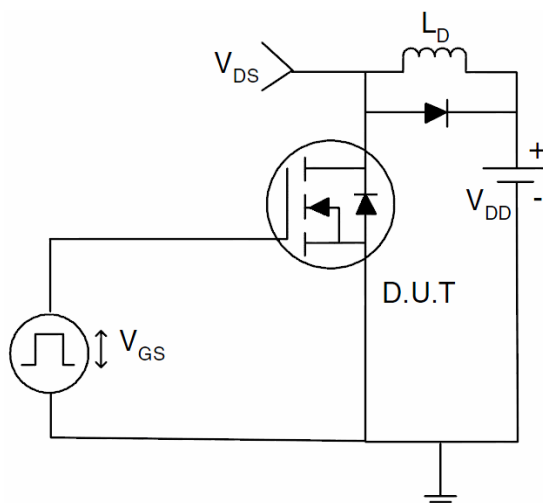
### 1) $E_{AS}$ test Circuits



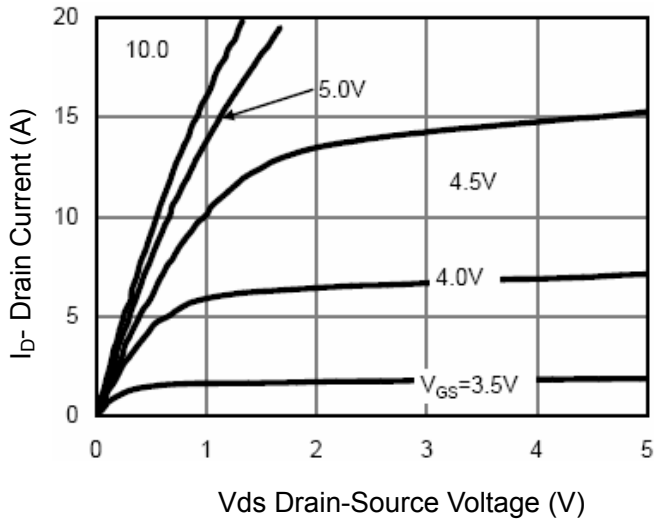
### 2) Gate charge test Circuit



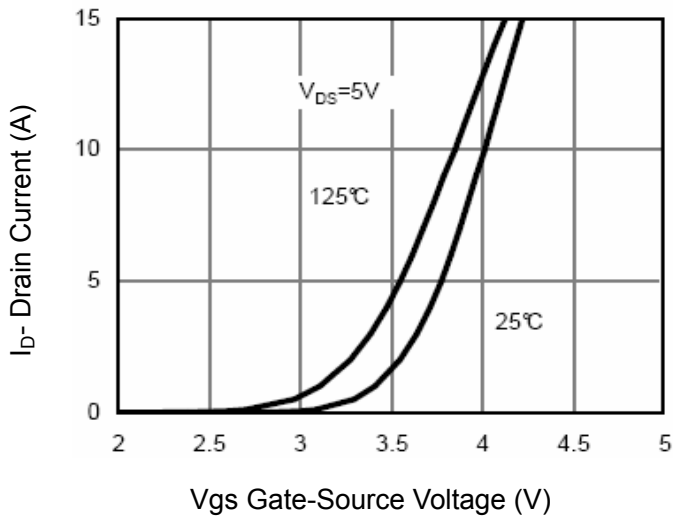
### 3) Switch Time Test Circuit



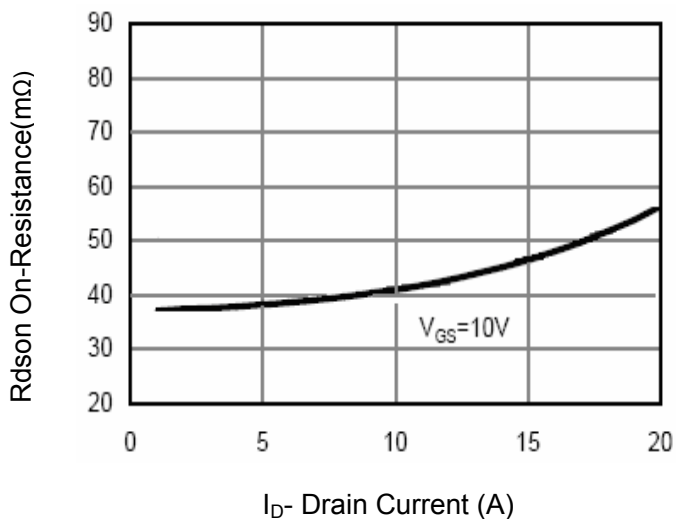
**Typical Electrical and Thermal Characteristics (Curves)**



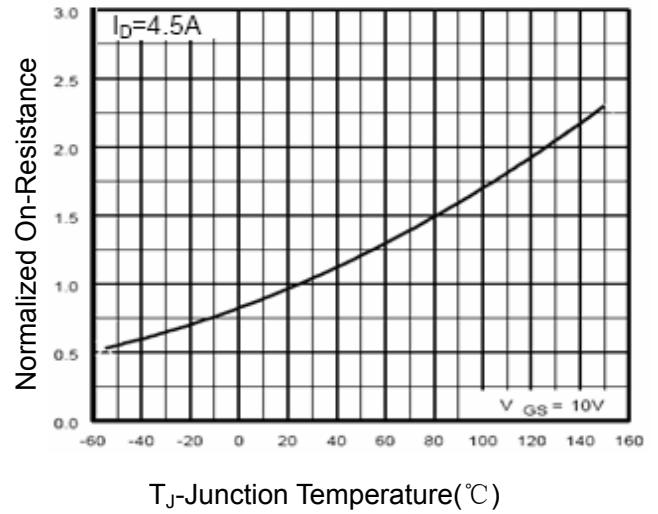
**Figure 1 Output Characteristics**



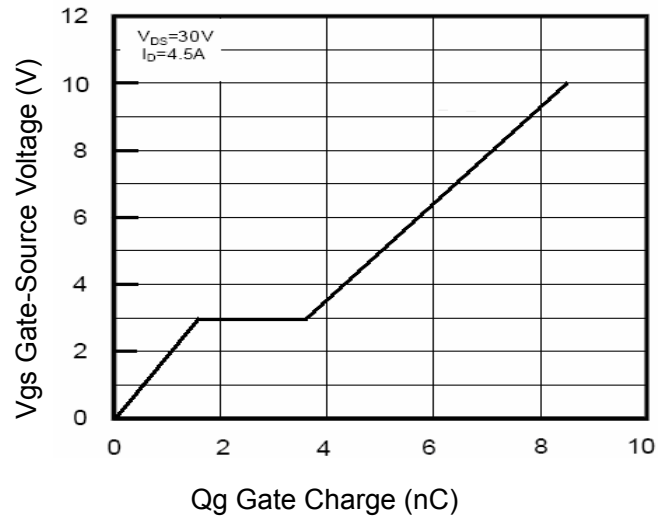
**Figure 2 Transfer Characteristics**



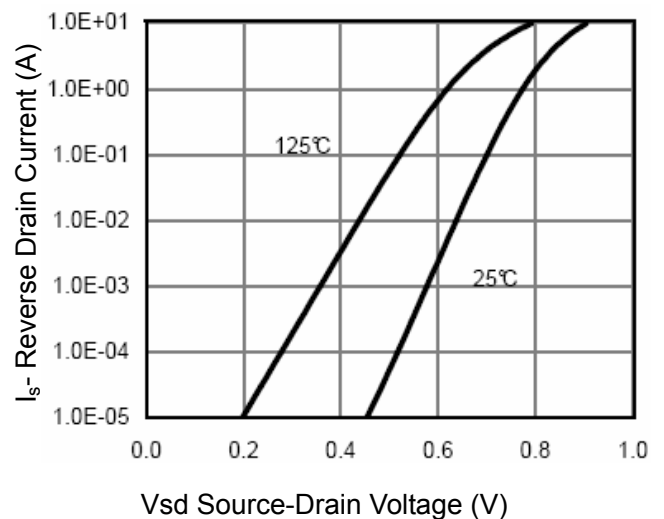
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

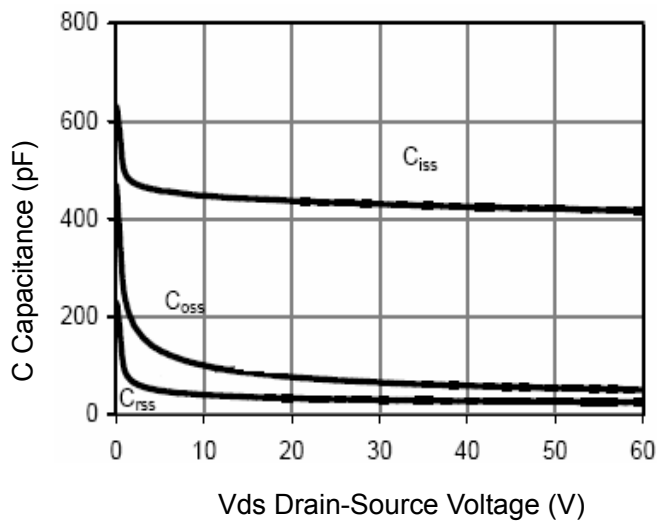


Figure 7 Capacitance vs Vds

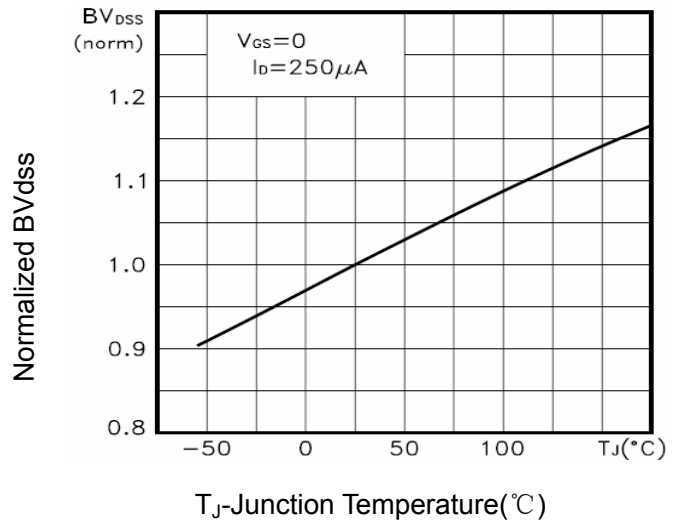
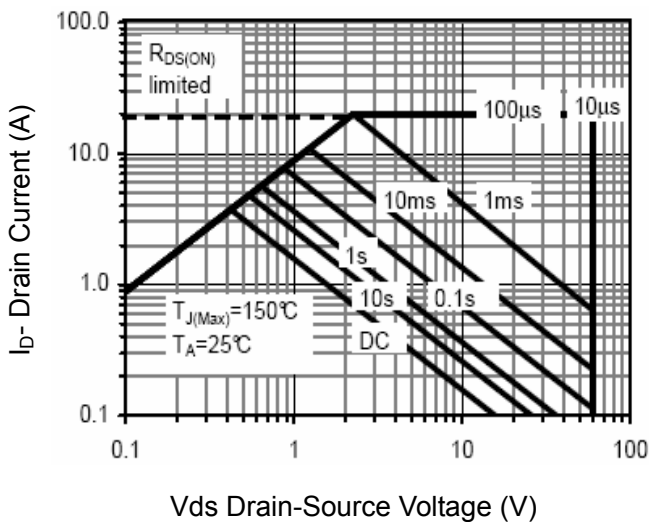

Figure 9 BV<sub>DSS</sub> vs Junction Temperature


Figure 8 Safe Operation Area

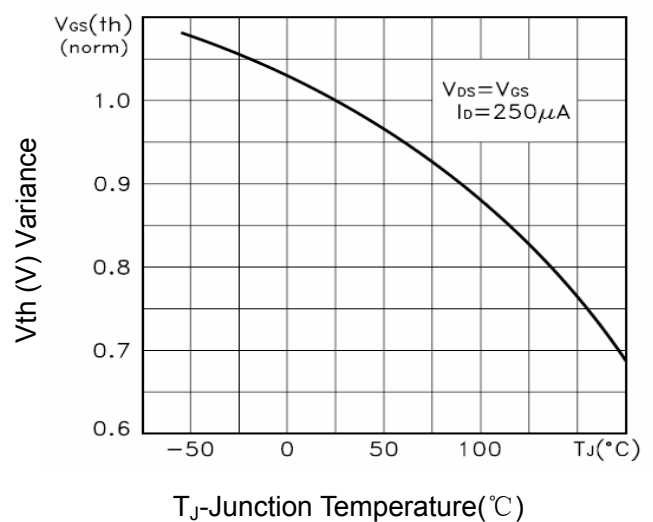
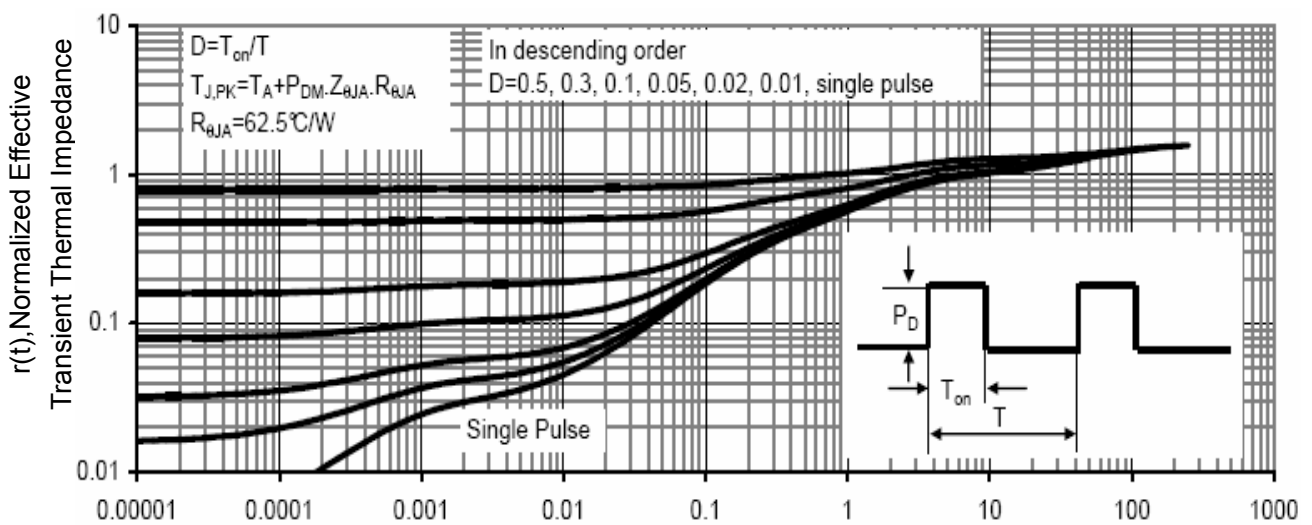
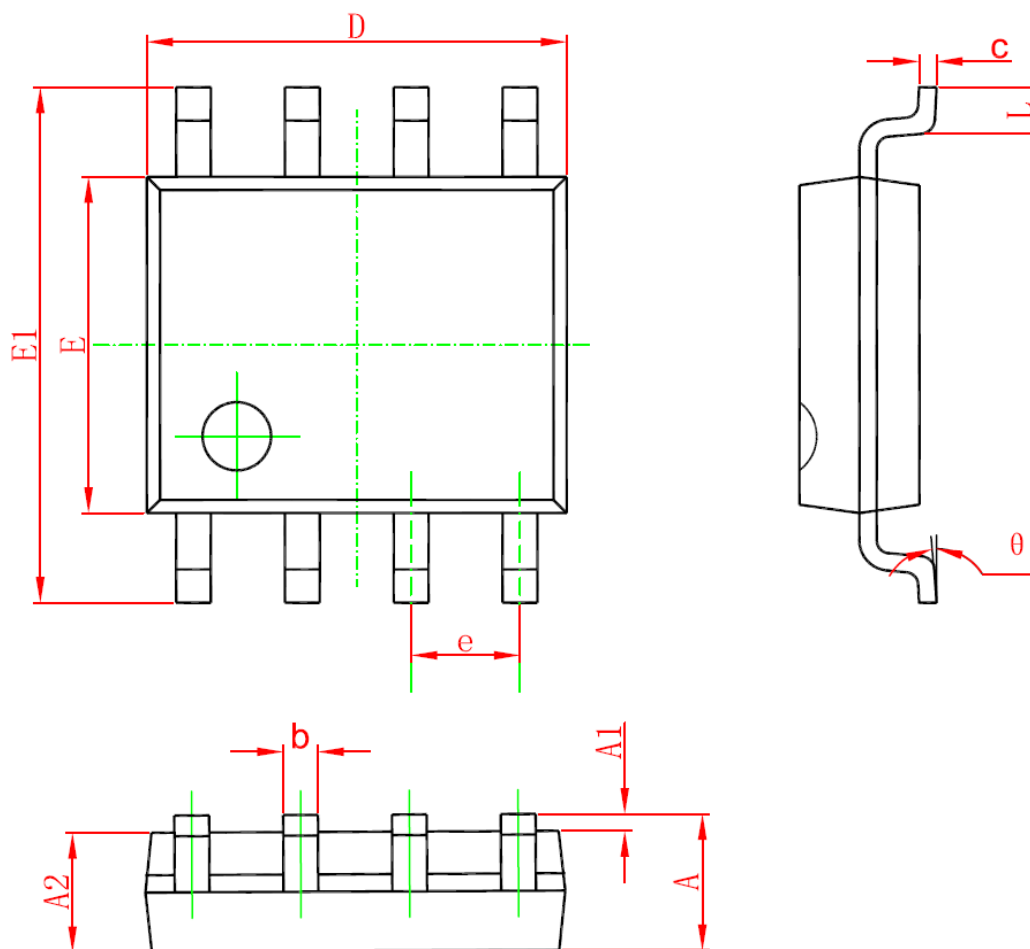

Figure 10 V<sub>GS(th)</sub> vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance

## SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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