1. GENERAL DESCRIPTION

The NAU8811 is a cost effective and low power wideband MONO audio CODEC. It is designed for voice telephony related applications. Functions include Automatic Level Control (ALC) with noise gate, PGA, standard audio interface I^2S, and PCM with time slot assignment. The device provides one differential microphone input and one single ended auxiliary input (multi purpose). There are few variable gain control stages in the audio path. It also includes Headphone (Headphone) line output and integrated BTL speaker driver.

The analog inputs have PGA on the front end, allowing dynamic range optimization with a wide range of input sources. The microphone amplifiers have a programmable gain from -12dB to +35.25dB to handle both amplified microphones. In addition to a digital high pass filter to remove DC offset voltages, the ADC also features voice band digital filtering. Voice-band data is accepted by the audio interface (I^2S). The DAC converter path includes filtering and mixing, programmable-gain amplifiers (PGA), and soft muting. The digital interface SPI have independent supply voltage to allow integration into multiple supply systems. The NAU8811 operates at supply voltages from 2.5V to 3.6V, although the digital core can operate at voltage as low as 1.71V to save power.

The NAU8811 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

2. FEATURES

24-bit signal processing linear Audio CODEC
- Audio DAC: 93dB SNR and -84dB THD
- Audio ADC: 91dB SNR and -79dB THD
- Support variable sample rates from 8 - 48kHz
- Integrated BTL Speaker Driver 1W (8Ω / 5V)
- Integrated Headset Driver 40mW (16Ω / 3.3V)

Analog I/O
- Integrated programmable Microphone Amplifier
- Integrated Line Input and Line Output
- Integrated Audio Switches
- Headphone / Speaker / Line Output selection
- Microphone / Line Inputs selection

Interfaces
- I^2S digital interface PCM time slot assignment
- SPI serial control Interface

Low Power, Low Voltage

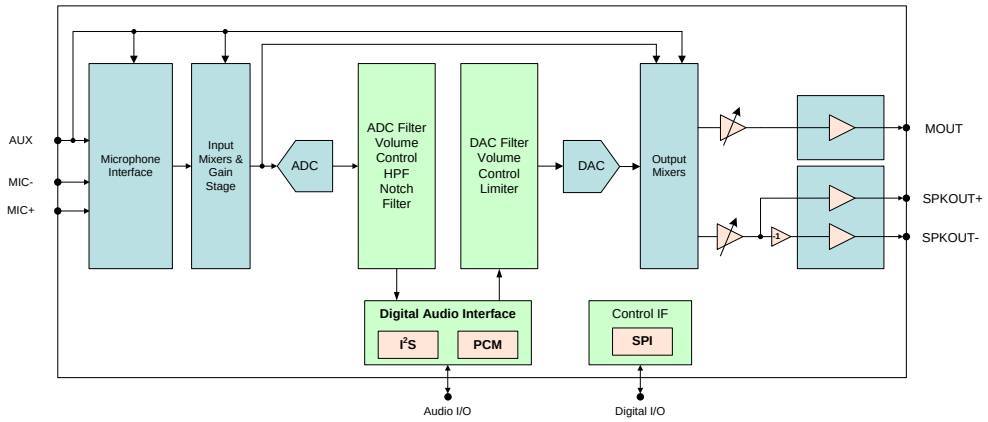
- Analog Supply: 2.5V to 3.6V
- Digital Supply: 1.71V to 3.6V
- Nominal Operating Voltage: 3.3V

Additional features

- Programmable ALC and ADC Notch Filter
- Programmable High Pass Filter
- Digital D/A Passthrough
- AEC-Q100 & TS16949 compliant device available upon request
- Industrial temperature: range: –40°C to +85°C

Applications

- VoIP Telephones
- IP PBX
- Mobile Telephone Hands-free Kits
- Residential & Consumer Intercoms
- General Purpose low power audio CODEC



3. PIN CONFIGURATION

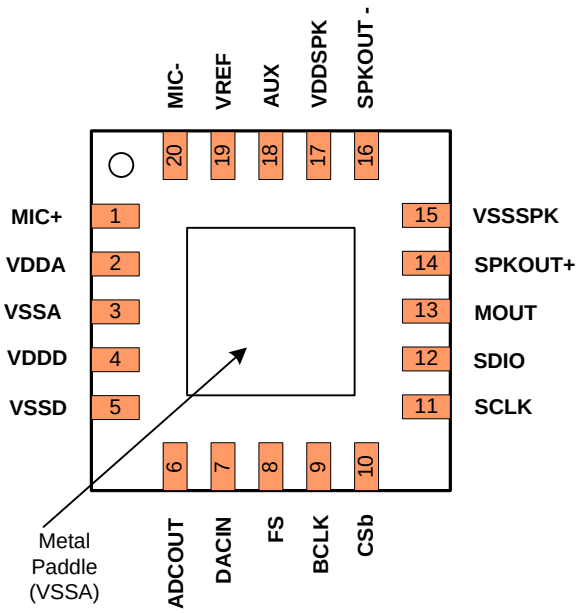


Figure 1: 20-Pin QFN Package

4. PIN DESCRIPTION

Pin Name	Pin#	Functionality	A/D	Pin Type
MIC+	1	Microphone Positive Input	A	I
VDDA	2	Analog Supply	A	I
VSSA	3	Analog Ground	A	O
VDDD	4	Digital Supply	D	I
VSSD	5	Digital Ground	D	O
ADCOUT	6	Digital Audio Data Output	D	O
DACIN	7	Digital Audio Data Input	D	I
FS	8	Frame Sync (Slave)	D	I/O
BCLK	9	Bit Clock (Slave)	D	I
CSb	10	SPI Chip Select	D	I/O
SCLK	11	SPI Serial Clock	D	I
SDIO	12	SPI Data In	D	O
MOUT	13	Headphone Output	A	O
SPKOUT+	14	Speaker Positive Output	A	O
VSSSPK	15	Speaker Ground	A	O
SPKOUT-	16	Speaker Negative Output	A	O
VDDSPK	17	Speaker Supply	A	I
AUX	18	Auxiliary Input	A	I
VREF	19	Decoupling internal analog mid supply reference voltage	A	O
MIC-	20	Microphone Negative Input	A	I
PADDLE_VSSA	PKG	The exposed metal paddle on the bottom of the IC supplies circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the IC.	A	O

Table 1: Pin Description

Notes

1. The 20-QFN package includes a bulk ground connection pad on the underside of the chip. This bulk ground should be thermally tied to the PCB, and electrically tied to the analog ground.
2. Unused analog input pins should be left as no-connection.
3. Under all condition when digital pins are not used they should be tied to ground.

5. BLOCK DIAGRAM

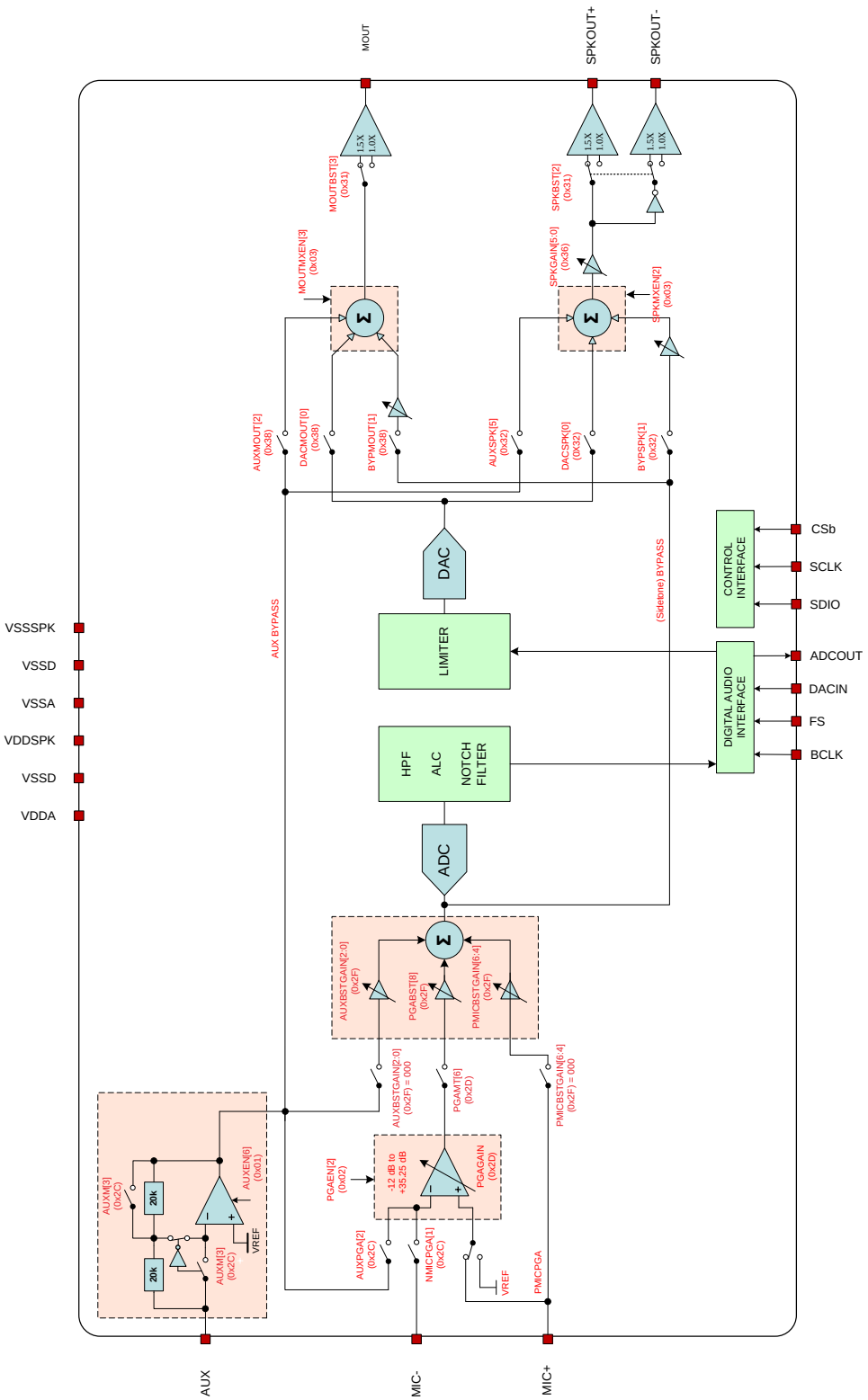


Figure 2: NAU8811 General Block Diagram

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9. ABSOLUTE MAXIMUM RATINGS

CONDITION		MIN	MAX	Units
VDDA supply voltage		-0.3	+3.63	V
VDDSPK supply voltage	MOUTBST=0, SPKBST=0	-0.3	+3.63	V
	MOUTBST=1, SPKBST=1	-0.3	+5.50	V
Digital Input Voltage range		VSSD – 0.3	VDDD + 0.30	V
Analog Input Voltage range		VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature		-40	+85	^{0}C
Storage temperature range		-65	+150	^{0}C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

10. OPERATING CONDITIONS

Condition	Symbol	Min Value	Typical Value	Max Value	Units
Analogue supplies range	VDDA	2.50		3.60	V
Digital supply range	VDDD	1.71		3.60	V
Speaker supply	VDDSPK	2.50		5.50	V
Ground	VSSD, VSSA, VSSSPK		0		V

1. VDDA must be ≥ VDDD

11. ELECTRICAL CHARACTERISTICS

VDDD = 1.8V, VDDA = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		V_{RMS} dBV
Signal to Noise Ratio [2]	SNR	Gain = 0dB, A-weighted	87	91		dB
Total Harmonic Distortion [3]	THD	Input = -1dBFS, Gain = 0dB		-79	-65	dB
Digital to Analogue Converter (DAC) to Headphone output (all data measured with 10kΩ / 50pF load)						
Full Scale output signal [1]		MOUTBST=0		1.0x (V_{REF})		V_{RMS}
		MOUTBST=1		1.5 x V_{REF}		
Signal to Noise Ratio [2]	SNR	A-weighted (ADC/DAC oversampling rate of 128)	90	93		dB
Total Harmonic Distortion [3]	THD	R_L = 10 kΩ; -1.5dBfs		-84	-70	dB
Auxiliary Analogue Input (AUX)						
Full-scale Input Signal Level [1]	V_{INFS}	Gain = 0dB		1 0		V_{RMS} dBV
Input Resistance	R_{AUX}	AUXM=0		20		kΩ
Input Capacitance	C_{AUX}			10		pF
Microphone Inputs (MICN & MICP) and MIC Input Programmable Gain Amplifier (PGA)						
Full-scale Input Signal Level [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1 0		V_{RMS} dBV
Programmable PGA gain			-12		35.25	dB
PGA Step Size		Guaranteed Monotonic		0.75		dB
Programmable Boost PGA gain		PGABST = 0		0		dB
		PGABST = 1		20		
Mute Attenuation				100		dB
PGA equivalent output noise		0 to 20kHz, Gain set to 35.25dB		110		µV
Auxiliary Input resistance	R_{AUX}	PGA Gain = 35.25dB		1.6		kΩ
		PGA Gain = 0dB		47		kΩ
		PGA Gain = -12dB		75		kΩ
Positive Microphone Input resistance	R_{MIC+}	PMICPGA = 1		94		kΩ
Input Capacitance	C_{MIC}			10		pF
Speaker Output PGA						
Programmable Gain			-57		6	dB
Programmable Gain Step Size		Guaranteed Monotonic		1		dB

VDDD = 1.8V, VDDA = VDDSPK = 3.3V (VDDSPK = 1.5*VDDA when Boost), T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
BTL Speaker Output (SPKOUT+, SPKOUT- with 8Ω bridge tied load)								
Full scale output [7]		SPKBST = 0 VDDSPK = VDDA				VDDA / 3.3		V_{RMS}
		SPKBST = 1 VDDSPK = 1.5 * VDDA				(VDDA / 3.3) * 1.5		
Output Power	PO	Output power is very closely correlated with THD						
Signal to Noise Ratio	SNR	VDDSPK=3.3V RL = 8Ω				90		dB
		VDDSPK =1.5*VDDA RL = 8Ω				90		dB
Total Harmonic Distortion	THD	PO =180mW	RL = 8Ω	VDDSPK=3.3V		-63		dB
		PO =400mW				-56		dB
		PO =360mW		VDDSPK = 1.5*VDDA		-60		dB
		PO =800mW				-61		dB
		PO =1W				-34		dB
Power Supply Rejection Ratio (50Hz - 22kHz)	PSRR	VDDSPK = 1.5*VDDA (boost)				50		dB
		VDDSPK = 3V (non-boost)				50		dB
Headphone' output (SPKOUTP, SPKOUTN with resistive load to ground)								
Full scale output [7]						VDDA / 3.3		V_{RMS}
Signal to Noise Ratio	SNR	A-weighted				90		dB
Total Harmonic Distortion	THD	Po=20mW, RL = 16Ω, VDDSPK = 3.3V				-84		dB
		Po=20mW, RL = 32Ω, VDDSPK = 3.3V				-85		dB
Automatic Level Control (ALC)/Limiter – ADC only								
Target Record Level					-28.5		-6	dB
Programmable Gain					-12		35.25	dB
Programmable Gain Step Size		Guaranteed Monotonic				0.75		dB
Gain Hold Time [4, 6]	tHOLD	BCLK=12.288MHz			0 / 2.67 / …/ 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time [5, 6]	tDCY	ALC Mode ALCM=0 BCLK=12.288MHz			3.3 / 6.6 / 13.1 / … / 3360 (time doubles every step)			ms
		Limiter Mode ALCM=1 BCLK=12.288MHz			0.73 / 1.45 / 2.91 / … / 744 (time doubles every step)			ms
Gain Ramp-Down (Attack) Time [5, 6]	tATK	ALC Mode ALCM=0 BCLK=12.288MHz			0.83 / 1.66 / 3.33 / … / 852 (time doubles every step)			ms
		Limiter Mode ALCM=1 BCLK=12.288MHz			0.18 / 0.36 / 0.73 / … / 186 (time doubles every step)			ms
Digital Input / Output								

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input HIGH Level	V_{IH}		0.7 × VDDD			V
Input LOW Level	V_{IL}				0.3 × VDDD	V
Output HIGH Level	V_{OH}	I_{OL} = 1mA	0.9 × VDDD			V
Output LOW Level	V_{OL}	I_{OH} = -1mA			0.1 x VDDD	V

Notes

1. Full Scale is relative to VDDA (FS = VDDA/3.3.) Input level to RIP and LIP is limited to a maximum of -3dB so that THD+N performance will not be reduced.
2. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full-scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
3. THD+N (dB) – THD+N are a ratio, of the RMS values, of (Noise + Distortion)/Signal.
4. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
5. Ramp-up and Ramp-Down times are defined as the time it takes to change the PGA gain by 6dB of its gain range.
6. All hold, ramp-up and ramp-down times scale proportionally with BCLK
7. The maximum output voltage can be limited by the speaker power supply. If MOUTBST or SPKBST is set then VDDSPK should be 1.5xVDDA to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).

12. FUNCTIONAL DESCRIPTION

The NAU8811 is a MONO Audio CODEC with very robust ADC and DAC. The device provides one single ended auxiliary input (AUX pin) and one differential microphone input (MIC- & MIC+ pins). The auxiliary input (AUX) can be configured to sum multiple signals into a single input. It has three different amplification paths with a total gain of up to +55.25dB. The differential input also has amplification paths similar to auxiliary input.

The PGA output has programmable ADC gain. An advanced Sigma Delta DAC is used along with digital decimation and interpolation filters to give high quality audio at sample rates from 8 kHz to 48 kHz. The Digital Filter blocks include ADC high pass filters, and Notch filter. The device has two output mixers, one for Headphone output and the other for the speaker output. It also has one input mixer.

The NAU8811 has serial control interface SPI for device control. The device also supports I^2S, PCM time slotting, Left Justified and Right Justified for audio interface and can only operate in slave only. It can operate with sample rates ranging from 8 kHz to 48 kHz, depending on the values of BCLK and its prescaler. The power control registers help save power by controlling the major individual functional blocks of the NAU8811.

12.1. INPUT PATH

The NAU8811 has two different types of microphone inputs single ended and differential. Figure 3 shows the different paths that the input signals can take.

All inputs are maintained at a DC bias at approximately half of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

12.1.1. The Single Ended Auxiliary Input (AUX)

The single ended auxiliary input (AUX) has three different paths to Headphone output (MOUT).

- Directly connected to the Headphone Mixer or Speaker Mixer to MOUT or SPKOUT+ and SPKOUT- respectively
- Connect through the PGA Boost Mixer which has a range of -12dB to +6dB
- Connect through both the input PGA Gain (range of -12dB to +35.25 dB) and PGA Boost Mixer (range of 0db or +20dB)

The last two paths above go through the ADC filters where the ALC loop controls the amplitude of the input signal. The device also has an internal configurable biasing circuit for biasing the microphone, reducing external components.

An internal inverting operational amplifier circuit allows the auxiliary input pin to connect multiple signals for mixing. This can be achieved by setting AUXM[3] address (0x2C) to LOW. The combination of the 20k ohm resistors can vary due to process variation in the gain stage. The block can also be configured to be used as a buffer by

setting AUXM[3] address (0x2C) to HIGH. The internal inverting circuit block can be enable/disable by setting AUXEN[6] address (0x01).

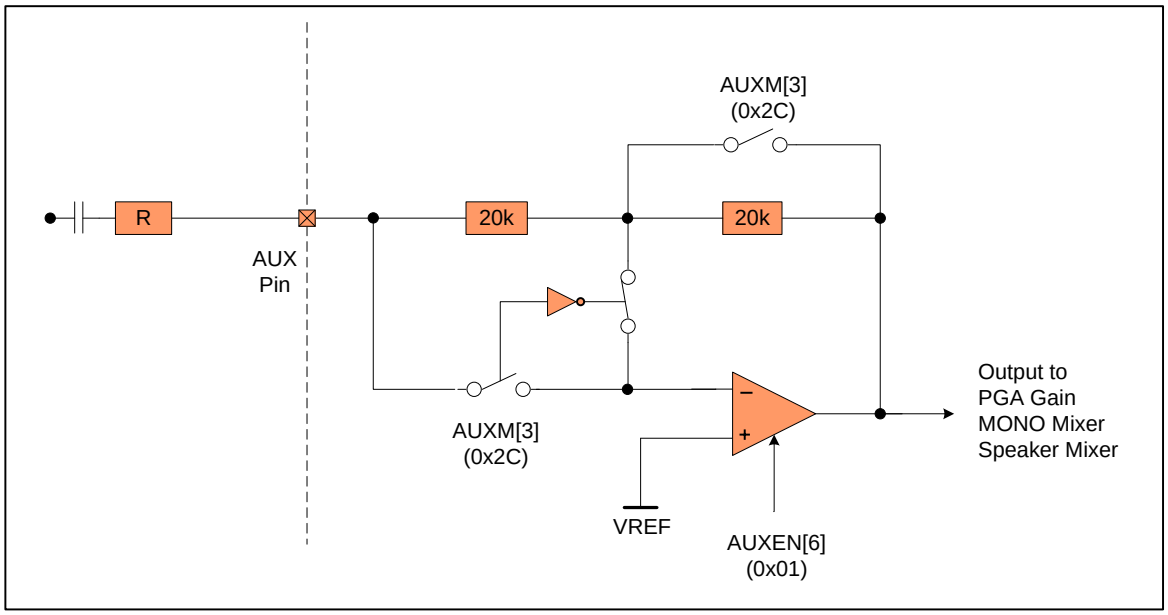


Figure 3: Auxiliary Input Circuit Block Diagram with AUXM[3] = 0

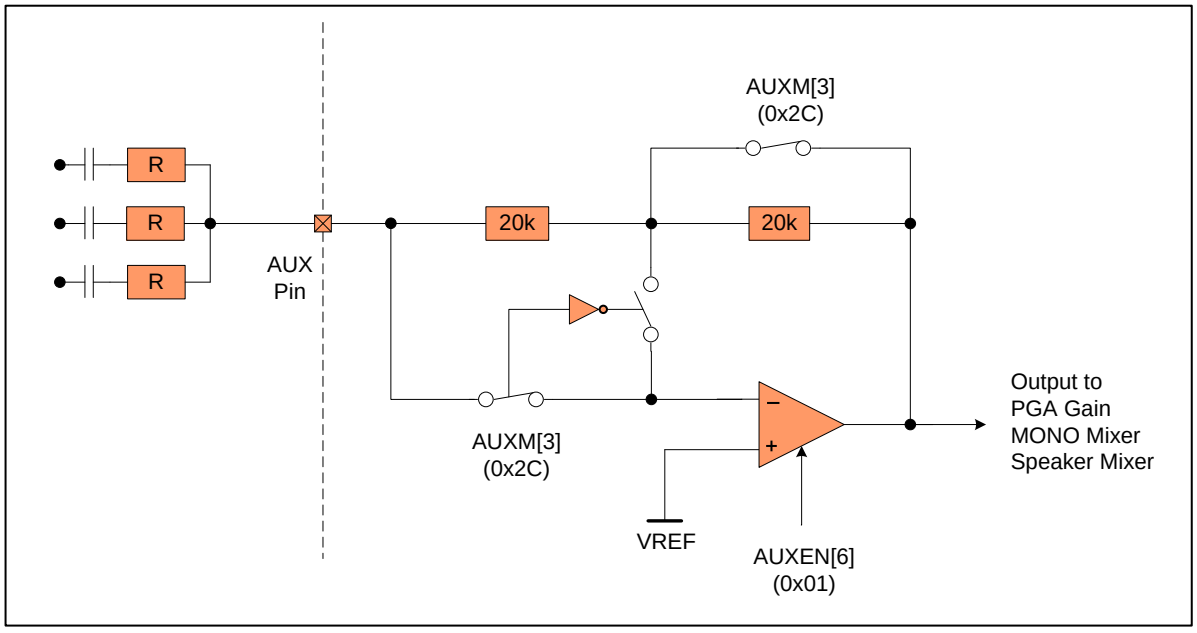


Figure 4: Auxiliary Input Circuit Block Diagram with AUXM[3] = 1

12.1.2. The differential microphone input (MIC- & MIC+ pins)

The NAU8811 features a low-noise, high common mode rejection ratio (CMRR), differential microphone inputs (MIC- & MIC+ pins) which are connected to a PGA Gain stage. The differential input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as notebooks and PDAs. When properly employed, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

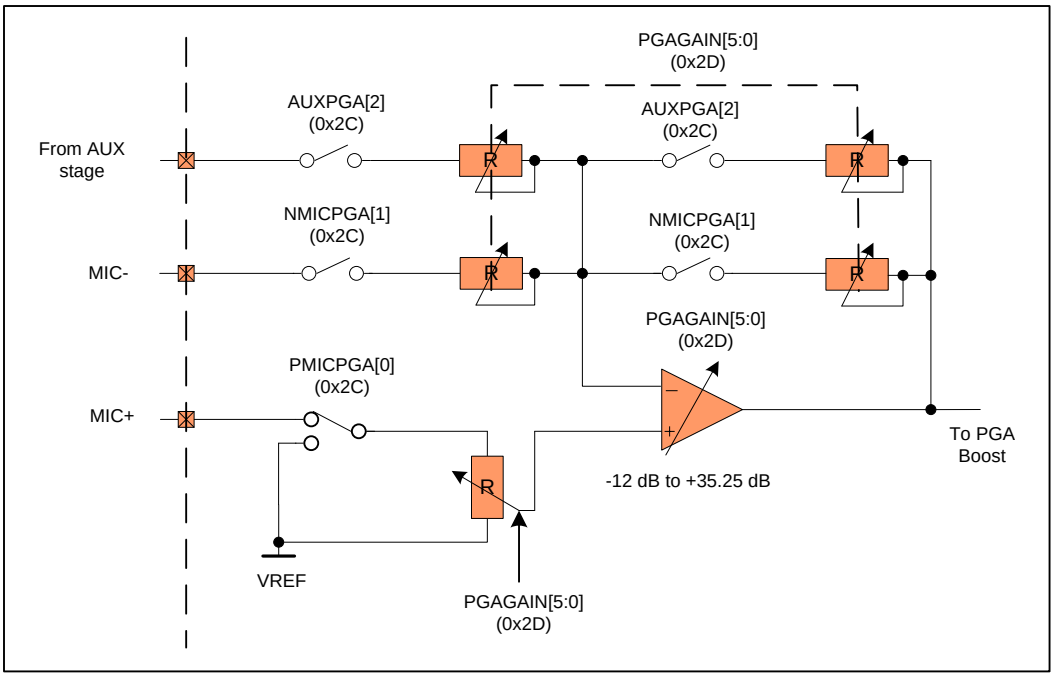


Figure 5: Input PGA Circuit Block Diagram

Bit(s)	Addr	Parameter	Programmable Range
PMICPGA[0]	0x2C	Positive Microphone to PGA	0 = Input PGA Positive terminal to VREF 1 = Input PGA Positive terminal to MICP
NMICPGA[1]	0x2C	Negative Microphone to PGA	0 = MICN not connected to input PGA 1 = MICN to input PGA Negative terminal.

Table 2: Register associated with Input PGA Control

12.1.2.1. Positive Microphone Input (MIC+)

The positive microphone input (MIC+) can be used as part of the differential input. It connects to the positive terminal of the PGA gain amplifier by setting PMICPGA[0] address (0x2C) to HIGH or can be connected to VREF by setting PMICPGA[0] address (0x2C) to LOW.

When the associated control bit is set logic = 1, the MIC+ pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MIC+ pin close to VREF at all times.

Note: In single ended applications where the MIC+ input is used without using MIC-, the PGA gain values will be valid only if the MIC- pin is terminated to a low impedance signal point. This termination should normally be an AC coupled path to signal ground. This input impedance is constant regardless of the gain value. The following table gives the nominal input impedance for this input. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

MIC+ to non-inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
-12	94
-9	94
-6	94
-3	94
0	94
3	94
6	94
9	94
12	94
18	94
30	94
35.25	94

Table 3: Microphone Non-Inverting Input Impedances

MIC- to inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
-12	75
-9	69
-6	63
-3	55
0	47
3	39
6	31
9	25
12	19
18	11
30	2.9
35.25	1.6

Table 4: Microphone Inverting Input Impedances

12.1.2.2. Negative Microphone Input (MIC-)

The negative microphone input (MIC-) has two distinctive configuration; differential input or single ended input. This input connects to the negative terminal of the PGA gain amplifier by setting NMICPGA[1] address (0x2C) to HIGH. When the MIC- is used as a single ended input, MIC+ should be conned to VREF by setting PMICPGA[0] address (0x2C) bit to LOW. The AUX input signal can also be mixed with the MIC- input signal by setting AUXPGA[2] address (0x2C) to HIGH.

When the associated control bit is set logic = 1, the MIC- pin is connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC

level of the MIC- pin close to VREF at all times. It is important for a system designer to know that the MIC-input impedance varies as a function of the selected PGA gain. This is normal and expected for a difference amplifier type topology. The above table gives the nominal resistive impedance values for this input over the possible gain range. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values.

12.1.2.3. PGA Gain Control

The PGA amplification is common to all three input pins MIC-, MIC+, AUX, and enabled by PGAEN[2] address (0x02). It has a range of -12dB to +35.25dB in 0.75dB steps, controlled by PGAGAIN[5:0] address (0x2D). Input PGA gain will not be used when ALC is enabled using ALCEN[8] address (0x20).

Addr	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x2D	0	PGAZC	PGAMT	PGAGAIN[5:0]						0x010
0x20	ALCEN	0	0	ALCMXGAIN[2:0]			ALCMNGAIN[2:0]			0x038

Table 5: Registers associated with ALC and Input PGA Gain Control

12.1.3. PGA Boost Stage

The boost stage has three inputs connected to the PGA Boost Mixer. All three inputs can be individually connected or disconnected from the PGA Boost Mixer. The boost stage can be enabled by setting BSTEN[4] address (0x02) to HIGH. The following figure shows the PGA Boost stage.

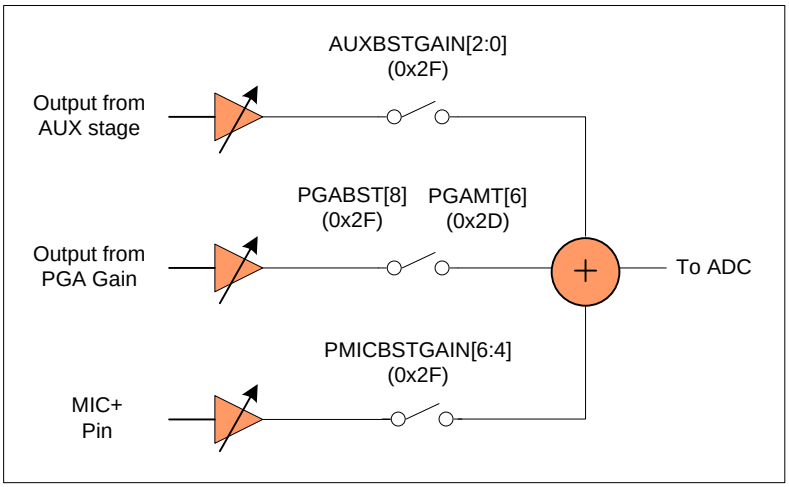


Figure 6: Boost Stage Block Diagram

The signal from AUX stage can be amplified at the PGA Boost stage before connecting to the Boost Mixer by setting a binary value from “001” – “111” to AUXBSTGAIN[2:0] address (0x2F). The path is disconnected by setting “000” to the AUXBSTGAIN bits.

Signal from PGA stage to the PGA Boost Mixer is disconnected or muted by setting PGAMT[6] address (0x2D) to HIGH. In this path the PGA boost can be a fixed value of +20dB or 0dB, controlled by the PGABST[8] address (0x2F) bit.

The signal from MIC+ pin to the PGA Boost Mixer is disconnected by setting ‘000’ binary value to PMICBSTGAIN[6:4] address (0x2F) and any other combination connects the path.

Bit(s)	Addr	Parameter	Programmable Range
BSTEN[4]	0x02	Enable PGA Boost Block	0 = Boost stage OFF 1 = Boost stage ON
PGAMT[6]	0x2D	Mute control for input PGA	0=Input PGA not muted 1=Input PGA muted
AUXBSTGAIN[2:0]	0x2F	Boost AUX signal	Range: -12dB to +6dB @ 3dB increment
PMICBSTGAIN[6:4]	0x2F	Boost MIC+ signal	Range: -12dB to +6dB @ 3dB increment
PGABST[8]	0x2F	Boost PGA stage	0 = PGA output has +0dB 1 = PGA output has +20dB

Table 6: Registers associated with PGA Boost Stage Control

12.2. ADC DIGITAL FILTER BLOCK

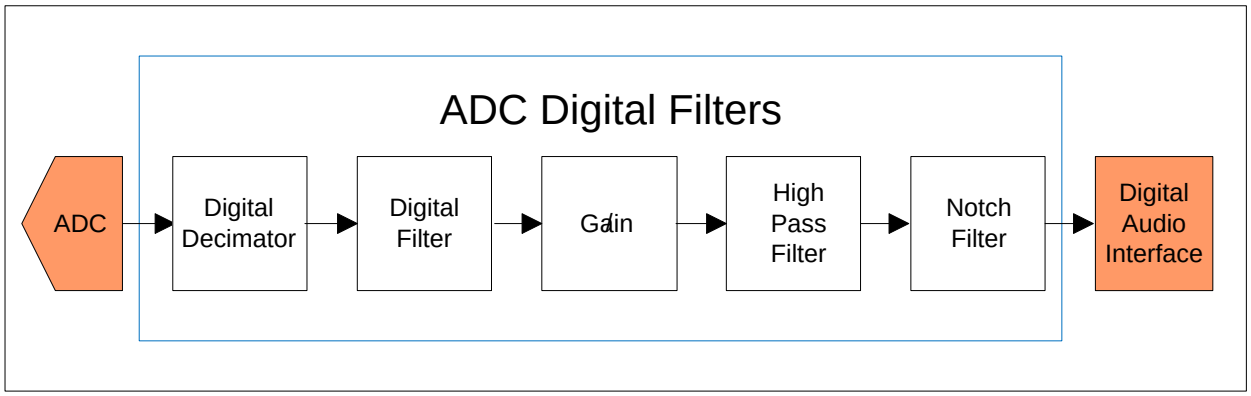


Figure 7: ADC Digital Filter Path Block Diagram

The ADC digital filter block performs a 24-bit signal processing. The block consists of an oversampled analog sigma-delta modulator, digital decimator, digital filter, high pass filter, and a notch filter. The oversampled analog sigma-delta modulator provides a bit stream to the decimation stages and filter. The ADC coding scheme is in twos-complement format and the full-scale input level is proportional to VDDA. With a 3.3V supply voltage, the full-scale level is $1.0V_{RMS}$ and any voltage greater than full scale may overload the ADC and cause distortion. The ADC is enabled by setting ADCEN[0] address (0x02) bit. Polarity and oversampling rate of the ADC output signal can be changed by ADCPL[0] address (0x0E) and ADCOS[3] address (0x0E) respectively.

Bit(s)	Addr	Parameter	Programmable Range
ADCPL[0]	0x0E	ADC Polarity	0 = Normal 1 = Inverted
ADCOS[3]	0x0E	ADC Over SampleRate	0=64x (Lowest power) 1=128x (best SNR at typical condition)
HPFEN[8]	0x0E	High Pass Filter Enable	0 = Disable 1 = Enable
HPFAM[7]	0x0E	Audio or Application Mode	0 = Audio (1^{st} order, fc ~ 3.7 Hz) 1 = Application (2^{nd} order, fc = HPF)
HPF[6:4]	0x0E	High Pass Filter frequencies	82 Hz to 612 Hz dependant on the sample rate
ADCEN[0]	0x02	Enable ADC	0 = Disable 1 = Enable
SMPLR[3:1]	0x07	Sample rate	8k Hz to 48 kHz

Table 7: Register associated with ADC

12.2.1. Programmable High Pass Filter (HPF)

The high pass filter (HPF) has two different modes that it can operate in either Audio or Application mode HPFAM[7] address (0x0E). In Audio Mode (HPFAM=0) the filter is first order, with a cut-off frequency of 3.7 Hz. In Application mode (HPFAM=1) the filter is second order, with a cut-off frequency selectable via the HPF[2:0] register bits. Cut-off frequency of the HPF depends on sample frequency selected by SMPLR[3:1] address (0x07). The HPF is enabled by setting HPFEN[8] address (0x0E) to HIGH. Table below shows the cut-off frequencies with different sampling rate.

HPF[2:0]	fs (kHz)								
	SMPLR=101/100			SMPLR=011/010			SMPLR=001/000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	156	131	180	156	131	180	156
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 8: High Pass Filter Cut-off Frequencies (HPFAM=1)

12.2.2. Programmable Notch Filter (NF)

The NAU8811 has a programmable notch filter where it passes all frequencies except those in a stop band centered on a given center frequency. The filter gives lower distortion and flattens response. The notch filter is enabled by setting NFCEN[7] address (0x1B) to HIGH. The variable center frequency is programmed by setting two's complement values to NFCA0[6:0] address (0x1C), NFCA0[13:7] address (0x1B) and NFCA1[6:0] address (0x1E), NFCA1[13:7] address (0x1D) registers. The coefficients are updated in the circuit when the NFCU[8] bit is set HIGH in a write to any of the registers NF1-NF4 address (0x1B, 0x1C, 0x1D, 0x1E).

Addr	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x1B	NFCU	NFCEN	NFCA0[13:7]							0x000
0x1C	NFCU	0	NFCA0[6:0]							0x000
0x1D	NFCU	0	NFCA1[13:7]							0x000
0x1E	NFCU	0	NFCA1[6:0]							0x000

Table 9: Registers associated with Notch Filter Function

	A_0	A_1	Notation	Register Value (DEC)
Coefficient	$\frac{1-\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}{1+\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}$	$-\left(1+A_0\right)\ x\ \cos\left(\frac{2\ \pi\ f_c}{f_s}\right)$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) fs = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ (then convert to 2's complement)

Table 10: Equations to Calculate Notch Filter Coefficients

12.2.3. Digital ADC Gain Control

The digital ADC can be muted by setting "0000 0000" to ADCGAIN[7:0] address (0x0F). Any other combination digitally attenuates the ADC output signal in the range -127dB to 0dB in 0.5dB increments].

Addr	Name	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x0F	**ADCG**	0	ADCGAIN								**0x0FF**

Table 11: Register associated with ADC Gain

12.3. PROGRAMMABLE GAIN AMPLIFIER (PGA)

NAU8811 has a programmable gain amplifier (PGA) which controls the gain such that the signal level of the PGA remains substantially constant as the input signal level varies within a specified dynamic range. The PGA has two functions

- Automatic level control (ALC) or
- Input peak limiter

The Automatic Level Control (ALC) seeks to control the PGA gain in response to the amplitude of the input signal such that the PGA output maintains a constant envelope. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level ALCSL[3:0] address (0x21). Note: When the ALC automatic level control is enabled, the function of the ALC is to automatically adjust PGAGAIN[5:0] address (0x2D) volume setting.

12.3.1. Automatic level control (ALC)

The ALC seeks to control the PGA gain such that the PGA output maintains a constant envelope. This helps to prevent clipping at the input of the sigma delta ADC while maximizing the full dynamic range of the ADC. The ALC monitors the output of the ADC, measured after the digital decimator has converted it to 1.23 fixed-point formats. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope.

Based on a comparison between the measured peak value and the target value, the ALC block adjusts the gain control, which is fed back to the PGA.

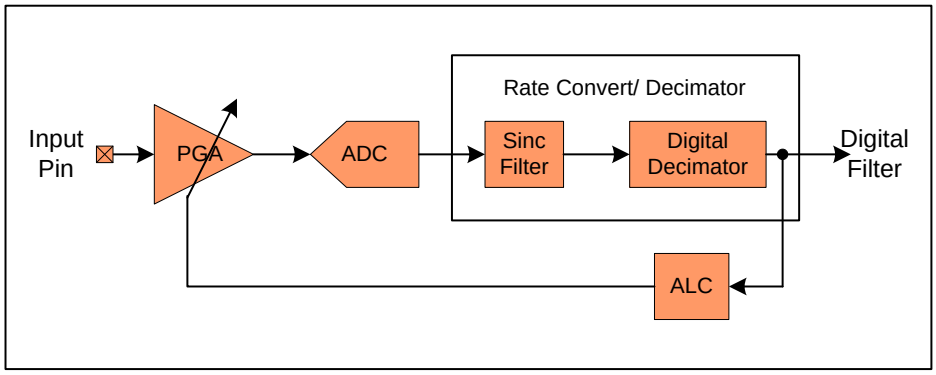


Figure 8: ALC Block Diagram

The ALC is enabled by setting ALCEN[8] address (0x20) bit to HIGH. The ALC has two functional modes, which is set by ALCM[8] address (0x22).

- Normal mode (ALCM = LOW)
- Peak Limiter mode (ALCM = HIGH)

When the ALC is disabled, the input PGA will immediately change to the value stored in PGAGAIN [5:0] address (0x2D). If it is desired that the PGA Gain match the last controlled value of the ALC, it is necessary to read the ALC gain in-use and explicitly write this gain into PGAGAIN [5:0] immediately before disabling the ALC. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level ALCSL[3:0] address (0x21).

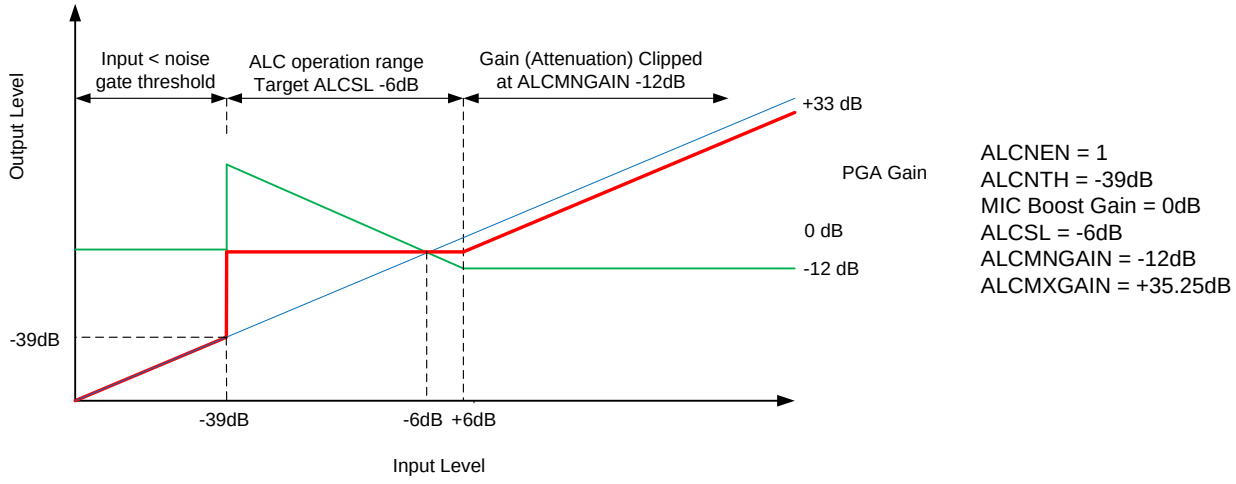


Figure 9: ALC Response Graph

The registers listed in the following section allow configuration of ALC operation with respect to:

- ALC target level
- Gain increment and decrement rates
- Minimum and maximum PGA gain values for ALC operating range
- Hold time before gain increments in response to input signal
- Inhibition of gain increment during noise inputs
- Limiter mode operation

Bit(s)	Addr	Parameter	Programmable Range
ALCMNGAIN[2:0]	0x20	Minimum Gain of PGA	Range: -12dB to +30dB @ 6dB increment
ALCMXGAIN[2:0]		Maximum Gain of PGA	Range: -6.75dB to +35.25dB @ 6dB increment
ALCEN[8]		Enable ALC function	0 = Disable 1 = Enable
ALCSL[3:0]	0x21	ALC Target	Range: -28.5dB to -6dB @ 1.5dB increment
ALCHT[3:0]		ALC Hold Time	Range: 0ms to 1s, time doubles with every step)
ALCZC[8]		ALC Zero Crossing	0 = Disable 1 = Enable
ALCATK[3:0]	0x22	ALC Attack time	ALCM=0 – Range: 125us to 128ms ALCM=1 – Range: 31us to 32ms (time doubles with every step)
ALCDCY[3:0]		ALC Decay time	ALCM=0 – Range: 500us to 512ms ALCM=1 – Range: 125us to 128ms (Both ALC time doubles with every step)
ALCM[8]		ALC Select	0 = ALC mode 1 = Limiter mode

Table 12: Registers associated with ALC Control

The operating range of the ALC is set by ALCMXGAIN[5:3] address (0x20) and ALCMNGAIN[2:0] address (0x20) bits such that the PGA gain generated by the ALC is between the programmed minimum and maximum levels. When the ALC is enabled, the PGA gain is disabled.

In Normal mode, the ALCMXGAIN bits set the maximum level for the PGA in the ALC mode but in the Limiter mode ALCMXGAIN has no effect because the maximum level is set by the initial PGA gain setting upon enabling of the ALC.

ALCMAXGAIN	Maximum Gain (dB)
111	35.25
110	29.25
ALC Max Gain Range 35.25dB to -6dB @ 6dB increments	
001	-0.75
000	-6.75

ALCMINGAIN	Minimum Gain (dB)
000	-12
001	-6
ALC Min Gain Range -12dB to 30dB @ 6dB increments	
110	24
111	30

Table 13: ALC Maximum and Minimum Gain Values

12.3.2. Normal Mode

Normal mode is selected when ALCM[8] address (0x22) is set LOW and the ALC is enabled by setting ALCEN[8] address (0x20) HIGH. This block adjusts the PGA gain setting up and down in response to the input level. A peak detector circuit measures the envelope of the input signal and compares it to the target level set by ALCSL[3:0] address (0x21). The ALC increases the gain when the measured envelope is greater than the target and decreases the gain when the measured envelope is less than – 1.5dB. The following waveform illustrates the behavior of the ALC.

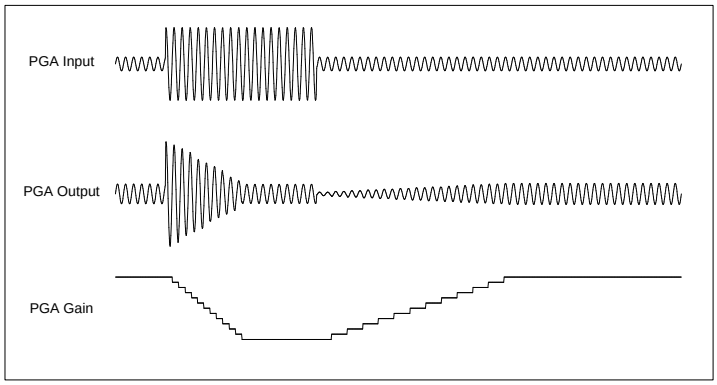


Figure 10: ALC Normal Mode Operation

12.3.3. ALC Hold Time (Normal mode Only)

The hold parameter ALCHT[3:0] configures the time between detection of the input signal envelope being outside of the target range and the actual gain increase.

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimal performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings; having a shorter hold time, on the other hand, may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes. The waveform below shows the operation of the ALCHT parameter.

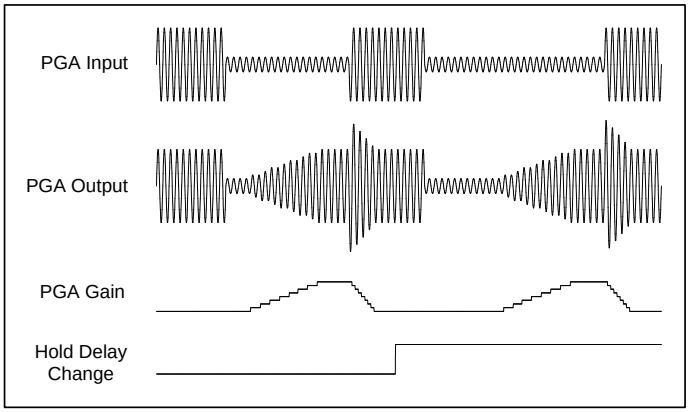


Figure 11: ALC Hold Time

12.3.4. Peak Limiter Mode

Peak Limiter mode is selected when ALCM[8] address (0x22) is set to HIGH and the ALC is enabled by setting ALCEN[8] address (0x20). In limiter mode, the PGA gain is constrained to be less than or equal to the gain setting at the time the limiter mode is enabled. In addition, attack and decay times are faster in limiter mode than in normal mode as indicated by the different lookup tables for these parameters for limiter mode. The following waveform illustrates the behavior of the ALC in Limiter mode in response to changes in various ALC parameters.

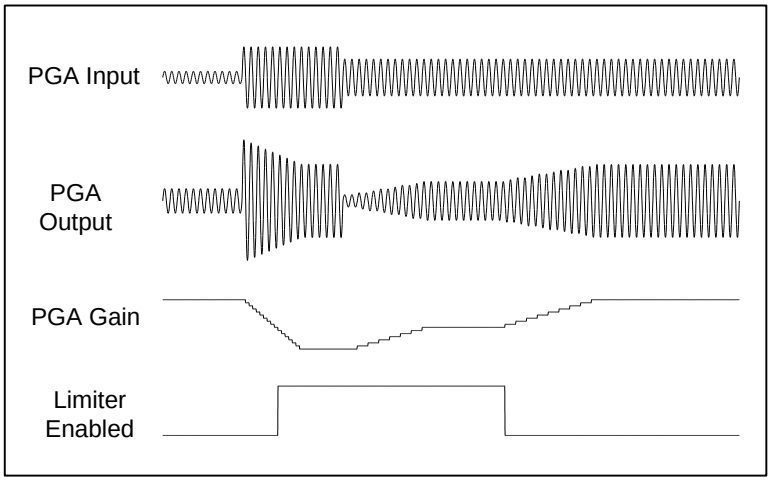


Figure 12: ALC Limiter Mode Operations

When the input signal exceeds 87.5% of full scale, the ALC block ramps down the PGA gain at the maximum attack rate (ALCATK=0000) regardless of the mode and attack rate settings until the ADC output level has been reduced below the threshold. This limits ADC clipping if there is a sudden increase in the input signal level.

12.3.5. Attack Time

When the absolute value of the ADC output exceeds the level set by the ALC threshold, ALCSL[3:0] address (0x21), attack mode is initiated at a rate controlled by the attack rate register ALCATK[3:0] address (0x22). The peak detector in the ALC block loads the ADC output value when the absolute value of the ADC output exceeds the current measured peak; otherwise, the peak decays towards zero, until a new peak has been identified. This sequence is continuously running. If the peak is ever below the target threshold, then there is no gain decrease at the next attack timer time; if it is ever above the target-1.5dB, then there is no gain increase at the next decay timer time.

12.3.6. Decay Times

The decay time ALCDCY[6:4] address (0x22) is the time constant used when the gain is increasing. In limiter mode, the time constants are faster than in ALC mode.

12.3.7. Noise gate (normal mode only)

A noise gate is used when there is no input signal or the noise level is below the noise gate threshold. The noise gate is enabled by setting ALCNEN[3] address (0x23) to HIGH. It does not remove noise from the signal. The noise gate threshold ALCNTH[2:0] address (0x23) is set to a desired level so when there is no signal or a very quiet signal (pause), which is composed mostly of noise, the ALC holds the gain constant instead of amplifying the signal towards the target threshold. The noise gate only operates in conjunction with the ALC and ONLY in Normal mode. The noise gate flag is asserted when

(Signal at ADC – PGA gain – MIC Boost gain) < ALCNTH (ALC Noise Gate Threshold) (dB)

Levels at the extremes of the range may cause inappropriate operation, so care should be taken when setting up the function.

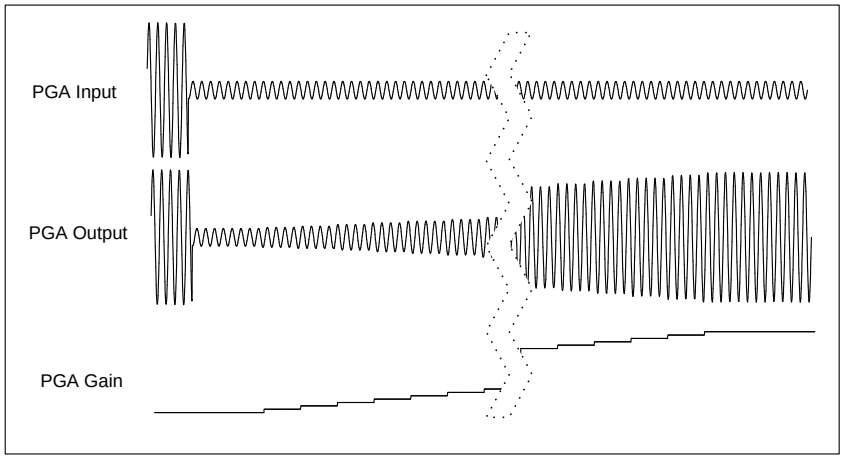


Figure 13: ALC Operation with Noise Gate disabled

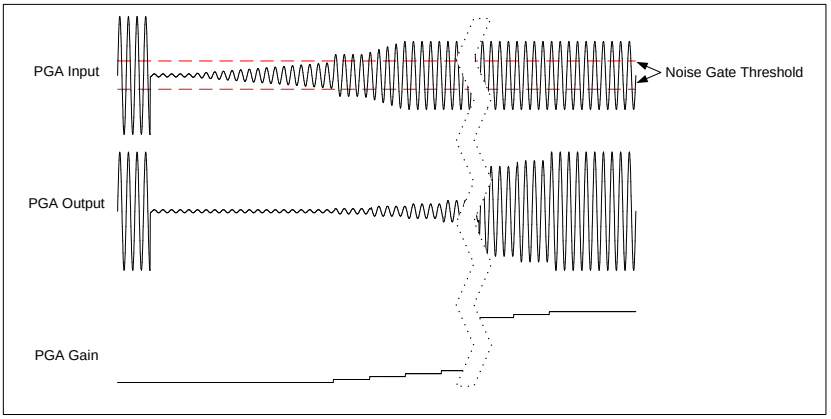


Figure 14: ALC Operation with Noise Gate Enabled

12.3.8. Zero Crossing

The PGA gain comes from either the ALC block when it is enabled or from the PGA gain register setting when the ALC is disabled. Zero crossing detection may be enabled to cause PGA gain changes to occur only at an input zero crossing. Enabling zero crossing detection limits clicks and pops that may occur if the gain changes while the input signal has a high volume.

There are two zero crossing detection enables:

- Register ALCZC[8] address (0x21) – is only relevant when the ALC is enabled.
- Register PGAZC[7] address (0x2D) – is only relevant when the ALC is disabled.

If the zero crossing function is enabled (using either register) and SCLKEN[0] address (0x07) is asserted, the zero cross timeout function may take effect. If the zero crossing flag does not change polarity within 0.25 seconds of a PGA gain update (either via ALC update or PGA gain register update), then the gain will update. This backup system prevents the gain from locking up if the input signal has a small swing and a DC offset that prevents the zero crossing flag from toggling.

12.4. DAC DIGITAL FILTER BLOCK

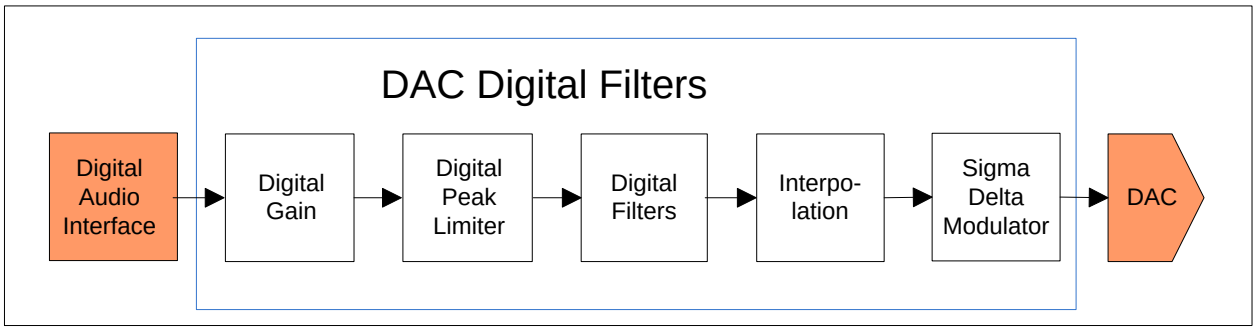


Figure 15: DAC Digital Filter Path

The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, high pass filter, digital gain/filters, de-emphasis, and analog mixers. The DAC coding scheme is in twos complement format and the full-scale output level is proportional to VDDA. With a 3.3V supply voltage, the full-scale output level is $1.0V_{RMS}$. The DAC is enabled by setting DACEN[0] address (0x03) bit HIGH.

Bit(s)	Addr	Parameter	Programmable Range
DACEN[0]	0x03	DAC enable	0 = Disable 1 = Enable
ADDAP[0]	0x05	Pass-through of ADC output data into DAC input	0 = Disable 1 = Enable
DACPL[0]	0x0A	DAC Polarity	0 = No Inversion 1 = DAC Output Inverted
AUTOMT[2]		Auto Mute	0 = Disable 1 = Enable
DEEMP[5:4]		Sample Rate	32 kHz, 44.1 kHz, and 48 kHz
DACMT[6]		Soft Mute	0 = Disable 1 = Enable
DACGAIN[7:0]	0x0B	DAC Volume Control	Range: -127dB to 0dB @ 0.5dB increment, 00 hex is Muted
DACLIMATK[3:0]	0x18	DAC Limiter Attack	Range: 68us to 139ms
DACLIMDCY[7:4]		DAC Limiter Decay	Range: 544us to 1.1s
DACLIMEN[8]		DAC Limiter Enable	0 = Disable 1 = Enable
DACLIMBST[3:0]	0x19	DAC Limiter Volume Boost	Range: 0dB to +12dB @ 1dB increment
DACLIMTHL[6:4]		DAC Limiter Threshold	Range: -6dB to -1bB @ 1dB increment

Table 14: Registers associated with DAC Gain Control

12.4.1. DAC Soft Mute

The NAU8811 also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. When removed, the gain will ramp back up to the digital gain setting. This function is disabled by default. This feature provides a tool that is useful for using the DACs without introducing pop and click sounds. To play back an audio signal, it must first be disabled by setting the DACMT[6] address (0x0A) bit to LOW.

12.4.2. DAC Auto Mute

The output of the DAC can be muted by the analog auto mute function. The auto mute function is enabled by setting AUTOMT[2] address (0x0A) to HIGH and applied to the DAC output when it sees 1024 consecutive zeros at its input.
If at any time there is a non-zero sample value, the DAC will be un-muted, and the 1024 count will be reinitialized to zero.

12.4.3. DAC Sampling / Oversampling rate, Polarity, DAC Volume control and Digital Pass-through

The sampling rate of the DAC is determined entirely by the frequency of its input clock and the oversampling rate setting. The oversampling rate of the DAC can be changed to 64x or 128x. In the 128x oversampling mode it gives an improved audio performance at slightly higher power consumption. Because the additional supply current is only 1mA, in most applications the 128x oversampling is preferred for maximum audio performance.
The polarity of the DAC output signal can be changed as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data are passed to other stages in the system.

The effective output audio volume of the DAC can be changed using the digital volume control feature. This processes the output of the DAC to scale the output by the amount indicated in the volume register setting. Included is a “digital mute” value which will completely mute the signal output of the DAC. The digital volume setting can range from 0dB through -127dB in 0.5dB steps.

Digital audio pass-through allows the output of the ADC to be directly sent to the DAC as the input signal to the DAC for DAC output. In this mode of operation, the external digital audio signal for the DAC will be ignored. The pass-through function is useful for many test and application purposes, and the DAC output may be utilized in any way that is normally supported for the DAC analog output signals.

12.4.4. Hi-Fi DAC De-Emphasis and Gain Control

The NAU8811 has Hi-Fi DAC gain control for signal conditioning. The level of attenuation for an eight-bit code X is given by: $0.5 \times (X-255)$ dB for $1 \le X \le 255$; MUTE for $X = 0$

It includes on-chip digital de-emphasis and is available for sample rates of 32 kHz, 44.1 kHz, and 48 kHz. The digital de-emphasis can be enabled by setting DEEMP[5:4] address (0x0A) bits depending on the input sample

rate. The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 μs pre-emphasis equalization as a means of noise reduction. The DAC output can be inverted (phase inversion) by setting DACPL[1:0] address (0x0A) to HIGH, non-inverted output is set by default.

12.4.5. Digital DAC Output Peak Limiter

Output Peak-Limiters reduce the dynamic range by ensuring the signal will not exceed a certain threshold, while maximizing the RMS of the resulted audio signal, and minimizing audible distortions. NAU8811 has a digital output limiter function. The operation of this is shown in figure below. In this diagram the upper graph shows the envelope of the input/output signals and the lower graph shows the gain characteristic. The limiter has a programmable threshold, DACLIMTHL[6:4] address (0x19), which ranges from -1dB to -6dB in 1dB increments. The digital peak limiter seeks to keep the envelope of the output signal within the target threshold +/- 0.5dB. The attack and decay rates programmed in registers DACLIMATK[3:0] address (0x18) and DACLIMDCY[7:4] address (0x18) specify how fast the digital peak limiter decrease and increase the gain, respectively, in response to the envelope of the output signal falling outside of this range. In normal operation LIMBST=000 signals below this threshold are unaffected by the limiter.

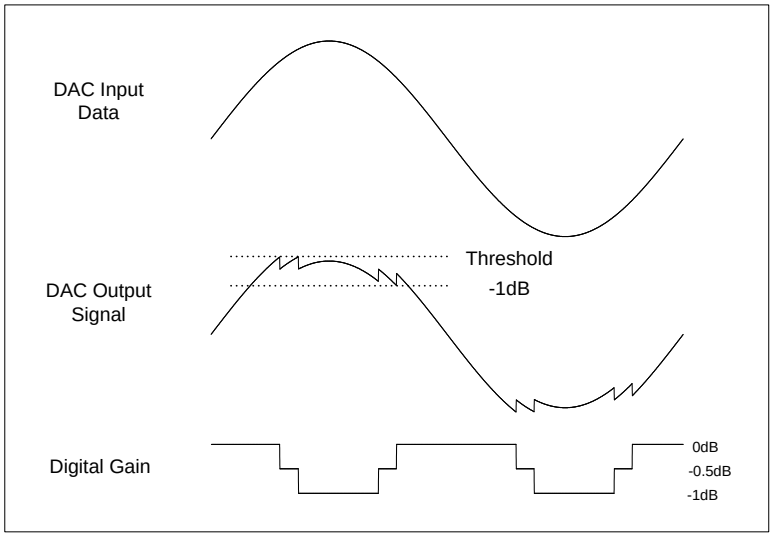


Table 15: DAC Digital Limiter Control

12.4.6. Volume Boost

The limiter has programmable upper gain, which boosts signals below the threshold to compress the dynamic range of the signal and increase its perceived loudness. This operates as an ALC function with limited boost capability. The volume boost is from 0dB to +12dB in 1dB steps, controlled by the DACLIMBST[3:0] register bits. The output limiter volume boost can also be used as a stand-alone digital gain boost when the limiter is disabled.

12.5. ANALOG OUTPUTS

The NAU8811 features two different types of outputs, a single-ended Headphone output (MOUT) and a differential speaker outputs (SPKOUT+ and SPKOUT-). The speaker amplifiers designed to drive a load differentially; a configuration referred to as Bridge-Tied Load (BTL).

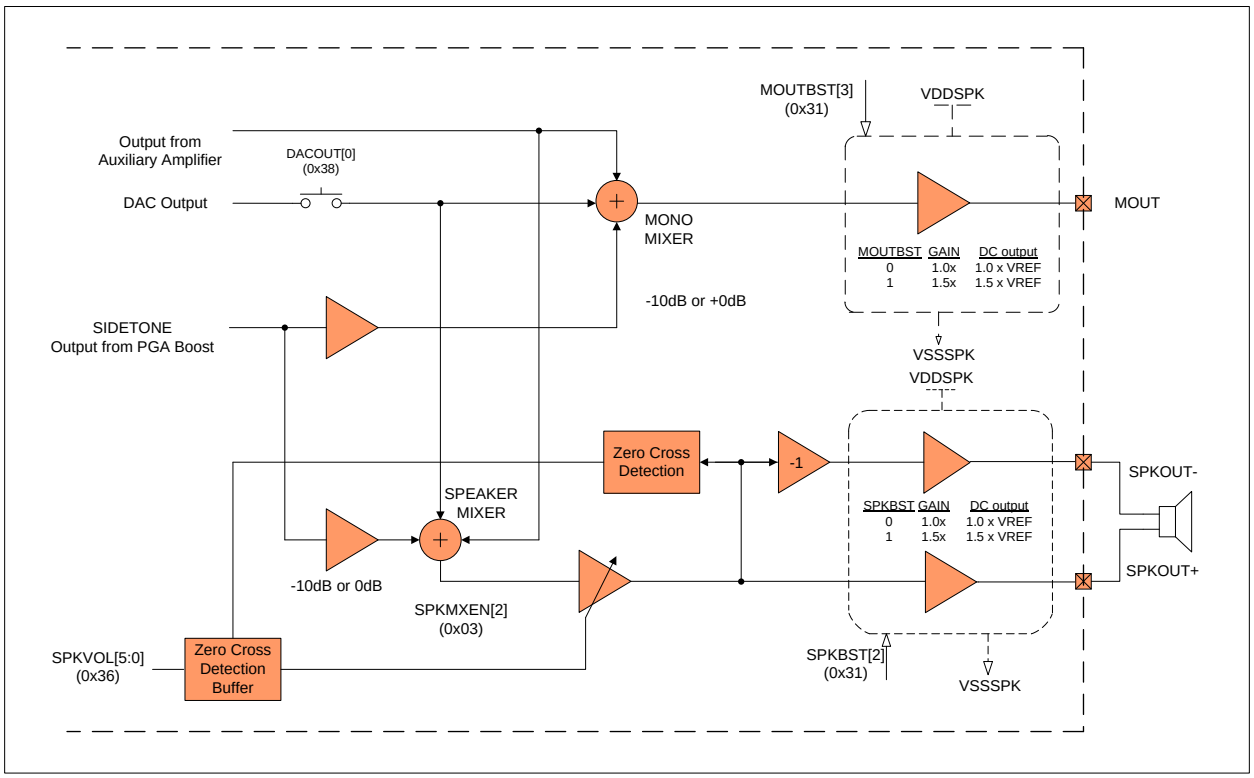


Figure 16: Speaker and Headphone Analogue Outputs

Important: For analog outputs depopping purpose, when powering up speakers, headphone, AUXOUTs, certain delays are generated after enabling sequence. However, the delays are created by MCLK and sample rate register. For correct operation, sending I2S signal no earlier than 250ms after speaker or headphone enabled and MCLK appearing.

12.5.1. Speaker Mixer Outputs

The speaker amplifiers are designed to drive a load differentially; a configuration referred to as Bridge-Tied Load (BTL). The differential speaker outputs can drive a single 8Ω speaker or two headphone loads of 16Ω or 32Ω or a line output. Driving the load differentially doubles the output voltage. The output of the speaker can be manipulated by changing attenuation and the volume (loudness of the output signal).

The output stage is powered by the speaker supply, VDDSPK, which are capable of driving up to $1.5V_{RMS}$ signals (equivalent to $3V_{RMS}$ into a BTL speaker). The speaker outputs can be controlled and can be muted individually. The output pins are at reference DC level when the output is muted.

Bit(s)	Addr	Parameter	Programmable Range
SPKMXEN[2]	0x03	Speaker Mixer enable	0 – Disabled 1 – Enabled
PSPKEN[5]	0x03	Speaker positive terminal enable	0 – Disabled 1 – Enabled
NSPKEN[6]	0x03	Speaker negative terminal enable	0 – Disabled 1 – Enabled
SPKATT[1]	0x28	Speaker output attenuation	0 – 0dB 1 - -10dB
SPKBST[2]	0x31	Speaker output Boost	0 – (1.0x VREF) Boost 1- (1.5 x VREF) Boost
SPKGAIN[5:0]	0x36	Speaker output Volume	Range: -57dB to +6dB @ 6dB increment
SPKMT[6]	0x36	Speaker output Mute	0 – Speaker Enabled 1 – Speaker Muted

Table 16: Speaker Output Controls

12.5.2. Headphone Mixer Output

The single ended output can drive headphone loads of 16Ω or 32Ω or a line output. The MOUT can be manipulated by changing attenuation and the volume (loudness of the output signal).

The output stage is powered by the speaker supply, VDDSPK, which are capable of driving up to $1.5V_{RMS}$ signals. The Headphone output can be enabled for signal output or muted. The output pins are at reference DC level when the output is muted.

Bit(s)	Addr	Parameter	Programmable Range
MOUTMXEN[3]	0x03	Headphone mixer enable	0 – Disabled 1 – Enabled
MOUTEN[7]	0x03	Headphone output enable	0 – Disabled 1 – Enabled
MOUTATT[2]	0x28	Headphone output attenuation	0 – 0dB 1 - -10dB
MOUTBST[3]	0x31	Headphone output boost	0 – (1.0x VREF) Boost 1- (1.5 x VREF) Boost
MOUTMT[6]	0x38	Headphone Output Mute	0 – Headphone Enabled 1 – Headphone Muted

Table 17: Headphone Output Controls

12.5.3. Unused Analog I/O

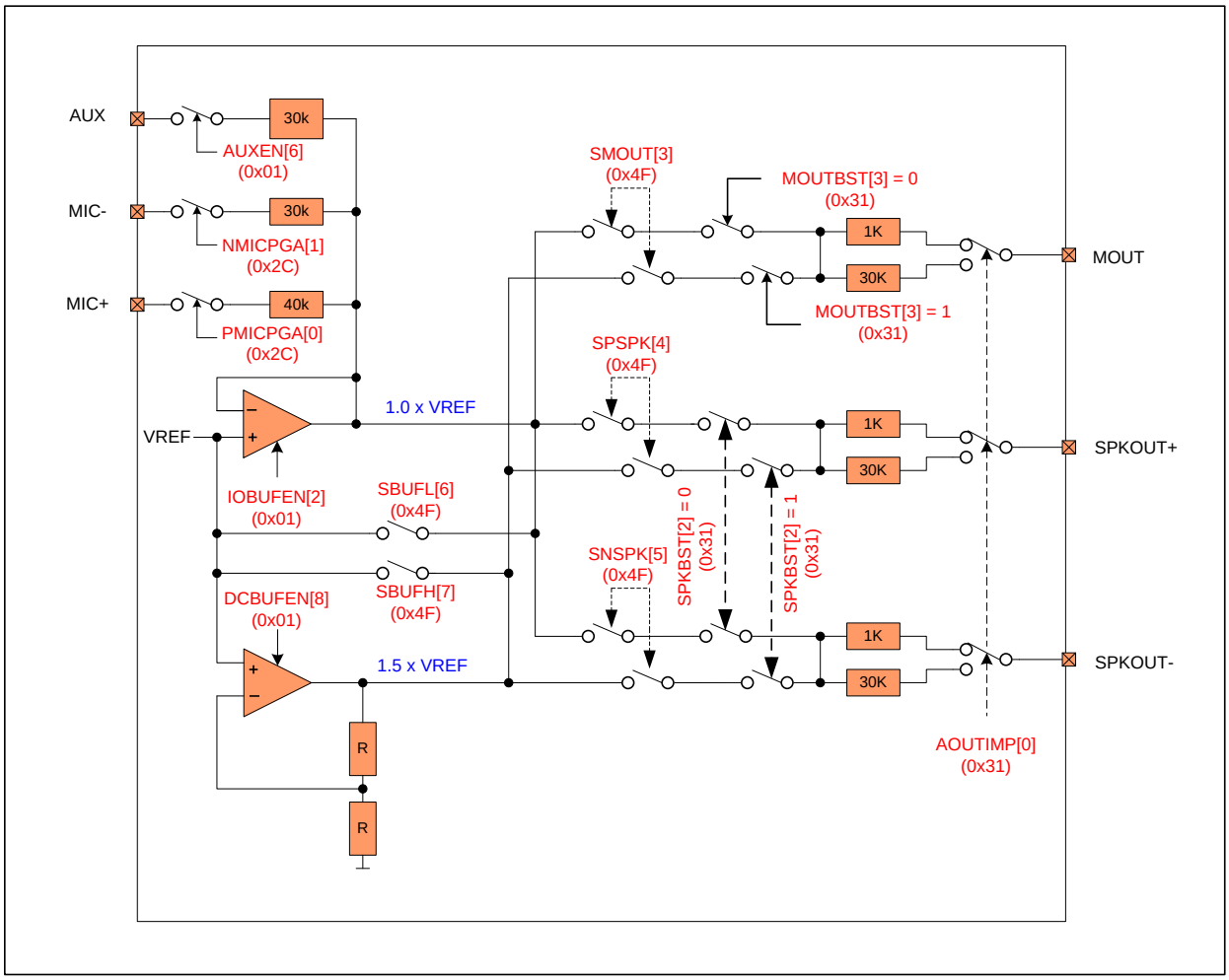


Figure 17: Tie-off Options for the Speaker and Headphone output Pins

In audio and voice systems, any time there is a sudden change in voltage to an audio signal, an audible pop or click

sound may be the result. Systems that change inputs and output configurations dynamically, or which are required to manage low power operation, need special attention to possible pop and click situations. The NAU8811 includes many features which may be used to greatly reduce or eliminate pop and click sounds. The most common cause of a pop or click signal is a sudden change to an input or output voltage. This may happen in either a DC coupled system, or in an AC coupled system.

The strategy to control pops and clicks is similar for either a DC coupled system, or an AC coupled system. The case of the AC coupled system is the most common and the more difficult situation, and therefore, the AC coupled case will be the focus for this information section. When an input or output pin is being used, the DC

level of that pin will be very close to half of the VDDA voltage that is present on the VREF pin. The only exception is that when outputs are operated in the 5-Volt mode known as the 1.5X boost condition, then the DC level for those outputs will be equal to 1.5xVREF. In all cases, any input or output capacitors will become charged to the operating voltage of the used input or output pin. The goal to reduce pops and clicks is to insure that the charge voltage on these capacitors does not change suddenly at any time.

When an input or output is in a not-used operating condition, it is desirable to keep the DC voltage on that pin at the same voltage level as the DC level of the used operating condition. This is accomplished using special internal DC voltage sources that are at the required DC values. When an input or output is in the not-used condition, it is connected to the correct internal DC voltage as not to have a pop or click. This type of connection is known as a "tie-off" condition.

Two internal DC voltage sources are provided for making tie-off connections. One DC level is equal to the VREF voltage value, and the other DC level is equal to 1.5X the VREF value. All inputs are always tied off to the VREF voltage value. Outputs will automatically be tied to either the VREF voltage value or to the 1.5xVREF value, depending on the value of the "boost" control bit for that output. That is to say, when an output is set to the 1.5X gain condition, then that same output will automatically use the 1.5xVREF value for tie-off in the not-used condition. The input pullups are connected to IOBUFEN[2] address (0x01) buffer with a voltage source (VREF). The output pullups can be connected two different buffers depending on the voltage source. IOBUFEN[2] address (0x01) buffer is enabled if the voltage source is (VREF) and DCBUFEN[8] address (0x01) buffer is enabled if the voltage source is (1.5 x VREF). IOBUFEN[2] address (0x01) buffer is shared between input and output pins.

To conserve power, these internal voltage buffers may be enabled/disabled using control register settings. To better manage pops and clicks, there is a choice of impedance of the tie-off connection for unused outputs. The nominal values for this choice are 1kΩ and 30kΩ. The low impedance value will better maintain the desired DC level in the case when there is some leakage on the output capacitor or some DC resistance to ground at the NAU8811 output pin. A tradeoff in using the low-impedance value is primarily that output capacitors could change more suddenly during power-on and power-off changes.

Automatic internal logic determines whether an input or output pin is in the used or un-used condition. This logic function is always active. An output is determined to be in the un-used condition when it is in the disabled unpowered condition, as determined by the power management registers. An input is determined to be in the un-used condition when all internal switches connected to that input are in the "open" condition.

12.6. CLOCKING BLOCK

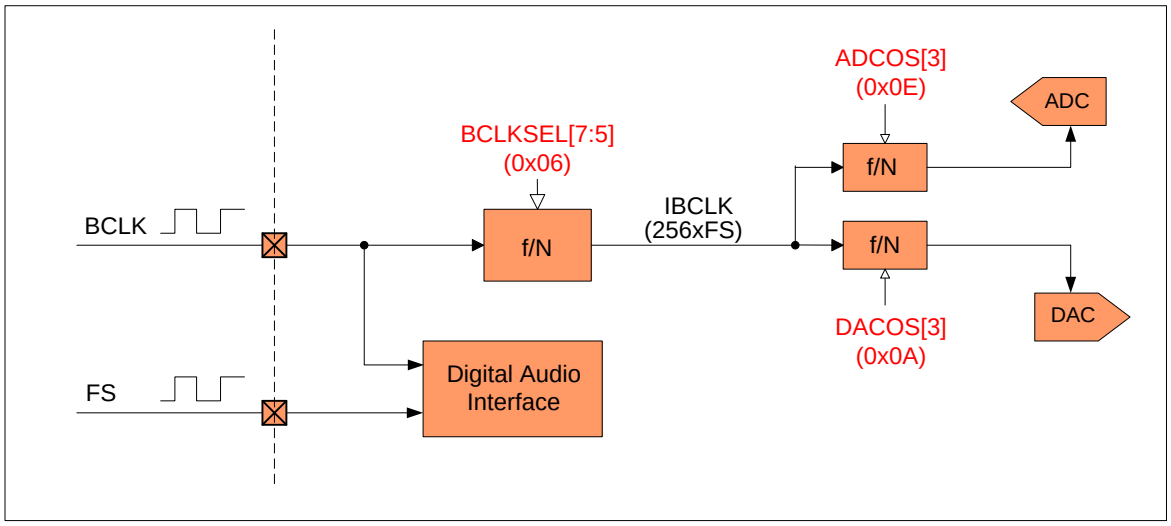


Figure 18: Clock Select Circuit

The NAU8811 can be operated only in slave mode, which means that the frame sync (FS) and the bit clock (BCLK) must be provided from an external source. FS and BCLK manage the bit rate and sample rate for this data flow. The internal bit Clock (IBCLK = 256 x FS) directly determines the sample rate of the ADC and DAC. FS directly determine the sample for the digital audio interface. If FS and IBCLK are not phase locked, then the sample rate for the codec and digital audio interface will be different. This can cause distortion and inharmonic audible tones. It is therefore a requirement of the device that the Digital Audio Interface and data converters be operated synchronously, and that the FS and BCLK signals are all derived from a common reference frequency. If these two clocks signals are not synchronous, audio quality will be reduced.

12.7. CONTROL INTERFACE

The NAU8811 features serial bus interfaces SPI that provide access to the control registers. NAU8811 provides two different SPI architecture which is compatible with other industry interfaces allowing operation on a simple 3-wire bus. Table below describes the selection of the architectures.

SPIEN[8] Bit (0x49)	Description
0	SPI Interface 16-bit
1	SPI Interface 24-bit

Table 18: Control Interface Selection

The Serial Peripheral Interface (SPI) is one of the widely accepted communication interfaces implemented in Nuvoton's Audio CODEC portfolio. SPI is a software protocol allowing operation on a simple 3-wire bus where the data is transferred MSB first. NAU8811 has two different architectures a 16-bit write (default) and a 24-bit write. The SPI interface consists of a clock (SCLK), chip select (CSb), serial data input (SDIO) to configure all the internal register contents. SCLK is static, allowing the user to stop the clock and then start it again to resume operations where it left off.

The 16-bit write operation consists of 7-bits of control register address, and 9-bits of data. The 24-bit write operation consists of 8-bits of device address, 7-bits of control register address, and 9-bits of data. To set the SPI 24-bit Write set SPIEN[8] address (0x49) is set to "1". This bit must to set to "0" using the 24-bit architecture to go back to 16-bit write mode.

12.7.1. 16-bit Write Operation (default)

The default control interface architecture is SPI 16-bit. This interface architecture consists of 7-bits of control register address, and 9-bits of control register data. The write operation requires a valid control register address, then a valid 9-bit Data Byte and the finally to complete the transaction the CSb has to transition from LOW to HIGH to latch the last 9-bits (data).

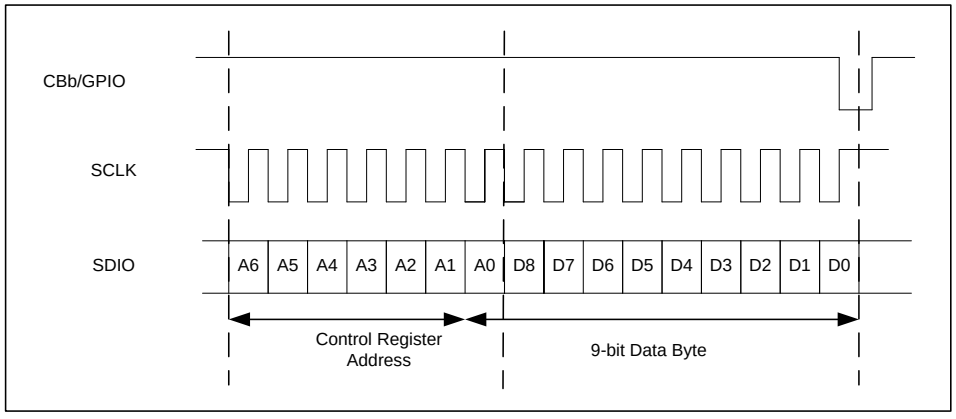


Figure 19: Register write operation using a 16-bit SPI Interface

12.7.2. 24-bit Write Operation

The 24-bit write operation is a three-byte operation. To start the operation the host controller transitions the CSb from HIGH to LOW. The host micro-controller sends valid device address, then a valid control register address following Data Byte. Finally the interface is terminated by toggling CSb pin from LOW to HIGH. The write operation will accept multiple 9-bit DATA blocks, which will be written in to sequential address beginning with the address, specified in the control register address. This is enabled by setting SPIEN[8] address (0x49) to "1". This bit must to set to "0" using the 24-bit architecture to go back to 16-bit write mode.

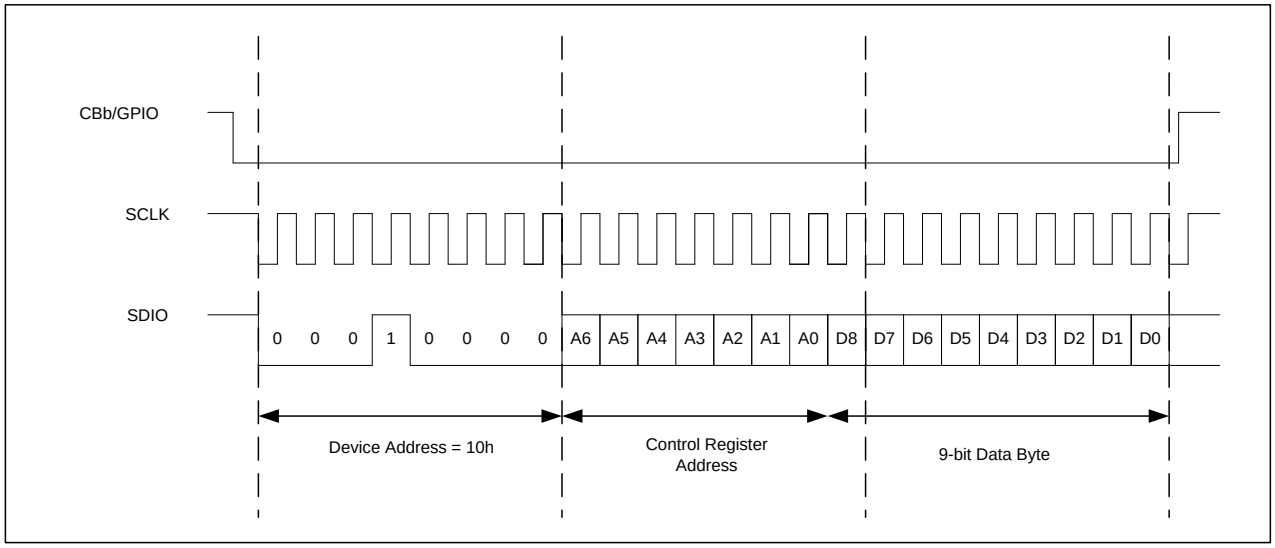


Figure 20: Register Write operation using a 24-bit SPI Interface

12.7.3. Software Reset

The control registers can be reset to default conditions by writing any value to RST address (0x00), using any of the control interface modes. Writing valid data to any other register disables the reset, but all registers will need to be initiated again appropriate to the operation. See the applications section on powering NAU8811 up for information on avoiding pops and clicks after a software reset.

12.8. DIGITAL AUDIO INTERFACES

NAU8811 is a Mono audio codec; supports standard audio interface which by definition has two separate channels Left and Right for data. In normal mode, NAU8811 receives mono data through the analog inputs and output digital data through the ADCOUT pin. Since NAU8811 is a mono device, it only output Left channel data. Although NAU8811 is a Mono device, it includes a special feature where Left channel data is copied to the Right channel. The resultant of this feature is stereo sound. This feature is implemented on to all the audio interfaces supported by NAU8811 and can be enabled by a register bit. The default audio format is I^2S interface.

NAU8811 audio interface is designed to operate in the slave mode, which means bit clock, and the frame sync must be provided to the device externally. The digital interface is used to input digital data to the DAC, or output digital data from the ADC. The BCLK of the digital interface is provided from an external clock either from a crystal oscillator or from a microcontroller.

The NAU8811 uses ADCOUT, DACIN, FS, and BCLK pins to control the digital interface. Bit Bit[0] and Bit[8] of address (0x06) must be set to “0” during initialization routine of the system configuration.

The output state of the ADCOUT pin by default is pulled-low. Depending on the application, the output can be configured to be Hi-Z, pull-low, pull-high, Low or High. To configure the output, three different bits have to be set. First the output switched to the mask by setting PUDOEN[5] address (0x3C), then the mask has to be enabled be setting PUDPE[4] address (0x3C) and finally output state select pulled up or down by PUDPS[3] address (0x3C). Six different audio formats are supported by NAU8811 with MSB first and they are as follows.

AIFMT[4]	AIFMT[3]	PCMTSEN[8]	PCM Mode
0	0	0	Right Justified
0	1	0	Left Justified
1	0	0	I^2S
1	1	0	PCM
1	1	1	PCM Time Slot

Table 19: Standard Interface modes

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x04	BCLKP	FSP	WLEN[1:0]		AIFMT[1:0]		DACPHS	ADCPHS	0	0x050
0x06	0	BCLKSEL[2:0]			0					0x040
0x3B	TSLOT[8:0]									0x000
0x3C	PCMTSEN	TRI	PCM8BIT	PUDOEN	PUDPE	PUDPS	LOUTR	PCMB	TSLOT[9:8]	0x000

Table 20: Audio Interface Control Registers

12.8.1. Right Justified audio data

In right justified interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the HIGH frame sync. The MSB data is sampled first. The data is latched on the last rising edge of BCLK before frame sync transition (FS). The LSB is aligned with the falling edge of the frame sync signal (FS). Right justified format is selected by setting AIFMT[1:0] address (0x04) to "00" binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

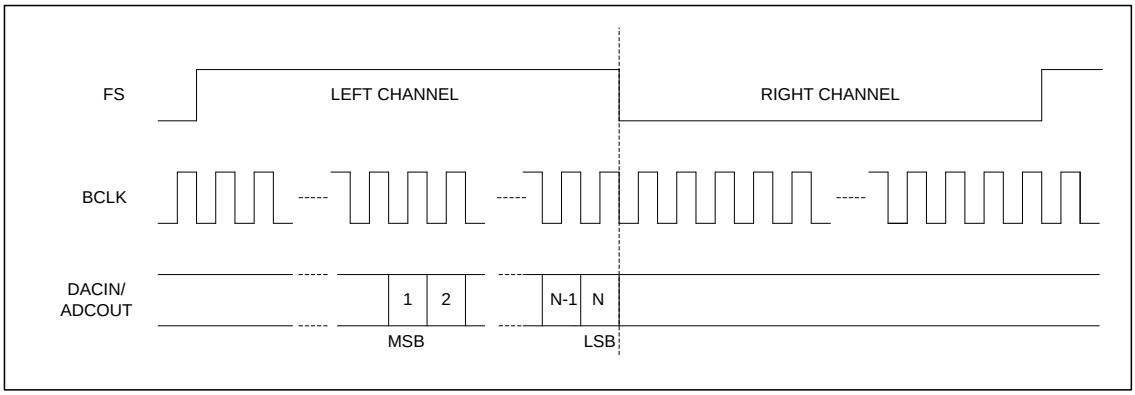


Figure 21: Right Justified Audio Interface (Normal Mode)

NAU8811 features a special mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LOUTR[2] address (0x3C) to "1"

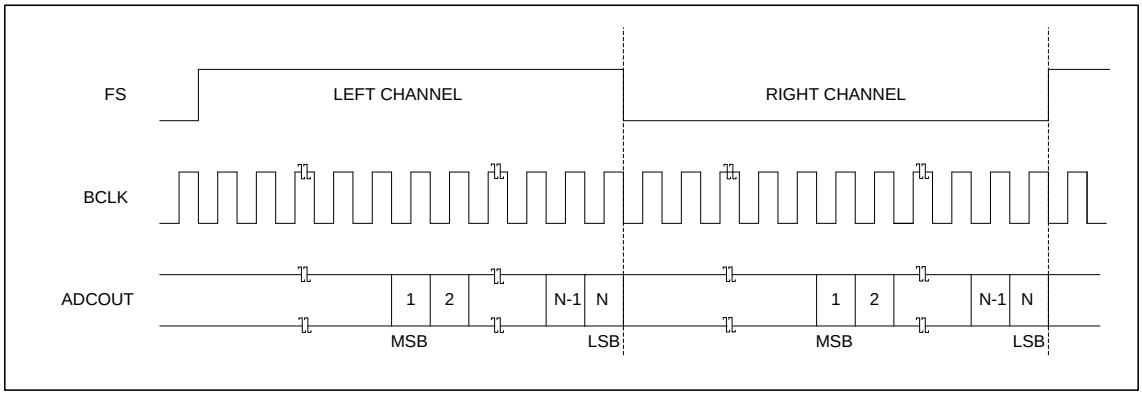


Figure 22: Right Justified Audio Interface (Special mode)

12.8.2. Left Justified audio data

In Left justified interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the HIGH frame sync. The MSB data is sampled first and is available on the first rising edge of BCLK following a frame sync transition (FS). Left justified format is selected by setting AIFMT[1:0] address (0x04) to “01” binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

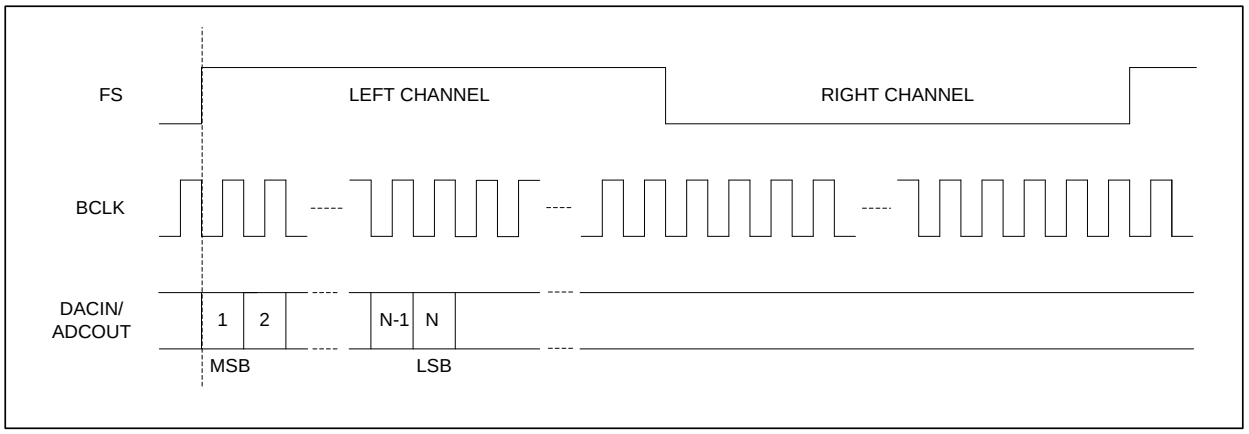


Figure 23: Left Justified Audio Interface (Normal Mode)

NAU8811 features a special mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LOUTR[2] address (0x3C) to “1”

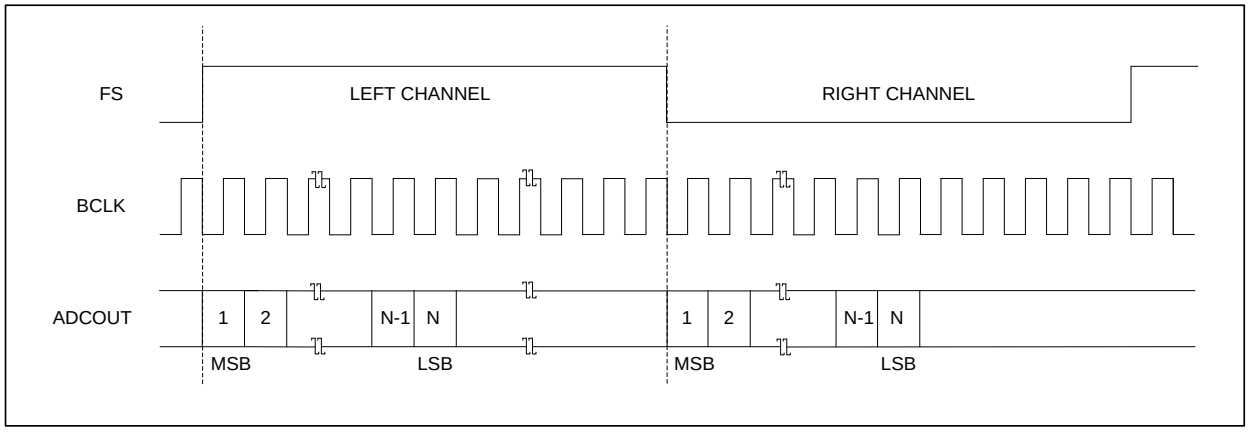


Figure 24: Left Justified Audio Interface (Special mode)

12.8.3. I²S audio data

In I²S interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the LOW frame sync. The MSB data is sampled first. The data is latched on the second rising edge of BCLK following a frame sync transition (FS). I²S format is selected by setting AIFMT[1:0] address (0x04) to "10" binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

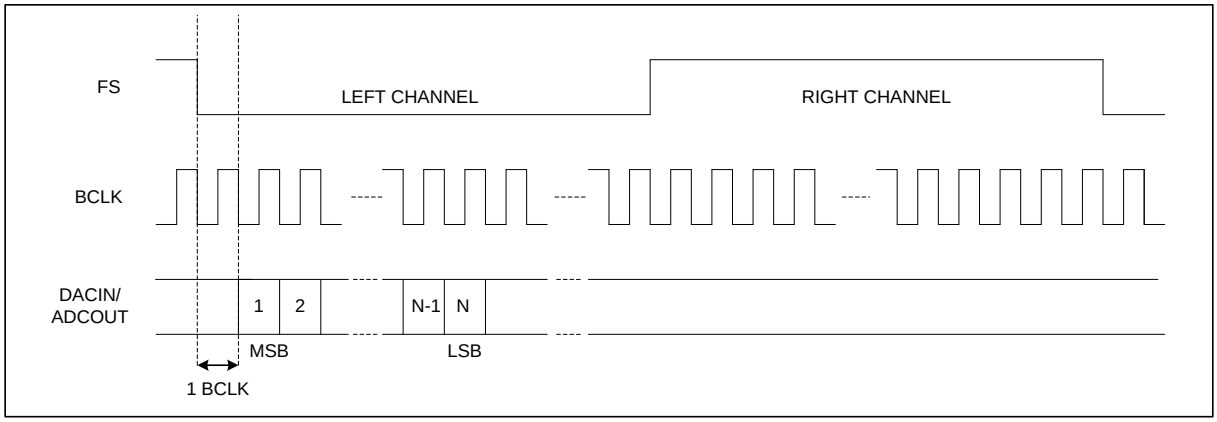


Figure 25: I2S Audio Interface (Normal Mode)

NAU8811 features a special mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LOUTR[2] address (0x3C) to "1"

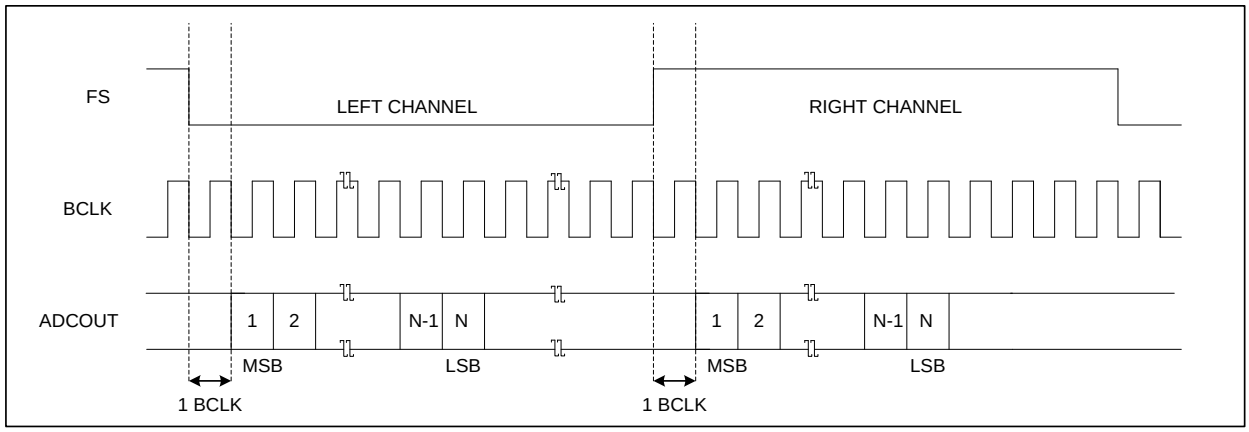


Figure 26: I2S Audio Interface (Special mode)

12.8.4. PCM audio data

In PCM interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the LOW frame sync. The MSB data is sampled first. The data is latched on the second rising edge of BCLK following a frame sync transition (FS). PCM format is selected by setting AIFMT[4:3] address (0x04) to "11" binary in conjunction with PCMTSEN[8] address (0x3C) set to LOW.

The digital data can be forced to appear on the right phase of the FS by setting ADCPHS[0] and DACPHS[1] address (0x04) bits to HIGH respectively. The starting point of the right phase data depends on the word length WLEN[6:5] address (0x04) after the frame sync transition (FS).

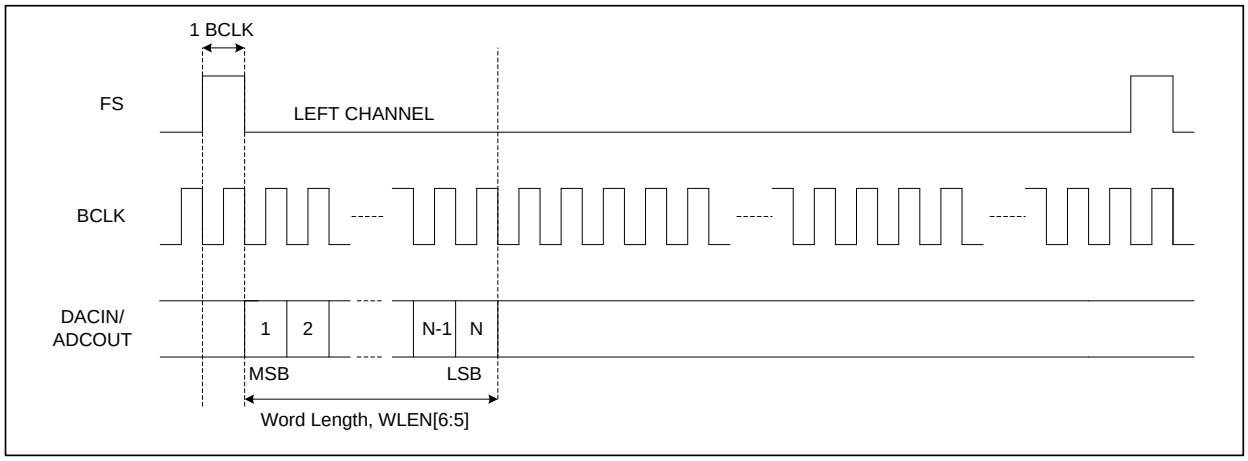


Figure 27: PCM Mode Audio Interface (Normal Mode)

NAU8811 features a special mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LOUTR[2] address (0x3C) to "1"

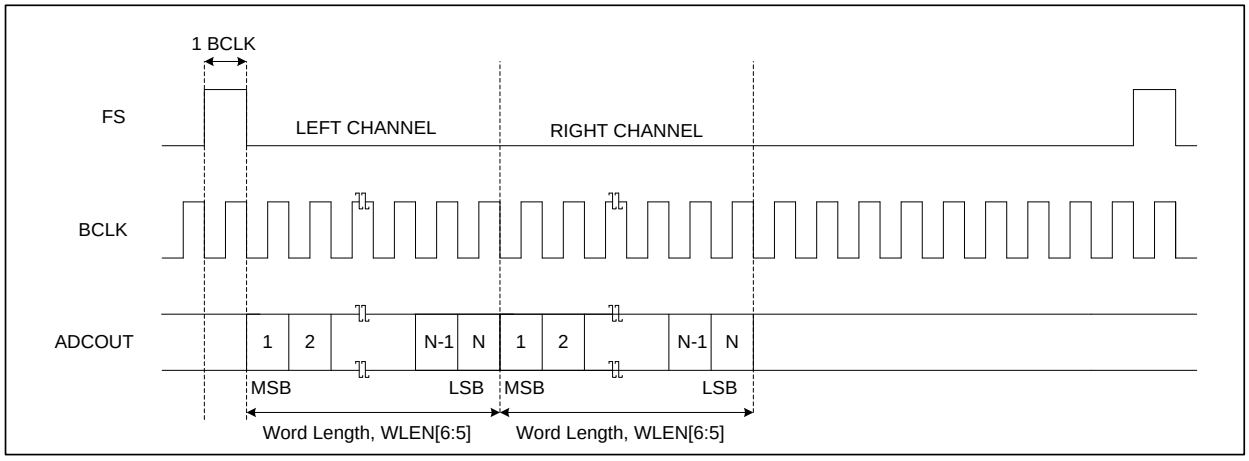


Figure 28: PCM Mode Audio Interface (Special mode)

12.8.5. PCM Time Slot audio data

In PCM Time-Slot interface (normal mode), the left channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the LOW frame sync. The MSB data is sampled first. The starting point of the timeslot is controlled by a 10-bit byte TSLOT[9:0] address (0x3B and 0x3C). The data is latched on the first rising edge of BCLK following a frame sync transition (FS) providing PCM is in timeslot zero (TSLOT[9:0] = 000). PCM Time-Slot format is selected by setting AIFMT[4:3] address (0x04) to "11" binary in conjunction with PCMTSEN[8] address (0x3C) set to HIGH. The digital data can be forced to appear on the right phase of the FS by setting ADCPHS[0] and DACPHS[1] address (0x04) bits to HIGH respectively. The starting point of the right phase data depends on the word length WLEN[6:5] address (0x04) and timeslot assignment TSLOT[9:0] address (0x3B and 0x3C) after the frame sync transition (FS). DACIN will return to the bus condition either on the negative edge of BCLK during the LSB, or on the positive edge of BCLK following the LSB depending on the setting of TRI[7] address (0x3C). Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots without the risk of driver contention.

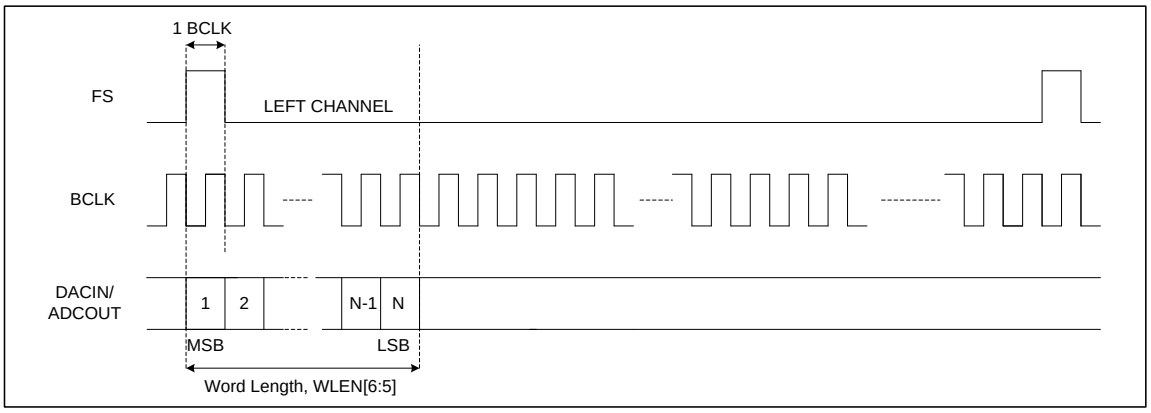


Figure 29: PCM Time Slot Mode (Time slot = 0) (Normal Mode)

NAU8811 features a special mode where the device outputs Left channel data to both Left and Right channels. This is accomplished by setting LOUTR[2] address (0x3C) to "1"

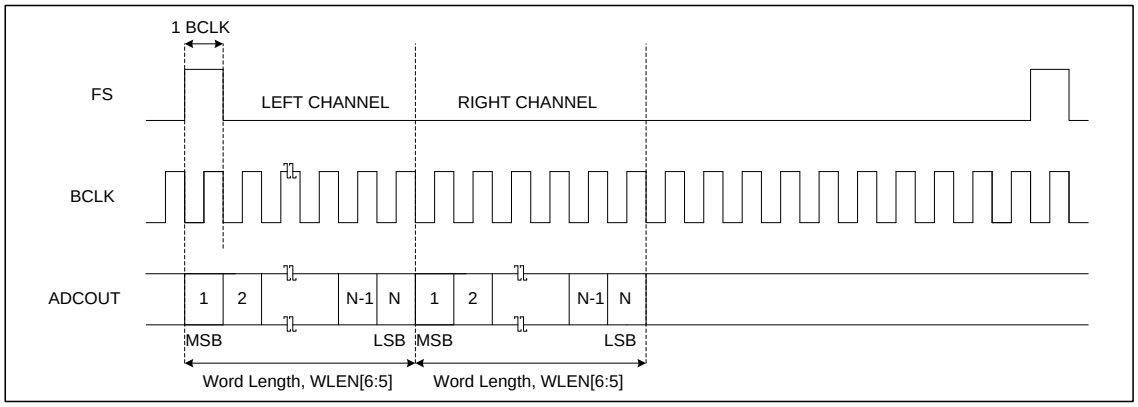


Figure 30: PCM Time Slot Mode (Time slot = 0) (Special mode)

12.8.6. Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, and make use of non-linear algorithms. NAU8811 supports two different types of companding A-law and µ-law on both transmit and receive sides. A-law algorithm is used in European communication systems and µ-law algorithm is used by North America, Japan, and Australia. This feature is enabled by setting DACCM[4:3] address (0x05) or ADCCM[2:1] address (0x05) register bits. Companding converts 13 bits (µ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits). As recommended by the G.711 standard (all 8-bits are inverted for µ-law, all even data bits are inverted for A-law).

Setting CMB8[5] address 0x05 to 1 will cause the PCM interface to use 8-bit word length for data transfer, overriding the word length configuration setting in WLEN[6:5] address 0x04.

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x05	0	0	0	CMB8	DACCM[1:0]		ADCCM[1:0]		ADDAP	**0x000**

Table 21: Companding Control

The following equations for data compression (as set out by ITU-T G.711 standard):

µ-law (where µ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $\quad -1 \le x \le 1$

2- **law (where A=87.6 for Europe):**

$F(x) = A|x| / (1 + \ln A)$ for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ for $1/A \le x \le 1$

12.9. POWER SUPPLY

This device has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. There are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harm to the device. However, pops and clicks may result from some sequences. Optimum handling of hardware and software power-on and power-off sequencing is described in more detail in the Power Up/Down Sequencing section of this document.

12.9.1. Power-On Reset

The NAU8811 does not have an external reset pin. The device reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that either VDDA or VDDD is lower than is required for reliable maintenance of internal logic conditions. The threshold voltage for VDDA is approximately 1.52Vdc and the threshold voltage for VDDD is approximately 0.67Vdc. Note that these are much lower voltages than are required for normal operation of the chip. These values are mentioned here as general guidance as to overall system design.

If either VDDA or VDDD is below its respective threshold voltage, an internal reset condition may be asserted. During this time, all registers and controls are set to the hardware determined initial conditions. Software access during this time will be ignored, and any expected actions from software activity will be invalid.

When both VDDA and VDDD reach a value above their respective thresholds, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset time is approximately 50 microseconds, but not longer than 100 microseconds. The reset condition remains asserted during this time. If either VDDA or VDDD at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until both VDDA and VDDD again higher than their respective thresholds. After VDDA and VDDD are again both greater than their respective threshold voltage, a new reset pulse will be generated, which again will extend the reset condition for not longer than an additional 100 microseconds.

12.9.2. Power Related Software Considerations

There is no direct way for software to determine that the device is actively held in a reset condition. If there is a possibility that software could be accessing the device sooner than 100 microseconds after the VDDA and VDDD supplies are valid, the reset condition can be determined indirectly. This is accomplished by writing a value to any register other than register 0x00, with that value being different than the power-on reset initial values. The optimum choice of register for this purpose may be dependent on the system design, and it is recommended the system engineer choose the register and register test bit for this purpose. After writing the value, software will then read back the same register. When the register test bit reads back as the new value, instead of the power-on reset initial value, software can reliably determine that the reset condition has ended.

Although it is not required, it is strongly recommended that a Software Reset command should be issued after power-on and after the power-on-reset condition is ended. This will help insure reliable operation under every power sequencing condition that could occur.

12.9.3. Power Up/Down Sequencing

Most audio products have issues during power up and power down in the form of pop and click noise. To avoid cuch issues the NAU8811 provides four different power supplies VDDA, VDDD and VDDSPK with separated grounds VSSA, VSSD and VSSSPK. The audio CODEC circuitry, the input amplifiers, output amplifiers and drivers, the audio ADC and DAC converters, and so on, can be powered up and down individually by software control via SPI interface. The zero cross function should be used when changing the volume in the PGAs to avoid any audible pops or clicks. There are two different modes of operation 5.0V and 3.3V mode. The recommended power-up and power-down sequences for both the modes are outlined as following.

		Power Up
Name	VDDSPK – 3.3V operation (Default)	VDDSPK – 5.0V operation
Power supplies	Analog – VDDA	Analog – VDDA
	Digital – VDDD	Digital – VDDD
	Output driver – VDDSPK	Output driver – VDDSPK
Mode	SPKBST[2] = 0	SPKBST[2] = 1
	MOUTBST = 0	MOUTBST = 1
Power Management	REFIMP[1:0] as required (value of the REFIMP bits based on the startup time which is a combination of the reference impedance and the decoupling capacitor on VREF)	
	ABIASEN[3] = 1 (enables the internal device bias for all analog blocks)	
	IOBUFEN[2] = 1 (enables the internal device bias buffer)	
Clock divider	BCLKSEL[7:5] if required	BCLKSEL[7:5] if required
DAC, ADC	DACEN[0] = 1	DACEN[0] = 1
	ADCEN[0] = 1	ADCEN[0] = 1
Mixers	SPKMXEN[2]	SPKMXEN[2]
	MOUTMXEN[3]	MOUTMXEN[3]
Output stages	MOUTEN[7]	MOUTEN[7]
	NSPKEN[6]	NSPKEN[6]
	PSPKEN[5]	PSPKEN[5]
Un-mute DAC	DACMT[6] = 0	DACMT[6] = 0

Table 22: Power up sequence

Name	Power Down Both Cases
Mute DAC	DACMT[6] = 1
Power Management	PWRM1 = 0x000
Output stages	MOUTEN[7]
	NSPKEN[6]
	PSPKEN[5]
Power supplies	Analog – VDDA
	Digital – VDDD
	Speaker Driver – VDDSPK

Table 23: Power down Sequence

12.9.4. Reference Impedance (REFIMP) and Analog Bias

Before the device is functional or any of the individual analog blocks are enabled REFIMP[1:0] address (0x01) and ABIASEN[3] address (0x01) must be set. The REFIMP[1:0] bits control the resistor values ("R" in Figure3) that generates the mid supply reference, VREF. REFIMP[1:0] bits control the power up ramp rate in conjunction with the external decoupling capacitor. A small value of "R" allows fast ramp up of the mid supply reference and a large value of "R" provides higher PSRR of the mid supply reference.

The master analog biasing of the device is enabled by setting ABIASEN[3] address (0x01). This bit has to be set before for the device to function.

12.9.5. Power Saving

Saving power is one of the critical features in a semiconductor device specially ones used in the Bluetooth headsets and handheld device. NAU8811 has two oversampling rates 64x and 128x. The default mode of operation for the DAC and ADC is in 64x oversampling mode which is set by programming DACOS[3] address (0x0A) and ADCOS[3] address (0x0E) respectively to LOW. Power is saved by choosing 64x oversampling rate compared to 128x oversampling rate but slightly degrades the noise performance. To each lowest power possible after the device is functioning set ABIASEN[3] address (0x01) bit to LOW.

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x01	DCBUFEN	0	AUXEN	0		ABIASEN	IOBUFEN	REFIMP		**0x000**
0x0A	0		DACMT	DEEMP[1:0]		DACOS	AUTOMT	0	DACPL	**0x000**
0x0E	HPFEN	HPFAM	HPF[2:0]			ADCOS	0		ADCPL	**0x100**
0x3A	LPIPBST	LPADC	LPSPKD	LPDAC	0	TRIMREG		IBADJ		**0x000**

Table 24: Registers associated with Power Saving

12.9.6. Estimated Supply Currents

NAU8811 can be programmed to enable or disable various analog blocks individually. The table below shows the amount of current consumed by certain analog blocks. Sample rate settings will vary current consumption of the VDDD supply. VDDD consumes approximately 4mA with VDDD = 1.8V and fs = 48kHz. Lower sampling rates will draw lower current.

BIT	Address	VDDA CURRENT
REFIMP[1:0]	0x01	10K => 300 uA 161k/595k < 100 uA
IOBUFEN[2]		100 uA
ABIASEN[3]		300 uA
DCBUFEN[8]		100 uA
ADCEN[0]	0x02	x64 - ADCOS= 0 =>2.6 mA x128 – ADCOS= 1 =>4.9 mA
PGAEN[2]		200 uA
BSTEN[4]		200 uA
DACEN[0]	0x03	X64 (DACOS=0)=>1.8 mA x128(DACOS=1)=>1.9 mA
SPKMXEN[2]		200 uA
MOUTMXEN[3]		200 uA
NSPKEN[6]		1 mA from VDDSPK + 200 uA (VDDA = 5V mode)
PSPKEN[5]		1 mA from VDDSPK + 200 uA (VDDA = 5V mode)
MOUTEN[7]		0.2

Table 25: Supply Current – VDDA 3.3V

13. REGISTER DESCRIPTION

Register Address			Register Bits									Default
DEC	HEX		D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	Software Reset	RESET (SOFTWARE)									
			POWER MANAGEMENT									
1	01	Power Management 1	DCBUFEN	0	AUXEN	0	0	ABIASEN	IOBUFEN	REFIMP		000
2	02	Power Management 2	0				BSTEN	0	PGAEN	0	ADCEN	000
3	03	Power Management 3	0	MOUTEN	NSPKEN	PSPKEN	0	MOUTMXEN	SPKMXEN	0	DACEN	000
			AUDIO CONTROL									
4	04	Audio Interface	BCLKP	FSP	WLEN[1:0]		AIFMT[1:0]		DACPHS	ADCPHS	0	050
5	05	Companding	0				DACCM[1:0]		ADCCM[1:0]		ADDAP	000
6	06	Clock Control 1	0	BCLKSEL[2:0]			0				0	040
7	07	Clock Control 2	0					SMPLR[2:0]			SCLKEN	000
10	0A	DAC CTRL	0		DACMT	DEEMP[1:0]		DACOS	AUTOMT	0	DACPL	000
11	0B	DAC Volume	0	DACGAIN								0FF
14	0E	ADC CTRL	HPFEN	HPFAM	HPF[2:0]			ADCOS	0		ADCPL	100
15	0F	ADC Volume	0	ADCGAIN								0FF
			DIGITAL TO ANALOG (DAC) LIMITER									
24	18	DAC Limiter 1	DACLIMEN	DACLIMDCY[3:0]				DACLIMATK[3:0]				032
25	19	DAC Limiter 2	0	0	DACLIMTHL[2:0]			DACLIMBST[3:0]				000
			NOTCH FILTER									
27	1B	Notch Filter 1	NFCU	NFCEN	NFCA0[13:7]							000
28	1C	Notch Filter 2	NFCU	0	NFCA0[6:0]							000
29	1D	Notch Filter 3	NFCU	0	NFCA1[13:7]							000
30	1E	Notch Filter 4	NFCU	0	NFCA1[6:0]							000
			ALC CONTROL									
32	20	ALC CTRL 1	ALCEN	0	0	ALCMXGAIN[2:0]			ALCMNGAIN[2:0]			038
33	21	ALC CTRL 2	ALCZC	ALCHT[3:0]				ALCSL[3:0]				00B
34	22	ALC CTRL 3	ALCM	ALCDCY[3:0]				ALCATK[3:0]				032
35	23	Noise Gate	0					ALCNEN	ALCNTH[2:0]			000
			INPUT, OUTPUT & MIXER CONTROL									
40	28	Attenuation CTRL	0						MOUTATT	SPKATT	0	000
44	2C	Input CTRL	0					AUXM	AUXPGA	NMICPGA	PMICPGA	003

Register Address			Register Bits									Default
DEC	HEX		D8	D7	D6	D5	D4	D3	D2	D1	D0	
45	2D	PGA Gain	0	PGAZC	PGAMT	PGAGAIN[5:0]						010
47	2F	ADC Boost	PGABST	0	PMICBSTGAIN			0	AUXBSTGAIN			100
49	31	Output CTRL	0					MOUTBST	SPKBST	TSEN	AOUTIMP	002
50	32	Mixer CTRL	0			AUXSPK	0			BYPSPK	DACSPK	001
54	36	SPKOUT Volume	0	SPKZC	SPKMT	SPKGAIN[5:0]						039
56	38	MONO Mixer Control	0		MOUTMXMT	0			AUXMOUT	BYPMOUT	DACMOUT	001
			LOW POWER BITS									
58	3A	Power Management 4	LPIPBST	LPADC	LPSPKD	LPDAC	0	TRIMREG		IBADJ		000
			PCM TIME SLOT CONTROL & ADCOUT IMPEDANCE OPTION CONTROL									
59	3B	Time Slot	TSLOT[8:0]									000
60	3C	ADCOUT Drive	PCMTSEN	TRI	PCM8BIT	PUDOEN	PUDPE	PUDPS	LOUTR	PCMB	TSLOT[9:8]	020
			REGISTER ID									
65	41	Reserved	1	0	0	1	0	0	1	0	0	124
69	45	High Voltage CTRL	0				MOUTMT	0	HVOPU	0	HVOP	001
70	46	ALC Enhancements 1	ALCTBLSEL	ALCPKSEL	ALCNGSEL	0						000
71	47	ALC Enhancements 2	PKLIMEN	0		1	1	1	0	0	1	039
73	49	Additional IF CTRL	SPIEN	FSERRVAL[1:0]		FSERFLSH	FSERRENA	NFDLY	DACINMT	0	0	000
75	4B	Power/Tie-off CTRL	0						MANVREFH	MANVREFM	MANVREFL	000
79	4F	Output tie-off CTRL	MANOUTEN	SBUFH	SBUFL	SNSPK	SPSPK	SMOUT	0	0	0	000

13.1. SOFTWARE RESET

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00	RESET (SOFTWARE)									**0x000**

This is device Reset register. Performing a write instruction to this register with any data will reset all the bits in the register map to default.

13.2. POWER MANAGEMENT REGISTERS

13.2.1. Power Management 1

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x01	DCBUFEN	0	AUXEN	0	0	ABIASEN	IOBUFEN	REFIMP[1:0]		**0x000**

Name	Buffer for DC level shifting Enable	AUX input buffer enable	Analogue amplifier bias control	Unused input/output tie off buffer enable
Bit	**DCBUFEN[8]**	**AUXEN[6]**	**ABIASEN[3]**	**IOBUFEN[2]**
0	Disable	Disable	Disable	Disable
1	Enable (required for 1.5x gain)	Enable	Enable	Enable

The DCBUFEN[8] address (0x01) is a dedicated buffer for DC level shifting output stages when in 1.5x gain boost configuration. There are three different reference impedance selections to choose from as follows:

VREF REFERENCE IMPEDANCE SELECTION ("R" refers to "R" as shown in Figure3)		
REFIMP[1]	**REFIMP[0]**	**Mode**
0	0	Disable
0	1	R = 80 kΩ
1	0	R = 300 kΩ
1	1	R = 3 kΩ

13.2.2. Power Management 2

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x02	0	0	0	0	BSTEN	0	PGAEN	0	ADCEN	**0x000**

Name	Input Boost Enable	MIC(+/-) PGA Enable	ADC Enable
Bit	**BSTEN[4]**	**PGAEN[2]**	**ADCEN[0]**
0	Stage Disable	Disable	Disable
1	Stage Enable	Enable	Enable

13.2.3. Power Management 3

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x03	0	MOUTEN	NSPKEN	PSPKEN	0	MOUTMXEN	SPKMXEN	0	DACEN	**0x000**

Name	MOUT Enable	SPKOUT- Enable	SPKOUT+ Enable	Headphone Mixer Enable	Speaker Mixer Enable	DAC Enable
Bit	**MOUTEN[7]**	**NSPKEN[6]**	**PSPKEN[5]**	**MOUTMXEN[3]**	**SPKMXEN[2]**	**DACEN[0]**
0	Disable	Disable	Disable	Disable	Disable	Disable
1	Enable	Enable	Enable	Enable	Enable	Enable

13.3. AUDIO CONTROL REGISTERS

13.3.1. Audio Interface Control

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x04	BCLKP	FSP	WLEN[1:0]		AIFMT[1:0]		DACPHS	ADCPHS	0	**0x050**

The following table explains the PCM control register bits.

Name	BCLK Polarity	Frame Clock Polarity	DAC Data 'right' or 'left' phases of FRAME clock	ADC Data 'right' or 'left' phases of FRAME clock
Bit	**BCLKP[8]**	**FSP[7]**	**DACPHS[2]**	**ADCPHS[1]**
0	Normal	Normal	DAC data appear in 'left' phase of FRAME	ADC data appear in 'left' phase of FRAME
1	Inverted	Inverted	DAC data appears in 'right' phase of FRAME	ADC data appears in 'right' phase of FRAME

There are three different CODEC modes to choose from as follows:

Word Length Selection		
WLEN[1]	**WLEN[0]**	**Bits**
0	0	16
0	1	20
1	0	24
1	1	32

Audio Data Format Select		
AIFMT[1]	**AIFMT[0]**	**Format**
0	0	Right Justified
0	1	Left Justified
1	0	I^2S
1	1	PCM A

13.3.2. Audio Interface Companding Control

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x05	0	0	0	0	DACCM[1:0]		ADCCM[1:0]		ADDAP	**0x000**

Bit Location	**Bit Description**	**Bit Name**	**Bit Value**	
			0	**1**
0	Connect ADC output to DAC input internally. In this mode, the DAC data cannot be seen at the DACIN pin of the device	**ADDAP**	Disable	Enable

DAC Companding Selection		
DACCM[1]	**DACCM[0]**	**Mode**
0	0	Disabled
0	1	Reserved
1	0	µ-Law
1	1	A-Law

ADC Companding Select		
ADCCM[1]	**ADCCM[0]**	**Mode**
0	0	Disabled
0	1	Reserved
1	0	µ-Law
1	1	A-Law

DAC audio data input option to route directly to ADC data stream	
ADDAP[0]	**Mode**
0	Normal Operation
1	ADC output data stream routed to DAC input data path

13.3.3. Clock Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x06	0	BCLKSEL[2:0]			0	0	0	0	0	**0x040**

Analog Clock Selection			
BCLKSEL [7]	**BCLKSEL [6]**	**BCLKSEL [5]**	**Mode**
0	0	0	÷ 1
0	0	1	÷ 1.5
0	1	0	÷ 2
0	1	1	÷ 3
1	0	0	÷ 4
1	0	1	÷ 6
1	1	0	÷ 8
1	1	1	÷ 12

Name	Source of Internal Clock
Bit	**CLKM[8]**
0	BCLK Pin
1	Disable

13.3.4. Audio Sample Rate Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x07	0	0	0	0	0	SMPLR[2:0]			0	**0x000**

The Audio sample rate configures the coefficients for the internal digital filters

Sample Rate Selection			
SMPLR[3]	**SMPLR[2]**	**SMPLR[1]**	**Mode (Hz)**
0	0	0	48 k
0	0	1	32 k
0	1	0	24 k
0	1	1	16 k
1	0	0	12 k
1	0	1	8 k
1	1	0	Reserved
1	1	1	Reserved

13.3.5. DAC Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0A	0	0	DACMT	DEEMP[1:0]		DACOS	AUTOMT	0	DACPL	**0x000**

Name	Soft Mute Enable	Over Sample Rate	Auto Mute enable	Polarity Invert
Bit	**DACMT[6]**	**DACOS[3]**	**AUTOMT[2]**	**DACPL[0]**
0	Disable	64x (Lowest power)	Disable	Normal
1	Enable	128x (best SNR)	Enable	DAC Output Inverted

De-emphasis		
DEEMP[5]	**DEEMP[4]**	**Mode**
0	0	No de-emphasis
0	1	32kHz sample rate
1	0	44.1kHz sample rate
1	1	48kHz sample rate

13.3.6. DAC Gain Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0B	0	DACGAIN								**0x0FF**

DAC Gain								
DACGAIN[7:0]								**Mode (dB)**
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	0	0	0	0	Digital Mute
0	0	0	0	0	0	0	1	-127.0
0	0	0	0	0	0	1	0	-126.5
DAC Gain Range -127dB to 0dB @ 0.5 increments								
1	1	1	1	1	1	1	0	-0.5
1	1	1	1	1	1	1	1	0.0

13.3.7. Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0E	HPFEN	HPFAM	HPF[2:0]			ADCOS	0	0	ADCPL	**0x100**

Name	High Pass Filter Enable	Audio or Application Mode	Over Sample Rate	ADC Polarity
Bit	**HPFEN[8]**	**HPFAM[7]**	**ADCOS[3]**	**ADCPL[0]**
0	Disable	Audio (1st order, fc ~ 3.7 Hz)	64x (Lowest power)	Normal
1	Enable	Application (2nd order, fc = HPF)	128x (best SNR)	Inverted

High Pass Filter			fs (kHz)								
HPF[6]	**HPF[5]**	**HPF[4]**	SMPLR=101 SMPLR=100			SMPLR=011 SMPLR=010			SMPLR=001 SMPLR=000		
B2	**B1**	**B0**	**8**	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**
0	0	0	82	113	122	82	113	122	82	113	122
0	0	1	102	141	153	102	141	153	102	141	153
0	1	0	131	180	156	131	180	156	131	180	156
0	1	1	163	225	245	163	225	245	163	225	245
1	0	0	204	281	306	204	281	306	204	281	306
1	0	1	261	360	392	261	360	392	261	360	392
1	1	0	327	450	490	327	450	490	327	450	490
1	1	1	408	563	612	408	563	612	408	563	612

13.3.8. ADC Gain Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0F	0	ADCGAIN								**0x0FF**

ADC Gain								
ADCGAIN[7:0]								**Mode (dB)**
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
0	0	0	0	0	0	0	0	Unused
0	0	0	0	0	0	0	1	-127.0
0	0	0	0	0	0	1	0	-126.5
ADC Gain Range -127dB to 0dB @ 0.5 increments								
1	1	1	1	1	1	1	0	-0.5
1	1	1	1	1	1	1	1	0.0

13.4. DIGITAL TO ANALOG CONVERTER (DAC) LIMITER REGISTERS

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x18	DACLIMEN	DACLIMDCY[3:0]				DACLIMATK[3:0]				**0x032**
0x19	0	0	DACLIMTHL[2:0]			DACLIMBST[3:0]				**0x000**

DAC Limiter Decay time (per 6dB gain change) for 44.1 kHz sampling. Note that these will scale with sample rate				
DACLIMDCY[3:0]				
B3	**B2**	**B1**	**B0**	**Decay Time**
0	0	0	0	544.0 us
0	0	0	1	1.1 ms
0	0	1	0	2.2 ms
0	0	1	1	4.4 ms
0	1	0	0	8.7 ms
0	1	0	1	17.4 ms
0	1	1	0	35.0 ms
0	1	1	1	69.6 ms
1	0	0	0	139.0 ms
1	0	0	1	278.5 ms
1	0	1	0	557.0 ms
1	0	1	1	1.1 s
To				
1	1	1	1	

DAC Limiter Attack time (per 6dB gain change) for 44.1 kHz sampling. Note that these will scale with sample rate				
DACLIMATK[3:0]				
B3	**B2**	**B1**	**B0**	**Attack Time**
0	0	0	0	68 us
0	0	0	1	136 us
0	0	1	0	272 us
0	0	1	1	544 us
0	1	0	0	1.1 ms
0	1	0	1	2.2 ms
0	1	1	0	4.4 ms
0	1	1	1	8.7 ms
1	0	0	0	17.4 ms
1	0	0	1	35 ms
1	0	1	0	69.6 ms
1	0	1	1	139 ms
To				
1	1	1	1	

DAC Limiter Programmable signal threshold level (determines level at which the limiter starts to operate)			
DACLIMTHL[3:0]			**Threshold (dB)**
B2	**B1**	**B0**	
0	0	0	-1
0	0	1	-2
0	1	0	-3
0	1	1	-4
1	0	0	-5
1	0	1	-6
To			
1	1	1	

DAC Digital Limiter	
Bit	**DACLIMEN[8]**
0	Disabled
1	Enabled

DAC Limiter volume Boost (can be used as a stand alone volume Boost when DACLIMEN=0)				
DACLIMBST[3:0]				**Boost (dB)**
B3	**B2**	**B1**	**B0**	
0	0	0	0	0
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7
1	0	0	0	+8
1	0	0	1	+9
1	0	1	0	+10
1	0	1	1	+11
1	1	0	0	+12
1	1	0	1	Reserved
To				
1	1	1	1	

13.5. NOTCH FILTER REGISTERS

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x1B	NFCU	NFCEN	NFCA0[13:7]							**0x000**
0x1C	NFCU	0	NFCA0[6:0]							**0x000**
0x1D	NFCU	0	NFCA1[13:7]							**0x000**
0x1E	NFCU	0	NFCA1[6:0]							**0x000**

The Notch Filter is enabled by setting NFCEN[7] address (0x1B) bit to HIGH. The coefficients, A_0 and A_1, should be converted to 2's complement numbers to determine the register values. A_0 and A_1 are represented by the register bits NFCA0[13:0] and NFCA1[13:0]. Since there are four register of coefficients, a Notch Filter Update bit is provided so that the coefficients can be updated simultaneously. NFCU[8] is provided in all registers of the Notch Filter coefficients but only one bit needs to be toggled for LOW – HIGH – LOW for an update. If any of the NFCU[8] bits are left HIGH then the Notch Filter coefficients will continuously update. An example of how to calculate is provided in the Notch Filter section.

Name	A_0	A_1	Notation	Register Value (DEC)
Coefficient	$\frac{1-\tan\left(\frac{2\pi f_b}{2f_s}\right)}{1+\tan\left(\frac{2\pi f_b}{2f_s}\right)}$	$-\left(1+A_0\right)x\cos\left(\frac{2\pi f_c}{f_s}\right)$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) fs = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ (then convert to 2's complement)

13.6. AUTOMATIC LEVEL CONTROL 1 REGISTER

13.6.1. ALC1 REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x20	ALCEN	0	0	ALCMXGAIN[2:0]			ALCMNGAIN[2:0]			**0x038**

Maximum Gain			
ALCMXGAIN[2:0]			**Mode**
B2	**B1**	**B0**	
0	0	0	-6.75dB
0	0	1	-0.75dB
0	1	0	+5.25dB
0	1	1	+11.25dB
1	0	0	+17.25dB
1	0	1	+23.25dB
1	1	0	+29.25dB
1	1	1	+35.25dB

Minimum Gain			
ALCMNGAIN[2:0]			**Mode**
B2	**B1**	**B0**	
0	0	0	-12dB
0	0	1	-6dB
0	1	0	0dB
0	1	1	+6dB
1	0	0	+12dB
1	0	1	+18dB
1	1	0	+24dB
1	1	1	+30dB

Name	ALC Enable
Bit	**ALCEN[8]**
0	Disabled (PGA gain set by PGAGAIN register bits)
1	Enabled (ALC controls PGA gain)

13.6.2. ALC2 REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x21	ALCZC	ALCHT[3:0]				ALCSL[3:0]				**0x00B**

ALC HOLD TIME before gain is increased.				
ALCHT[3:0]				**ALC Hold Time (sec)**
B7	**B6**	**B5**	**B4**	
0	0	0	0	0
0	0	0	1	2 ms
Time Doubles with every increment				
1	0	0	1	512 ms
1	0	1	0	1 s
To				
1	1	1	1	

ALC TARGET – sets signal level at ADC input				
ALCSL[3:0]				**ALC Target Level (dB)**
B3	**B2**	**B1**	**B0**	
0	0	0	0	-28.5 fs
0	0	0	1	-27 fs
ALC Target Level Range -28.5dB to -6dB @ 1.5dB increments				
1	1	0	0	-10.5 fs
1	1	0	1	-9 fs
1	1	1	0	-7.5 fs
1	1	1	1	-6 fs

Name	ALC Zero Crossing Detect
Bit	**ALCZC[8]**
0	Disabled
1	Enabled

It is recommended that zero crossing should not be used in conjunction with the ALC or Limiter functions

13.6.3. ALC3 REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x22	ALCM	ALCDCY[3:0]				ALCATK[3:0]				**0x032**

ALC DECAY TIME									
ALCDCY[3:0]				**ALCM = 0 (Normal Mode)**			**ALCM = 1 (Limiter Mode)**		
B3	**B2**	**B1**	**B0**	**Per Step**	**Per 6dB**	**90% of Range**	**Per Step**	**Per 6dB**	**90% of Range**
0	0	0	0	500 us	4 ms	28.78 ms	125 us	1 ms	7.2 ms
0	0	0	1	1 ms	8 ms	57.56 ms	250 us	2 ms	14.4 ms
0	0	1	0	2 ms	16 ms	115 ms	500 us	4 ms	28.8 ms
Time doubles with every increment									
1	0	0	0	128 ms	1 s	7.37 s	32 ms	256 ms	1.8 s
1	0	0	1	256 ms	2 s	14.7 s	64 ms	512 ms	3.7 s
1	0	1	0	512 ms	4 s	29.5 s	128 ms	1 s	7.37 s
To									
1	1	1	1						

ALC ATTACK TIME									
ALCATK[3:0]				**ALCM = 0 (Normal Mode)**			**ALCM = 1 (Limiter Mode)**		
B3	**B2**	**B1**	**B0**	**Per Step**	**Per 6dB**	**90% of Range**	**Per Step**	**Per 6dB**	**90% of Range**
0	0	0	0	125 us	1 ms	7.2 ms	31 us	248 us	1.8 ms
0	0	0	1	250 us	2 ms	14.4 ms	62 us	496 us	3.6 ms
0	0	1	0	500 us	4 ms	28.85 ms	124 us	992 us	7.15 ms
Time doubles with every increment									
1	0	0	0	26.5 ms	256 ms	1.53 s	7.9 ms	63.2 ms	455.8 ms
1	0	0	1	53 ms	512 ms	3.06 s	15.87 ms	127 ms	916 ms
1	0	1	0	128 ms	1 s	7.89 s	31.7ms	254 ms	1.83 s
To									
1	1	1	1						

13.7. NOISE GAIN CONTROL REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x23	0	0	0	0	0	ALCNEN	ALCNTH[2:0]			**0x000**

Noise Gate Enable	
Bit	**ALCNEN[3]**
0	Disabled
1	Enabled

Noise Gate Threshold			
ALCNTH[2:0]			**Mode**
B2	**B1**	**B0**	
0	0	0	-39 dB
0	0	1	-45 dB
0	1	0	-51 dB
0	1	1	-57 dB
1	0	0	-63 dB
1	0	1	-69 dB
1	1	0	-75 dB
1	1	1	-81 dB

13.8. INPUT, OUTPUT, AND MIXERS CONTROL REGISTER

13.8.1. Attenuation Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x28	0	0	0	0	0	0	MOUTATT	SPKATT	0	**0x000**

	Attenuation Control	
Name	**Attenuation control for bypass path (output of input boost stage) to speaker mixer and Headphone mixer input**	
Bit	**MOUTATT[2]**	**SPKATT[1]**
0	0 dB	0 dB
1	-10 dB	-10 dB

13.8.2. Input Signal Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x2C	0	0	0	0	0	AUXM	AUXPGA	NMICPGA	PMICPGA	**0x003**

	Auxiliary Input mode	AUX amplifier output to input PGA signal source	MICN to input PGA negative terminal	Input PGA amplifier positive terminal to MIC+ or VREF
Bit	**AUXM[3]**	**AUXPGA[2]**	**NMICPGA[1]**	**PMICPGA[0]**
0	Inverting Buffer	AUX not connected to input PGA	MICN not connected to input PGA	Input PGA Positive terminal to VREF
1	Mixer (Internal Resistor bypassed)	AUX to input PGA Negative terminal	MICN to input PGA Negative terminal.	Input PGA Positive terminal to MICP through variable resistor

13.8.3. PGA Gain Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x2D	0	PGAZC	PGAMT	PGAGAIN[5:0]						**0x010**

Programmable Gain Amplifier Gain						
PGAGAIN[5:0]						
B5	**B4**	**B3**	**B2**	**B1**	**B0**	**Gain**
0	0	0	0	0	0	-12.00 dB
0	0	0	0	0	1	-11.25 dB
0	0	0	0	1	0	-10.50 dB
:::	:::	:::	:::	:::	:::	:::
0	0	1	1	1	1	-0.75 dB
0	1	0	0	0	0	0 dB
0	1	0	0	0	1	+0.75 dB
PGA Gain Range -12dB to +35.25dB @ 0.75 increment						
:::	:::	:::	:::	:::	:::	:::
1	1	1	1	0	1	33.75
1	1	1	1	1	0	34.50
1	1	1	1	1	1	35.25

	PGA Zero Cross Enable	Mute Control for PGA
Bit	**PGAZC[7]**	**PGAMT[6]**
0	Update gain when gain register changes	Normal Mode
1	Update gain on 1st zero cross after gain register write	PGA Muted

13.8.4. ADC Boost Control Registers

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x2F	PGABST	0	PMICBSTGAIN			0	AUXBSTGAIN			**0x100**

MIC+ pin to the input Boost Stage (NB, when using this path set PMICPGA=0):			
PMICBSTGAIN[2:0]			Gain (dB)
B2	B1	B0	
0	0	0	Path Disconnected
0	0	1	-12
0	1	0	-9
0	1	1	-6
1	0	0	-3
1	0	1	0
1	1	0	+3
1	1	1	+6

Auxiliary to Input Boost Stage			
AUXBSTGAIN[2:0]			Gain (dB)
B2	B1	B0	
0	0	0	Path Disconnected
0	0	1	-12
0	1	0	-9
0	1	1	-6
1	0	0	-3
1	0	1	0
1	1	0	+3
1	1	1	+6

Name	Input Boost
Bit	**PGABST[8]**
0	PGA output has +0dB gain through input Boost stage
1	PGA output has +20dB gain through input Boost stage

13.8.5. Output Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x31	0	0	0	0	0	MOUTBST	SPKBST	TSEN	AOUTIMP	**0x002**

	Headphone Output Boost Stage	Speaker Output Boost Stage	Thermal Shutdown	Analog Output Resistance
Bit	**MOUTBST[3]**	**SPKBST[2]**	**TSEN[1]**	**AOUTIMP[0]**
0	(1.0 x VREF) Gain Boost	(1.0 x VREF) Gain Boost	Disabled	~1kΩ
1	(1.5 x VREF) Gain Boost	(1.5 x VREF) Gain Boost	Enabled	~30 kΩ

13.8.6. Speaker Mixer Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x32	0	0	0	AUXSPK	0	0	0	BYPSPK	DACSPK	**0x001**

	Auxiliary to Speaker Mixer	Bypass path (output of Boost stage) to Speaker Mixer	DAC to Speaker Mixer
Bit	**AUXSPK[5]**	**BYPSPK[1]**	**DACSPK[0]**
0	Disconnected	Disconnected	Disconnected
1	Connected	Connected	Connected

13.8.7. Speaker Gain Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x36	0	SPKZC	SPKMT	SPKGAIN[5:0]						**0x039**

Speaker Gain						
SPKGAIN[5:0]						
B5	B4	B3	B2	B1	B0	Gain (dB)
0	0	0	0	0	0	-57.0
0	0	0	0	0	1	-56.0
:::	:::	:::	:::	:::	:::	:::
1	1	1	0	0	1	0.0
Speaker Gain Range -57 dB to +6 dB @ +1 increment						
:::	:::	:::	:::	:::	:::	:::
1	1	1	1	1	1	+6.0

	Speaker Gain Control Zero Cross	Speaker Output
Bit	**SPKZC[7]**	**SPKMT[6]**
0	Change Gain on Zero Cross ONLY	Speaker Enabled
1	Change Gain Immediately	Speaker Muted

13.8.8. Headphone Mixer Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x38	0	0	MOUTMXMT	0	0	0	AUXMOUT	BYPMOUT	DACMOUT	**0x001**

	MOUT Mute	Auxiliary to Headphone Mixer	Bypass path (output of Boost Stage) to Headphone Mixer	DAC to Headphone Mixer
Bit	**MOUTMXMT[6]**	**AUXMOUT[2]**	**BYPMOUT[1]**	**DACMOUT[0]**
0	Not Muted	Disconnected	Disconnected	Disconnected
1	Muted	Connected	Connected	Connected

During mute, the Headphone output will output VREF that can be used as a DC reference for a headphone out.

13.9. LOWER POWER REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3A	LPIPBST	LPADC	LPSPKD	LPDAC	0	TRIMREG[3:2]		IBADJ[1:0]		**0x000**

B1	**B0**	Trim Output Regulator (V)	Adjust Master Bias of the Analog Portion
		TRIMREG[3:2]	**IBADJ[1:0]**
0	0	1.800	Default Current Consumption
0	1	1.610	25% Current Increase from Default
1	0	1.400	14% Current Decrease from Default
1	1	1.218	25% Current Decrease from Default

Trim regulator bits can be used only when VDDD <2.7V.

	Low Power IP Boost	Low Power ADC	Low Power Speaker Driver	Low Power DAC
Bit	**LPIPBST[8]**	**LPADC[7]**	**LPSPKD[6]**	**LPDAC[5]**
0	Normal Function	Normal Function	Normal Function	Normal Function
1	Cut power in half	Cut power in half	Cut power in half	Cut power in half

Note cutting the power in half will directly affect the audio performances.

13.10. PCM TIME SLOT CONTROL & ADCOUT IMPEDANCE OPTION CONTROL

13.10.1. PCM1 TIMESLOT CONTROL REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3B	TSLOT[8:0]									**0x000**

Transmit and receive timeslot are expressed in number of BCLK cycles in a 10-bit word. The most significant bit TSLOT[9] is located in register PCMTS2[0] address (0x3C). Timeslot, TSLOT[9:0], determines the start point for the timeslot on the PCM interface for data in the transmit direction.

13.10.2. PCM2 TIMESLOT CONTROL REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3C	PCMTSEN	TRI	PCM8BIT	PUDOEN	PUDPE	PUDPS	LOUTR	PCMB	TSLOT[9]	**0x000**

Name	PCM Mode1	Tri-state PCMT LSB	PCM Word Length	Left and Right Channel have same data	PCM Mode2
Bit	**PCMTSEN[8]**	**TRI[7]**	**PCM8BIT[6]**	LOUTR	PCMB
0	PCM A	Drive the full Clock of LSB	Use WLEN[6:5] to select Word Length	Disable	Disable
1	PCM Time Slot	Tri-State the 2nd half of LSB	Audio interface will be 8 Bit Word Length	Enable	Enable

If TRI = 1 and PUDOEN = 0, the device will drive the LSB bit 1st half of BCLK out of the ADCOUT pin (stop driving after LSB BCLK Rising edge) but if TRI = 0 or PUDOEN = 1 this feature is disabled, full BCLK of LSB will be driven the LSB value.

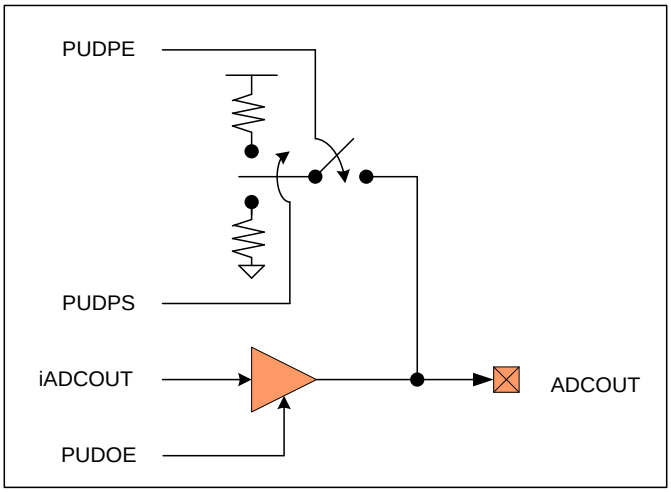


Figure 31: The Programmable ADCOUT Pin

Internal ADC out data	Power Up and Down Output Enable	Power Up and Down Pull Enable	Power Up and Down Pull Select	OUTPUT
iADCOUT	**PUDOEN[5]**	**PUDPE[4]**	**PUDPS[3]**	**PAD**
0	1	x	x	0
1	1	x	x	1
x	0	0	x	Hi-Z
x	0	1	0	Pull-Low
x	0	1	1	Pull-High

13.11. Reserved

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x41	1	0	0	1	0	0	1	0	0	**0x124**

13.12. OUTPUT Driver Control Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x45	0				MOUTMT	0	HVOPU	0	HVOP	**0x001**

Bit Location	Bit Description	Bit Name	Bit Value	
			0	**1**
0	Override to automatic 3V/5V bias selection	**HVOP**	set internal output biasing to be optimal for 3.6Vdc or lower operation **Note: For this to be effective HVOPU[2] address 0x45 must set**	set internal output biasing to be optimal for higher than 3.6Vdc operation **Note: For this to be effective HVOPU[2] address 0x45 must set**
2	Update bit for HV override feature	**HVOPU**	High Voltage override Disable	This bit must set in conjunction with HVOP[0] address 0x45 for the automatic override to be effective
4	Headphone out mute	**MOUTMT**	Disable	Enable

During mute, the MONO output will output VREF that can be used as a DC reference for a headphone out.

13.13. AUTOMATIC LEVEL CONTROL ENHANCED REGISTER

13.13.1. ALC1 Enhanced Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x46	ALCTBLSEL	ALCPKSEL	ALCNGSEL	0						**0x001**

Bit Location	Bit Description	Bit Name	Bit Value	
			0	**1**
6	Selects one of two tables used to set the target level for the ALC	**ALCNGSEL**	default recommended target level table spanning -1.5dB through -22.5dB FS	optional ALC target level table spanning -6.0dB through -28.5dB FS
7	Choose peak or peak-to-peak value for ALC threshold logic	**ALCPKSEL**	use rectified peak detector output value	use peak-to-peak detector output value
8	Choose peak or peak-to-peak value for Noise Gate threshold logic	**ALCTBLSEL**	use rectified peak detector output value	use peak-to-peak detector output value

13.13.2. ALC Enhanced 2 Register

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x47	PKLIMEN	0								**0x000**

Bit Location	Bit Description	Bit Name	Bit Value	
			0	**1**
8	Enable control for ALC fast peak limiter function	**PKLIMEN**	Enable	Disable

13.14. MISC CONTROL REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x49	SPIEN	FSERRVAL[1:0]		FSERFLSH	FSERRENA	NFDLY	DACINMT	0		**0x000**

Bit Location	Bit Description	Bit Name	Bit Value	
			0	**1**
2	Enable control to mute DAC limiter output when softmute is enabled	**DACINMT**	DAC limiter output may not move to exactly zero during Softmute (default)	DAC limiter output muted to exactly zero during softmute
3	Enable control to delay use of notch filter output when filter is enabled	**NFDLY**	delay using notch filter output 512 sample times after notch enabled (default)	use notch filter output immediately after notch filter is enabled
4	Enable control for short frame cycle detection logic	**FSERRENA**	short frame cycle detection logic enabled	short frame cycle detection logic disabled
5	Enable DSP state flush on short frame sync event	**FSERFLSH**	ignore short frame sync events (default)	set DSP state to initial conditions on short frame sync event
8	Set SPI control bus	**SPIEN**	Default Operation SPI Interface 16-bit	SPI Interface 24-bit

B1	**B0**	Short frame sync detection period value **FSERRVAL[1:0]**
0	0	trigger if frame time less than 255 MCLK edges
0	1	trigger if frame time less than 253 MCLK edges
1	0	trigger if frame time less than 254 MCLK edges
1	1	trigger if frame time less than 255 MCLK edges

13.15. Output Tie-Off REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x4B	0						MANVREFH	MANVREFM	MANVREFL	**0x000**

Bit Location	Bit Description	Bit Name	Bit Value	
			0	**1**
0	Direct manual control for switch for Vref 6k-ohm resistor to ground	MANVREFL	switch to ground controlled by Register 0x01 setting	switch to ground in the closed position
1	Direct manual control for switch for Vref 160k-ohm resistor to ground	MANVREFM	switch to ground controlled by Register 0x01 setting	switch to ground in the closed position
2	Direct manual control of switch for Vref 600k-ohm resistor to ground	MANVREFH	switch to ground controlled by Register 0x01 setting	switch to ground in the closed positioin

13.16. Output Tie-off Direct Manual Control REGISTER

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x4F	MANOUTEN	SBUFH	SBUFL	SNSPK	SPSPK	SMOUT	0	0	0	**0x000**

Bit Location	Bit Description	Bit Name	Bit Value	
			0	1
3	If MANUOUTEN = 1, use this bit to control Auxout1 output tie-off resistor switch	**SMOUT**	tie-off resistor switch for MOUT output is forced open	tie-off resistor switch for MOUT output is forced closed
4	If MANUOUTEN = 1, use this bit to control left speaker output tie-off resistor switch	**SPSPK**	tie-off resistor switch for SPKOUTP speaker output is forced open	tie-off resistor switch for SPKOUTP speaker output is forced closed
5	If MANUOUTEN = 1, use this bit to control left speaker output tie-off resistor switch	**SNSPK**	tie-off resistor switch for SPKOUTN speaker output is forced open	tie-off resistor switch for SPKOUTN speaker output is forced closed
6	If MANUOUTEN = 1, use this bit to control bypass switch around 1.0x non-boosted output tie-off buffer amplifier	**SBUFL**	normal automatic operation of bypass switch	bypass switch in closed position when output buffer amplifier is disabled
7	If MANUOUTEN = 1, use this bit to control bypass switch around 1.5x boosted output tie-off buffer amplifier	**SBUFH**	normal automatic operation of bypass switch	bypass switch in closed position when output buffer amplifier is disabled
8	Enable direct control over output tie-off resistor switching	**MANOUTEN**	ignore Register 0x4F bits to control input tie-off resistor/buffer switching	use Register 0x4F bits to override automatic tie-off resistor/buffer switching

14. CONTROL INTERFACE TIMING DIAGRAM

14.1. SPI WRITE TIMING DIAGRAM

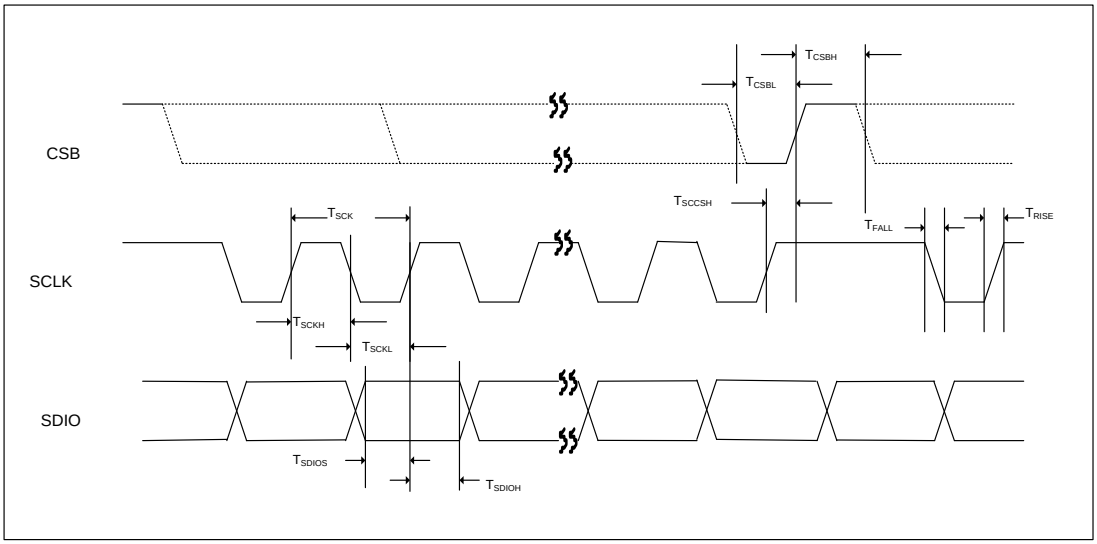


Figure 32: SPI Write Timing Diagram

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	80	---	---	ns
T_{SCKH}	SCLK High Pulse Width	35	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	35	---	---	ns
T_{RISE}	Rise Time for all SPI Signals	---	---	10	ns
T_{FALL}	Fall Time for all SPI Signals	---	---	10	ns
T_{SCCSH}	Last SCLK Rising Edge to CSb Rising Edge Hold Time	30	---	---	ns
T_{CSBL}	CSb Low Time	30	---	---	ns
T_{CSBH}	CSb High Time between CSb Lows	30	---	---	ns
T_{SDIOS}	SDIO to SCLK Rising Edge Setup Time	20	---	---	ns
T_{SDIOH}	SCLK Rising Edge to SDIO Hold Time	20	---	---	ns

Table 26: SPI Timing Parameters

15. AUDIO INTERFACE TIMING DIAGRAM

15.1. AUDIO INTERFACE IN SLAVE MODE

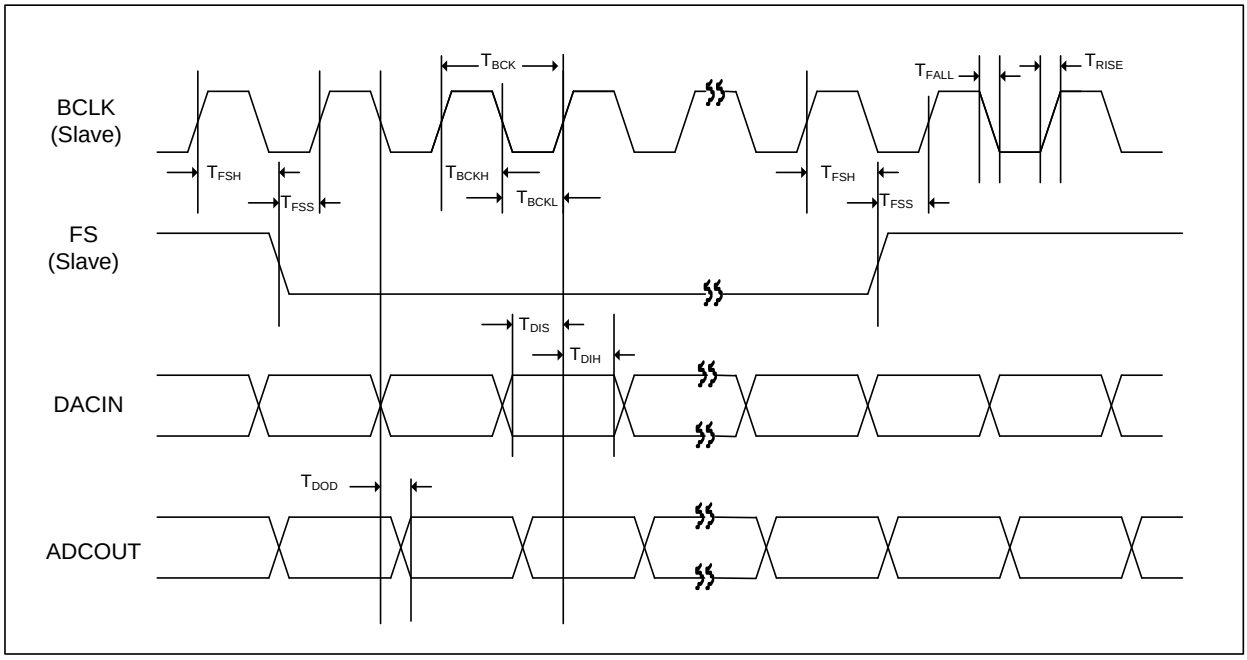


Figure 33: Audio Interface Slave Mode Timing Diagram

15.2. PCM AUDIO INTERFACE IN SLAVE MODE (PCM Audo Data)

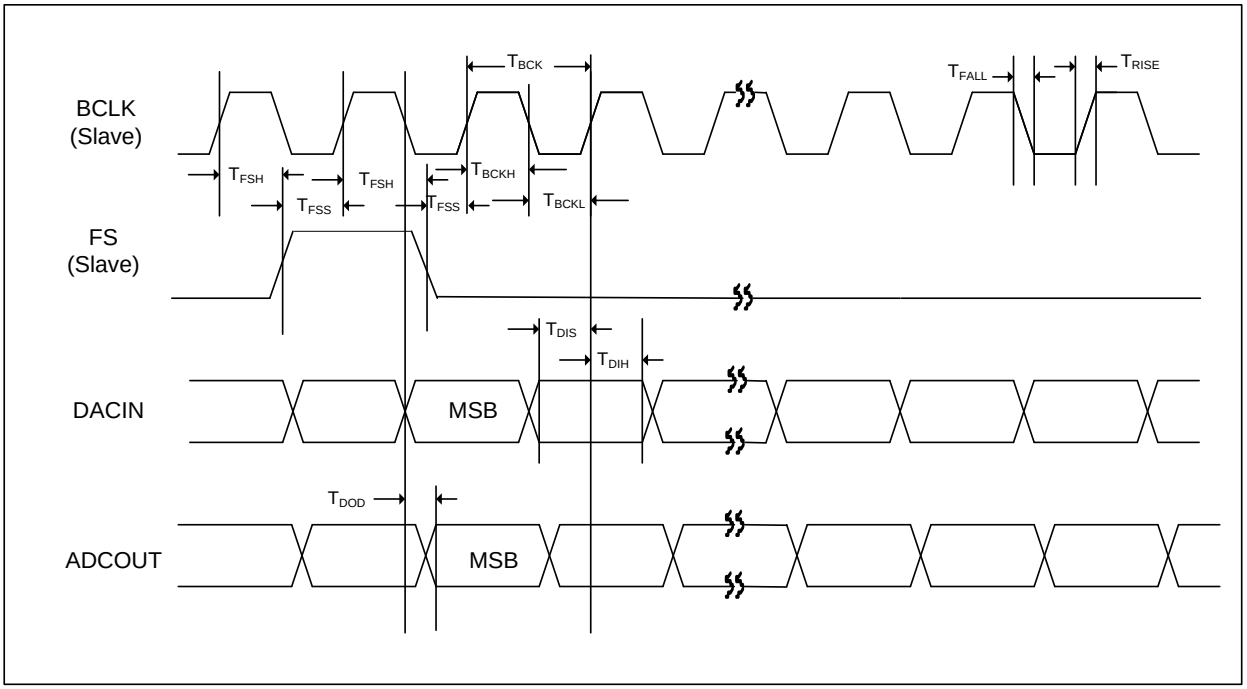


Figure 34: PCM Audio Interface Slave Mode Timing Diagram

15.3. PCM AUDIO INTERFACE IN SLAVE MODE (PCM Time Slot Mode)

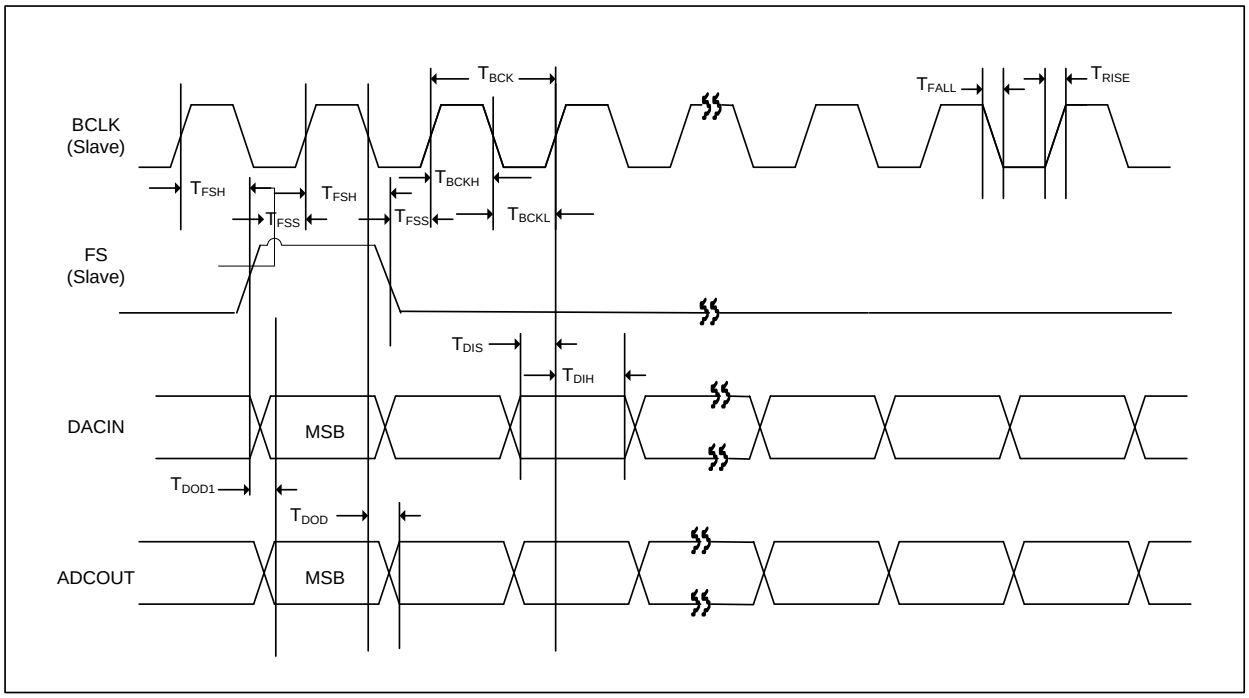


Figure 35: PCM Audio Interface Slave Mode (PCM Time Slot Mode)Timing Diagram

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{BCK}	BSCK Cycle Time	50	---	---	ns
T_{BCKH}	BSCK High Pulse Width	20	---	---	ns
T_{BCKL}	BSCK Low Pulse Width	20	---	---	ns
T_{FSS}	fs to SCK Rising Edge Setup Time	20	---	---	ns
T_{FSH}	SCK Rising Edge to fs Hold Time	20	---	---	ns
T_{RISE}	Rise Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{FALL}	Fall Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{DIS}	ADCIN to SCK Rising Edge Setup Time	15	---	---	ns
T_{DIH}	SCK Rising Edge to ADCIN Hold Time	15	---	---	ns
T_{DOD}	Delay Time from SCLK falling Edge to DACOUT	---	---	10	ns

Table 27: Audio Interface Timing Parameters

15.4. μ-LAW ENCODE DECODE CHARACTERISTICS

Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
	D7	D6	D5	D4	D3	D2	D1	D0	
	Sign	Chord	Chord	Chord	Step	Step	Step	Step	
8159									
	1	0	0	0	0	0	0	0	8031
7903 : 4319	:	:	:	:	:	:	:	:	:
	1	0	0	0	1	1	1	1	4191
4063 : 2143	:	:	:	:	:	:	:	:	:
	1	0	0	1	1	1	1	1	2079
2015 : 1055	:	:	:	:	:	:	:	:	:
	1	0	1	0	1	1	1	1	1023
991 : 511	:	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	1	1	495
479 : 239	:	:	:	:	:	:	:	:	:
	1	1	0	0	1	1	1	1	231
223 : 103	:	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	1	1	99
95 : 35	:	:	:	:	:	:	:	:	:
	1	1	1	0	1	1	1	1	33
31 : 3	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0	2
1	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	1	0
0									

Notes:
Sign bit = 0 for negative values, sign bit = 1 for positive values

15.5. A-LAW ENCODE DECODE CHARACTERISTICS

Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
	D7	D6	D5	D4	D3	D2	D1	D0	
	Sign	Chord	Chord	Chord	Step	Step	Step	Step	
4096									
	1	0	1	0	1	0	1	0	4032
3968 : 2176	:	:	:	:	:	:	:	:	:
	1	0	1	0	0	1	0	1	2112
2048 : 1088	:	:	:	:	:	:	:	:	:
	1	0	1	1	0	1	0	1	1056
1024 : 544	:	:	:	:	:	:	:	:	:
	1	0	0	0	0	1	0	1	528
512 : 272	:	:	:	:	:	:	:	:	:
	1	0	0	1	0	1	0	1	264
256 : 136	:	:	:	:	:	:	:	:	:
	1	1	1	0	0	1	0	1	132
128 : 68	:	:	:	:	:	:	:	:	:
	1	1	1	0	0	1	0	1	66
64 : 2	:	:	:	:	:	:	:	:	:
	1	1	0	1	0	1	0	1	1
0									

Notes:
1. Sign bit = 0 for negative values, sign bit = 1 for positive values
2. Digital code includes inversion of all even number bits

15.6. µ-LAW / A-LAW CODES FOR ZERO AND FULL SCALE

Level	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- Full Scale	0	000	0000	0	010	1010

15.7. µ-LAW / A-LAW OUTPUT CODES (DIGITAL MW)

Sample	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
1	0	001	1110	0	011	0100
2	0	000	1011	0	010	0001
3	0	000	1011	0	010	0001
4	0	001	1110	0	011	0100
5	1	001	1110	1	011	0100
6	1	000	1011	1	010	0001
7	1	000	1011	1	010	0001
8	1	001	1110	1	011	0100

16. DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.025dB	0		0.454*fs	
	-6dB		0.5*fs		
Passband Ripple				+/-0.025	dB
Stopband		0.546*fs			
Stopband Attenuation	f > 0.546*fs	-60			dB
Group Delay			21/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter					
Passband	+/- 0.035dB	0		0.454*fs	
	-6dB		0.5*fs		
Passband Ripple				+/-0.035	dB
Stopband		0.546*fs			
Stopband Attenuation	f > 0.546*fs	-55			dB
Group Delay			29/fs		

Table 57 Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include

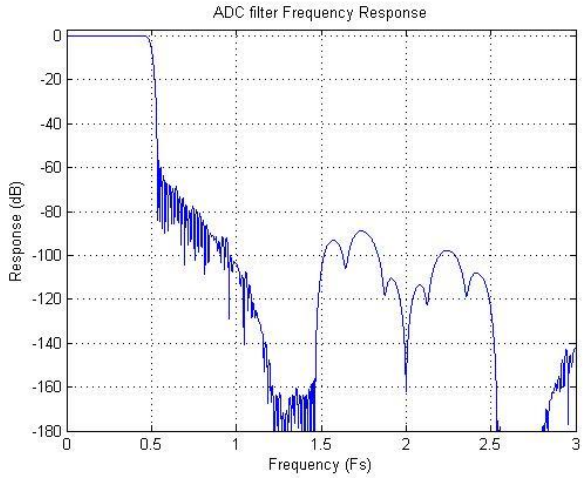


Figure 36: DAC Filter Frequency Response

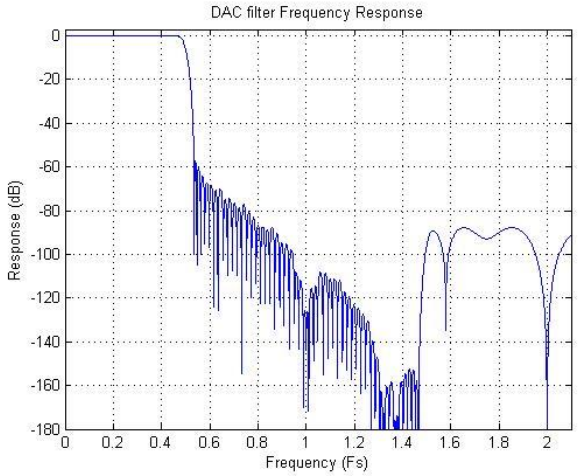


Figure 37: ADC Filter Frequency Response

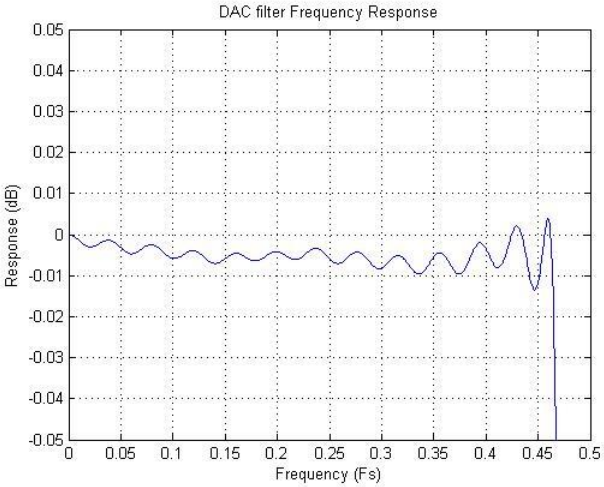


Figure 38: DAC Filter Ripple

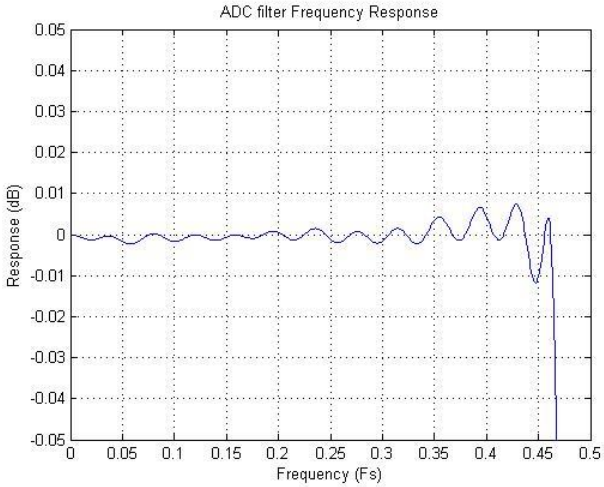


Figure 39: ADC Filter Ripple

17. TYPICAL APPLICATION

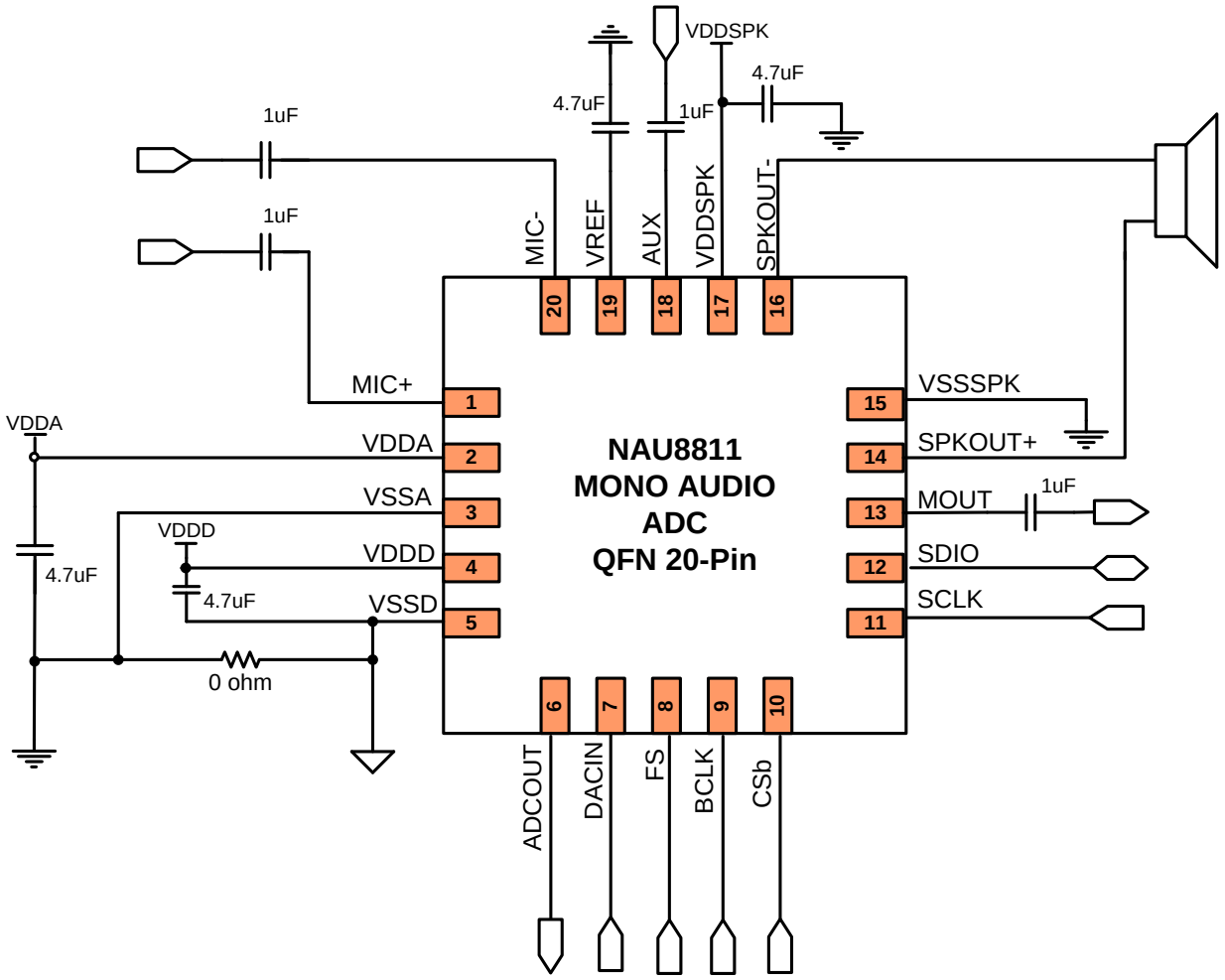


Figure 40: Application Diagram For 20-Pin QFN

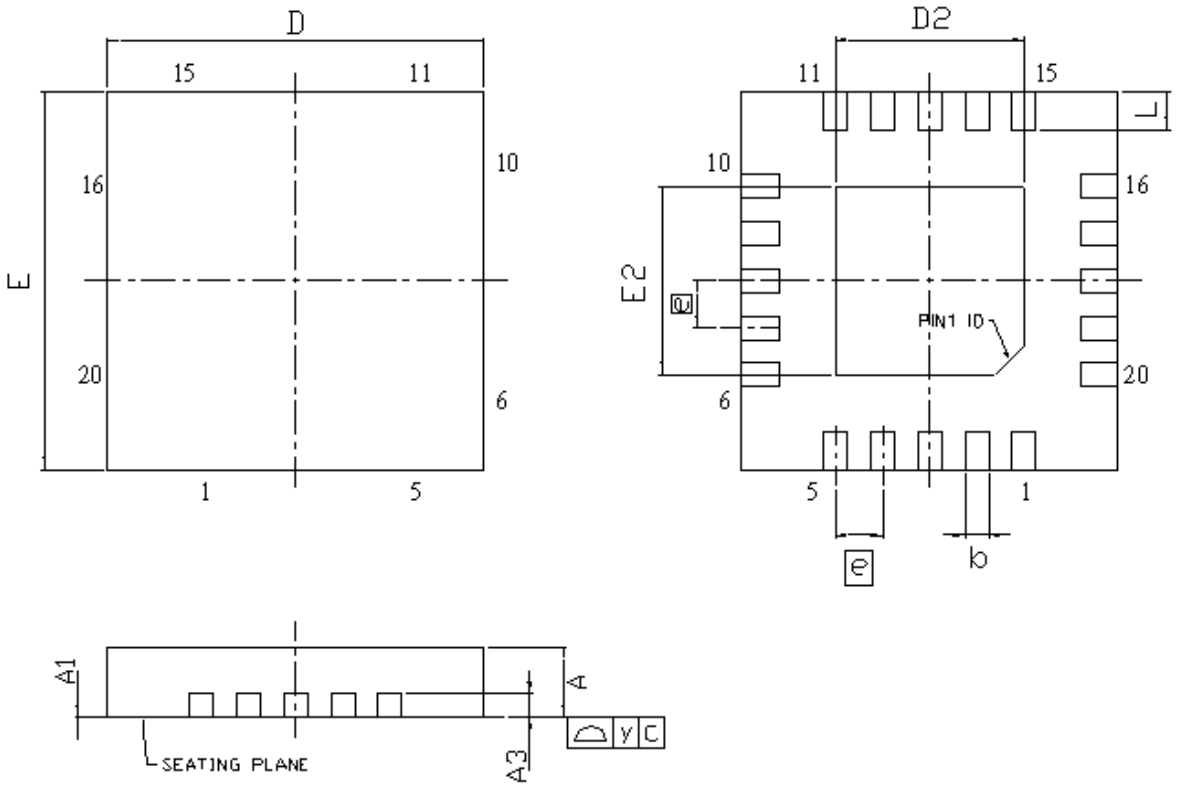
Note 1: All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR, additional 0.1uF and/or 0.01uF capacitors may be necessary in parallel with the bulk 4.7uF capacitors on the supply rails.

Note 2: Load resistors to ground on outputs may be helpful in some applications to insure a DC path for the output capacitors to charge/discharge to the desired levels. If the output load is always present and the output load provides a suitable DC path to ground, then the additional load resistors may not be necessary. If needed, such load resistors are typically a high value, but a value dependent upon the application requirements.

Note 3: To minimize pops and clicks, large polarized output capacitors should be a low leakage type.

Note 4: Depending on the microphone device and PGA gain settings, common mode rejection can be improved by choosing the resistors on each node of the microphone such that the impedance presented to any noise on either microphone wire is equal.

18. PACKAGE SPECIFICATION (20-Pin QFN)



Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note:D2,E2 by die size difference .

19. ORDERING INFORMATION

Nuvoton Part Number Description

NAU8811_ _

Package Material:
Package Type:
G = Pb-free Package
Y = 20-Pin QFN Package

20. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
1.0	September 2009		Preliminary Revision
1.1	October 2009	83	Package diagram updated.
1.2	November 2009	55 56 33 35 48	Register 0x05 description updated Register 0x06 description updated Table 16 updated Table 17 updated Table 22 updated
1.3	December 2009	3 52 72 82	Note added Register 0x49 info updated Register 0x49 info updated Application diagram updated
1.4	January 2010	13 81	BTL spec THD updated Application diagram updated
1.5	January 2010	12 -14 13	Electrical Specification table format updated BTL Speaker spec updated
1.6	March 2010	4 37 52, 70	Figure 2 updated Clocking block explanation updated Register 0x41 info updated
1.7	November 2011	24	Clarification regarding matching ALC gain with PGA gain when disabling ALC.
2.0	January 2011	Various 38 52	Removed Preliminary Status Removed trailing clock cycle from SPI timing diagram Corrected Register 0x38 Register name
2.1	January 2014	11 - 12	An additional remark of VDDSPK boost mode
2.2	March 2014	12 75 81	Headphone full scale output Corrected rising/falling time specification of I2S Modified application circuit
2.3	January 2015	1	AEC-Q100 note updated
2.4	July 2015	20,21,57	Change 3.7KHz to 3.7Hz
2.5	March 2016	Section 12.5	Add Important Notice

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.