NAU83G20
DataSheet

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1 GENERAL DESCRIPTION

1.1 Overview

The NAU83G20 is a monophonic amplifier device with DSP and V/I sense. The DSP ROM is programmed with a speaker excursion control algorithm. The target application for this device is mobile phone, tablet, and laptop market, where small speaker is used. Compared to traditional Class D amp, the NAU83G20 has 2 ADCs integrated such that speaker voltage and current can be sensed and sent back to the DSP for speaker excursion control. This speaker excursion control can prevent the speaker membrane excursion from exceeding its rated limit and provide ample headroom for overall loudness and sound quality.

1.2 Features

The NAU83G20 Monophonic Amplifier, with DSP and I/V Sense, and utilizes a powerful Class-D Amplifier. The chip features high output power capability, low-current shutdown mode, and click-and-pop suppression. Equipped with a DSP Core, numerous types of device protection schemes are supported, as well as speaker protection schemes, including ambient temperature monitoring input for enhanced speaker module design. The temperature monitoring in the NAU83G20 protects both the chip and the speaker from overheating. The chip is available in a 50-ball Wafer Level Chip Scale Package (WLCSP).

Key Feature List

- Powerful Class-D Amplifier:
  - Up to 10.8 Watts into an 8 Ohm load at 10% Total Harmonic Distortion and Noise (THD+N)
  - Up to 20 Watts into an 4 Ohm load at max. power
- ≥ 90 dB Power Supply Rejection Ratio (PSRR)
- Low Current Shutdown Mode
- Click-and-Pop Suppression (30 µVRMS)
- Programmable Serial Interfaces:
  - I2C Interface
  - I2S Interface
  - PCM Interface
- Device Protection:
  - Over Current Protection (OCP),
  - Over Voltage Protection (OVP)
  - Under Voltage Lock Out (UVLO)
  - Over Temperature Protection (OTP)
  - Clock Termination Protection (CTP)
- Speaker Protection:
  - Current & Voltage Sensing
  - Anti-Clip Protection (ACP)
  - Speaker Module Temperature Sense Input
- Battery Protection: Limiter
- Filter-less Electro Magnetic Interference (EMI) mitigation
- 50-Ball Wafer Level Chip Scale Package (WLCSP) (0.5 mm Pitch)
- Package is Halogen-free, RoHS-compliant and TSCA-compliant

Applications

- Smartphones
- Notebooks /Tablets/ Personal Computers
- Personal Media Players/Portable Televisions
- MP3 Lossless Standard Audio Compression Format Players
- Portable Game Players
- Digital Camcorders

2 PIN CONFIGURATIONS

2.1 Pin Diagrams

The NAU83G20 Monophonic Class-D Amplifier with DSP and I/V-Sense is available in a 50-Ball WLCSP package as shown in **Figure 1**.

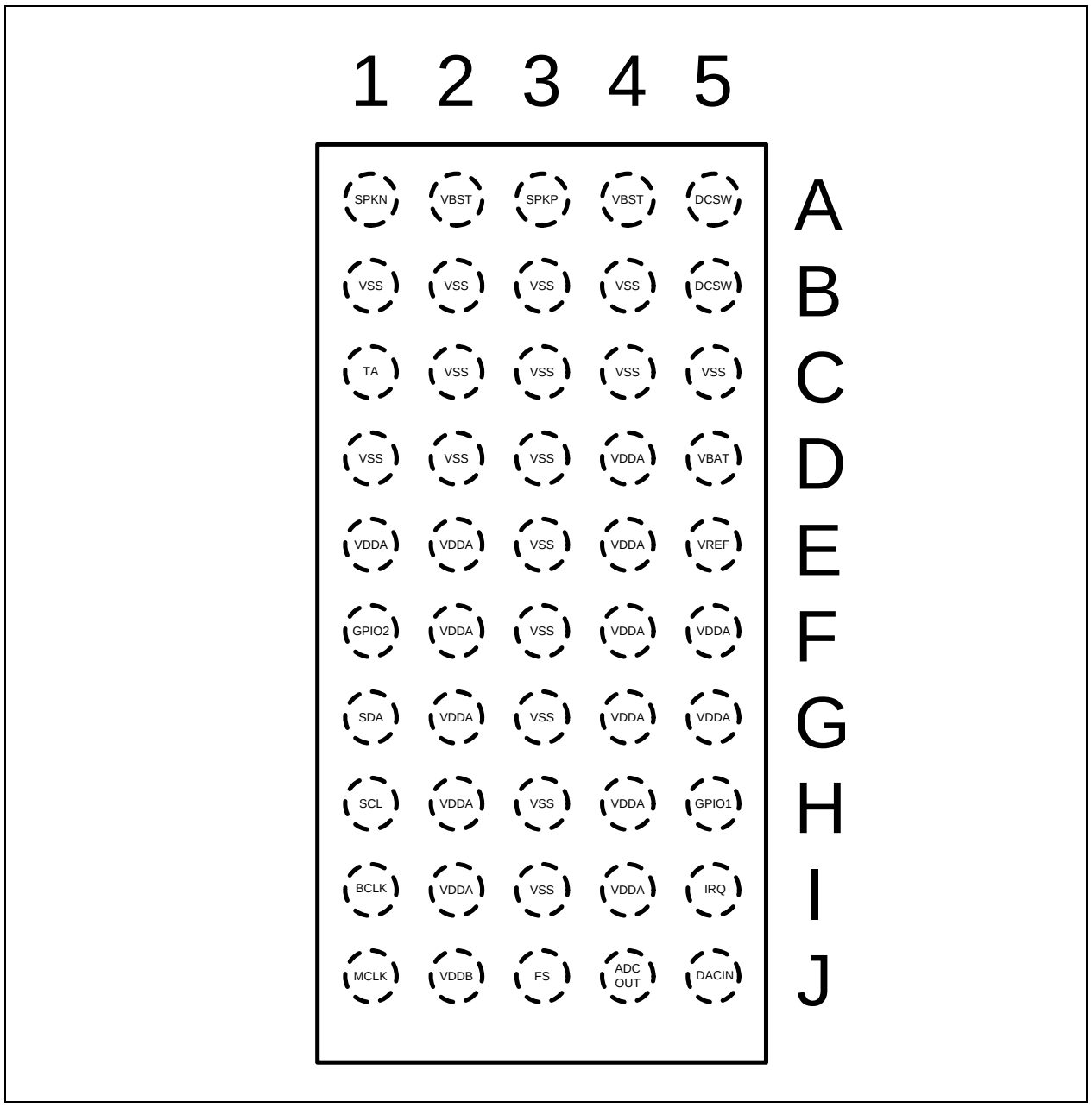


Figure 1 Pin Diagram of NAU83G20 (Top View)

2.2 PIN DESCRIPTIONS

Pin descriptions for the NAU83G20 Mono Class-D Amplifier with DSP and I/V Sense are provided in **Table 1.**

Table 1 Pin Descriptions for the NAU83G20

Pin #	Name	Type, (Supply Domain)	Description
A1	SPKN	Analog Output (VBAT)	Class-D Negative Speaker Output Terminal
A2	VBAT	Supply	Battery Supply
A3	SPKP	Analog Output (VBAT)	Class-D Positive Speaker Output Terminal
A4	VBAT	Supply	Battery Supply
A5	VDDD	Supply	Analog Supply Voltage
B1	VSS	Ground	Supply Ground
B2	VSS	Ground	Supply Ground
B3	VSS	Ground	Supply Ground
B4	VSS	Ground	Supply Ground
B5	VDDD	Supply	Analog Supply Voltage
C1	TA	Analog Input (VDDA)	Ambient Temperature Sense Input, tie to VSS if not used
C2	VSS	Ground	Supply Ground
C3	VSS	Ground	Supply Ground
C4	VSS	Ground	Supply Ground
C5	VSS	Ground	Supply Ground
D1	VSS	Ground	Supply Ground
D2	VSS	Ground	Supply Ground
D3	VSS	Ground	Supply Ground
D4	VDDA	Supply	Analog & Core Supply Voltage
D5	VDDD	Supply	Analog Supply Voltage
E1	VDDA	Supply	Analog & Core Supply Voltage
E2	VDDA	Supply	Analog & Core Supply Voltage
E3	VSS	Ground	Supply Ground
E4	VDDA	Supply	Analog & Core Supply Voltage
E5	VREF	Analog I/O (VDDA)	Internal DAC & ADC Voltage Reference Decoupling I/O
F1	GPIO2	Digital I/O (VDDB)	General Purpose IO2/Address Selection 2
F2	VDDA	Supply	Analog & Core Supply Voltage
F3	VSS	Ground	Supply Ground
F4	VDDA	Supply	Analog & Core Supply Voltage
F5	VDDA	Supply	Analog & Core Supply Voltage
G1	SDA	Digital I/O (VDDB)	Serial Data for I2C
G2	VDDA	Supply	Analog & Core Supply Voltage
G3	VSS	Ground	Supply Ground

Pin #	Name	Type, (Supply Domain)	Description
G4	VDDA	Supply	Analog & Core Supply Voltage
G5	VDDA	Supply	Analog & Core Supply Voltage
H1	SCL	Digital Input (VDDB)	Serial Data Clock for I2C
H2	VDDA	Supply	Analog & Core Supply Voltage
H3	VSS	Ground	Supply Ground
H4	VDDA	Supply	Analog & Core Supply Voltage
H5	GPIO1	Digital I/O (VDDB)	General Purpose IO1/Address Selection 1
I1	BCLK	Digital I/O (VDDB)	Serial Audio Data Bit Clock I2S/PCM Input
I2	VDDA	Supply	Analog & Core Supply Voltage
I3	VSS	Ground	Supply Ground
I4	VDDA	Supply	Analog & Core Supply Voltage
I5	IRQ	Digital Output (VDDB)	Programmable Interrupt Output
J1	MCLK	Digital Input (VDDB)	Master Clock
J2	VDDB	Supply	Digital IO Supply
J3	FS	Digital I/O (VDDB)	Frame Sync I2S/PCM Input
J4	ADCOUT	Digital Output (VDDB)	Serial Audio I2S/PCM Data Output
J5	DACIN	Digital Input (VDDB)	Serial Audio Data I2S/PCM Input

3 BLOCK DIAGRAM

A Block Diagram for the NAU83G20 is provided in **Figure 2**.

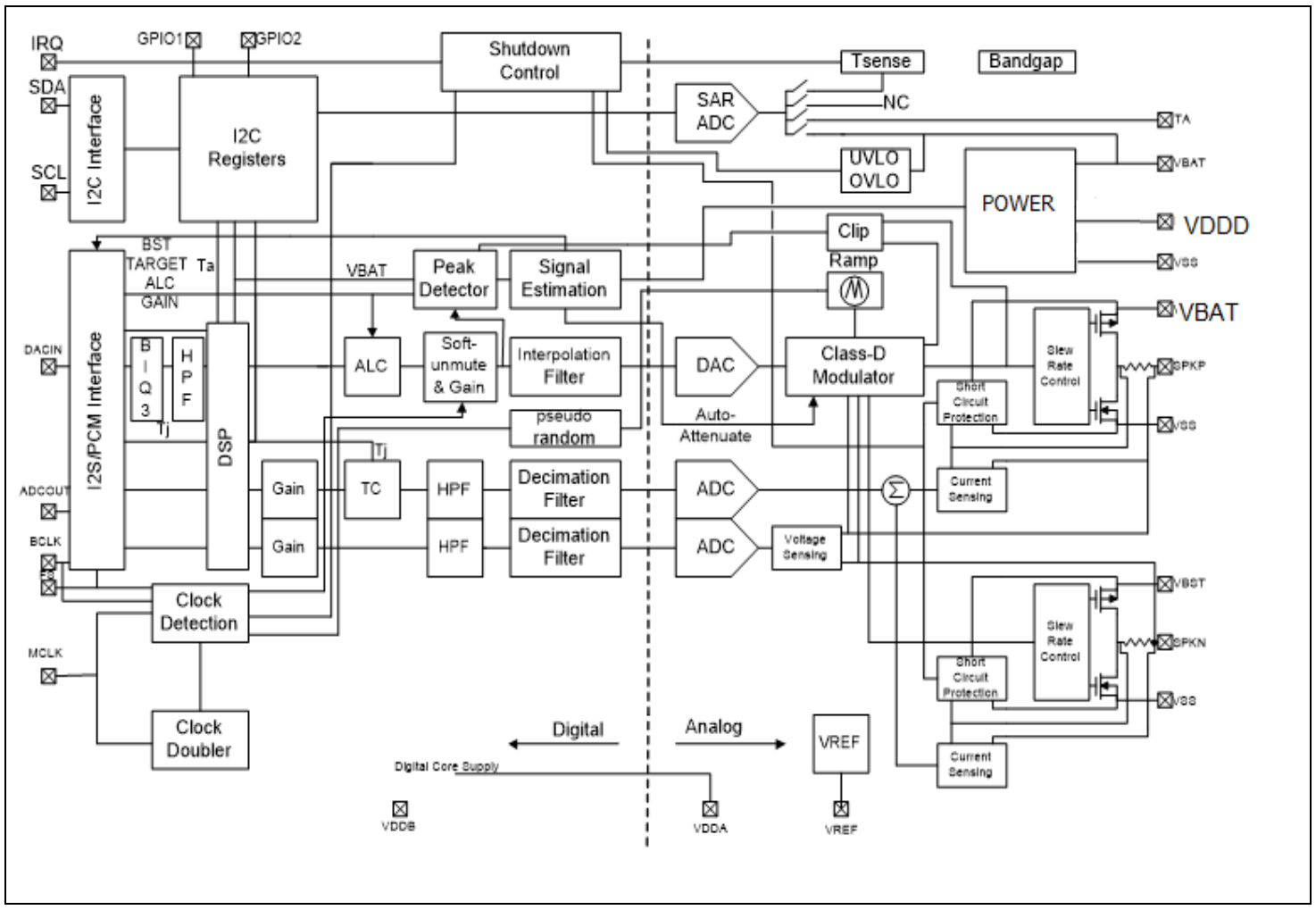


Figure 2 NAU83G20 Block Diagram

4 ELECTRICAL CHARACTERISTICS

The tables in this chapter provide the various electrical parameters for the NAU83G20 and their values.

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Min	Max	Units
VDDB Digital I/O Supply Range	-0.3	4.0	V
VDDD Analog Supply Range	-0.3	6.0	V
VBAT Supply Range	-0.3	16.5	V
VDDA Analog Supply Range	-0.3	2.2	V
Voltage Input Analog Range	VSS - 0.3	VDDA + 0.3	V
Voltage Input I/O Range	VSS - 0.3	VDDB + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

4.2 Operating Conditions

Table 3 Recommended Operating Conditions for the NAU83G20

Condition	Symbol	Min	Typical	Max	Units
Analog Supply Range	VDDD	2.90	4.2	5.50	V
Analog Supply Range	VDDA	1.62	1.8	1.98	V
Digital I/O Supply Range	VDDB	1.62	3.0	3.6	V
VBAT Analog Supply	VBAT	VDDD	12.6	14	V
Ground	VSS		0		V
Industrial Operating Temperature		-40		+85	°C

CAUTION: The following conditions needed to be followed for regular operation: VDDD > V_{DD}A -1.2V; VDDB > VDDA – 0.6V.

4.3 Thermal Information

Table 4 Thermal Information for the NAU83G20

Package	Power (W)	Ta (°C)	Theta JA (°C/W)			Theta JC (°C/W)
			0 m/s	1 m/s	2 m/s	
WLCSP50 2.57x5.28mm	1	85	34.21	31.47	30.42	3.46

4.4 Electrical Parameters

Table 5 Electrical Characteristics

Conditions: $V_{DD}A$ = $V_{DD}B$ = 1.8V; VDDD= 4.2V. VBAT=12.6V R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, MCLK=12.288MHz, Limits apply for T_A = 25°C

Symbol	Parameter		Conditions	Typical	Limit	Units
ISD	Shutdown Mode* Supply Current	$V_{DD}A$	all clocks off	15.0		µA
		$V_{DD}B$	all clocks off	0.3	2	
		VDDD	all clocks off	0.4	4	
		VBAT	All clocks off	0.1	TBD	
ISB	Standby Mode** Supply Current	$V_{DD}A$	clocks off, clock gating on	15.0		µA
		$V_{DD}B$	clocks off, clock gating on	0.3		
		VDDD	clocks off, clock gating on	0.4		
		VBAT	clocks off, clock gating on	0.3	TBD	
IDD	Idle Channel Operating Mode*** Supply Current	$V_{DD}A$	idle Channel , DSP off	8		mA
		$V_{DD}B$	idle Channel, DSP off	0.2		
		VDDD	idle Channel, DSP off	3		
		VBAT	idle Channel, DSP off	4		
Class-D Channel						
P_O	Output Power		RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	9.4		W
			RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%	10.8		W
			RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	17		W
			RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%	20		W
THD+N	Total Harmonic Distortion + Noise		R_L = 8 Ω + 33 µH, f=1kHz, P_O = 1 W	0.021		%

Symbol	Parameter	Conditions	Typical	Limit	Units
e_{OS}	Output Noise	A-Weighted, 20Hz-20kHz, no DAC input signal, gain = 19.1dB	65		µVrms
PSRR	Power Supply Rejection Ratio	DC, VDDD = 2.9V – 5.5V, GAIN = 19.1dB	88		dB
		f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} GAIN = 19.1dB	92		dB
		f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 200mV_{P_P} GAIN = 19.1dB	86		dB
		f_{RIPPLE} = 4kHz, V_{RIPPLE} = 200mV_{P_P} GAIN = 19.1dB	84		dB
Fres	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, R_L = 8 Ω + 33 µH	+-0.8		dB
V_{OS}	Output Offset Voltage	Idle Channel, Gain= 0dB	±0.7	±5	mV
Kpop	Pop and Click Noise	A-weighted, Idle DAC input, Clock Gating, toggling clocks on/off	0.03		mVrms
		A-weighted, Idle DAC input, toggling between -120dBFs DAC In & 2048 zero samples	0.03		mVrms
Rdson-P	Driver P MOS-FET ON-resistance	VDDD= 5.0V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.127		Ohm
Rdson-N	Driver N MOS-FET ON-resistance	VDDD= 5.0V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.129		Ohm
Fsw	Switching Frequency	Average	300		kHz
Voltage Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise	VDDD = 5.5V, +10dBVrms, Class-D off	0.004		%
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	101		dB
FS_{ADC}	ADC Full Scale Input Level		15.4		V_{PK}
Current Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise		0.37		%
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	82		dB
FS_{ADC}	ADC Full Scale Input Level		4.04		A_{PK}
Battery Sense ADC					
INL	Integrated Non-Linearity	VDDD= 2.9V-5.5V (gain & offset compensated)	+/-1		LSB
DNL	Differential Non-Linearity	VDDD= 2.9V-5.5V	+/-1		LSB

Symbol	Parameter	Conditions	Typical	Limit	Units
Class-D					
Neff	Power Efficiency	Output Power = 3 W, VDDD= 12 V	77		%
		Output Power = 6.0 W, VDDD = 12 V	85		%
		Output Power = 9.5 W, VDDD = 12 V	93		%

Note: *Shutdown mode: device has supplies without register loaded

** Standby Mode: device register settings loaded without I2S clocks appear

***Idle Channel operating mode: device register loaded and I2S clocks appear without DACIN

4.5 Digital I/O Parameters

Table 6 Digital I/O Characteristics

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	$V_{DD}B$ = 1.8V			0.3*$V_{DD}B$	V
		$V_{DD}B$ = 3.3V			0.34*$V_{DD}B$	
Input HIGH level	V_{IH}	$V_{DD}B$ = 1.8V		0.7*$V_{DD}B$		V
		$V_{DD}B$ = 3.3V		0.66*$V_{DD}B$		
Output HIGH level	V_{OH}	I_{Load} = 1mA	$V_{DD}B$=1.8V	0.9*$V_{DD}B$		V
			$V_{DD}B$ = 3.3V	0.95*$V_{DD}B$		
Output LOW level	V_{OL}	I_{Load} = 1mA	$V_{DD}B$ = 1.8V		0.1*$V_{DD}B$	V
			$V_{DD}B$=3.3V		0.05*$V_{DD}B$	
MCLK Dutycycle	D_{MCLK}	Clock Multiplier Enabled N1=1		48	52	%
		Clock Multiplier Enabled N1=1/3		44	56	
MCLK Jitter	j_{MCLK}	Clock Multiplier Enabled N1=1		-	0.1	nsec (Standard Deviation)
		Clock Multiplier Enabled N1=1/3		-	0.3	

4.6 THD+N Plots

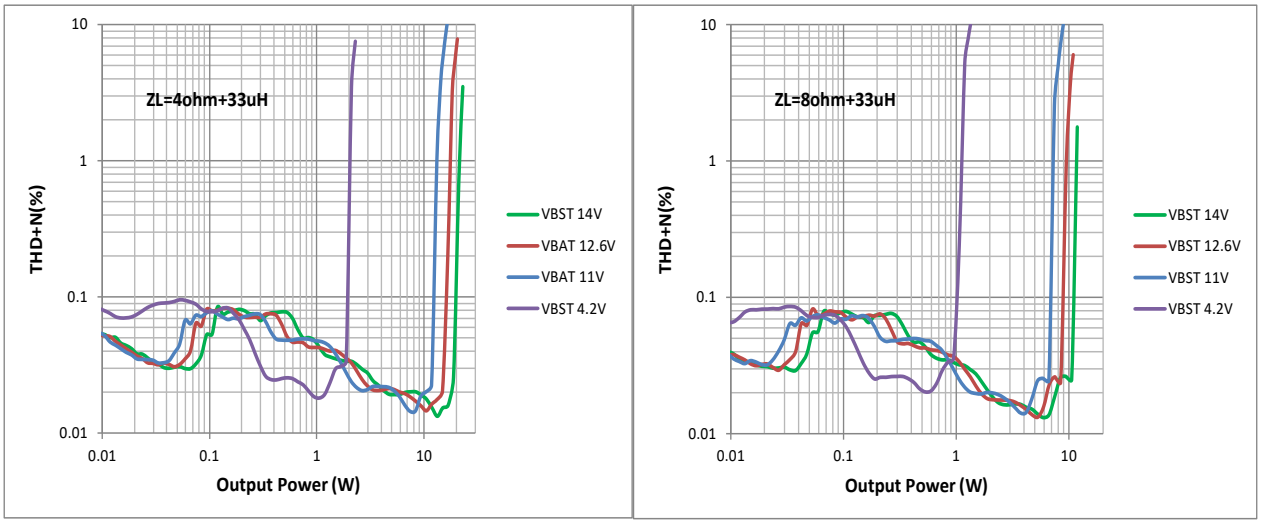


Figure 3 THD vs Po

4.7 PSRR Plots

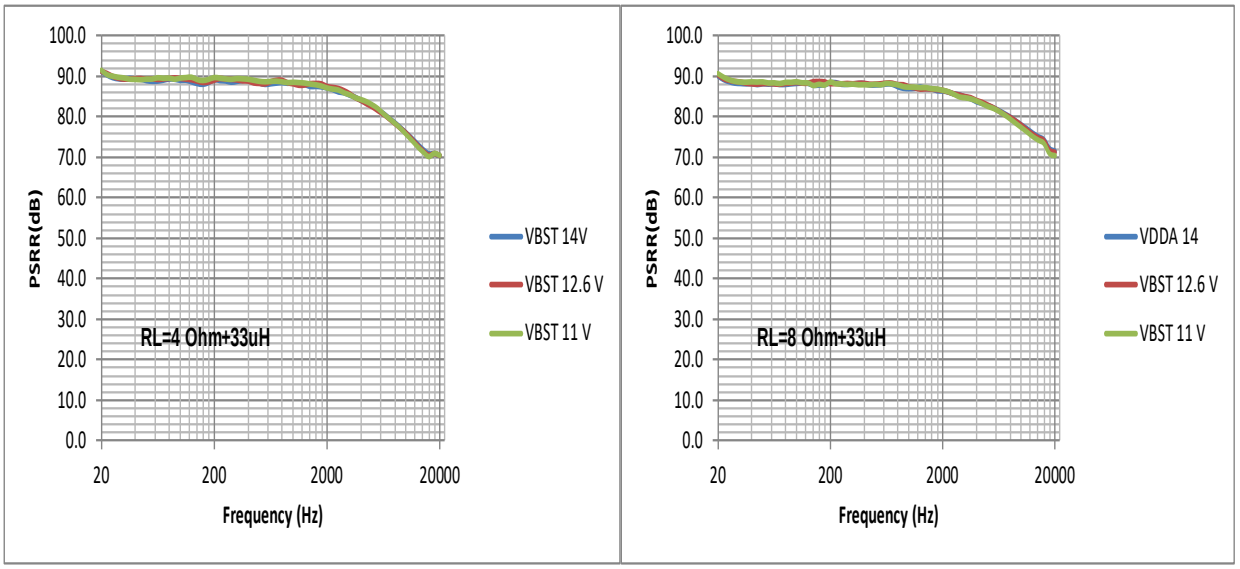


Figure 4 VBAT PSRR

4.8 Frequency Response Plots

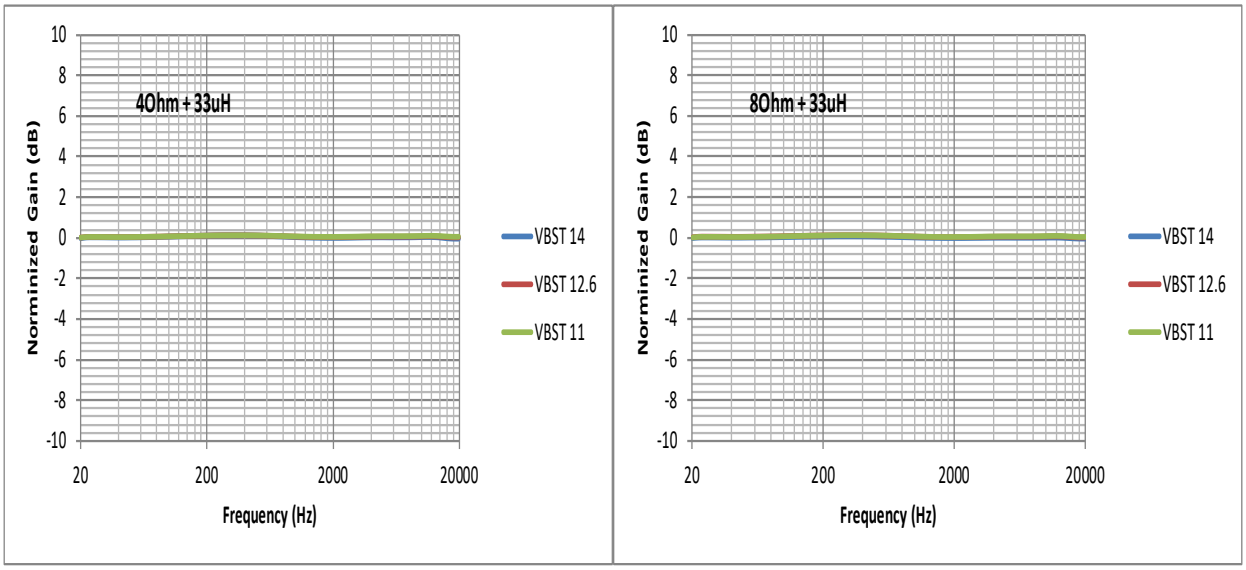


Figure 5 Frequency Response

4.9 Power Plots

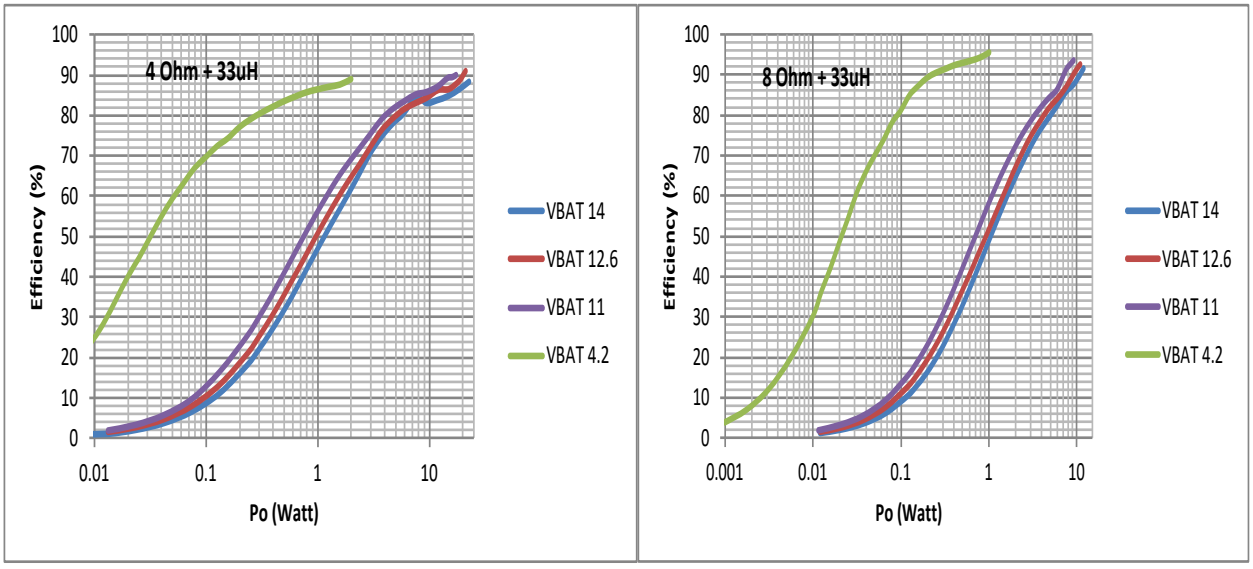


Figure 6 Efficiency vs Po

5 FUNCTIONAL DESCRIPTION

This chapter provides detailed descriptions of the major functions of the NAU83G20 Monophonic Amplifier.

5.1 Inputs

The NAU83G20 provides digital inputs to acquire and process audio signals with high fidelity and flexibility. There is an input path from an I2S/PCM Interface. Additionally, the NAU83G20 has logic control inputs and a temperature monitoring input.

5.2 Outputs

The NAU83G20 Amplifier has a Class-D PWM driver that can drive an 8 Ohm speaker up a peak voltage of 14 V. The Class-D output voltage and current sensing data are provided at the I2S/PCM Interface output. Additionally, the NAU83G20 has an output for the interrupt.

5.3 ADC, DAC and Digital Signal Processing

The NAU83G20 has two independent, high-quality Analog-to-Digital Converters (ADCs) and one Digital-to-Analog Converter (DAC). These are high-performance, 24-bit sigma-delta converters, which are suitable for a very wide range of applications.

The ADC and DAC blocks also support advanced Digital Signal Processing (DSP) subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and to maximize the audio dynamic range supported by the NAU83G20.

The ADC and DAC digital signal process can support four-point Dynamic Range Compressors (DRCs), high-pass filters, Automatic Level Control (ALC), soft mute, soft unmute and gain compensation. Two-point DRCs can be programmed to limit the maximum output level and/or amplify a low output level.

5.4 Digital Interfaces

Command and control of the device are accomplished by using a Serial Control Interface. The simple, but highly flexible, 2-wire Serial Control Interface is compatible with most commonly used command and control serial data protocols and host drivers, and industry standard I2S and PCM devices.

The digital audio I/O data streams can be transferred separately from command and control using either I2S or PCM audio data protocols.

5.5 Power Supply

This NAU83G20 has been designed to operate reliably under a wide range of power supply conditions and Power-On/Power-Off sequences. However, the Electro Static Detection (ESD) protection diodes between the supplies impact the application of the supplies. Because of these diodes, the following conditions need to be met:

$$VDDD > VDDA - 1.2\ V \text{ and } VDDB > VDDA - 0.6\ V$$

5.6 Power-On-and-Off Reset

The NAU83G20 includes a Power-On-and-Off Reset circuit on-chip. The circuit resets the internal logic control at VDDD and VDDA supply power-up and this reset function is automatically generated internally when power supplies are too low for reliable operation. Reset thresholds are 1.4 V for VDDA during a power-

on ramp and 1.2 V for VDDA during a power-down ramp. Reset thresholds are 1.6 V for VDDD during a power-on ramp, and 1.2 V for VDDD during a power-down ramp. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

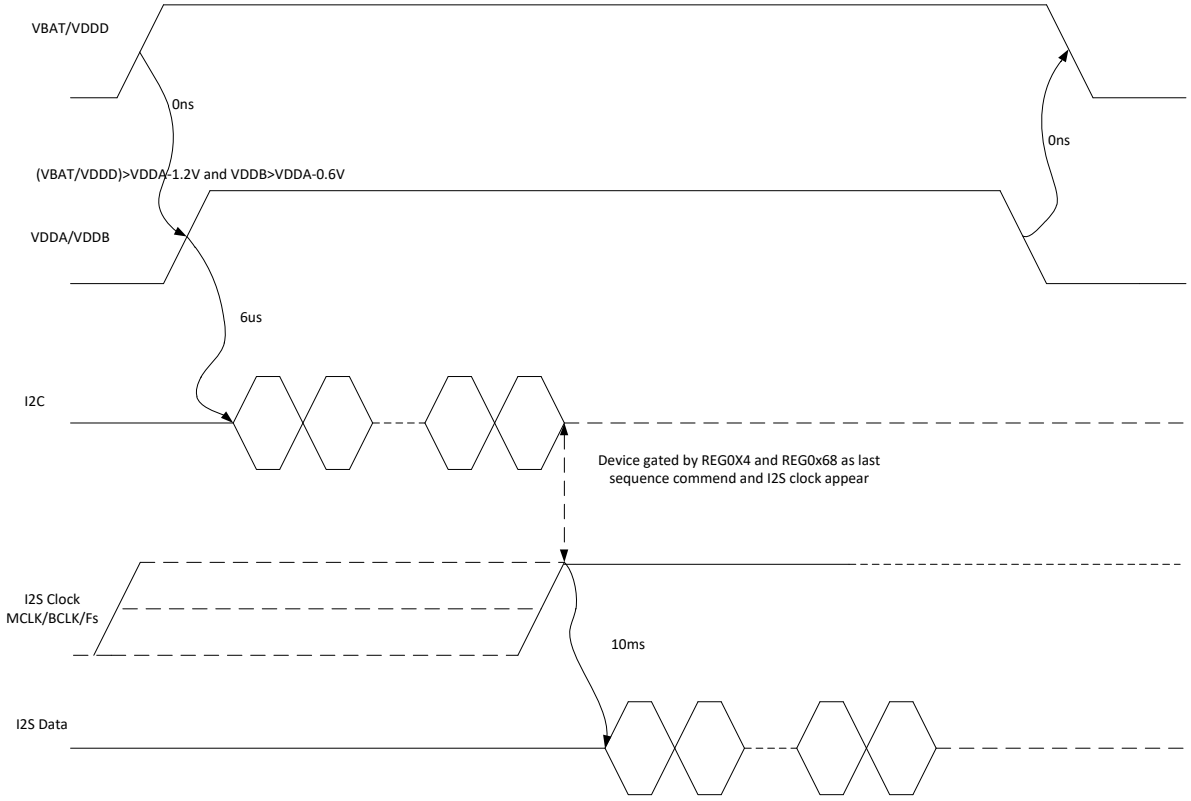
The reset is held ON while the power levels for VDDD and VDDA are below their respective thresholds. Once the power levels rise above their thresholds, the reset is released. Once the reset is released, the registers are ready to be written to.

NOTE: It is also important that all the registers should be kept in their reset state for at least 6 µsec.

An additional internal RC filter-based circuit is added which helps the circuit to respond for fast ramp rates (~3 µsec) and to generate the desired reset period width (~3 µsec at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50 nsec.

For reliable operation, it is recommended to write to register **REG0X00** upon power-up. This will reset all registers to the known default state.

NOTE: When VDDA is below the power-on reset threshold, the digital IO pins will go to a tri-state condition.



Power-on-and-off Reset

5.7 Voltage Reference (VREF)

The NAU83G20 includes a mid-supply, reference circuit that produces voltage close to VDDA/2 that is decoupled to VSS through the VREF pin by means of an external bypass capacitor. Because VREF is used as a reference voltage for the majority of the NAU83G20, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 µF is used. The Reference Voltage circuitry is shown in **Figure 7**.

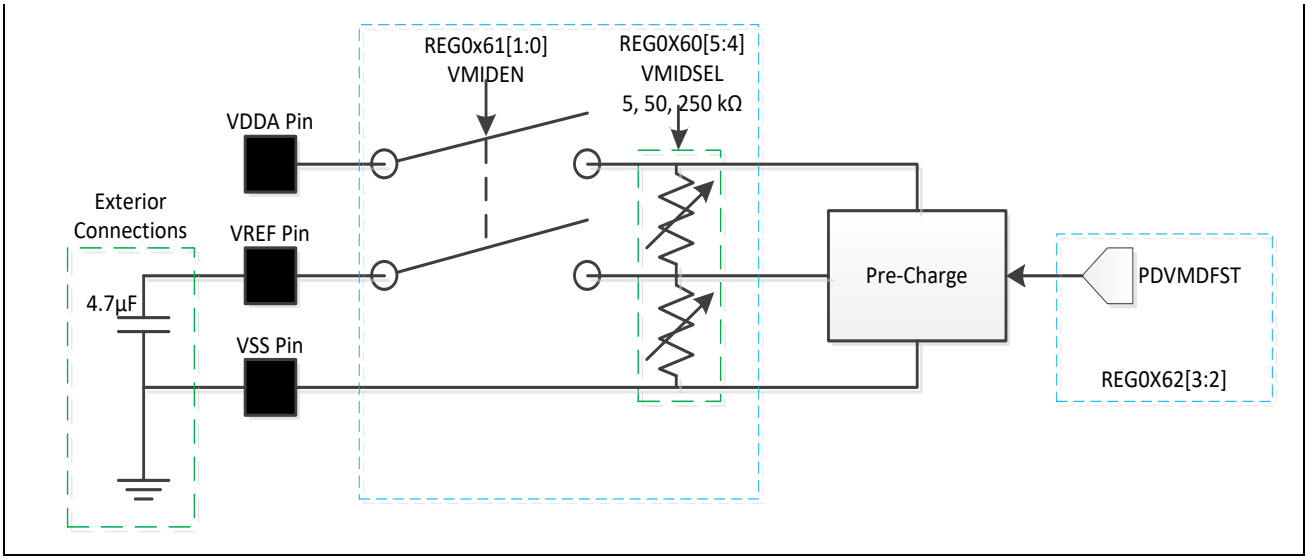


Figure 7 VREF Circuitry

The output impedance can be set using **VMID_SEL REG0X60[5:4]**. Refer to **Table 7.**

Table 7 VREF Output Impedance Selection

VMID_SEL REG0X60[5:4]	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50 kOhm	2 5 kOhm
10	250 kOhm	125 kOhm
11	5 kOhm	2.5 kOhm

APPLICATION NOTES:

- Larger capacitances can be used but increase the rise time of VREF and delay the line output signal.
- Due to the high impedance of the VREF pin, it is important to use a low-leakage capacitor.
- A pre-charge circuit has been implemented to reduce the VREF rise time. Once charged, this can be disabled using **PVDMFST REG0X62[3:2]** to save power or to prevent rapid changes in level due to fluctuations in VDDA.

5.8 DAC Soft Mute

The Soft Mute function ramps down the DAC digital volume to zero when it is enabled by **SMUTE_EN REG0X13[15]**. When disabled, the volume increases to the register-specified volume level for each channel. This function is beneficial for using the DAC without introducing pop-and-click sounds. When **DACEN_SM REG0X13[13]** is set to '0', the volume will ramp up to the register-specified volume level if the DAC path has been enabled by setting **DACEN REG0X4[3]**. The volume will ramp down to zero if the DAC path is disabled.

5.9 Hardware and Software Reset

The NAU83G20 and all of its control registers can be reset to initial default power-up conditions by writing any value to **REG0X00** ***once*** using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will be set to their power-on default values. This is typically done during hardware reset.

The NAU83G20 can be reset to initialized power-up conditions by writing any value to **REG0X01** ***twice*** using any of the control interface modes. Writing to **REG0X01** will reset the NAU83G20, but all registers values will be unaffected. This is typically done during operation to quickly force NAU83G20 in the known initialized startup state.

5.10 SAR ADC

The SAR ADC is an 8-bit Analog-to-Digital Converter (ADC) used to detect the voltage level on the VDDD supply voltage, the junction temperature sensor, and the ambient temperature sensor.

5.10.1 SAR ADC Functions

The SAR ADC is enabled by **SAR_ENA_REG0X07[0].** Setting this bit to 1 enables the SAR ADC; setting the bit to 0 disables the function. After the SAR ADC has been enabled using **SAR_ENA**, the SAR ADC enters a sampling phase. During this phase, the voltage level on the input is sampled at a speed determined by **SAMPLE_SPEED_REG0X07[3:2]**. This time can be adjusted from 2 µsec to 16 µsec, doubling each step, as shown in Table 8 Voltage Sampling Phase Time. During the sampling phase, the sample signal will be high together with the Most Significant Bit (MSB) and low with the Least Significant Bit (LSB).

Table 8 Voltage Sampling Phase Time

SAMPLE_SPEED_REG0X07[3:2]	Voltage Sampling Time
00	2 µsec
01	4 µsec
10	8 µsec
11	16 µsec

The maximum input current of the ADC can be reduced by selecting a bigger input resistor in series with the sampling capacitor. The value of the input resistor can track the sampling time. The SAR series resistor default setting = 001. Additional input limit resister values and settings are shown in Table 9 SAR ADC Current Limit Resistor Selection.

Table 9 SAR ADC Current Limit Resistor Selection

REL_SEL REG0X07[9:7]	Input Resistor Value
000	35 kOhm
001	70 kOhm
010	170 kOhm

011	360 kOhm
1xx	Short

After the sampling phase, the ADC enters a conversion phase that consists of eight compare cycles. Each of these compare cycles can last from 500 nsec to 4 µsec, doubling each step. See Table 10 Compare Cycle Time Settings. Use COMP_SPEED_REG0X07[6:5] to adjust the compare time. The total conversion has 8 compare cycles.

Table 10 Compare Cycle Time Settings

COMP_SPEED REG0X07[6:5]	Time Settings
00	500 nsec
01	1 µsec
10	2 µsec
11	4 µsec

APPLICATION NOTE:

- SAMPLE_SPEED_REG0x07[3:2] is used for the SAR ADC sampling rate. Before changing the sampling rate, SAR_ENA_REG0X07[0] needs to be set to 0. After the sample speed is set, **SAR_ENA** sets to 1.

5.10.2 SAR ADC Control

The NAU83G20 needs to process and monitor three inputs: Battery Supply Voltage (VBAT), Junction Temperature (Tj), and Ambient Temperature (Ta), as shown in **Figure 8**.

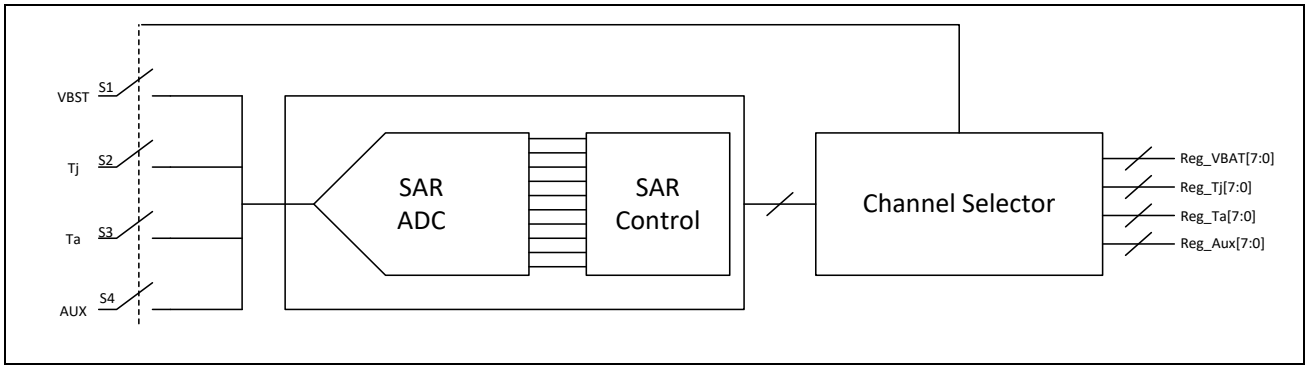


Figure 8 SAR ADC Control

Notes: The gain for all SAR ADC Channels is fixed to 1.0 * VDDA; the raw data can be read from SAR_ADC_OUT_01_REG0x020 and SAR_ADC_OUT_23_REG0x021. To convert from raw SAR ADC from **SAR_ADCOUT_01** and **SAR_ADC_OUT23** please refer to the equation below:

$$Tj = [(raw\ Tj) - 89] * 1.6077$$

The SAR ADC reads a full scale of 16.5V on VBAT. Below is a table of the VBAT voltage and the SAR reading

*VBAT = ((SAR ADC 0x20 [7:0]) * 0.0622) + 0.5869*

VBAT (V)	SAR ADC (DEC)
4	55
5	71
6	87
7	103
8	119
9	135
10	151
11	168
12	184
13	200
14	216
15	232
16	248
16.5	255

Ta requires additional configuration through the output pin to activate its output.

5.11 Clock Detection

The NAU83G20 includes a Clock Detection circuit that can be used to enable and disable the audio paths, based on an initialized audio path setting. Enable the audio path through the I2C Interface; but, the actual power up/down can be gated by the clock detection circuit. Clock detection works with BCLK in 32bits or more than 32bits Fs format. The block diagram of the clock detection circuit is shown in **Figure 9**. Control register is located at CLK_DET_CTRL_REG0X40. Divider N1 is selectable as 1, 2 or 3 and divider N2 is selectable as 1, 2, 4, 8.

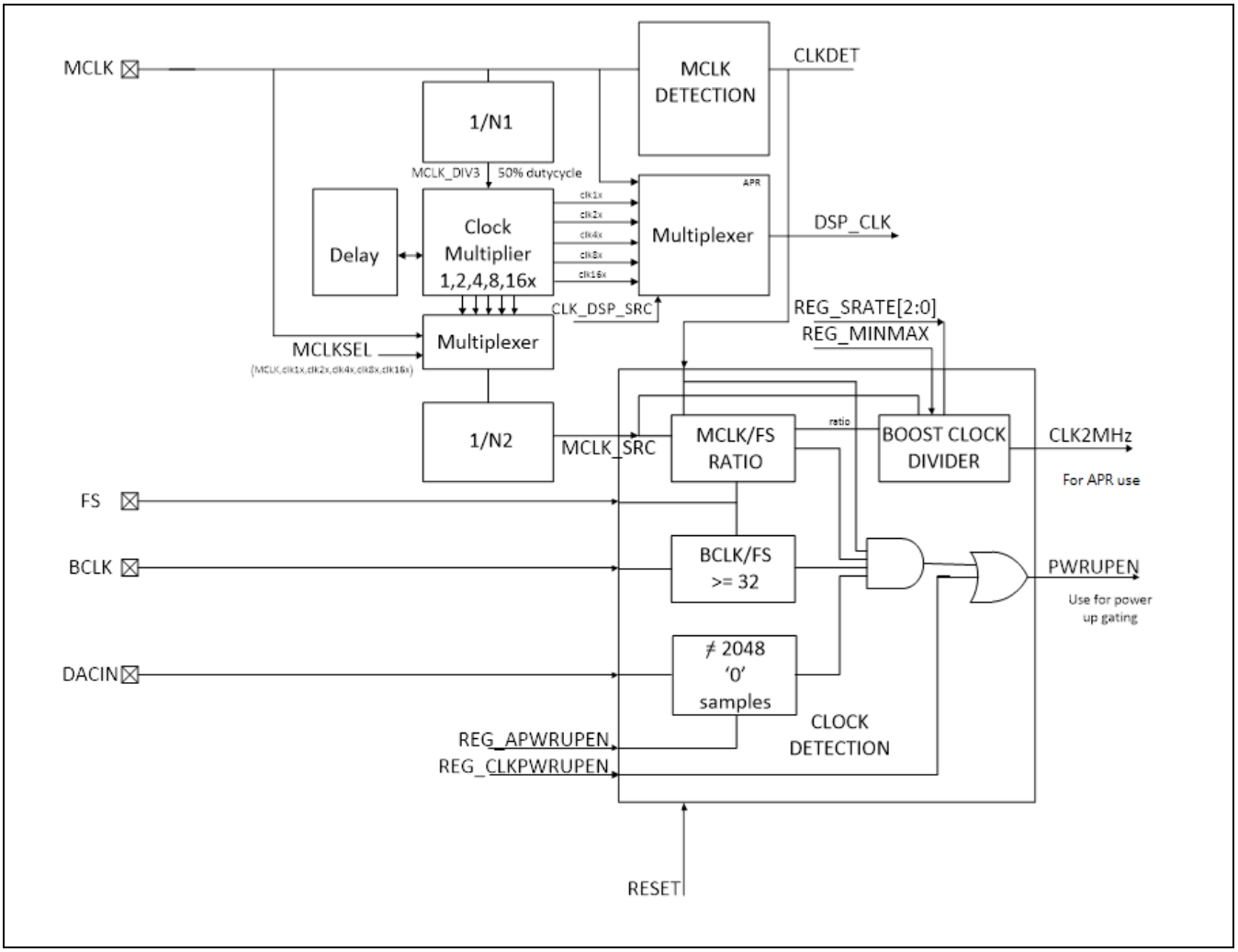


Figure 9 NAU83G20 Clock Detection Circuit

5.11.1 Enabling Clock Detection

Clock detection in the NAU83G20 is enabled by setting **REG_CLKPWRUPEN** = 0 (default) and meeting three or four conditions, depending on the configuration. If all conditions are met, the **PWRUPEN** signal will be asserted to 1. If any of the conditions are not met, the **PWRUPEN** signal is set to 0.

Conditions for enabling clock detection:

1) The NAU83G20 has custom logic clock detection circuits that detect if MCLK is present. Upon MCLK detection, the detector output MCLKDET goes to 1. When the MCLK disappears, MCLKDET goes back to 0. Up to 1 µsec is required to detect MCLK and the MCLK release time is about 50 µsec.
2) Clock detection logic uses the CLKDET and MCLK_SRC to initiate detection of MCLK/FS ratio. MCLK_SRC is derived from MCLK after programmable multiplication and/or division. The target ratios for MCLK/FS after programmable multiplication and/or division are 256, 400 & 500. When the clock detection logic detects a ratio of between 254 and 258 or between 398 and 402 or between 498 and 502 for one frame sync it will assert a valid MCLK/FS ratio. When the detection logic detects a ratio outside these valid ranges for two consecutive frame syncs it will assert an invalid MCLK/FS ratio. Even though it is required for the ratios to be exact 256, 400 or 500, having two extra cycles tolerance allows for occasional clock jitter, without disabling the audio path.

3) Clock detection logic also needs to detect the BCLK to make sure data can be recorded and played back. There needs to be at least 32 BCLK cycles per Frame Sync. MCLK can be used to count the number of BCLK with each Frame Sync.
4) If **REG_APWRUPEN** is set to 1, clock detection will require non-zero samples to enable output of a power-up signal. Any non-zero sample will be sufficient. After power-up, if 2048 zero samples are detected, the **PWRUPEN** signal is asserted to 0. If **REG_APWRUPEN** is set to 0, this function does not control the **PWRUPEN** signal.

5.11.2 Disabling Clock Detection

Clock detection in the NAU83G20 is disabled by setting **REG_CLKPWRUPEN** to 1. In this state, **PWRUPEN** is no longer controlled by the enabling conditions listed above, but is set to 1. However, the MCLKDET and clock dividers are still active.

The range of the input clocks is shown in **Table 11**.

Table 11 Range of Input Clocks

Signal	Min	Max
Frame Synch (FS) (kHz)	8	96
Master Clock MCLK (MHz)	2.048	24.576

5.11.3 Sampling and Over Sampling Rates

Possible Sampling Rate and MCLK_SRC selections are shown in **Table 12** and

Table 13. Note that **REG_SRATE REG 0X40** must be programmed to identify the target sample rate.

Table 12 Sampling and Over Sampling Rates (Ranges 1-3)

REG_SRATE												
MCLK_SRC/FS Ratio	Range 1 000				Range 2 001				Range 3 010			
	FS (kHz)		MCLK_SRC (MHz)		FS (kHz)		MCLK_SRC (MHz)		FS (kHz)		MCLK_SRC (MHz)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
256	8	12	2.048	3.072	16	24	4.096	6.144	32	48	8.192	12.288
400	8	12	3.2	4.8	16	24	6.4	9.6	32	48	12.8	19.2
500	8	12	4	6	16	24	8	12	32	48	16	24

Table 13 Sampling and Over Sampling Rates (Ranges 4-5)

REG_SRATE				
MCLK_SRC/FS Ratio	Range 4 011			
	FS (kHz)		MCLK_SRC (MHz)	
	Min	Max	Min	Max
256	64	96	16.384	24.576
400	64	96	25.6	38.4
500	64	96	32	48

The only internal MCLK_SRC/FS ratios allowed are: 256, 400 & 500. The clock divider or multiplier in register 0x03 needs to be setup to achieve one these three possible ratios.

Effective MCLK/FS ratios can be achieved with the clock multiplier under MCLK > 2Mhz condition, as shown in **Table 14**.

Table 14 Effective MCLK/FS Ratios (MCLK > 2Mhz)

MCLK_SRC/FS ratio	Clock Multiplier (Reg0x03)	Effective ratio MCLK/FS
256	8	32
400	8	50
500	8	62.5
256	4	64
400	4	100
500	4	125
256	2	128
400	2	200
500	2	250
256	1	256
400	1	400
500	1	500

- For MCLK_SRC/FS ratios of 256 the Over Sampling Ratio (OSR) can be set in register 0x28 & 0x29 to: 32, 64, 128 & 256. Note that the ADC & DAC clocks need to be set to their matching values in register 0x03.

- For MCLK_SRC/FS ratios of 400 & 500 the Over Sampling Ratio (OSR) is fixed to 100. For MCLK_SRC/FS ratios of 400 the ADC & DAC clock dividers need to be set to ¼ in register 0x03. For MCLK_SRC/FS ratios of 500 the ADC & DAC clock dividers are automatically set to 1/5.

5.12 High Pass Filters

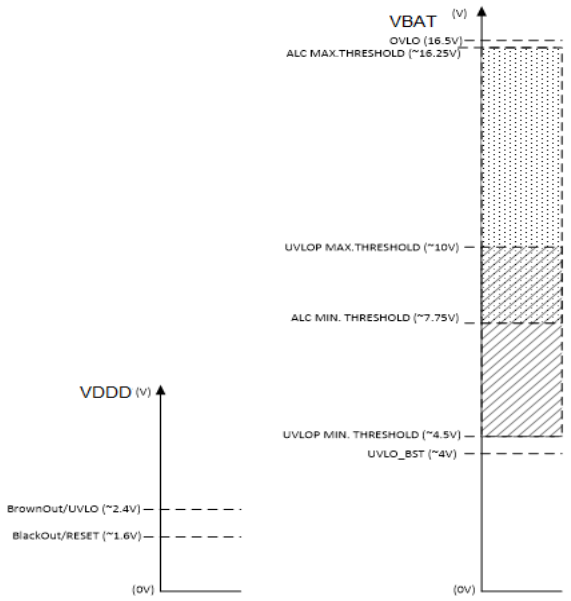
There is a High-Pass Filter for each ADC Channel and each DAC Channel. The High-Pass Filters may be enabled by setting **HPF_EN REG0X12[15}, [13],** and **[5].** The High-Pass Filter has two operation modes that apply to both channels simultaneously. In the Audio Mode, the filter is a simple first-order DC blocking filter, with a cut-off frequency of 3.7 Hz. In the Application-Specific Mode, the filter is a second-order audio frequency filter, with a programmable cut-off frequency. The programmable filter mode may be enabled by setting **HPF_APP REG0X12[14], [9],** and **[4].**

Table 15 identifies the cut-off frequencies with different sample rates.

Table 15 High-Pass Filter Cut-Off Frequencies

HPFCUT	Sample Rate in KHz (FS)							
	REG_SRATE= 3'b000		REG_SRATE= 3'b001		REG_SRATE= 3'b010		REG_SRATE= 3'b011	
	8	12	16	24	32	48	64	96
000	87	130	87	130	87	130	87	130
001	103	155	103	155	103	155	103	155
010	132	198	132	198	132	198	132	198
011	165	248	165	248	165	248	165	248
100	207	311	207	311	207	311	207	311
101	265	398	265	398	265	398	265	398
110	335	503	335	503	335	503	335	503
111	409	614	409	614	409	614	409	614

5.13 Automatic Level Control



VBAT and VDDD Limit Threshold

The NAU83G20 employs several limit thresholds on the battery voltage VBAT. This limit threshold can be used to program gain changes in order to protect the system from shutting down or to prevent excessive current draw. On VBAT an ALC threshold between 7.75V and 16.25V can be programmed in order to adjust the digital gain when the battery voltage drops due to discharge. The ALC can reduce the output level in order to reduce the power consumed from the battery supply. See the NAU83G20 ALC section below for more details. When the battery voltage drops further down an Under Voltage Lockout Prevention (UVLOP) threshold can be set between 10.0V and 4.5V in order to limit the input current. This will prevent large currents from being drawn at low battery voltages as the device tries to supply the load and allow for the battery voltage to recover such that it does not approach the Under Voltage Lockout Threshold (UVLO). In addition, a second gain limiter can be activated to reduce the gain even further at a faster attack rate. The operation of this limiter will be described in this specification.

When the battery drops even further down despite the gain and current limiters, the class-D driver will shut down at the Under Voltage Lockout Threshold (UVLO) threshold of about 4.0V. If the VBAT drops even further below 1.6V then the device control and registers will reset.

On the VBAT output, the NAU83G20 employs only two limits. The NAU83G20 VBAT has an Over Voltage LockOut (OVLO) voltage of about 16.5V. If VBAT reaches above this voltage, the class-D driver will shut down and the outputs will remain at ground until the VBAT reaches below the OVLO threshold.

This section describes the various level control options based on the thresholds outlined above.

The digital Automatic Level Control (ALC) supports the input digital audio path of the NAU83G20 by providing an optimized signal level at the output of the Class-D Amplifier. This is achieved by automatically decreasing the amplitude of the input signal according to the user's set amplitude, clipping, or low battery voltage, and restoring amplitude when conditions are lifted. **Figure 10** illustrates the basic relationship of the ALC to other major functions of the NAU83G20.

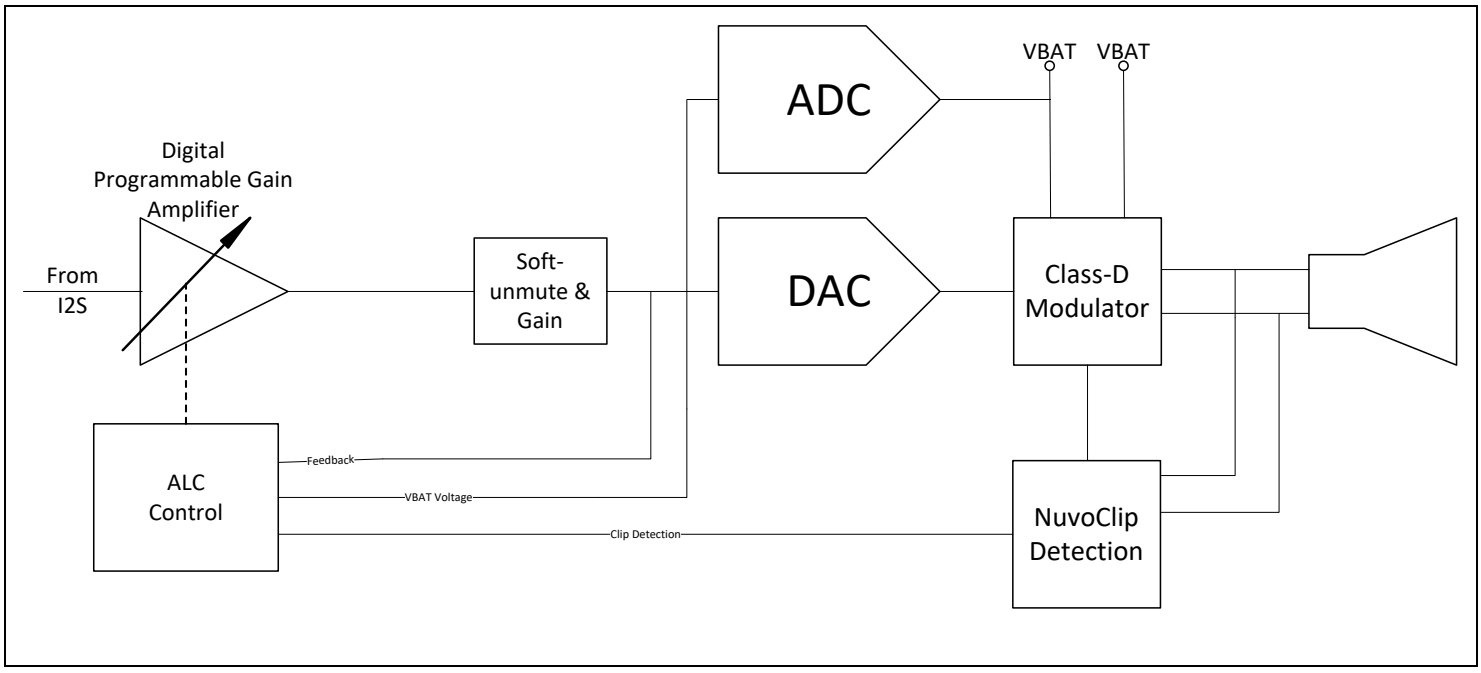


Figure 10 Automatic Level Control

5.13.1 ALC Operation

The ALC is enabled by **ALC_CTRL3.ALC_EN_REG0X2E[15]** and operates according to the Limiter Mode register **ALC_CTRL3.LIM_MDE_REG0X2E[14:12]**. It uses feedback to detect the signal output level from either the output of the digital Programmable Gain Amplifier (**dPGA**) or output of the soft mute gain compensation through a Peak Detector, set by **ALC_CTRL4.PEAK_SEL_REG0X2F[13]**. Using the output of the **dPGA** provides a direct feedback for control while using the output of the soft mute gain compensation allows for the ALC to adjust based on the activation of the soft mute, deactivating when the soft-mute function drops the signal below the user's set amplitude or reactivating when disabling the soft mute when signal rises above the set amplitude and/or clipping. More information can be read about the soft mute in Section **5.8**.

The Peak Detector can be configured by either using a full-wave rectification peak, ensuring equal ALC operation on both positive and negative signals, or absolute value calculated peak, which updates at every peak and degrades until a new peak is detected. This is set in **ALC_CTRL1.ALCPKSEL_REG0X2C[11]**. Additionally, the ALC can update either from the zero crossing point of the signal or immediately upon triggering. This is determined by the register **ALC_CTRL1.ALC_ZC_REG0X2C[14]** and when enabled also overrides the register **ALC_CTRL4.LPGAZC_REG0X2F[14]** to ensure zero crossing point reference consistency. ALC updating on the zero crossing point ensures that if the ALC responds faster than the signal degrades, the ALC will wait until the signal reaches close to zero before changing the gain on the **dPGA**, or input signal gain. This may be helpful depending on the application and can reduce popping on speakers. If immediate action is needed for input signal attenuation then **ALC_ZC** can be disabled. The ALC has three operational states: ALC *Attack*, ALC *Release*, and ALC *Hold*. In the ALC *Attack* state, the ALC decreases the **dPGA** gain at a single dB decrement at a time, gradually based on the **ALCATK** register; in the ALC *Release* state, the ALC increases the **dPGA** gain at a single dB increment at a time gradually based on the **ALCDCY** register; in the ALC *Hold* state, the ALC holds constant the **dPGA** gain for a specified time determined by the **ALCHLD** register. While the attack state is immediate upon meeting conditions, the ALC will enter the hold state before releasing the signal. This is to account for any noise or fluctuations that may occur on the input signal.

The registers below are used in every ALC operational mode that are defined in ALC_CTRL3.LIM_MDE_REG0X2E[14:12].

- **ALC_CTRL3.ALC_EN_REG0X2E[15]** – ALC Enable Register, enables the ALC for operation.
- **ALC_CTRL1.ALCPKSEL_REG0X2C[11]** – Selects between full-wave rectification peak (0) or absolute value calculated peak (1).
- **ALC_CTRL1.ALC_ZC_REG0X2C[14]** – Selects whether the ALC should update immediately at peak detection or at the zero crossing point of the signal. This is recommended as it prevents sudden changes that may occur.
- **ALC_CTRL1.ALCMAXGAIN_REG0X2C[7:5]** – The maximum gain level allowed to be set by the ALC on the **dPGA** when enabled. This is applied automatically when ALC is enabled and acts as the upper limit the input signal is allowed until ALC is disabled.
- **ALC_CTRL1.ALCMINGAIN_REG0X2C[3:1]** – The minimum gain level allowed to be set by the ALC on the **dPGA** when enabled. This acts as the lowest limit the input signal is allowed until the ALC is disabled.
- **ALC_CTRL2.ALCDCY_REG0X2D[15:12]** – The rate at which the ALC will *release*, or increase the gain of, the signal determined by step time doubling its increment from 2µs to 4196µs at 0.1875dB per step. Typically, the decay time is much slower than the attack time. When the DAC output level is below the ALC Target value by at least 1.5 dB, the gain increases at a rate determined by this parameter. In Limiter Mode, the time constants are faster than in ALC mode.
- **ALC_CTRL2.ALCATK_REG0X2D[11:8]** – The rate at which the ALC will *attack*, or attenuate, the signal determined by step time doubling its increment from 2µs to 4196µs at 0.1875dB per step. Typically, the attack time is much faster than the decay time. In the NAU83G20, when the absolute value of the DAC output exceeds the ALC Target Value **ALCLVL**, the gain will be reduced at a step-size and rate determined by this parameter. When the peak DAC output is at least 1.5 dB lower than the **ALCLVL**, the stepped gain reduction will halt.
- **ALC_CTRL2.ALCHLD_REG0X2D[7:4]** – The length of time at which the ALC will hold the signal for, ranging from 0ms to 512ms. Hold time refers to the duration of time when no action is taken. This is typically used to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU83G20, the hold time value is the duration of time that the ADC output peak value must be less than the target value, **ALCLVL**, before there is an actual gain increase.
- **ALC_CTRL2.ALCLVL_REG0X2D[3:0]** – A requirement for the input signal level to hold at after clearing the conditions specified in each of the ALC operational mode for the amount of time set in the **ALCHLD** register before entering the ALC Release state, or increase the gain of the **dPGA** at the rate specified by the **ALCDCY** register. This value is expressed as a fraction of Full Scale (FS) output from the DAC. Depending on the logic conditions, the output value used in the comparison may be either the instantaneous value of the DAC ***or*** a time weighted average of the DAC peak output level.

NOTE: See **Chapter 6** Registers 0x2C to 0x2F for more information regarding settings for ALC functions.

The following are different operational modes allowed by the **LIM_MDE** control register:

- Clip Limiting Mode
- Low-Battery Clip Limiting Mode
- Normal Limiting Mode
- Low-Battery Limiting Mode
- Low-Battery Limiting Mode with Preprogrammed VBAT Ratio

***NOTE*:** The gain range for the **dPGA** is restricted between **ALCMAXGAIN** and **ALCMINGAIN**. Upon enabling of the ALC, the **dPGA** is automatically set to the **ALCMAXGAIN** and when an ALC event triggers, the gain is adjusted according to the conditions as long as the target attenuation level is below the **ALCMAXGAIN** and above the **ALCMINGAIN** restrictions.

5.13.1.1 Clip Limiting Mode

Registers used in Clip Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0X2E[14:12] = 000** – ALC limiter mode set to **000** for operation based on clipping
- **ALC_CTRL4.ALCCLIPSTEP_REG0X2F[12:10]** – *Maximum attenuation* adjustment level as a comparison from the level clipping is detected. This value can range between the ranges of 0 to -1.75dB and will act as a soft wall, limiting the max gain change in each *Attack* State session or clipping event. This adjustment is limited by the **ALCMINGAIN** register, restricted to -32dB in this mode, where the *maximum attenuation* change cannot surpass this value.
- **CLIP_CTRL_REG0X69[4]** – Activation register for clip detection circuit is set to enable for detecting clipping. This is required to detect clipping in this mode.

Description:

In **Clip Limiting Mode**, **ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=000**, the DAC output is programmed to limit clipping by lowering the **dPGA** gain when clipping is detected. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay. A clip detection signal is provided by the NuvoClip detection circuit so long as the **CLIP_CTRL** register is enabled. As soon as a clipping event is detected, the ALC goes into the *Attack* State, lowering the **dPGA** gain at the pre-programmed rate in the **ALCATK** register. This continues until the clipping detection no longer detects a clipping signal or if the *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached. If another consecutive clipping event occurs the ALC gain continues ramping down until another *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached or until the **ALCMINGAIN** has been reached. The gain setting applied by this method will remain constant until the output signal no longer clips ***AND*** the input signal level becomes 1.5dBFS ***below*** the ALC Target Level specified in the **ALCLVL** register for the entirety of the ALC *Hold* state specified in the ALC Hold Register **ALCHLD**, before the ALC enters the *Release* State to increase the gain at the rate specified in the **ALCDCY** register until the signal is at full scale or it clips again. If clipping again, the ALC will repeat this process to ensure no clipping.

Example Problem Set: Ensure that no clipping occurs. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0X2C** = 0x***20E2***
  - [14] **ALC_ZC** set to update the ALC instantaneously prevent clipping as soon as possible
  - [11] **ALCPK_SEL** set to update Peak Detection on rectified value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- **ALC_CTRL2.REG0X2D** = 0x***5353***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes another step. If the signal peak is ***higher***, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
  - [3:1] **ALCLVL** set to -3dBFS. This is the comparison level which triggers the state of the ALC to go into Release or Hold and can affect stability of the signal.

- The rest is left at default.

- **ALC_CTRL3.REG0X2E** = 0x***8010***
  - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
  - [14:12] **LIM_MDE** is set to 000. This is set to Clip Limiting mode and follows the operation explained in the description portion of this section.
  - The rest is left at default.
- **ALC_CTRL4.REG0X2F** = 0x***0C20***
  - [12:10] **ALCCLIPSTEP** set to -0.75dB as a soft-wall to change at a single clipping event.
- **CLIP_CTRL_REG0X69** = 0x***0010***
  - [4] Enable the Nuvo Clip Detection Circuit.

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I^2C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.13.1.2 Low VBAT Clip Limiting Mode

Registers used in Low Battery Clip Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0X2E[14:12] = 001** – ALC limiter mode set to **001** for operation based on low battery and clipping mode
- **ALC_CTRL3.VBAT_THRESHOLD_REG0X2E[9:5]** – VBAT threshold value as an additional condition for ALC activation. This can be paired with other conditions or can require additional settings depending on the ALC operational mode.
- **ALC_CTRL4.ALCCLIPSTEP_REG0X2F[12:10]** – *Maximum attenuation* adjustment level as a comparison from the level clipping is detected. This value can range between the ranges of 0 to -1.75dB and will act as a soft wall, limiting the max gain change in each *Attack* State session or clipping event. This adjustment is limited by the **ALCMINGAIN** register, restricted to -32dB in this mode, where the *maximum attenuation* change cannot surpass this value.
- **CLIP_CTRL_REG0X69[4]** – Activation register for clip detection circuit is set to enable for detecting clipping. This is required to detect clipping in this mode.

Description:

In **Low VBAT Clip Limiting Mode,** **ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=001**, the DAC output is programmed to limit clipping by lowering the **dPGA** gain when clipping is detected with the condition of activating during low battery voltage operation. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay. A clip detection signal is provided by the NuvoClip detection circuit so long as the **CLIP_CTRL** register is enabled. Immediately when a clipping event is detected ***AND*** the VBAT voltage is below the voltage specified in the **VBAT_THRESHOLD** register, ALC will go into ALC *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the **ALCATK** register until the clipping detection no longer detects a clipping signal or if the *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached. If another consecutive clipping event occurs the ALC gain continues ramping down until another *maximum attenuation* (**CLIP_GAINADJUST**) per clipping event has been reached or until the **ALCMINGAIN** has been reached. If either of the conditions are lifted, i.e. battery voltage is above **VBAT_THRESHOLD** or the clipping is no longer detected, then the ALC will wait until the input signal level becomes 1.5dBFS ***below*** the ALC Target Level, set in the **ALCLVL** register, for the period of the ALC *Hold* state, based on time specified in the **ALCHLD** register. The ALC will then enter the *Release* state, increasing the gain at the rate specified in the **ALCDCY** register until reaching the maximum gain allowed, **ALCMAXGAIN**, or another clipping event is detected.

Example Problem Set: Ensure that no clipping occurs when VBAT lowers below 3.83V, this is most likely to happen when using a battery. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0X2C** = 0x***20E2***
  - [14] **ALC_ZC** set to update the ALC instantaneously prevent clipping as soon as possible
  - [11] **ALCPK_SEL** set to update Peak Detection on rectified value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- **ALC_CTRL2.REG0X2D** = 0x***5353***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes another step. If the signal peak is ***higher***, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
  - [3:1] **ALCLVL** set to -3dBFS. This is the comparison level which triggers the state of the ALC to go into Release or Hold and can affect stability of the signal.
  - The rest is left at default.
- **ALC_CTRL3.REG0X2E** = 0x***9310***
  - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
  - [14:12] **LIM_MDE** is set to 001. This is set to Low VBAT Clip Limiting mode and follows the operation explained in the description portion of this section.
  - [9:5] **VBAT_THRESHOLD** is set to 9.75V to ensure ALC activation at this voltage.
  - The rest is left at default.
- **ALC_CTRL4.REG0X2F** = 0x***0C20***
  - [12:10] **ALCCLIPSTEP** set to -.75dB as a soft-wall to change at a single clipping event.
- **CLIP_CTRL_REG0X69** = 0x***0010***
  - [4] Enable the Nuvo Clip Detection Circuit.

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I^2C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.13.1.3 Normal Limiting Mode

Registers used in Normal Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=010** – ALC limiter mode set to **010** for operation based on user's set amplitude.

Description:

In **Normal Limiting Mode**, **ALC_CTRL3.LIM_MDE REG0X2E[14:12] =010,** a maximum DAC output level is programmed to limit the full scale output level. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay. The signal peak is read continuously until the level reaches above the user's set amplitude in the **ALCLVL** register. Upon overstepping the set amplitude, the ALC will enter the *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the

ALCATK register until the peak detector returns a lower level than the **ALCLVL** register. When the input signal level becomes 1.5dBFS below the ALC target level (**ALCLVL** register), then the ALC enters *Hold* state, holding the **dPGA** gain for a specified time determined by the **ALCHLD** register. The ALC then goes into the *Release* state, increasing the **dPGA** gain at the pre-programmed rate specified in the **ALCDCY** register until the **dPGA** gain is at maximum or until the peak returns a level above the **ALCLVL** register, in which the ALC will be triggered and enter the *Attack* state again.

Example Problem Set: Limit maximum output to not exceed -3dBFS limit and update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0X2C** = 0x***68E2***
  - [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
  - [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- **ALC_CTRL2.REG0X2D** = 0x***5353***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes another step. If the signal peak is ***higher***, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
  - [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
  - The rest is left at default.
- **ALC_CTRL3.REG0X2E** = 0x***A010***
  - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
  - [14:12] **LIM_MDE** is set to 010. This is set to Normal Limiting mode and follows the operation explained in the description portion of this section.
  - The rest is left at default.
- **ALC_CTRL4.REG0X2F** = 0x***0020***
  - Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I^2C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.13.1.4 Low Battery Limiting Mode

Registers used in Low Battery Limiting Mode:

- **ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=011** – ALC limiter mode set to **011** for operation based on low battery mode.
- **ALC_CTRL3.VBAT_THRESHOLD_REG0X2E[9:5]** – VBAT threshold value as the condition for ALC activation within **LIM_MDE** = 011 and 100. The available values range from 7.75V (11111) to 16.25V (00000) at ~0.25V steps. For exact values, please refer to the Section **5.23**, the Control Register List.

Description:

In **Low-Battery Limiting Mode**, **ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=011**, a maximum DAC output level is programmed to limit the full scale output level with the additional constraint of low-battery activation. Immediately upon enable, the ALC will set the **dPGA** gain according to the **ALCMAXGAIN** value without delay or decay.

The ALC activates when the VBAT voltage declines below the set value in the **VBAT _THRESHOLD** register. The signal peak is read continuously until the level reaches above the user's set amplitude in the **ALCLVL** register. Upon overstepping the set amplitude, the ALC will enter the *Attack* state, lowering the **dPGA** gain at the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a lower level than the **ALCLVL** register.

When the input signal level becomes 1.5dBFS below the ALC target level (**ALCLVL** register), then the ALC enters *Hold* state, holding the **dPGA** gain for a specified time determined by the **ALCHLD** register. The ALC then goes into the *Release* state, increasing the **dPGA** gain at the pre-programmed rate specified in the **ALCDCY** register until the **dPGA** gain is at maximum or until the peak returns a level above the **ALCLVL** register, in which the ALC will be triggered and enter the *Attack* state again.

If VBAT were to be recharged at any given moment, the ALC will cease triggering and return to an idle state until VBAT lowers its level below the **VBAT _THRESHOLD** register again.

Example Problem Set: When battery becomes discharged lower than 3.53V, limit maximum output to not exceed -3dBFS limit to lessen battery discharge. Additionally, update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0X2C** = 0x***68E2***
  - [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
  - [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- **ALC_CTRL2.REG0X2D** = 0x***5353***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes another step. If the signal peak is ***higher***, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
  - [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the

ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
    - [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
    - The rest is left at default.
- ALC_CTRL3.REG0X2E = 0x***B2D0***
    - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
    - [14:12] **LIM_MDE** is set to 011. This is set to Low Battery Limiting mode and follows the operation explained in the description portion of this section.
    - [9:5] **VBAT_THRESHOLD** is set to 10.25V for ALC activation at this voltage.
    - The rest is left at default.
- ALC_CTRL4.REG0X2F = 0x***0020***
    - Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I²C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.13.1.5 Low Battery Limiting Mode with Pre-programmed VBAT Ratio

Registers used in Low Battery Limiting Mode with Pre-programmed VBAT Ratio:

- ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=100 – ALC limiter mode set to **100** for operation based on a split operation, #1 or #2, between above or below VBAT threshold, respectively. Operation 1: Normal Limiting Mode as specified in 0. Operation 2: ALC Target Level follows a ratio of the sense VBAT voltage. More information of the two modes can be found in the description of this section.
- ALC_CTRL3.VBAT_THRESHOLD_REG0X2E[9:5] – VBAT threshold value as the condition for ALC activation within **LIM_MDE** = 011 and 100. The available values range from 7.75V (11111) to 16.25V (00000) at ~0.25V steps. For exact values, please refer to the Section 5.23, the Control Register List.
- ALC_CTRL3.VBAT_RATIO_REG0X2E[11:10] – VBAT ratio, an additional setting only used for LIM_MDE=100. This changes the ALC output level based on the sensed VBAT voltage.

Description:

In **Low-Battery Limiting Mode with Preprogrammed VBAT Ratio,** ALC_CTRL3.LIM_MDE_REG0X2E[14:12]=100**,** there are two modes within its operation, one above the VBAT Threshold and another below the VBAT Threshold, in which the threshold can be set in the **VBAT_THRESHOLD** register. Above the VBAT Threshold (Operation 1), the ALC functions the same as Normal Limiting Mode as specified in 0. Below the VBAT Threshold (Operation 2), the maximum DAC output level is programmed to attenuate the full scale output level based on the ratio, specified in the **VBAT_RATIO** register, of the **VBAT_THRESHOLD,** also in its own register, minus the sensed VBAT voltage. The equation describing this operation is shown below:

$$V_{out} = V_{out\,(VBAT>VBAT_{threshold})} - [RATIO_{VBAT} * (VBAT_{threshold} - V_{BAT})]$$

The output voltage, V_{peak}, is determined by the VBAT acquired when VBAT is greater than the threshold voltage, minus by the ratio multiplied by the difference of threshold voltage and current VBAT voltage. The ALC activates when the VBAT voltage declines below the set value in the **VBAT_THRESHOLD** register. Before the activation, the peak voltage of the output is recorded from the peak detector and used for the variable $V_{out(VBAT>VBATthreshold)}$ in the equation above. The $V_{out(VBAT>VBATthreshold)}$ is determined by the **ALCLVL** register. For example, if **ALCLVL** register is set to -3dBFs, since the max voltage supported in this chip is 14V, we can take it as 0dBFs, then we can calculate the $V_{out(VBAT>VBATthreshold)}$ as below:

$V_{out(VBAT>VBATthreshold)}$ =14 * 10^(-3/20) = 9.9V.

Immediately upon activation, the ALC will enter the *Attack* state, lowering the **dPGA** gain by the pre-programmed rate specified in the **ALCATK** register until the peak detector returns a level lower or equal to the *Vout* described in the equation above where *Vout* is the representation of the output ALC level. This level can be calculated from the equation below and is rounded to the nearest whole number:

$$ALC\ Attenuation\ Level = 20\log\left(\frac{V_{out}}{V_{out\ (VBAT>VBAT_{threshold})}}\right)$$

Actually the calculated *Vout* will be the new target level instead of the **ALCLVL** register. Continue the example above, if the **ALCLVL** register is set to -3dBFs, the **VBAT_THRESHOLD** register is set to 7.5V, the **VBAT_RAT**IO register is set to 3:1, if the VBAT is down to 4.0V, then the *Vout* will be:

Vout = 9.9V – (3 * (7.5-7)) = 8.4V

So the new ALCLVL will be:

ALCLVL = 20log(8.4/14) = -4.4dBFs instead of -3dBFs.

Also *Vout* should be larger than 0, since the voltage cannot be minus, which means that in the operation:

$$V_{out} = V_{out\ (VBAT>VBAT_{threshold})} - [RATIO_{VBAT} * (VBAT_{threshold} - V_{BAT})]$$

If $V_{out\ (VBAT>VBAT_{threshold})} < [RATIO_{VBAT} * (VBAT_{threshold} - V_{BAT})]$, then the Vout should be the last value it can get from the decrementing VBAT which make it larger than 0.

Take note that the ALC attenuation occurs at incremental steps of 1dB and thus the steps can be accurately calculated if the V_{out} is known. If the input signal extends beyond *Vout* while the VBAT voltage is lower than the VBAT Threshold, the ALC enters the ALC *Attack* state, lowering the **dPGA** gain at the pre-programmed rate set in the **ALCATK** register. This continues until the DAC output level has been reduced to below the limit threshold. This limits DAC clipping if there is a sudden increase in the input signal level. During the whole of Operation 2, while the VBAT is charging and the ALC has been activated, the ALC will remain at its current gain level until VBAT has increased above **VBAT_Threshold**. An example of this is when VBAT starts at 8V, while **VBAT_Threshold** is 7.5V, and drops to 7V, this is theoretically enough make the ALC gain at -1dB when there's constant input, i.e. music or a wave. When the VBAT is being charged, the ALC gain will remain at -1dB until the VBAT is above 7.5V.

NOTE: The maximum gain at full scale input is set by the ALC Target Level, **ALCLVL**.

Example Problem Set: When battery becomes discharged lower than 12.5V, limit maximum output to not exceed -3dBFS limit to lessen battery discharge. Additionally, update on the zero crossing point to prevent any spontaneous change in the signal. Limit the attenuation and release rate by a manageable amount to prevent any audible change.

Register Settings for problem set:

- **ALC_CTRL1.REG0X2C** = 0x***68E2***
  - [14] **ALC_ZC** set to update the ALC on the zero crossing point of the signal, so there is no instantaneous changes on the signal when ALC adjusts.
  - [11] **ALCPK_SEL** set to update Peak Detection on a calculated absolute value.
  - [7:5] **ALCMAXGAIN** set to 0dB. The absolute maximum gain that the **dPGA** is allowed. Upon enable, the ALC will immediately set the **dPGA** to this level and will restrict the *Release* state from going beyond this level.
  - [3:1] **ALCMINGAIN** set to -6dB. The absolute minimum gain that the **dPGA** is allowed. Upon enable, the ALC will restrict the *Attack* state from going beyond this level.
  - The rest is left at default.
- **ALC_CTRL2.REG0X2D** = 0x***5353***
  - [15:12] **ALCDCY** set to 16ms/step at 0.1875dB ***increase*** per step. Main occurrence in the ALC *Release* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is ***lower***, then the ALC takes another step. If the signal peak is

higher, then the ALC enters the ALC *Attack* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.

- [11:8] **ALCATK** set to 16us/step at 0.1875dB ***decrease*** per step. Main occurrence in the ALC *Attack* state. After each step the signal peak level is compared to the **ALCLVL** register. If the signal peak is higher, then the ALC takes another step. If the signal peak is lower, then the ALC enters the ALC *Hold* state. This setting is the recommended rate but can be adjusted to be faster or slower depending on user design.
- [7:4] **ALCHLD** set to 32ms pause that occurs after the ALC *Attack* state where the ALC attenuates the signal based on the rate set in the **ALCATK** register. After occurring, the ALC will enter the ALC *Release* state. This setting is the recommended delay but can be adjusted to be faster or slower depending on user design.
- [3:1] **ALCLVL** set to -3dBFS. The main component for ALC Normal Limiting Mode. This is the comparison level which triggers the state of the ALC to go into Attack, Release, or Hold as mentioned above.
- The rest is left at default.

- **ALC_CTRL3.REG0X2E** = 0x***B5D0***
  - [15] **ALC_EN** is set to 1. This is the ALC Enable bit and should be the last register to write to ensure proper setup.
  - [14:12] **LIM_MDE** is set to 011. This is set to Low Battery Limiting mode and follows the operation explained in the description portion of this section.
  - [11:10] **VBAT_RATIO** is set to 6:1 to lower the input signal gain following this linear pattern based on VBAT. As VBAT lowers, the input signal gain will also lower by this amount in 1dB increments.
  - [9:5] **VBAT_THRESHOLD** is set to 12.5 V for ALC activation at this voltage.
  - The rest is left at default.
- **ALC_CTRL4.REG0X2F** = 0x***0020***
  - Left at default settings

The register settings above should be implemented as either part of or after the desired ON-sequence. To ensure proper sequence control, use I^2C to write to each of the addresses in the following sequence from first to last: ***0x2C***, ***0x2D***, ***0x2E***. The register ***0x2E*** is written to last as it holds the enable bit and will ensure proper activation of the ALC.

5.13.1.6 Under Voltage Lock Out Prevention Limiter

The NAU83G20 incorporates another battery voltage dependent gain limiter, which can be used independently from the digital ALC described above. The limiter can be used to prevent the system from reaching the Under Voltage Lock Out threshold of 4.0V. Hence, this limiter is referred to as the Under Voltage Lock Out Prevention limiter (UVLOP limiter). The UVLOP limiter provides an attenuation directly at the modulator inputs, allowing for minimal group delay. The gain can be attenuated from 0 to -15.5dB in 0.5dB steps. However, up to 2 dB attack steps can be chosen. The block diagram of the UVLOP Gain Limiter is shown below.

The UVLOP limiter is enabled by setting REG0x31[11] ENABLE_UVLOP=1. When the voltage VBAT goes below the threshold set in REG0x6B_ANALOG_CTRL_8[7:4], the UVLOP limiter will start to attenuate the output signal at the attack rate set in REG0x31[10:8] UVLO_CTRL0.UVLOP_ATK and the gain step set in REG0x31{1:0} UVLO_CTRL0.UVLOP_STEP. The UVLOP limiter attenuations stops at the minimum gains set in UVLO_CTRL1.UVLOP_ATTN. Once the battery voltage recovers above the threshold, the UVLOP limiter will gain up the signal back to 0dB after a hold time UVLO_CTRL0.UVLOP_HLD and using a release step time of UVLO_CTRL0.UVLOP_RLS.

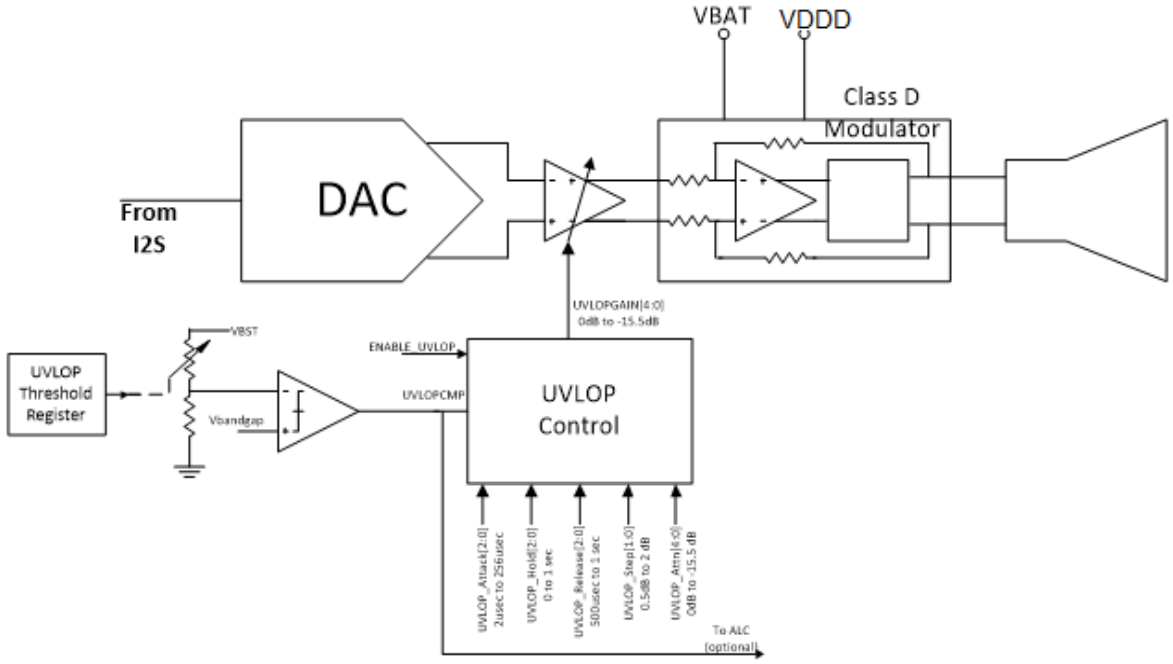


Figure 11 UVLOP Gain Limiter

5.13.1.7 Stereo ALC Gain Tracking Operation

The NAU83G20 incorporates ALC gain communication paths to be used in stereo applications, supported in both I2S and PCM modes. The stereo devices can be setup such that each other's ALC gain can be received. The actual gain applied will then be set to the minimum value of either ALC gain of the stereo devices. Note that this only applies to the ALC gain limiter gain and not the UVLOP limiter gain.

In order to establish the ALC gain communication between the two NAU83G20 devices, the gain data is mutually passed from one device to the other by connecting GPIO1 pins of the two devices together. The communication is enabled by setting **I2S_PCM_CTRL0.ALC_MODE REGx0B [15]** to 1. By default, NAU83G20 receives 6-bit ALC gain data from GPIO1 on the first 8 BCLK cycles after the LRCLK falling edge, and transmits its in-use 6-bit ALC gain data to GPIO1 on the second 8 BCLK cycles. The gain data is outputted on the BCLK falling edge, and received on the BCLK rising edge. The BCLK falling edge needs to align with the LRCLK falling edge, and occur at least 15ns before the LRCLK falling edge in order to receive the data correctly. To reverse the order of transmitting and receiving phases, **I2S_PCM_CTRL0.ALC_SEND_ON_LOC REG0xB [14]** needs to be set to 1. The stereo ALC gain tracking mode is enabled when **ALC_CTRL1.ALCGAIN_SEL_MODE REGx2C [0]** is set to 1. In this mode, NAU83G20 selects the minimum ALC gain value between the two devices, and both shall apply the same minimum ALC gain to their outputs.

A simple test case (Figure 11.1) is to configure both chips into the Low Battery Limiter mode with pre-programmed limit level (**ALC_CTRL3.LIM_MDE REGx2E [14:12] = 3'b011**), and set two different battery threshold for the chips, for example, one is 4.2V, one is 3.2V. When the battery drops below 4.2V, the ALC gain of one device shall be reduced while the other one stays unchanged. When the stereo ALC gain tracking mode is enabled, both devices shall use the lower gain. The applied ALC gain can be monitored in the register **ALC_READOUT1.PGA_GAIN REGx22 [13:8]**, and from ALC gain data on GPIO1. The ALC gain tracking can be reflected by observing these two monitors before and after enabling the mode.

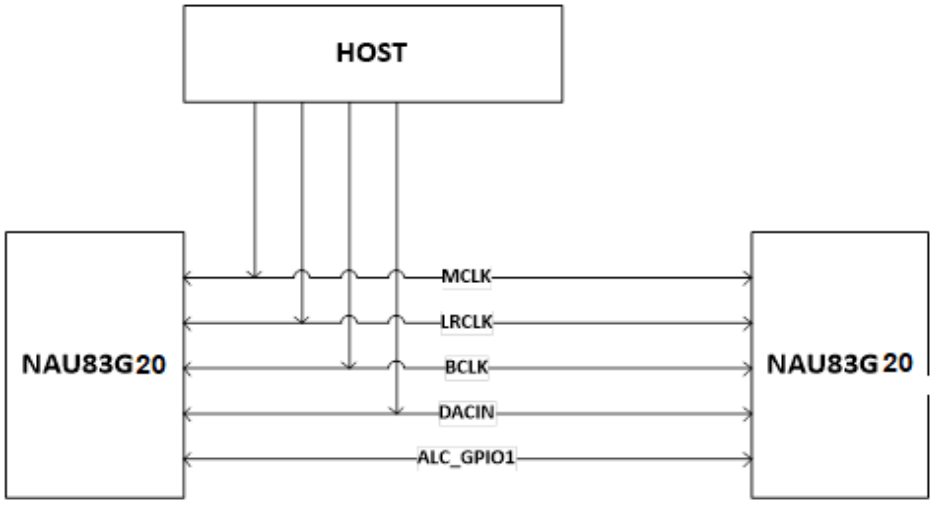


Figure 11.1 Stereo ALC Gain Tracking

5.13.2 Example ALC Values ALC Hold Time

Input signals with different characteristics (such as voice vs. music) may require different settings of the ALC Hold Time parameter for optimum performance. A shorter Hold Time may be useful in voice applications where a faster reaction time helps adjust the volume setting for speakers with different volumes. **Figure 12** shows ALC Input and Output waveforms when no Hold Time is set.

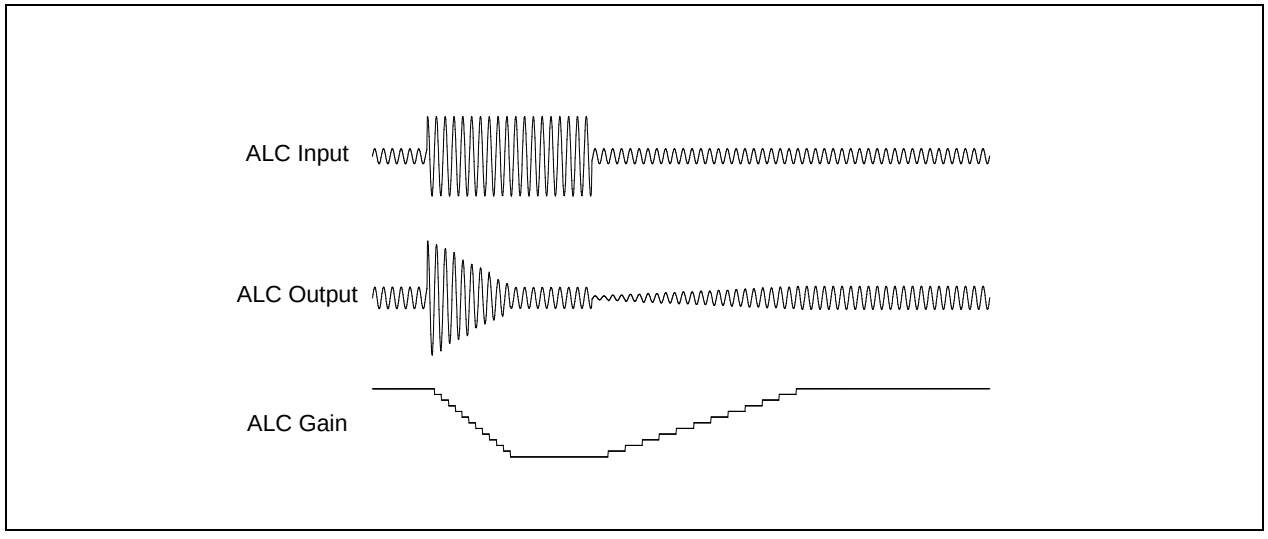


Figure 12 ALC Operation without Hold Time

Increasing the ALC Hold Time prevents the ALC from reacting too quickly to brief periods of silence such as those that may occur in music recordings. **Figure 13** shows ALC Input and Output waveforms when a Hold Time has been set. The Hold Time parameter is set in the **ALC_CTRL2 ALCHLD REG0x2D[7:4]**. In the example, a Hold Time of 16 msec has been set.

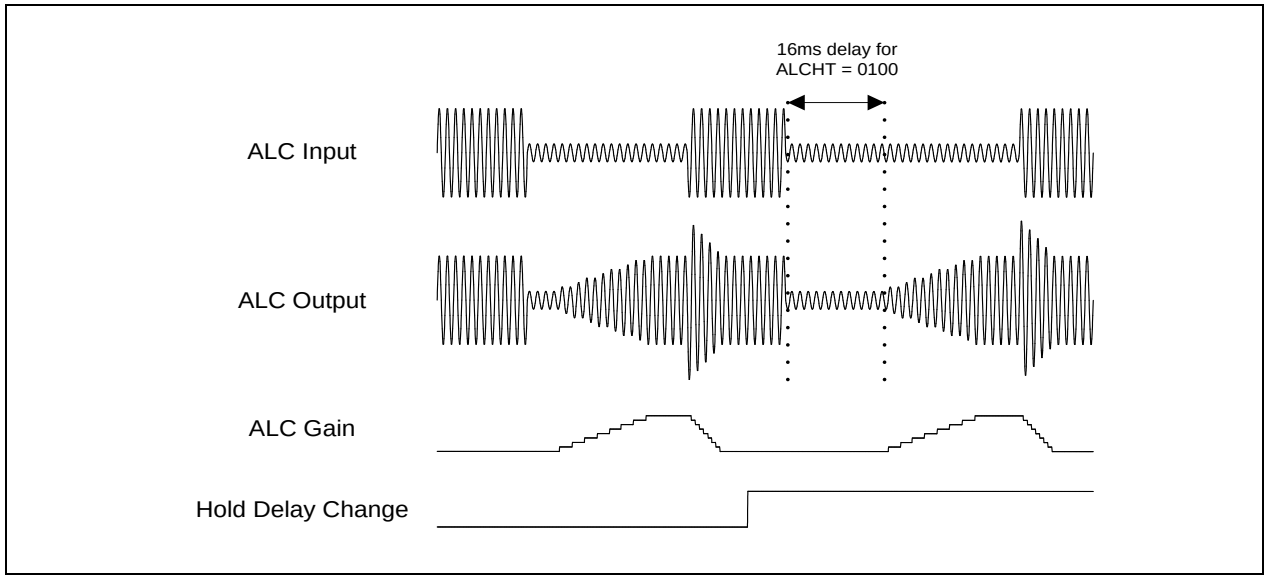


Figure 13 ALC Operation with Hold Time

5.14 Device Protection

The NAU83G20 includes the following types of device protection:

- Over Current Protection (OCP)
- Supply Over Voltage Protection (OVP)
- Under Voltage Lock Out (UVLO)
- Over Temperature Protection (OTP)
- Clock Termination Protection (CTP)

Over Current Protection is provided in the NAU83G20. If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 16.7 µsec, the output drivers will be disabled for 100 msec. The output drivers will then be enabled again and checked for the short circuit. If the short circuit is still present, the output drivers are disabled after 16.7 µsec. This cycle will continue until the short circuit is removed. The short circuit threshold crossing class-D output is 4.0 A at VDDD is 3.6 V.

Supply Over Voltage Protection (OVP) is provided in the NAU83G20. If the VBAT supply voltage reaches 16.5 V, the output drivers will be set to pull down to ground while the NAU83G20 control circuitry continues to operate. If the supply drops below 12 V, the output drivers are re-enabled.

Under Voltage Lock Out (UVLO) provides Supply Under Voltage Protection in the NAU83G20. If the VDD supply voltage drops below 2.4 V or VBAT drops below 4V, the output drivers will be disabled while the NAU83G20 control circuitry continues to operate. This will prevent the battery supply from going too low before the host processor can safely shut down the devices on the system. If the supply goes back up, the drivers will be enabled again at VDDD 2.55 V. If the supply drops further (below 1.6 V), the internal power-on reset is activated and puts the entire device into the power-down state.

Over Temperature Protection (OTP) is provided in the event of thermal overload. When the internal junction temperature of the device reaches 135°C, the NAU83G20 will disable the output drivers. When the device cools down and a safe operating temperature of 120°C has been achieved for at least 100 usec, the output drivers will be enabled again.

Clock Termination Protection (CTP) is provided in the NAU83G20. If the clock stops running, the NAU83G20 automatically shuts down the Class-D driver, if Clock Detection is enabled (see clock detection section).

5.15 Power-up and Power-Down Control

When the supply voltage ramps up, the internal power on reset circuit is triggered. At this time, all internal circuits will be set to the power-down state. The device can be enabled by initializing the registers and starting the clocks. Upon starting the clocks, the device will go through an internal power-up sequence in order to minimize 'pops' on the speaker output. The complete power-up sequence requires about 4 msec. The device will power down in about 30 µsec, when the clocks are stopped.

NOTE: It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize the 'pops' when the clocks are stopped.

5.16 Bypass Capacitors

Bypass capacitors are required to remove the AC ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 10 µF and 0.1 µF are sufficient to achieve good performance.

5.17 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. It is better to use low-resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

5.17.1 Recommended PCB Footprint

The recommended footprint for the PCB layout for the NAU83G20 is provided in **Figure 14**, as viewed from the top of the pcb.

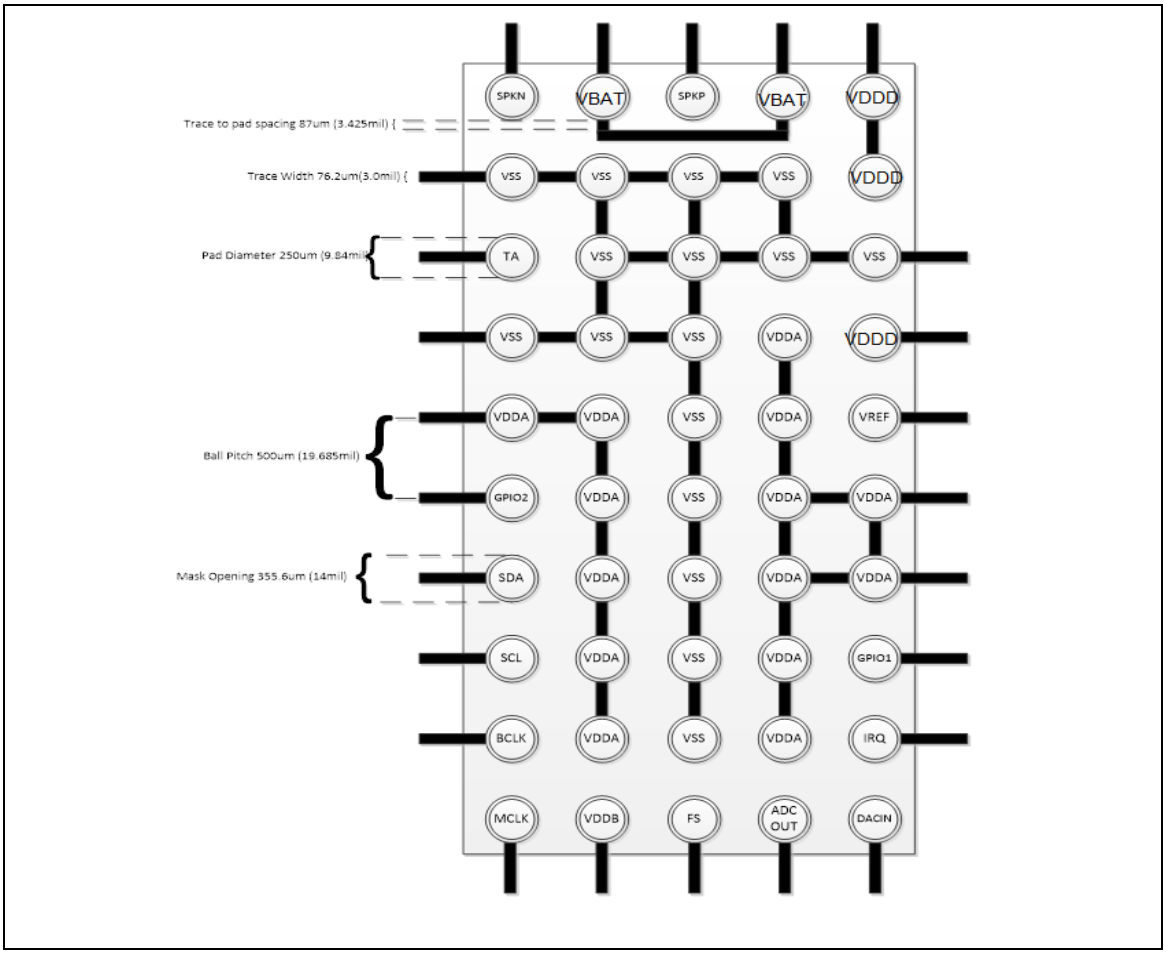


Figure 14 Recommended PCB Footprint

5.17.2 PCB Layout Notes

Given the efficiency of the Class-D Amplifier, this requires up to 3 Amperes of peak current. The Class-D Amplifier is a high power switching circuit that can cause Electro Magnetic Interference (EMI) when it is poorly connected. Therefore, care must be taken in designing the PCB to eliminate Electro Magnetic Interference (EMI), reduce IR drops, and maximize heat dissipation.

The following notes are provided to assist product design and enhance product performance:

- Use a VSS plane, preferably on both sides, to shield clocks and reduce EMI
- Maximize the copper to the VSS balls and have solid connections to the plane
- Planes on VDDA, VDDB, VDDD & VBAT are optional
- The VBAT connection needs to be a solid piece of copper
- Use thick copper options on the supply layers if cost permits
- Use 2Mil copper or plated copper on the top layer
- Place the VBAT decoupling capacitor close to the NAU83G20
- Use a big VIA outside the NAU83G20 to connect the VBAT balls in parallel with the inner trace
- Keep the speaker connections short and thick. Do not use VIAs
- Use a small speaker connector like a wire terminal block (Phoenix Contact)
- Keep the VREF capacitor close to the ball.
- For better heat dissipation, use ball VIAs to conduct heat to the other side of the PCB
- Do not use VIA's to connect C1, C2, C6, SPK+ & SPK- to U1. Use a direct top layer copper connection to the balls. Thick copper is preferred.
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane

- The digital IO lines can be shielded between power planes
- The ground return of D0 should run separately back to the NAU83G20
- For the traces that run between the balls, follow the guidelines listed in **Figure 14** and see the example illustrated in **Figure 15.**

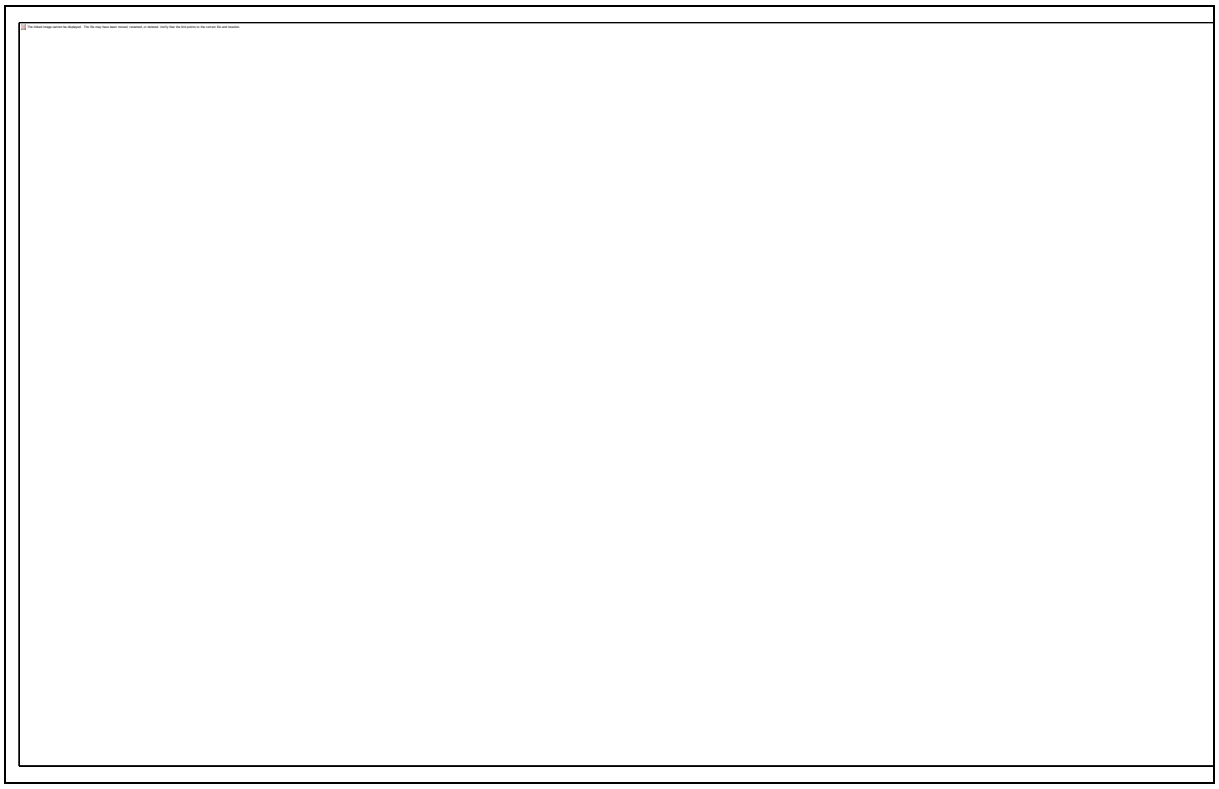


Figure 15 Layout Traces Example

5.18 Filters

The NAU83G20 is designed for use without any filter on the output line. However, the NAU83G20 may be used with or without various types of filters, depending on the needs of the application.

5.18.1 Class D without Filters

The NAU83G20 is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filter-less design is suitable for portable applications where the speaker is very close to the amplifier. In other words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. **Figure 16** illustrates this simple configuration.

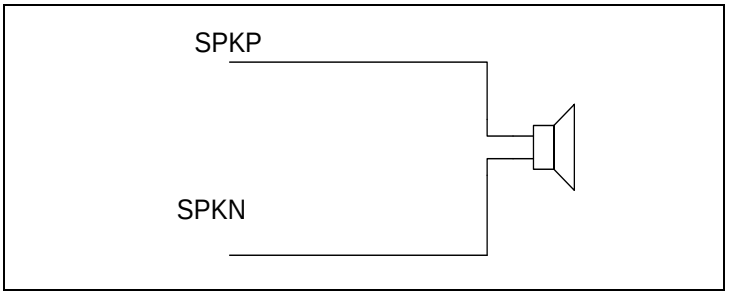


Figure 16 NAU83G20 Speaker Connections without Filter

5.18.2 Class D with Filters

In some applications, shorter trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, long traces will cause EMI issues. Several types of filter circuits are available to reduce the EMI effects. These are Ferrite Bead Filters, LC filters, Low-Pass LCR Filters, and High-Pass Filters.

Ferrite Bead Filters are used to reduce high-frequency emissions. The characteristic of a Ferrite Bead Filter is such that it offers higher impedance at high frequencies. For better EMI performance, select a Ferrite Bead Filter which offers the highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. The typical circuit diagram using a Ferrite Bead Filter for each output to the speaker is shown Figure 17 NAU83G20 Speaker Connections with Ferrite Bead Filters.

NOTE: Usually, the ferrite beads have low impedance in the audio range, so they will act as pass-through filters in the audio frequency range.

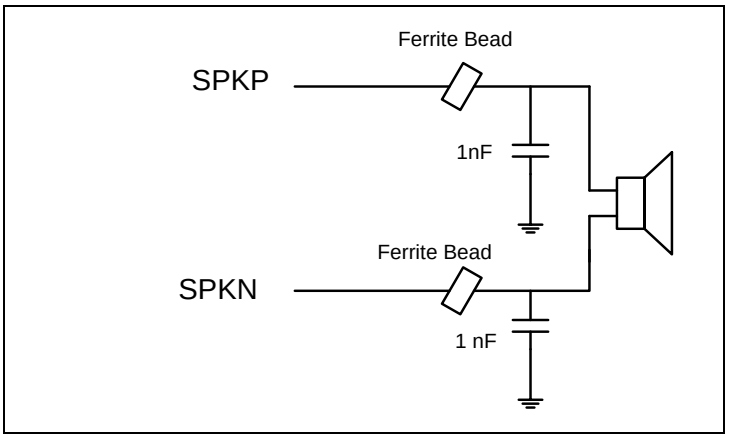


Figure 17 NAU83G20 Speaker Connections with Ferrite Bead Filters

LC Filters are used to suppress low-frequency emissions. The diagram in **Figure 18** shows the NAU83G20 outputs connected to the speaker with an LC Filter circuit. R_L is the resistance of the speaker coil.

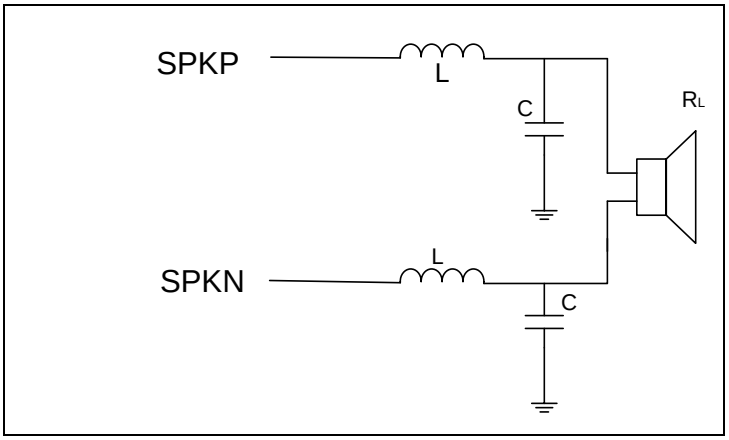


Figure 18 NAU83G20 Speaker Connections with LC Filters

Low-Pass LCR Filters may also be useful in some applications where long traces or wires to the speakers are used. **Figure 19** shows the speaker connections using standard Low-Pass LCR Filters.

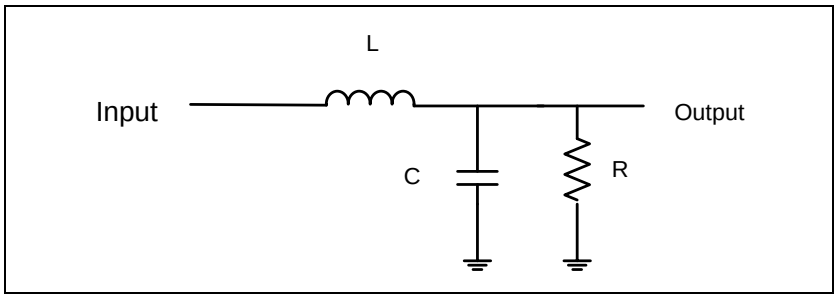


Figure 19 NAU83G20 Speaker Connections with Low-Pass Filters

The following equations apply for critically damped (ζ = 0.707) standard Low-Pass LCR Filters:

$$2\pi fc = \frac{1}{\sqrt{(LC)}} \qquad fc \text{ is the cut-off frequency}$$

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

NOTE: The L and C values for differential configuration can be calculated by duplicating the single-ended configuration values and substituting RL = 2R.

5.19 Control Interfaces

The NAU83G20 includes a serial control bus that provides access to all of the device control registers and may be configured as a 2-wire interface that conforms to industry standard implementations of the I2C serial bus.

5.19.1 2-Wire-Serial Control Mode (I²C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU83G20 can function only as a slave device when in the 2-wire interface configuration.

5.19.2 2-Wire Protocol Convention

To initiate communication, all 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH.

Following a START condition, the master must output a device address byte consisting of a 7-bit device address, and a Read/Write control bit in the LSB of the address byte. To read from the slave device, the R/W bit must be set to 1. To initiate a write to the slave device, the R/W bit must be 0. If the device address matches the address of a slave device, the slave will output an acknowledgement bit.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits and during the ninth clock cycle, the receiver (slave) pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

To terminate a read/write session, all 2-Wire interface operations must end with a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

Application Notes:

The NAU83G20 is programmed with 0x10, 0x11, 0x40, and 0x41 as the Device Address.

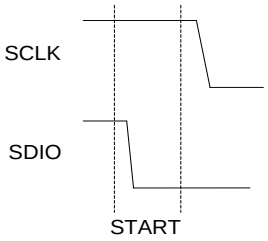


Figure 20 Valid START Condition

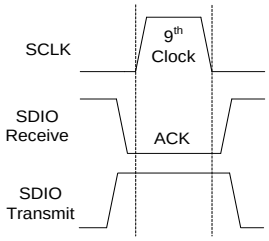


Figure 21 Valid Acknowledge

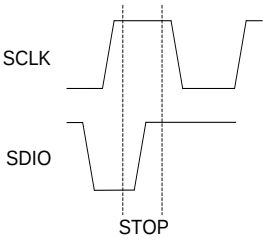


Figure 22 Valid STOP Condition

5.19.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more data bytes as seen in Figure 23 . These instructions consist of the Address byte and two Control Address bytes that precede the START condition and are followed by the STOP condition. Figure 24 shows the data bus and the corresponding clock cycles with device address is 0x10 case as an example.

0	0	1	0	0	0	0	R/W	Device Address Byte
A15	A14	A13	A12	A11	A10	A9	A8	Control Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	
D15	D14	D13	D12	D11	D10	D9	D8	Data Byte
D7	D6	D5	D4	D3	D2	D1	D0	

Figure 23 Slave Address Byte, Control Address Byte, and Data Byte

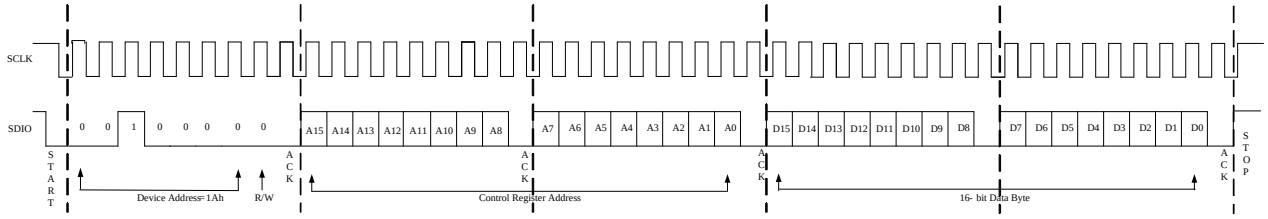


Figure 24 2-Wire Write Sequence

5.19.4 2-Wire Read Operation

A Read operation consists of the three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, Device Address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the NAU83G20 which of its control registers is going to be accessed.

After this, the NAU83G20 will respond with an ACK as it accepts the Control Register Address that the master is transmitting to it. After the Control Register Address has been sent, the master will send a second START condition and Device address but with R/W = 1.

After the NAU83G20 recognizes its Device Address the second time, it will transmit an ACK followed by a two byte value containing the 16 bits of data in the NAU83G20 control registers requested by the master. During this phase, the master generates an ACK with each byte of data transferred.

After the two bytes have been transmitted, the master will send a STOP condition ending the read phase. If no STOP condition is received, the NAU83G20 will automatically increment the target Control Register Address and then start sending the two bytes of data for the next register in the sequence. This will continue as long as the master continues to send ACK signals. Once the target register reaches 0xFFFF, it will send the associated data then roll over to 0x0000 and continue as before.

Figure 25 shows the data bus and the corresponding clock cycles with device address is 0x10 case as an example.

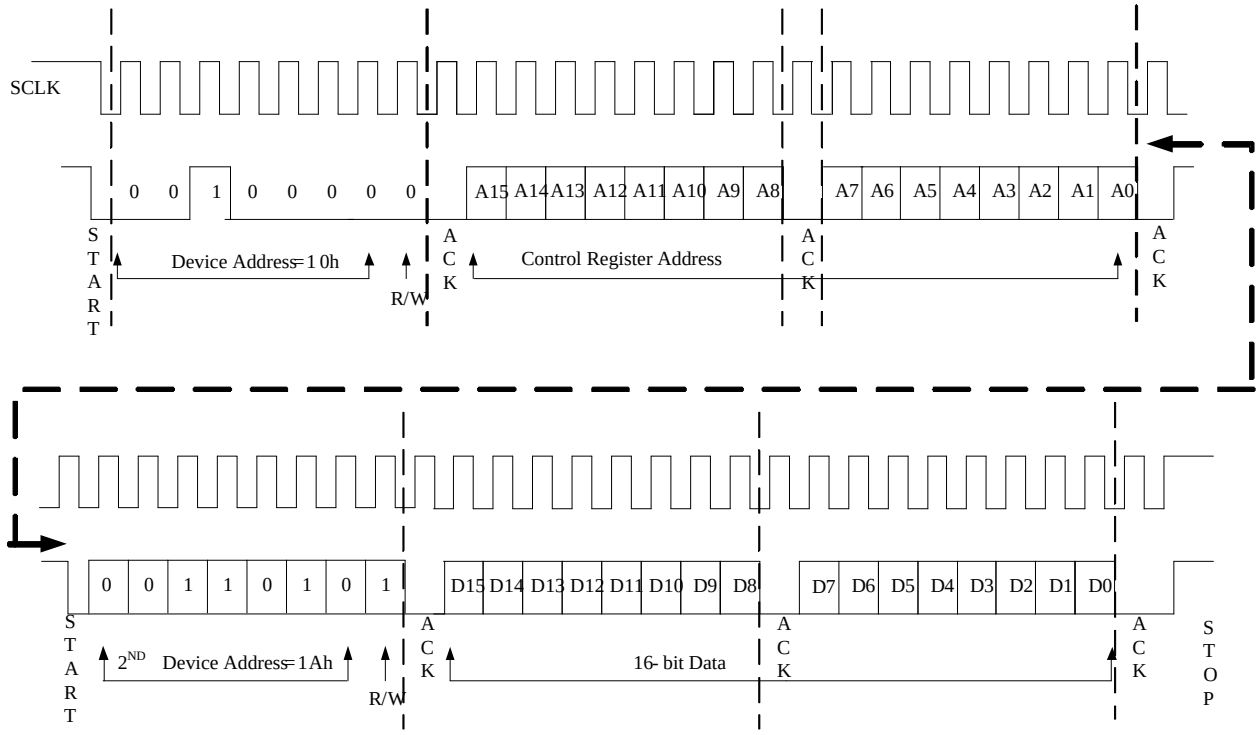


Figure 25 2-Wire Read Sequence

5.19.5 Digital Serial Interface Timing

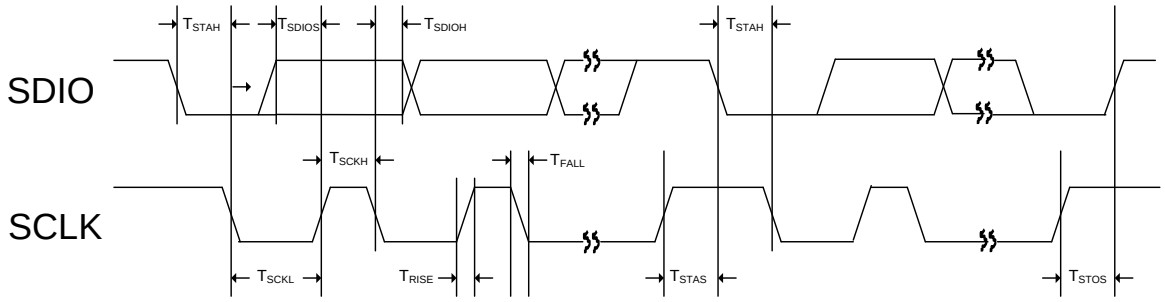


Figure 26 Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

5.19.6 Software Reset

The NAU83G20 and all of its control registers can be reset to default initial conditions by writing any value to REG0X00 twice using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their power-on default values.

5.20 Digital Audio Control Interface

The NAU83G20 includes an I2C Control Interface as well as an I2S/PCM Audio Interface. The following sections describe the Control and Audio Interfaces and registers.

5.20.1 Digital Control Interface

The NAU83G20 uses an I2C Interface with pin programmable (GPIO1, GPIO2) addresses. The I2C address = 0x10, 0x11, 0x40, 0x41.

GPIO2 = 0, GPIO1 = 0, selects I2C_DEVID = 7'h10
GPIO2 = 0, GPIO1 = 1, selects I2C_DEVID = 7'h11
GPIO2 = 1, GPIO1 = 0, selects I2C_DEVID = 7'h40
GPIO2 = 1, GPIO1 = 1, selects I2C_DEVID = 7'h41

5.20.2 Digital Audio Interface

The NAU83G20 can be configured as either the Master or the Slave, by setting register **I2S_PCM_CTRL2 MS0 REG0XE[3]** to 1 for Master Mode or setting it to 0 for Slave Mode. Slave Mode is the default if this bit is not written. In Master Mode, NAU83G20 outputs both Frame Sync (FS) and the audio data Bit Clock (BCLK) and has full control of the data transfer. In Slave Mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; and ADCOUT clocks out ADC data, while DACIN clocks in data for the DACs.

When not transmitting data, ADCOUT pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the Time Slot function is enabled, there are additional output state modes, including controlled tri-state capability (see **Section 9.2.9**).

The NAU83G20 has one DAC channel and two ADC channels. The ADC left and right channel data could be swapped in the I2S Interface by setting register **I2S_PCM_CTRL1 ADCPHS0 REG0XD[5]** to 1.

WHEN ADC_RATE I2S_MODE REG0X28[15], the I2S Interface ADC path will transmit normal audio data . If both of them are set to 0, the ADC path will transmit I/V Sense data and SAR ADC data, which could be in either signed or unsigned format by setting **TDM_CTRL UNSIGN_IV REG0XC[9]** to be 0 or 1, respectively. The I2S Interface DAC path will transmit normal audio data at any situation.

The NAU83G20 supports four port data lengths: 16, 20, 24, and 32 bits by setting **I2S_PCM_CTRL1 WLEN0 REG0XD[3:2]** The chip also supports 8-bit word length for Compounding Mode operation by setting **I2S_PCM_CTRL1 CMB8_0 REG0XD[10]** to 1.

The NAU83G20 supports ten audio formats: I2S, Right Justified, Left Justified, TDM I2S, TDM Right Justified, TDM Left Justified, PCM A, PCM B, PCM Offset, and PCM Time Slot.

When operated in the TDM I2S, TDM Right Justified, or TDM Left Justified mode and in all PCM modes, the NAU83G20 supports 8-channel data transmission on both ADC and DAC paths simultaneously. **TDM_CTRL TDM REG0XC[15]** should be set = 1 if using TDM I2S, TDM Right Justified, or TDM Left Justified modes.

Table 16 Digital Audio Interface Mode Settings

PCM Mode	I2S_PCM_ CTRL1 AIFMT0 **REG0XD[1:0]**	I2S_PCM_ CTRL1 LRP0 **REG0XD[6]**	I2S_PCM_CTRL2 PCM_TS_EN0 **REG0XE[10]**	TDM_CTRL PCM_OFFSET_MODE_CTRL **REG0XC[14]**
Right Justified	00	0	0	0
Left Justified	01	0	0	0
I2S	10	0	0	0
PCM A	11	0	0	0
PCM B	11	1	0	0
PCM Offset	11	Don't care	0	1
PCM Time Slot	11	Don't care	1	0

Left-Justified Audio Data

In Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is HIGH, Channel 0 data are transmitted; when FS is LOW, Channel 1 data are transmitted. This can be seen in **Figure 27**.

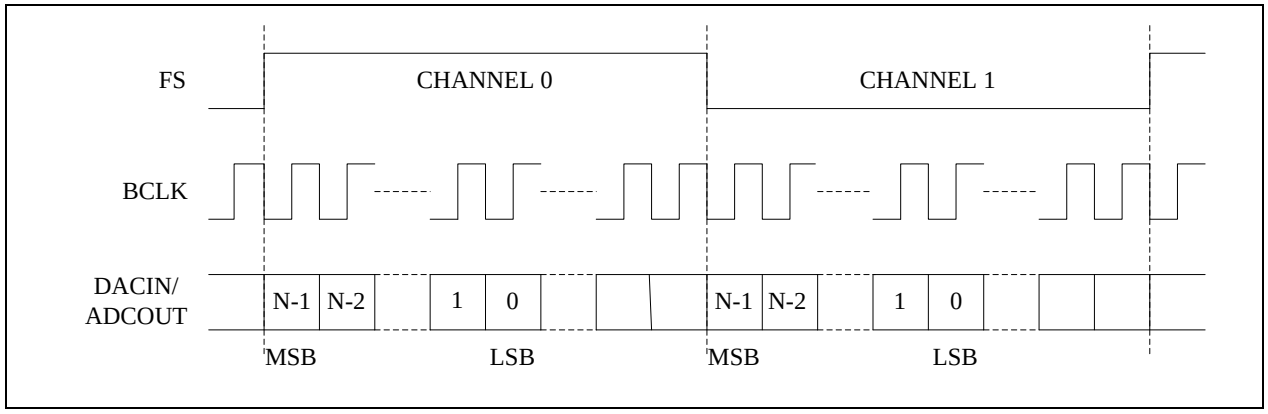


Figure 27 Left-Justified Audio Data

I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Left Channel data are transmitted; when FS is HIGH, Right Channel data are transmitted. This can be seen in **Figure 28**. Note: In standard I2S mode the V-sense channel has one sample delay with respect to the I-sense channel.

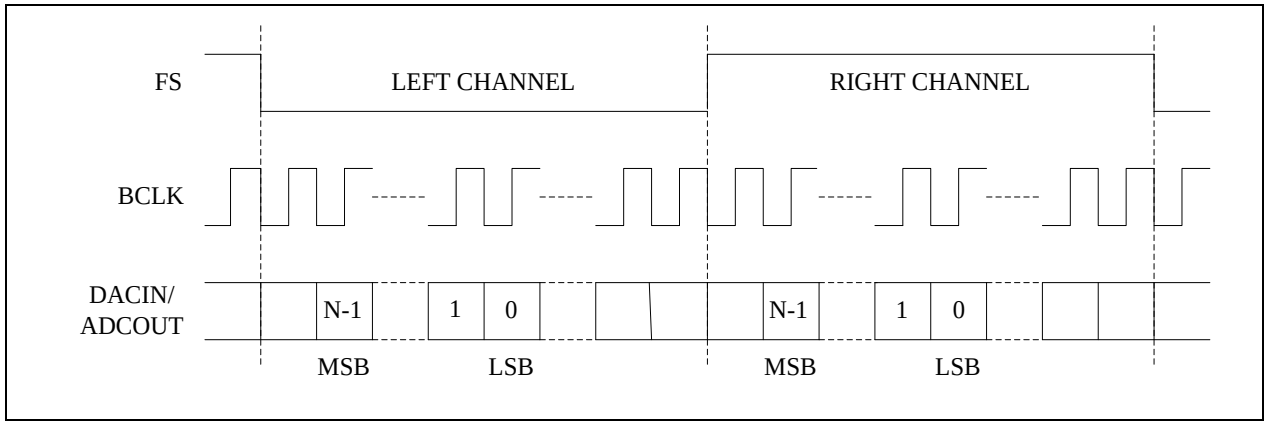


Figure 28 I2S Audio Data

TDM Left-Justified Audio Data

In TDM Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is LOW, Channel 1 data are transmitted, then Channel 3, 5, and 7 data are transmitted; when FS is HIGH, Channel 0 data are transmitted, then Channel 2, 4, and 6 data are transmitted. This is shown in **Figure 29**.

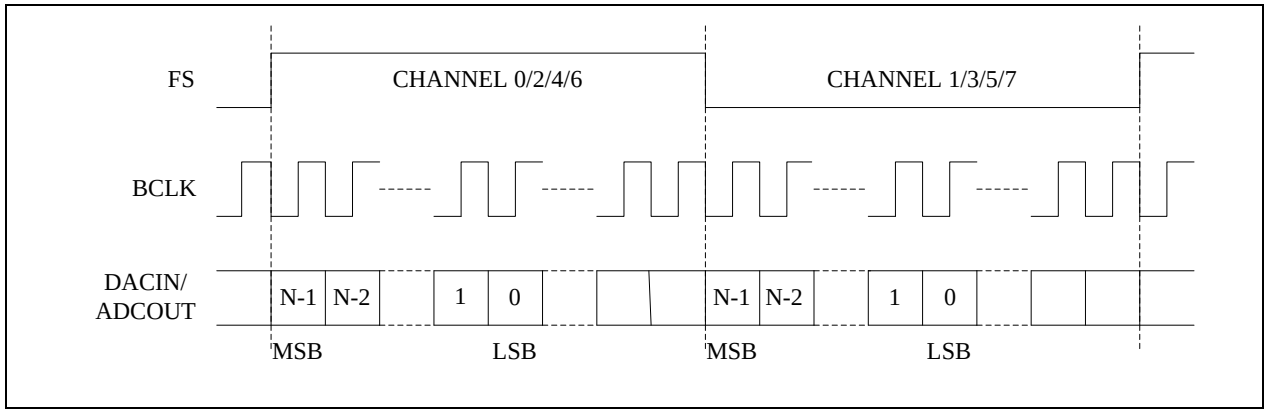


Figure 29 TDM Left-Justified Audio Data

TDM I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Channel 0 data are transmitted, then Channel 2, 4, and 6 data are transmitted; when FS is HIGH, Channel 1 data are transmitted, then Channel 3, 5, and 7 data are transmitted. This is shown in **Figure 30.**

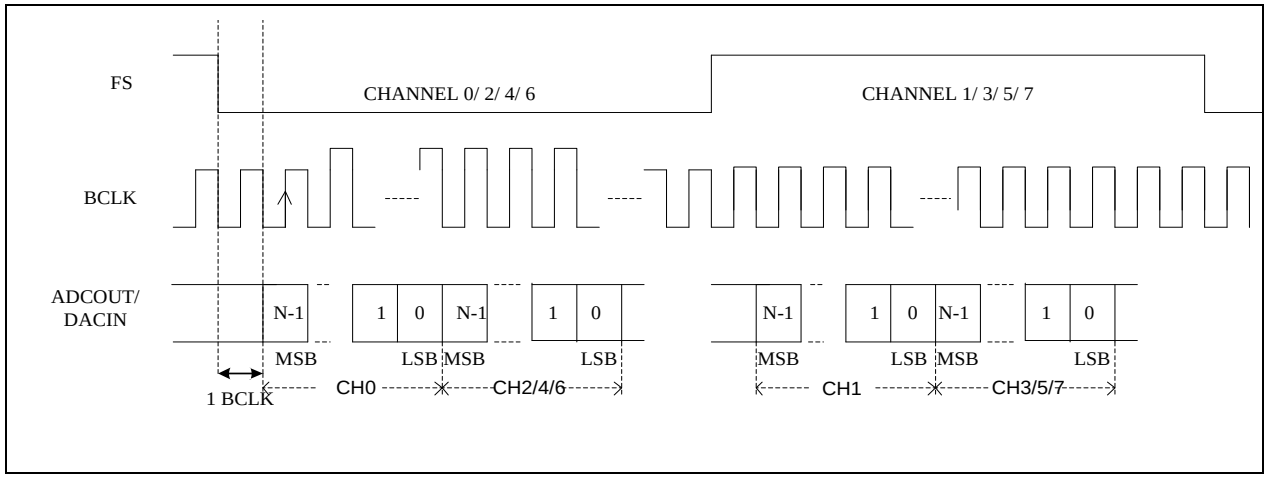


Figure 30 TDM I2S Audio Data

PCM A Audio Data

In PCM A Mode, Channel 0 data are transmitted first, followed sequentially by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in **Figure 31.** Note that this supports only 8 channels as shown here.

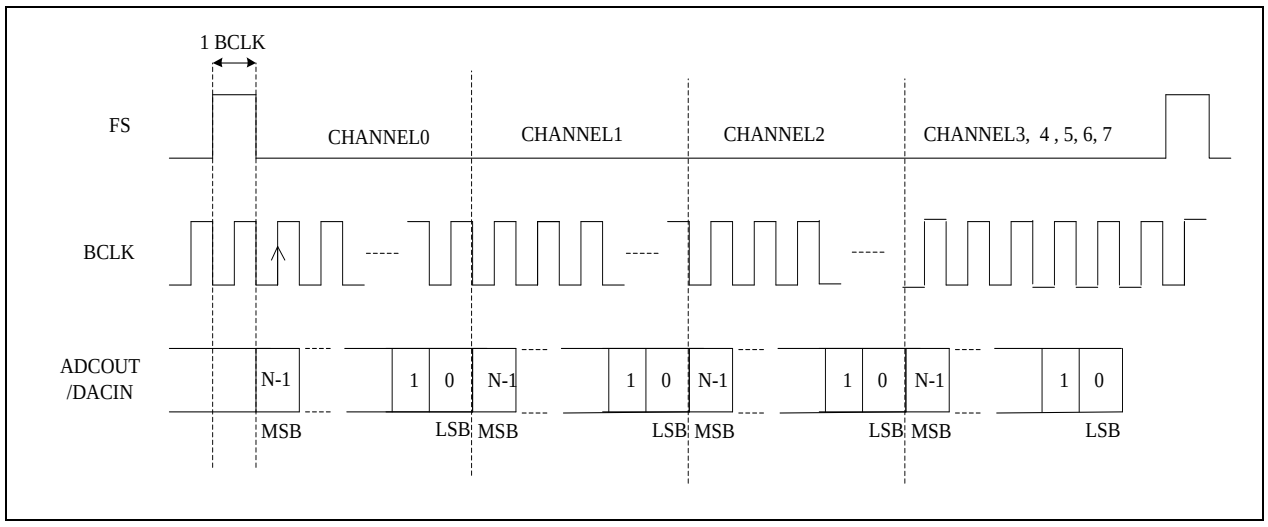


Figure 31 PCM A Audio Data

PCM B Audio Data

In PCM B Mode, Channel 0 data are transmitted first, followed immediately by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the Channel 1 MSB is clocked on the next SCLK after the Channel 0 LSB. This is shown in **Figure 32**.

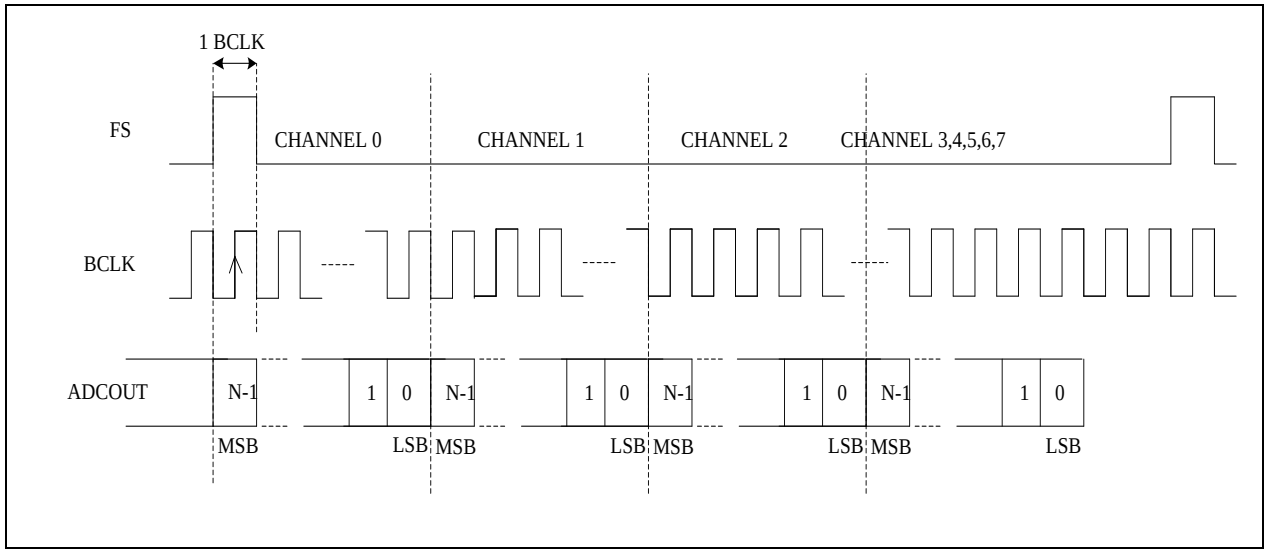


Figure 32 PCM B Audio Data

PCM Time Slot Audio Data

PCM Time Slot Mode is used to delay the time at which the DAC and/or ADC data are clocked. This can be useful when multiple NAU83G20 chips or other devices share the same audio bus. This will allow the audio from the chips to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS); however, in PCM Time Slot Mode, the audio data can be delayed by setting **LEFT_ TIME_SLOT TSLOT_L0 REG0XF[9:0]** and **RIGHT_ TIME_SLOT TSLOT_R0 REG0X10[9:0]** for the left and right channels, respectively. **I2S_PCM_ CTRL2 PCM_TS_ EN0 REG0XE[10]** needs to be set to 1. These delays can be seen before the MSB in **Figure 33**.

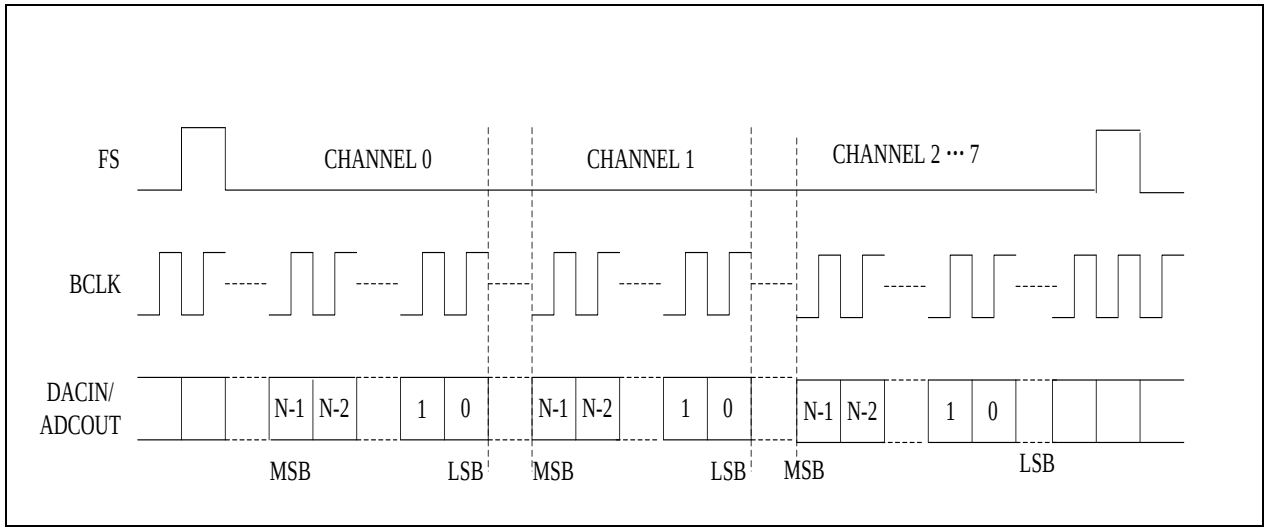


Figure 33 PCM Time Slot Audio Data

APPLICATION NOTES:

- When using the NAU83G20 with other driver chips, the ADCOUT pin can be set to pull up or pull down by enabling **I2S_PCM_CTRL2_ADCDAT0_PE_REG0XE[6]** and selecting up or down with **I2S_PCM_CTRL2 ADCDAT0_PS REG0XE[5]**. This allows for wired-OR type bus sharing. If both are set to 0, ADCOUT is high impedance, except when transmitting channel audio data. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent time slots with reduced risk of bus- driver contention.
- If **I2S_PCM_CTRL2 ADCDAT0_OE REG0XE[4]** is set to 0, ADCOUT is a output buffer. After ADCOUT sent the last bit, ADCOUT bus line will stay at the last bit value after ADCOUT finished the data. If the last bit is high, then it will slowly drain down to ground, because the output buffer is still on. If 0xE[4] is set to 1, after the last bit, ADCOUT becomes high Z, ADCOUT bus line become 0.

PCM Time Offset Audio Data

PCM Time Offset Mode is used to delay the time at which the DAC and/or ADC data are clocked. This increases the flexibility of the NAU83G20 for use in a wide range of system designs. One key application of this feature is to enable multiple NAU83G20 chips or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data. **TDM_CTRL PCM_OFFSET_MODE_CTRL REG0XC[14]** must be set to 1 for this application.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS). In this mode, audio data are delayed by a delay count specified in the device control registers. The Channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in **LEFT_TIME_SLOT TSLOT_L0 REG0XF[9:0]**. The subsequent channel's MSB is clocked on the next BCLK after the LSB of the previous channel. This can be seen in **Figure 34**.

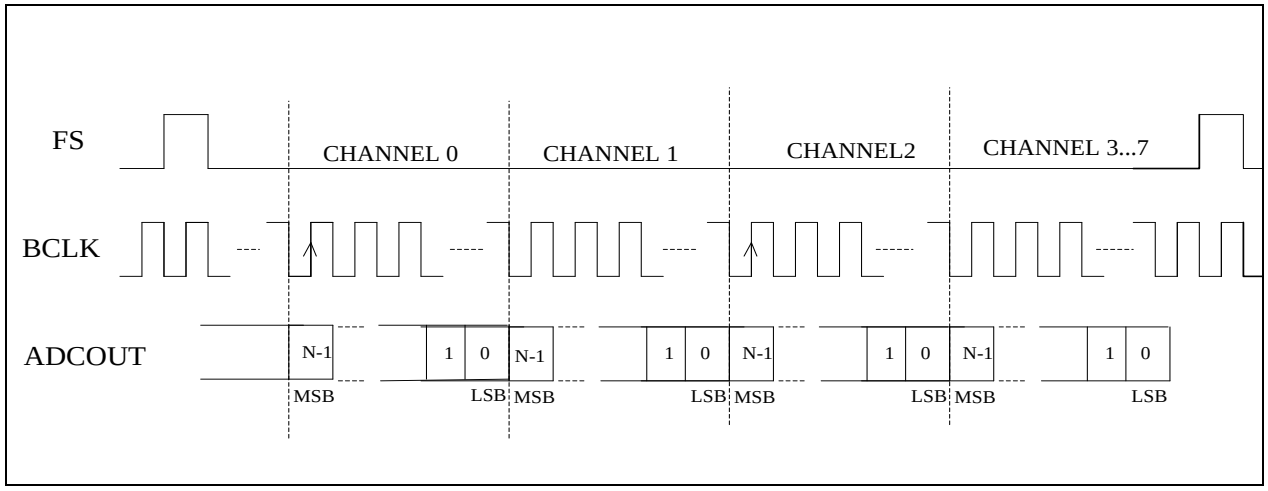


Figure 34 PCM Time Offset Audio Data

Stereo ALC Data

Stereo ALC uses are using GPIO to do the transmission. Two independent stereo configurations are okay. For one group, you set ALC_SEND_ON_LOC to 0 for one devices and ALC_SEND_ON_LOC to 1 for other devices.For the second group , you also set ALC_SEND_ON_LOC to 0 for one devices and ALC_SEND_ON_LOC to 1 for other devices.

We are not using the I2S channel. The device which ALC_SEND_ON_LOC is 0 will receive ALC gain data from GPIO1 on the first 8 BCLK cycles after the LRCLK falling edge, and transmits its in-use ALC gain data to GPIO1 on the second 8 BCLK cycles.

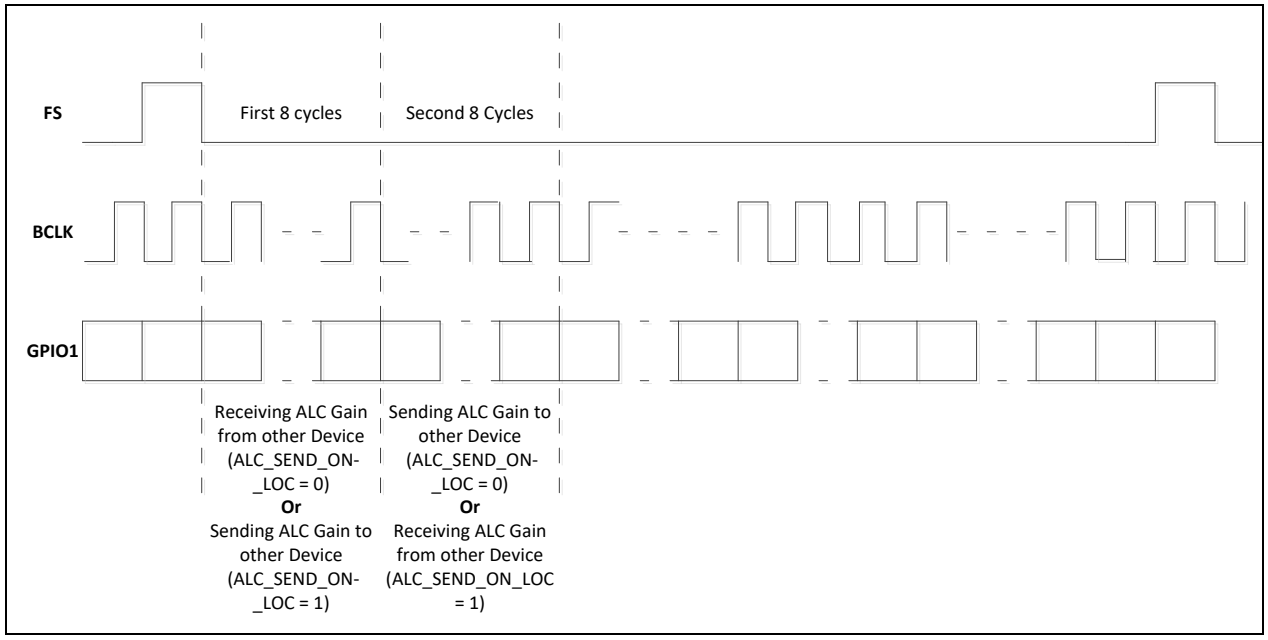


Figure 35 Stereo ALC Audio Data

I/V Sense Data Stereo Mode

I/V Sense Data Stereo Mode is used to transmit I/V Sense data and SAR ADC data in two ADC channels. This mode may be operated in all ten audio formats and three port word lengths when **ADC_RATE I2S_MODE REG0X28[15]** and **ADC_RATE UNSIGN_IV REG0X28[7]** are both set to 0 and **TDM_CTRL PINGPONG_MODE REG0XC[8]** is also set to 0.

The ADC path Left and Right Channel transmission data could be swapped in the I2S Interface by setting register **I2S_PCM_CTRL1 ADCPHS0 REG0XD[5]** to 1. By default, the Left Channel will transmit V Sense data and SAR ADC output type; the Right Channel will transmit I Sense data and SAR ADC output messages. The exact bit definition depends on the port word length. Refer to **Table 17** for I/V Sense port word length options. See **Figure 36**, **Figure 37**, and **Figure 38** for the 16-, 24-, and 32-bit timing diagrams.

Table 17 I/V Sense Data Stereo Mode Settings

16-bit	ADCOUT[16:0]
Left Channel	16-bit V Sense Data
Right Channel	16-bit I Sense Data

24-bit	ADCOUT[24:8]	ADCOUT[7:4]	ADCOUT[3:0]
Left Channel	16-bit V Sense Data	4-bit Preamble	4-bit Type
Right Channel	16-bit I Sense Data	8-bit Message[7:4]	8-bit Message [3:0]

32-bit	ADCOUT[32:16]	ADCOUT[16:12]	ADCOUT[11:8]	ADCOUT[3:0]
Left Channel	16-bit V Sense Data	4-bit Preamble	4-bit Type	8-bit Consecutive Zero
Right Channel	16-bit I Sense Data	8-bit Message [7:4]	8-bit Message [3:0]	8-bit Consecutive Zero

The Preamble is a fixed value set to be 4-bit 1010.

The 4-bit type and 8-bit data corresponding chart is shown in **Table 18.** The 8 bit message can also retrieve from Reg0x 20 SAR_ADC_OUT_01 and Reg0x21 SAR_ADC_OUT_23.

Table 18 4-Bit Type and 8-Bit Message Values

4-bit Type	8-bit Message
0000	Tj
0001	Ta
0011	VDDD

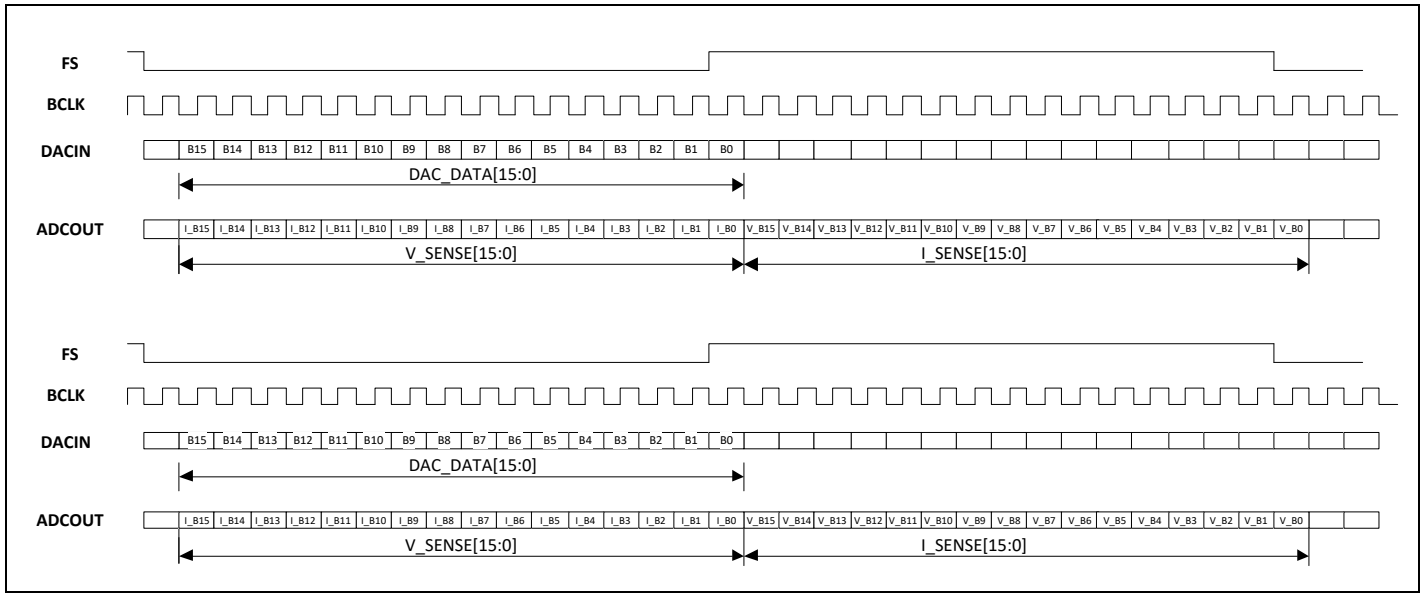


Figure 36 16-Bit I2S Stereo Mode Timing Diagram

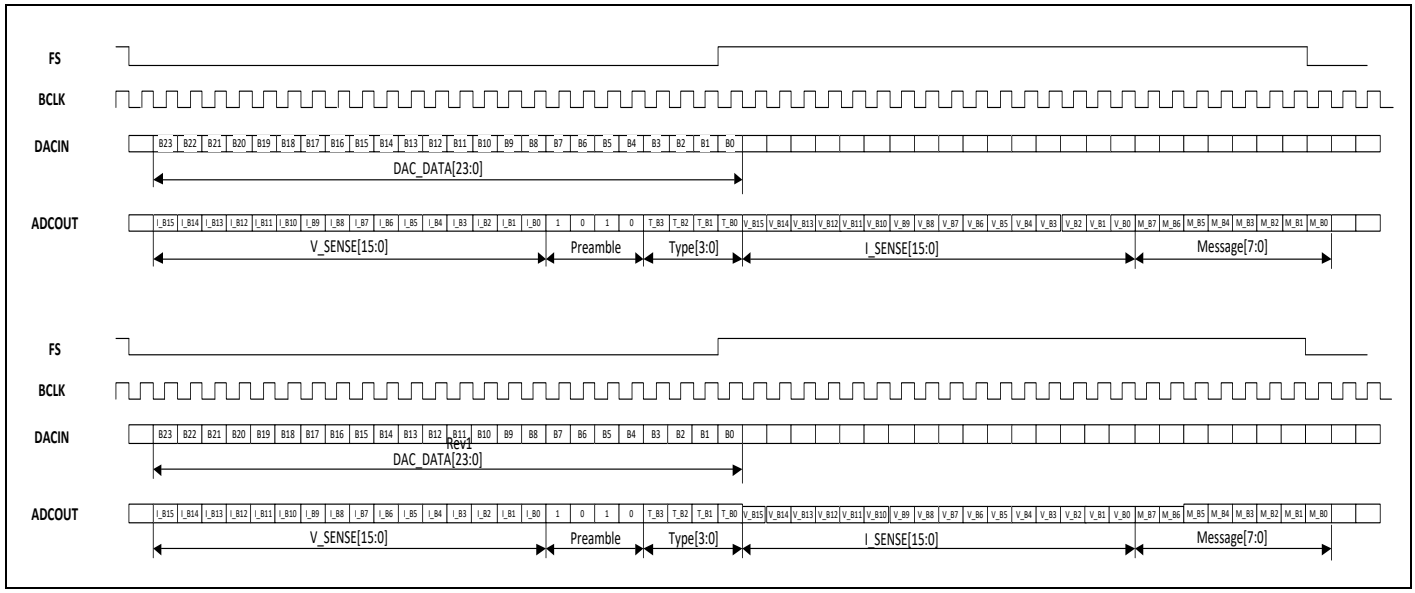


Figure 37 24-Bit I2S Stereo Mode Timing Diagram

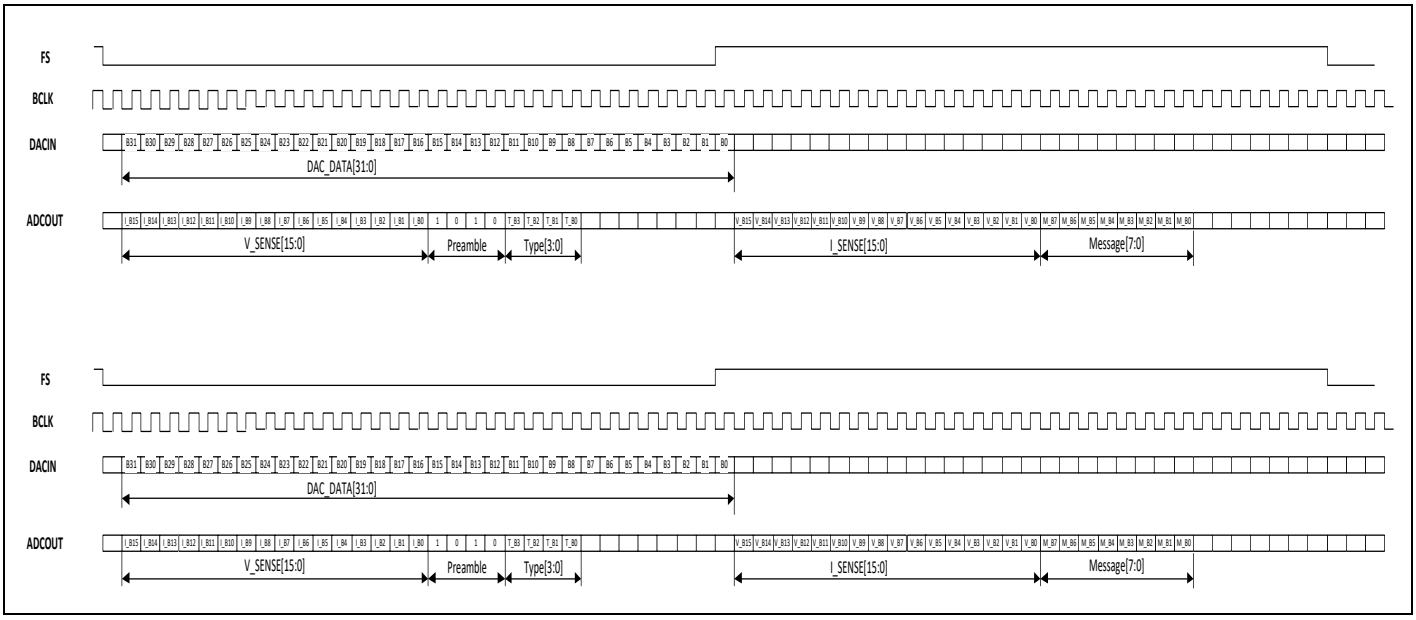


Figure 38 32-Bit I2S Stereo Mode Timing Diagram

I/V Sense Data Ping Pong Mode

I/V Sense Data Ping Pong Mode is used to transmit I/V Sense data and SAR ADC data in a single ADC channel. This mode may be operated in all ten audio formats and three port word lengths when **ADC_RATE I2S_MODE REG0X28[15]** and **ADC_RATE UNSIGN_IV REG0X28[7]** are both set to 0 and **TDM_CTRL PINGPONG_MODE REG0XC[14]** is set to 1.

The ADC path Left or Right Channel will transmit I Sense data and SAR ADC output type in one FS time frame and transmit V Sense data and SAR ADC output messages in the next FS time frame, alternately. The exact bit definition depends on the port word length. Refer to **Table 19** for I/V Sense Ping Pong Mode port word length options. See **Figure 39**, **Figure 40,** and **Figure 41** for the 16-, 24-, and 32-bit timing diagrams for I/V Sense Ping Pong Mode.

Table 19 I/V Sense Data PingPong Mode Settings

16-bit	ADCOUT[16:0]			
FS Phase I	16 bit V Sense Data			
FS Phase II	16 bit I Sense Data			
24-bit	**ADCOUT[24:8]**	**ADCOUT[7:4]**	**ADCOUT[3:0]**	
FS Phase I	16-bit V Sense Data	4-bit Preamble	4-bit Type	
FS Phase II	16-bit I Sense Data	8-bit Message[7:4]	8-bit Message [3:0]	
32-bit	**ADCOUT[32:16]**	**ADCOUT[16:12]**	**ADCOUT[11:8]**	**ADCOUT[7:0]**
FS Phase I	16-bit V Sense Data	4-bit Preamble	4-bit Type	8- bit consecutive zero
FS Phase II	16-bit I Sense Data	8-bit Message [7:4]	8-bit Message [3:0]	8- bit consecutive zero

The Preamble is a fixed value set to be 4-bit 1010.

The 4-bit type and 8-bit data corresponding chart is shown in **Table 20.** The 8 bit message can also retrieve from Reg0x20 SAR_ADC_OUT_01 and Reg0x21 SAR_ADC_OUT_23**.**

Table 20 4-Bit Type and 8-Bit Message Values

4-bit Type	8-bit Message
0000	Tj
0001	Ta
0011	VDDD

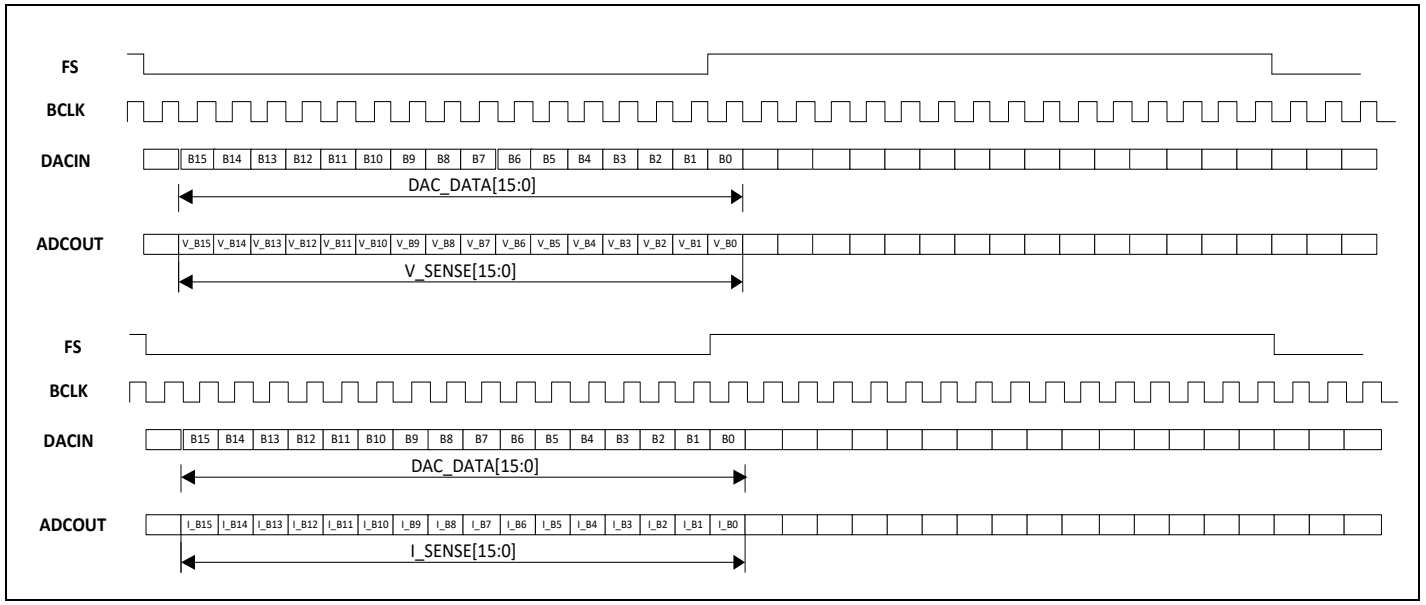


Figure 39 16-Bit I2S PingPong Mode Timing Diagram

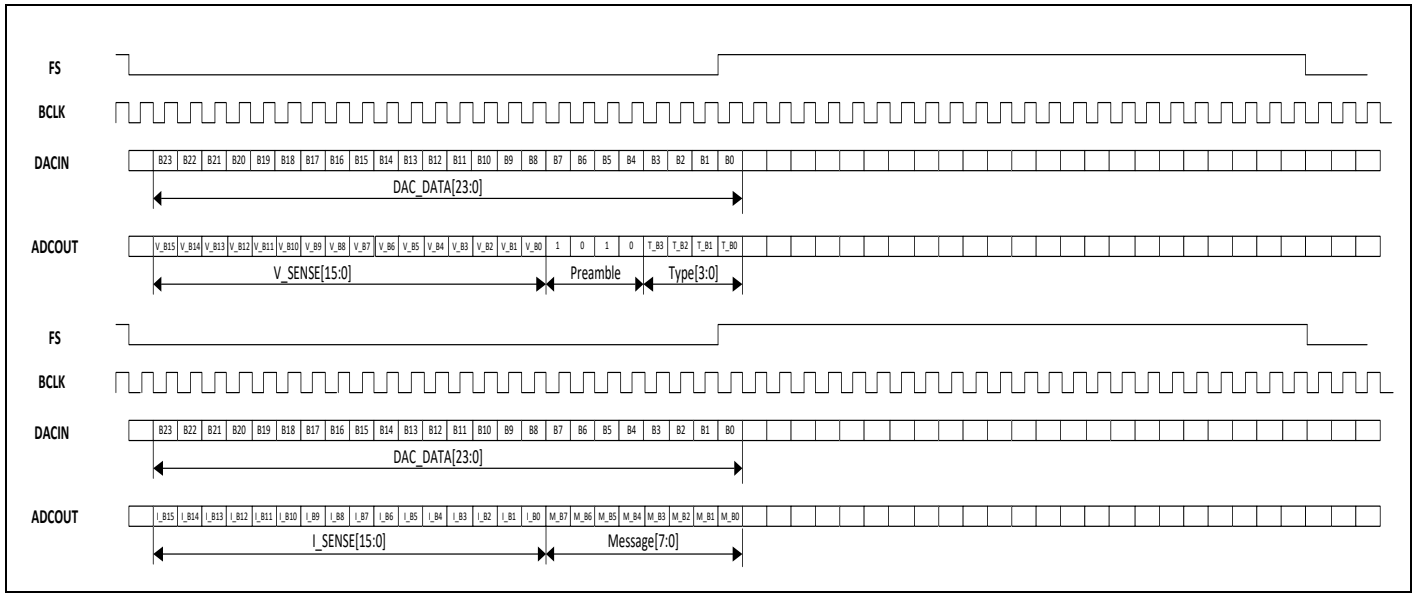


Figure 40 24-Bit I2S PingPong Mode Timing Diagram

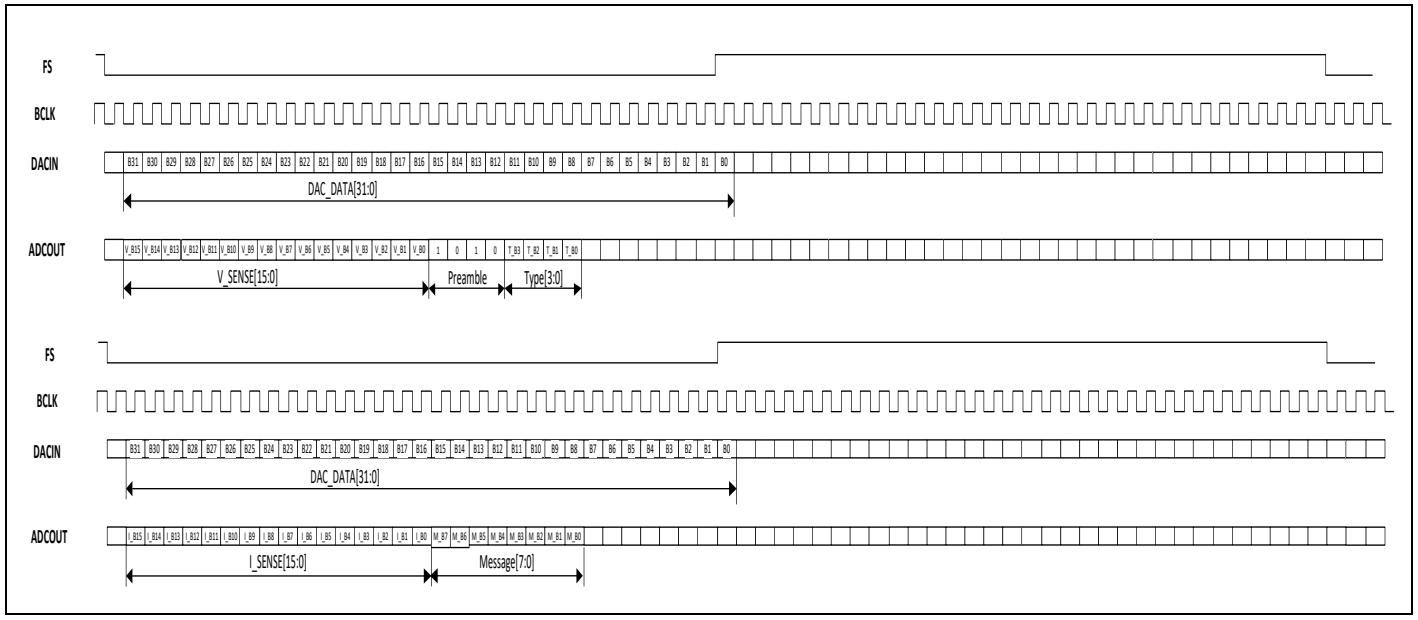


Figure 41 32-Bit I2S PingPong Mode Timing Diagram

I/V Sense Data Ping Pong Mode using in TDM Mode

For multiple channels more than stereo, I/V Sense Data Ping Pong Mode is used to transmit I/V Sense data and SAR ADC data in a single ADC channel by using TDM mode. This condition may be operated in 24 bits or 32 bits port word lengths when **ADC_RATE I2S_MODE REG0X28[15]** and **ADC_RATE UNSIGN_IV REG0X28[7]** are both set to 0 and **TDM_CTRL TDM_REG0XC[15]** and **TDM_CTRL PINGPONG_MODE REG0XC[14]** are set to 1.

See **Figure 42** and **Figure 43** for the 24-, and 32-bit timing diagrams for I/V Sense Ping Pong Mode in TDM operation.

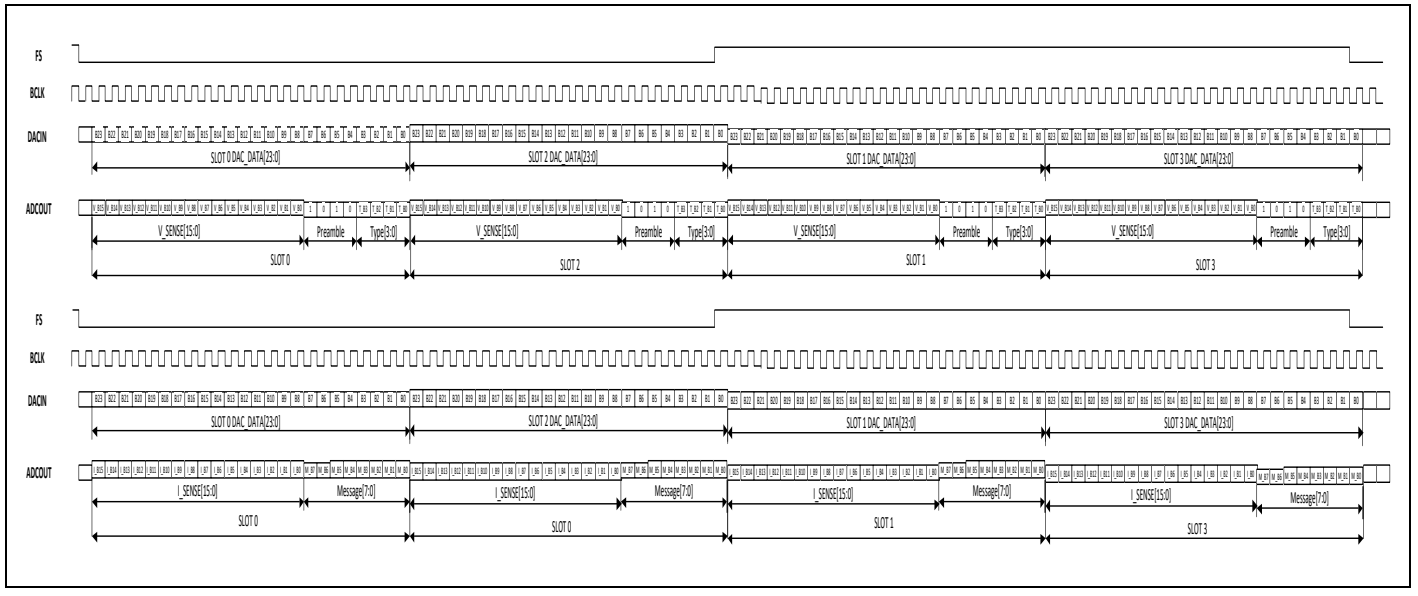


Figure 42 24-Bits I2S PingPong Mode in TDM Timing Diagram

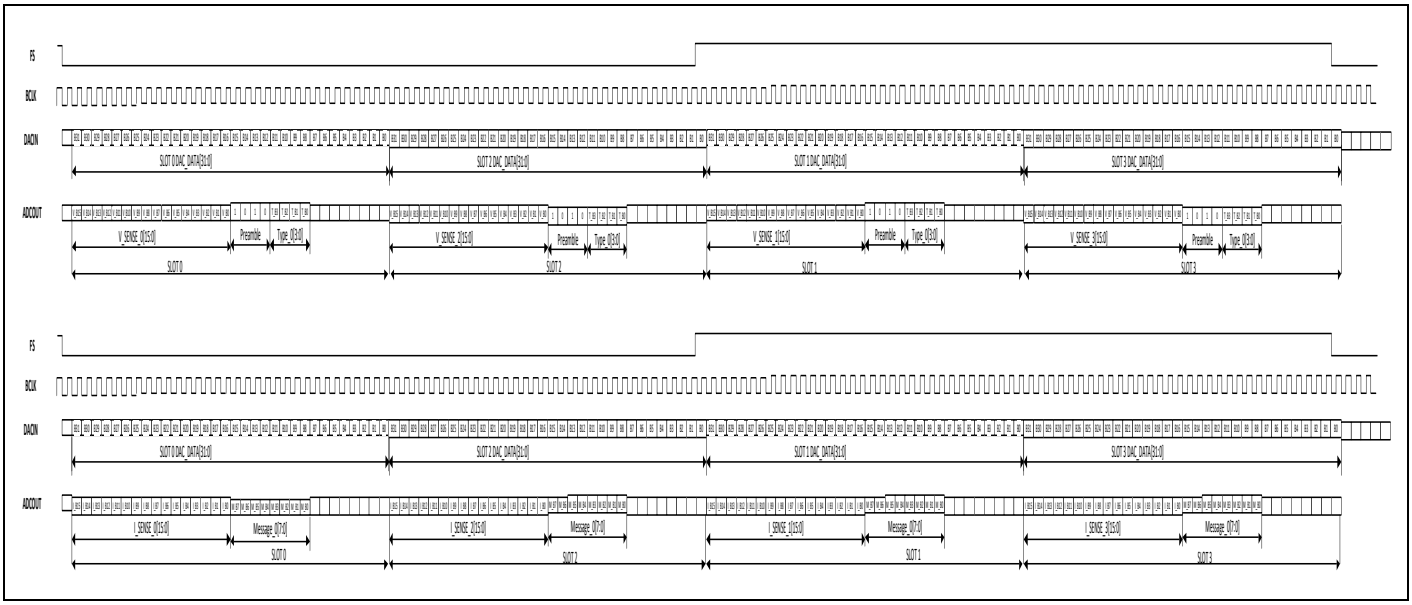


Figure 43 32-Bits I2S PingPong Mode in TDM Timing Diagram

5.20.3 Digital Audio Interface Timing Diagrams

Audio Interface Slave Mode

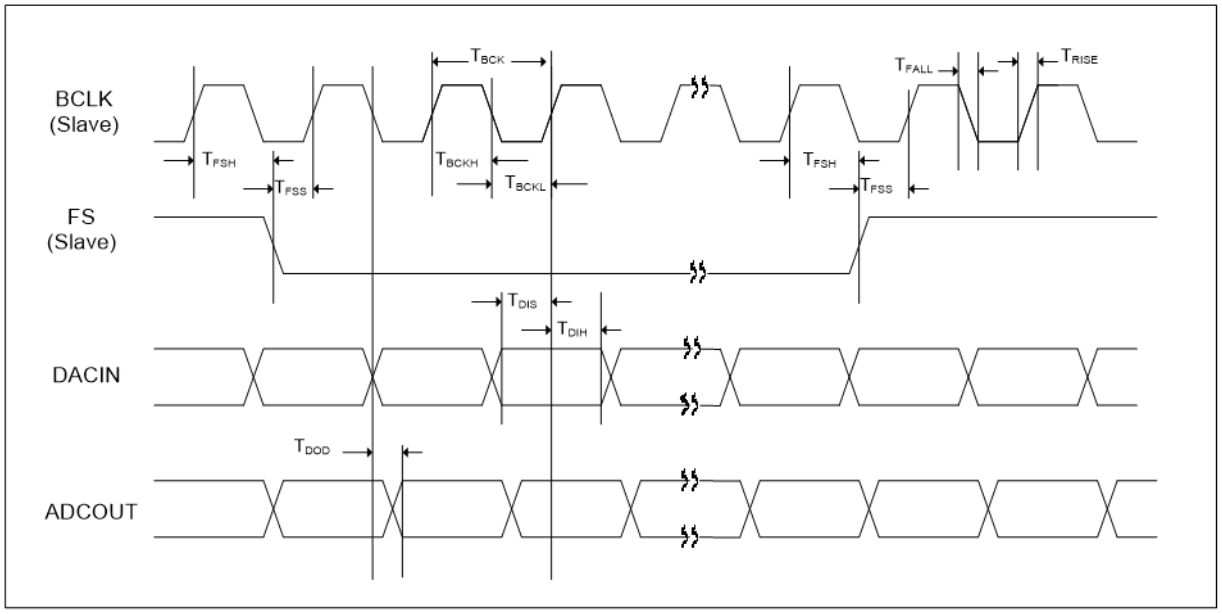


Figure 44 Audio Interface Slave Mode

Audio Interface Master Mode

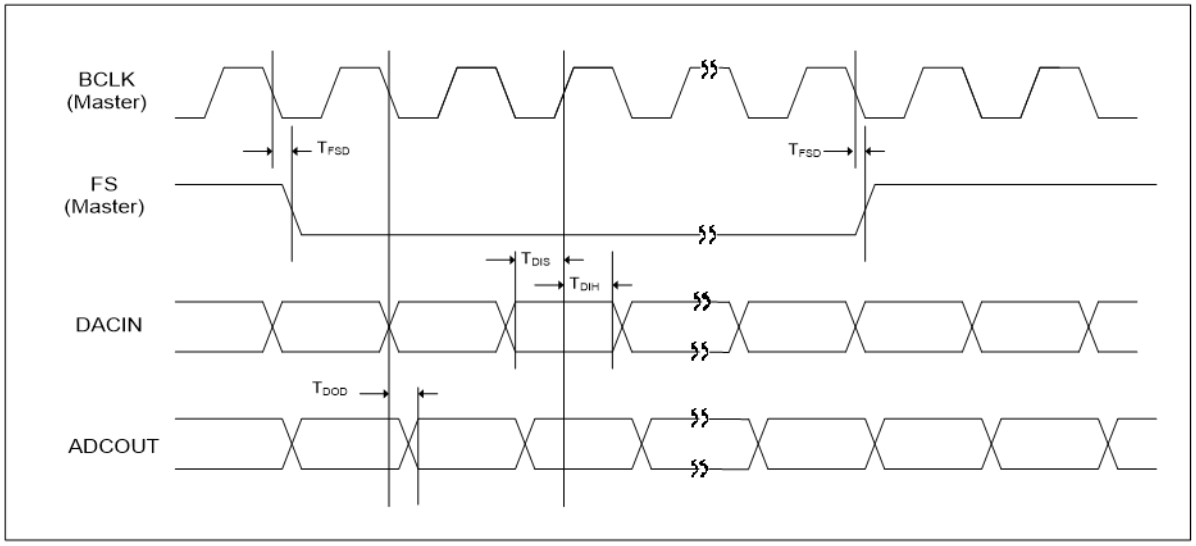


Figure 45 Audio Interface Master Mode

PCM Audio Interface Slave Mode

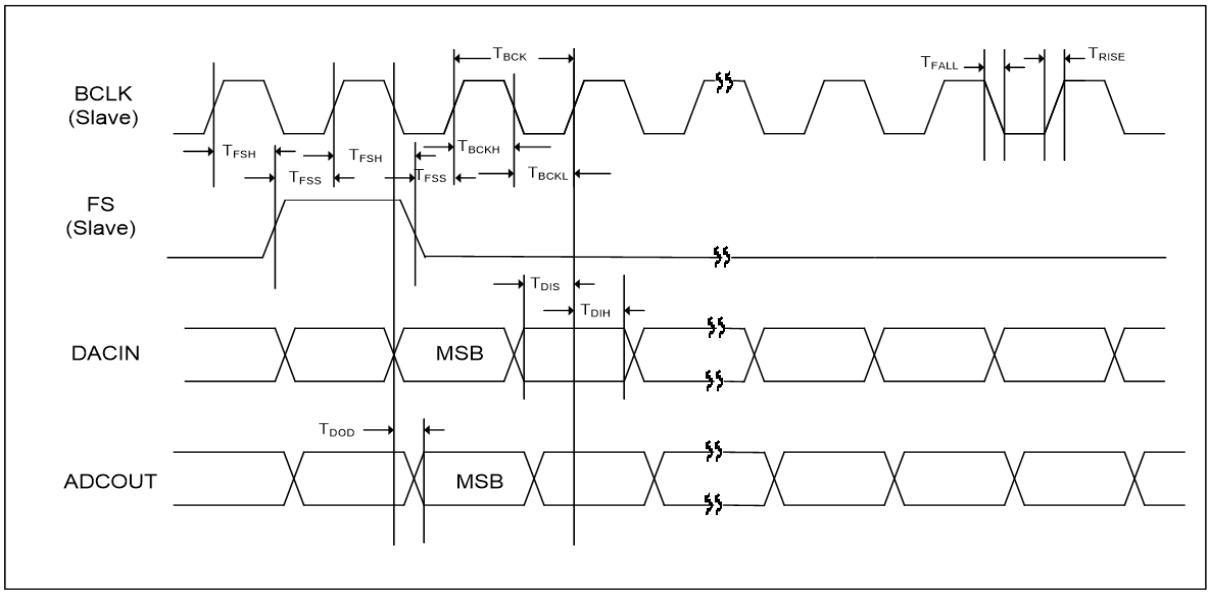


Figure 46 PCM Audio Interface Slave Mode

PCM Audio Interface Master Mode

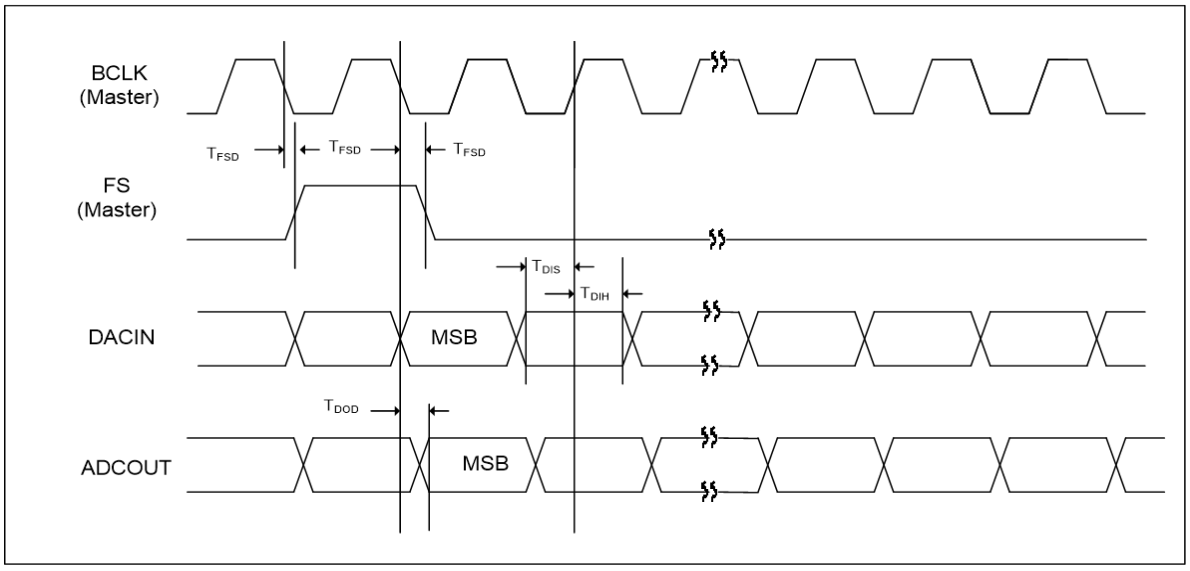


Figure 47 PCM Audio Interface Master Mode

PCM Time Slot Audio Interface Slave Mode

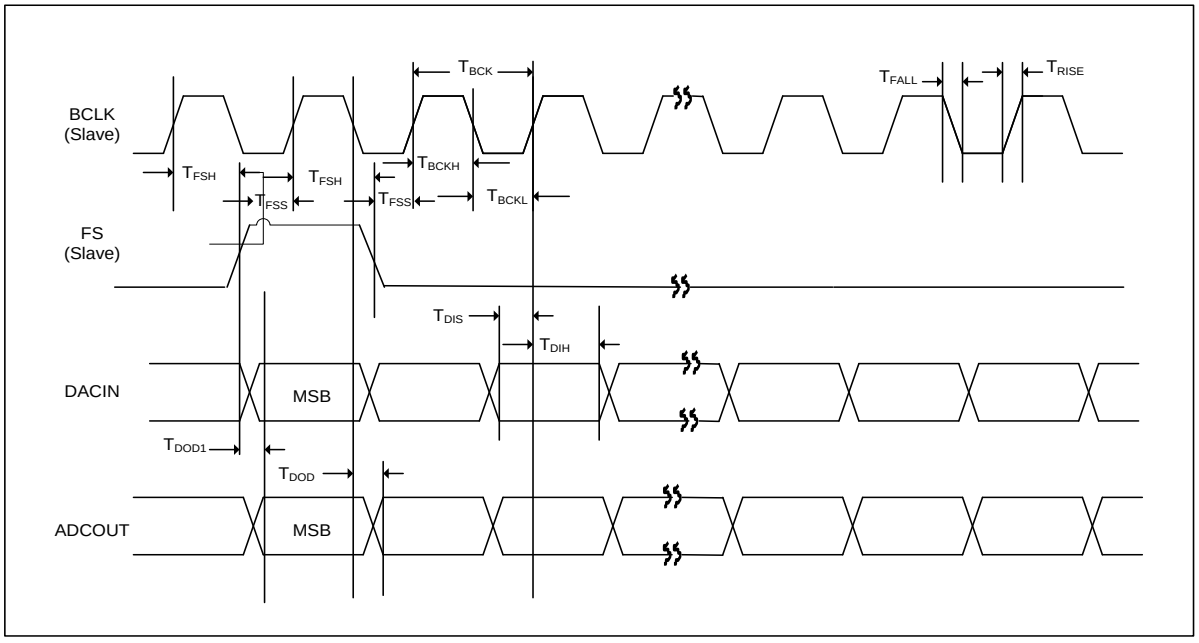


Figure 48 PCM Time Slot Audio Interface Slave Mode

PCM Time Slot Audio Interface Master Mode

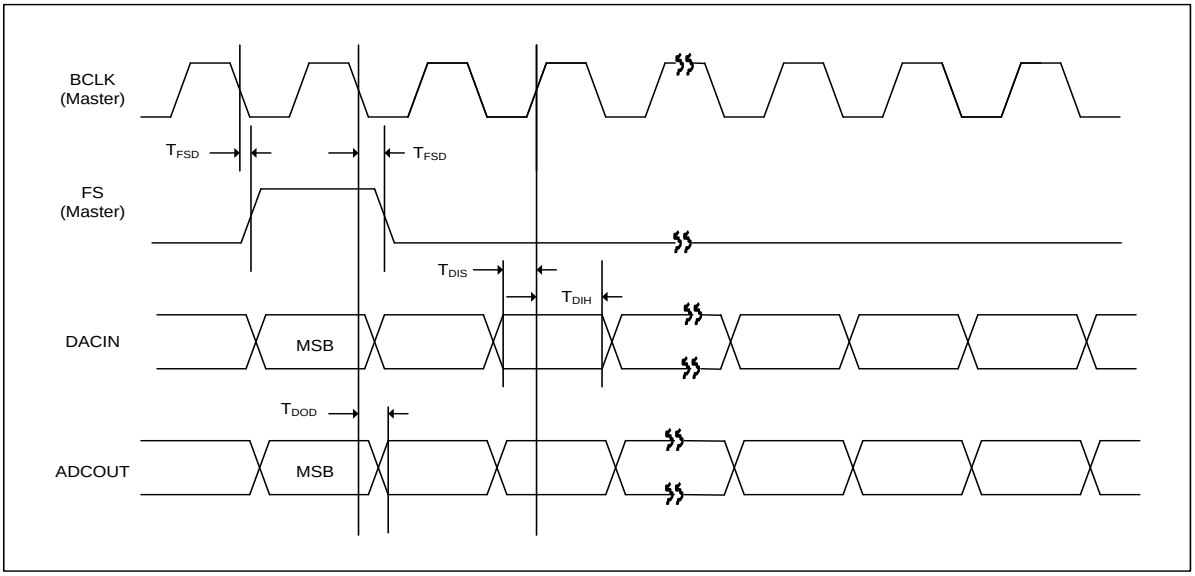


Figure 49 PCM Time Slot Audio Interface Master Mode

5.20.4 Digital Audio Interface Timing Parameters

Table 21 Digital Audio Interface Timing Parameter

Description	Symbol	Min	Typ	Max	Unit
BCLK Cycle Time (Slave Mode)	T_{BCK}	50	---	---	ns
BCLK High Pulse Width (Slave Mode)	T_{BCKH}	20	---	---	ns
BCLK Low Pulse Width (Slave Mode)	T_{BCKL}	20	---	---	ns
Fs to CLK Rising Edge Setup Time (Slave Mode)	T_{FSS}	20	---	---	ns
BCLK Rising Edge to Fs Hold Time (Slave Mode)	T_{FSH}	20	---	---	ns
Fs to SCK Falling to Fs Transition (Master Mode)	T_{FSD}	---	---	10	ns
Rise Time for All Audio Interface Signals	T_{RISE}	---	---	$0.135T_{BCK}$	ns
Fall Time for All Audio Interface Signals	T_{FALL}	---	---	$0.135T_{BCK}$	ns
ADCIN to BCLK Rising Edge Setup Time	T_{DIS}	15	---	---	ns
BCLK Rising Edge to DACIN Hold Time	T_{DIH}	15	---	---	ns
Delay Time from SCLK Falling Edge to ADCOUT	T_{DOD}	---	---	80	ns

For Stereo ALC

BCLK Rising Edge to Fs Hold Time(Slave Mode)	T_{FSH}	½ BCLK	---	---	ns

5.21 Interrupt Request

Interrupt Request is a useful error checking feature that can indicate problems on the amplifier during use. Below is the registers used to control the nature of the request. Please refer to the corresponding register for more information.

- INTERRUPT_CTRL_REG0X05
- INT_CLR_STATUS_REG0X06
- IO_CTRL_REG0X0A[15:11]

A brief overview of the feature is that the physical **IRQ** pin **[E4]** Figure 1 goes to active logic when one of the bits in **INT_CLR_STATUS** become activated. The **IRQ** pin can be configured in **IO_CTRL**[15:11], in which we will be assuming that it is using active high logic (meaning the register will become one when triggered) set in IO_CTRL_REG0X0A[15]. Additionally, this **IRQ** pin **[E4]** should be connected to the external interrupt of its controller, of which the controller will activate its Interrupt Service Routine (ISR) when IRQ pin goes high. The ISR should then read **INT_CLR_STATUS** register, reset the same register by sending a single bit 1 to the activated bit in that register, and trigger a flag to fix what may have happened depending on the interrupt status shown in **INT_CLR_STATUS**. NOTE: Only one bit can be reset at a time.

What shows in the **IRQ** pin [E4] and the status register is controlled by the **INTERRUPT_CTRL** register. The top bits (disable) [14:8] control whether the conditions would show up in both the **INT_CLR_STATUS** register and **IRQ** pin while the lower bits (mask) [7:0] will let it show on the **INT_CLR_STATUS** register but not on

the **IRQ** pin. In short, the **IRQ** pin is latched to all of the triggering bits in the **INT_CLR_STATUS** register and will go low when all bits in the **INT_CLR_STATUS** register is reset.

An example of this is when Over Voltage Protection (OVP) occurs during activation of output. On initial register loading, we set **IO_CTRL** to ***0x8800*** meaning **IRQ** logic is active high and output is enable. Additionally we want to set the **INTERRUPT_CTRL** to ***0x6070*** which enables the current/temperature protection, clipping, low/over voltage protection, and power detection and masks the interrupt detecting clipping on the output.

Interrupt Triggers:

- **INT_CLR_STATUS_REG0X06[0]** – Power Interrupt Status: Triggered by providing supply power, activating **ENA_CTRL_REG0X04**, and based on the **PWRUPEN** signal.
- **INT_CLR_STATUS_REG0X06[1]**– Over Voltage Protection (OVP) Detection: Triggered by VBAT reaching 16.5V

Activating output by triggering **ENA_CTRL**, **INT_CLR_STATUS** bit ***0*** becomes activated and the **IRQ** pin latches causing a trigger on the external interrupt on the controller. The controller can then acknowledge this in its check on the status register and reset both the **IRQ** pin and status register by writing ***0x0001*** to **INT_CLR_STATUS**. However, the **IRQ** pin is still active, indicating there is something wrong with the NAU83G20. The controller must then invoke a check on **INT_CLR_STATUS** again in which it sees **INT_CLR_STATUS** bit ***1*** is still high. From this we can deduce that after a short time after resetting the status register, the OVP detection interrupt triggered meaning the VBAT voltage ramped up after setting output but slow enough to occur right after resetting the status register. The controller must realize this and take appropriate steps to fix this occurrence.

NOTE: When activating the Class-D Driver output either manually through registers or through the **PWRUPEN** signal, OVP may trigger and will require reset.

NOTE: Because the on/off trigger is based on the **PWRUPEN** signal and when inducing the **PWRUPEN** signal through the clock detection circuit (Section **5.11**) using the I^2S communication protocol, if any of the incoming signals are stopped, specifically DACIN, then the **PWRUPEN** signal is set to 0 and awaits the signal is present again. When present again, the **PWRUPEN** signal will trigger and the on/off interrupt will also trigger.

5.22 Digital Signal Processor (DSP)

5.22.1 DSP Core Control and Usage

The NAU83G20 consist of a Cadence Tensilica LX7 Core, with Fusion F1 core package that runs a specialized Klippel™ Speaker Protection Algorithm capable of extending life on a speaker while maintaining premium, consistent audio quality.

The DSP core is equipped with 128KB Instruction ROM (IROM0) that houses the Klippel™ Speaker Protection Algorithm, and 24KB Data RAM (DRAM0). In addition, a communication protocol is implemented through I^2C to provide different the ability to load speaker configurations, called Klippel Controlled Sound (KCS) Setups. These speaker configurations are fine-tuned to the speakers that the device will be outputting and utilizes Klippel™ non-linear control algorithm to maximize volume and frequency without causing any harm to the speaker.

Figure 50 DSP Connection Diagram describes the different interfaces connected to the DSP Core.

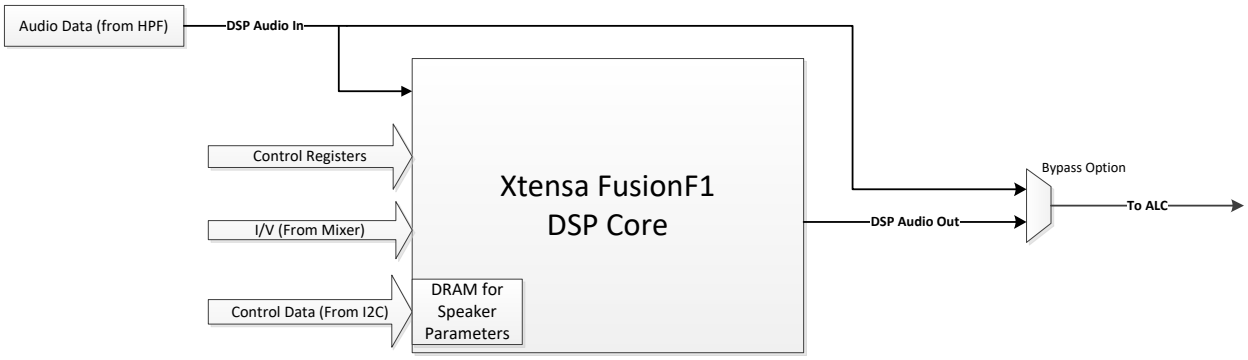


Figure 50 DSP Connection Diagram

A typical setup would be to initialize through register settings and introduce a KCS setup unique to the speaker used. This KCS setup uses an I²C communication protocol which can be found in Section 5.22.2 for register initialization.

5.22.2 Base Register Initialization for DSP

There are a total of 7 registers associated to the DSP Core that utilizes the I²C protocol integrated into the NAU83G20 package for all control and status registers.

- **CLK_CTRL.ADC_DIV2/4_REG0X03[12:13]**
  - Used in conjunction with **CLK_DET_CTRL_REG0X40**. It is the divider of the sampling rate on the ADC from the input DAC sampling rate, or Frame Sync. Be sure to set only one or the other as setting both is an **invalid** configuration and may have detrimental effects to your design.
- **ENA_CTRL.CLK_DSP_SRC_REG0X04[5:3]**
  - Selection of the DSP core clock multiplier which utilizes the DAC MCLK. The minimum value of the core clock should be 2000 times the audio sampling rate but not above 102MHz, which is the maximum speed allowed.
- **DSP_CORE_CTRL2_REG0X1A**
  - Controls the DSP Bypass and stall the DSP Core.
- **CLK_DET_CTRL_REG0X40**
  - Used with Register 0x03 to set the sampling rate and set min or max divider for the input DAC sampling rate.
  - [9] REG_ALT_SRATE is a special register bit that determines between (0) 48kHz/12kHz or (1) 44.1kHz/11.025kHz DAC/ADC sampling rate. If the sampling rate is any other value, this setting does not matter in the configuration.
- **ANALOG_CONTROL_7_REG0X68**
  - Used to activate the MCLK multipliers to be used for the DSP. The DSP can use the MCLK directly but it is recommended to multiply then divide within chip to reduce jitter.
- **COMMUNICATION_REGISTER_REG0XF000**
  - Used as the main channel to communicate directly to the DSP. Can request status information, get or set the current speaker parameters, or get speaker diagnostic data. This is a special register which has a two byte address and will return with four bytes of data. When read without invoking a command, this register will either return all zeros, **0x00000000** in byte segments, or an idle word **0xF4F3F2F1** in byte segments. For more information, please refer to (**TBD**).

Finally to complete the setup, **three additional tasks must be enacted**. **First**, **MCLK, BCLK, and Frame Sync**, as part of the I2S Signal input, must be provided before the chip is fully initialized. Second, the DSP needs to be stalled during the initialization by setting **DSP_CORE_CTRL2 REGX1A[4]** = ***0x1***. Third, after loading the register settings the chip must go through a **soft-reset and followed by at least 60ms delay**.

This is done by writing 0x0 twice to SOFTWARE_RST_REG0X1. The DSP then shall be released by setting DSP_CORE_CTRL2 REGX1A[4] = 0 to un-stall, and DSP_CORE_CTRL2 REGX1A[5] = 1 to select DSP output. This will ensure that the chip is fully initialized.

To verify a correct setup, the register **0xF000** can be read and is the main line of communication to the DSP through the I²C communication protocol. After setting the correct register settings, the NAU83G20 will return the four byte idle word, **0xF4F3F2F1**.

Depending on your chosen input DAC frequency, governed by the I²S signal Frame Sync, the basic configuration of the DSP must follow a set table of settings for DSP clock and Sense sampling rate. This is detailed in Table 22 Supported Audio/Sense Rates. **Take note that the maximum rate the DSP clock can be is 102MHz.**

Table 22 Supported Audio/Sense Rates[1]

Audio Sampling Rate	Sense Sampling Rate	Minimum DSP_CLK
8kHz	8kHz	16MHz
16kHz	16kHz	32MHz
24kHz	12kHz	48MHz
32kHz	16kHz	64MHz
44.1kHz	11.025kHz	88.2MHz
48kHz	12kHz	96MHz

Example Initial Setup

For a typical 48kHz Frame Sync I²S signal, the ADC Sampling rate must be 12kHz and DSP clock ran at the minimum of 96MHz.

- CLK_CTRL_REG0X03 = **0x08E0**
  - Used in conjunction with CLK_DET_CTRL_REG0X40. It is the divider of the sampling rate on the ADC from the input DAC sampling rate, or Frame Sync.
- ENA_CTRL_REG0X04 = **0x0067**
  - Selection of the DSP core clock multiplier which utilizes the DAC MCLK. The minimum value of the core clock should be 2000 times the audio sampling rate but not above 102MHz, which is the maximum speed allowed.
- DSP_CORE_CTRL2_REG0X1A = **0x0020**
  - Controls the DSP Bypass and stall the DSP Core.
- CLK_DET_CTRL_REG0X40 = **0x0801**
  - Used with Register 0x03 to set the sampling rate and set min or max divider for the input DAC sampling rate.
- ANALOG_CONTROL_7_REG0X68 = **0x064F**
  - Used to activate the MCLK multipliers to be used for the DSP. The DSP can use the MCLK directly but it is recommended to divide then multiply within chip to reduce jitter. Also selects the Vsense and Isense reference voltage which may be dependent on speaker loading.

5.22.2.1 Supported Commands

Table 23 DSP Supported Commands

CMD_ID	Pnemonic	Parameters	Description
0x01	CMD_GET_COUNTER	None	Returns an increasing counter each time the command is called, can be used as a heartbeat to see that DSP is alive.
0x09	CMD_GET_FRAME_STATUS	None	Returns FRAME_STATUS 32bit word that contains the current KCS init, audio/sense sampling rates, and HW indication
0x0A	CMD_GET_REVISION	None	Retruns the ROM Code revision and KCS revision.
0x04	CMD_GET_KCS_RSLTS	Offset, Length	Gets Data from internal algorithm results structure. Returns *Length* bytes from address *Offset* relative to KCS start
0x06	CMD_GET_KCS_SETUP	Offset, Length	Gets Data from internal algorithm configuration structure. Returns *Length* bytes from address *Offset* relative to KCS start
0x07	CMD_SET_KCS_SETUP	Offset, Length, Data	Sets *Data* to internal algorithm configuration structure. Write *Length* bytes of *Data*, starting at address *Offset*. Returns Execution status only

DSP ROM Code Frame Status (FRAME_STATUS)

The following table describes the 32 bit word that the DSP returns after issuing CMD_ID 0x09 (CMD_GET_FRAME_STATUS).

31	30	29	28	27	26	25	24
SNS_OVF	AUD_UVF	AUD_OVF	ALC_STS	HW_IND_STS [7:4]			
23	22	21	20	19	18	17	16
HW_IND_STS [3:0]				SNSR_RATE [7:4]			
15	14	13	12	11	10	9	8
SNSR_RATE [3:0]				AUDIO_RATE [7:4]			
7	6	5	4	3	2	1	0
AUDIO_RATE [3:0]				Reserved		FEED_TRU	ALGO_OK

Bits	Description	
[31]	SNS_OVF	**Sensor Data Overflow** This bit indicates that the sensor data input buffer overflowed and some sensor samples were ommited and not buffered to the protection algorithm. This may happen at power up, and if clock configuration is incorrect. After reading FRAME_STATUS, DSP sets this bit to 0.

[30]	**AUD_UVF**	**Audio Data Underflow** This bit indicates that the audio data underflowed, meaning was no new processed samples to transmit on frame sync. After reading FRAME_STATUS, DSP sets this bit to 0.
[29]	**AUD_OVF**	**Audio Data Overflow** This bit indicates that the audio data input buffer overflowed and some sensor samples were ommited and not buffered to the protection algorithm. This may happen at power up, and if clock configuration is incorrect. After reading FRAME_STATUS, DSP sets this bit to 0.
[28]	**ALC_STS**	**ALC Status** This bit represents the latest ALC Change indication the DSP ROM Code used for the protection algorithm. It is set to 1 whenever the DSP detects ALC gain is different from zero.
[27:20]	**HW_IND_STS**	**HW Indication Status** This field is a reflection of the latest status the DSP read from RD_INT_STATUS before calling the protection algorithm
[19:12]	**SNSR_RATE**	**Sensor Data Rate** This field contains the sensor sampling rate the DSP calculated according to the chip registers, divided by 1000 (e.g. for sensor rate of 12kHz, this field will have 12).
[11:4]	**AUDIO_RATE**	**Audio Data Rate** This field contains the audio sampling rate the DSP calculated according to the chip registers, divided by 1000 (e.g. for audio rate of 48kHz, this field will be 48)
[3:2]	**Reserved**	
[1]	**FEED_TRU**	**Feed Through Mode** This bit indicates that the DSP is in feed through mode. In this mode DSP discards sensors samples, and bypass the audio samples (i.e. audio out equals to audio in).
[0]	**ALGO_OK**	**Algorithm Initilazition OK** This bit indicates that the audio protection algorithm was initialized successfully.

5.23 Control Registers

Table 24 provides detailed information for the NAU83G20 Control Registers. Note that all registers marked as 'Reserved' should not be overwritten, unless it is requested to do so by Nuvoton Technology Corporation.

REG	Function
0	HARDWARE_RST
1	SOFTWARE_RST

REG	Function
25	DSP_STATUS_0
26	DSP_STATUS_1

2	I2C_ADDR
3	CLK_CTRL
4	ENA_CTRL
5	INTERRUPT_CTRL
6	INT_CLR_STATUS
7	SAR_CTRL1
8	GPIO12_CTRL
9	GPIOOUT
A	IO_CTRL
B	GPIO12_CTRL
C	TDM_CTRL
D	I2S_PCM_CTRL1
E	I2S_PCM_CTRL2
F	LEFT_TIME_SLOT
10	RIGHT_TIME_SLOT
12	HPF_CTRL
13	MUTE_CTRL
14	ADC_VOL_CTRL
15	RESERVED
16	RESERVED
17	RESERVED
18	CTRL2
19	DSP_CORE_CTRL1
1A	DSP_CORE_CTRL2
1B	CLK_DOUBLER_O
1C	RESERVED
1D	GENERAL_STATUS0
1E	GENERAL_STATUS1
1F	GENERAL_STATUS2
20	SAR_ADC_OUT_01
21	SAR_ADC_OUT_23
22	ALC_READOUT1
23	ALC_READOUT2
24	ALC_READOUT3

27	DSP_STATUS_2
28	ADC_RATE
29	DAC_CTRL1
2A	DAC_CTRL2
2C	ALC_CTRL1
2D	ALC_CTRL2
2E	ALC_CTRL3
2F	ALC_CTRL4
30	TEMP_COMP_CTRL
31	UVLO_CTRL0
32	UVLO_CTRL1
33	LPF_CTRL
40	CLK_DET_CTRL
46	I2C_DEVICE_ID
4A	ANALOG_READ
55	MISC_CTRL
60	BIAS_ADJ
61	ANALOG_CONTROL_1
62	ANALOG_CONTROL_2
63	ANALOG_CONTROL_3
64	ANALOG_CONTROL_4
65	ANALOG_CONTROL_5
66	ANALOG_CONTROL_6
68	ANALOG_CONTROL_7
69	CLIP_CTRL
6B	ANALOG_CONTROL_8
71	ANALOG_ADC_1
72	ANALOG_ADC_2
73	RDAC
76	PGA
77	FEPGA
7F	PGA_GAIN
80-9D	BIQUAD CONTROL

Table 24 Control Registers

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	HARDWARE_RST	RESET_N1																	Write any value to this register ***once*** to reset all the registers.
1	SOFTWARE_RST	RESET_N_SOFT_PRE																	Write any value to this register ***twice*** to reset all internal stated machines without resetting the registers.
2	I2C_ADDR	I2C_ADDR_SEL																	I2C address latch Write operation I2C_ADDR_SEL[0] = 1 to latch the I2C address per the status of GPIO1 and GPIO2. Read operation I2C_ADDR_SEL[6:0] = latched or non-latched I2C address.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
3	CLK_CTRL	CLK_DAC_INV																	DAC clock inversion in analog domain 1 = Enable 0 = Disable
		CLK_ADC_DIV_SRC																	Choose the CLK ADC source 1 = from the MCLK divided by 5 0 = from the MCLK
		ADC_DIV2																	In the new design, support different sample Rate for the ADC path and DAC path. 1 = SR of DAC is twice SR of ADC 0 = SR of DAC is equal to SR of ADC For example, if the DAC path sample rate (SR) is 48kHz, then set this bit to 1, the ADC path sample rate will be 24kHz
		ADC_DIV4																	In the new design, support different sample Rate for the ADC path and DAC path. 1 = SR of DAC four times the SR of ADC 0 = SR of DAC is equal to SR of ADC For example, if the DAC path sample rate is 48kHz, then set this bit to 1, the ADC path sample rate will be 12kHz
		CLK_ADC_PL																	Invert ADC Clock Polarity 1 = Invert 0 = No change
		Reserved																	Reserved
		CLK_ADC_SRC																	Scaling for ADC clock: 00 = 1/2 01: 1/4 10 = 1/8 11: 1/16
		CLK_DAC_SRC																	Scaling for DAC clock: 00 = 1 01: 1/2 10 = 1/4 11: 1/8
		MCLK_SRC																	Scaling for MCLK (N2 Clock Divider): 000: 1 001: 1/2 010: 1/4 011:1/ 8 100 - 111: Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
4	ENA_CTRL	DSP_OSC_ ENA																	Reserved
		DSP_MCLK_ SEL																	Reserved
		MCLK_SEL																	Selection of the MCLK from the Clock Multiplier 000 = From MCLK_PIN 001: 1 010: 2 011: 4 (Requires 0x68[0]=1) 100: 8 (Requires 0x68[1:0]=11) 101: 16 (Requires 0x68[3:0]=1111) 110-111: no clock input
		CLK_MUL_ SRC																	Selection of the Clock Multiplier Input Clock Speed (N1 clock divider) 00: 1 ** 01: 1/2 10: 1/3 ** 11: no clock input Note that the N1 Divider only works when x04[10:8] = x1,2,4,8,16 ** Requires accurate duty-cycle (see 'Digital I/O Parameters')
		CLK_DSP_ SRC																	Selection of the DSP core clock speed multiplier from MCLK 000: 8 (Requires 0x68[1:0]=11) 001: 4 (Requires 0x68[0]=1) 010: 2 011: 1 100: 16 (Requires 0x68[3:0]=1111) 101-111: no clock input
		DACEN																	DAC Channel Enable 1 = ON 0 = OFF
		ADCEN_I																	Current ADC Channel Enable 1 = ON 0 = OFF
		ADCEN_V																	Voltage ADC Channel Enable 1 = ON 0 = OFF
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
5	INTERRUPT _CTRL	WD_INTP_ MASK																	Watch Dog Timer Interrupt mask 1 = Mask the interrupt 0 = Unmask

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DSP2I2C_ INTP_MASK																	DSP to I2C outbound data Interrupt mask 1 = Mask the interrupt 0 = Unmask
		APR_ EMRGENCY SHTDWN1_ INTP_MASK																	APR Emergency Shutdown (OCP or OTP) Interrupt mask 1 = Mask the interrupt 0 = Unmask
		CLIP_INTP_ MASK																	Clip (when output on class D is clipped , it is detected with 0x69[4]=1) Interrupt mask 1 = Mask the interrupt 0 = Unmask
		LOVDDDETB _INTP_MASK																	Low Voltage Detection (VDDD<2.4V or VBAT< 4V) Interrupt mask 1 = Mask the interrupt 0 = Unmask
		OVP_INTP_ MASK																	Over Voltage Protection (VBAT > 16.5V) Interrupt mask 1 = Mask the interrupt 0 = Unmask
		PWRUPEN_ INTP_MASK																	Power Up (when Power and I2S Clocks are provided with clock detection is triggered) Interrupt mask 1 = Mask the interrupt 0 = Unmask
		WD_INT_DIS																	Watch Dog Timer (when clocks are running and DSP (KCS algorithm) have not outputted audio data to DAC) Interrupt Disable Control 1 = Disable 0 = Enable
		DSP2I2C_INT _DIS																	DSP to I2C outbound data (When DSP becomes available) Interrupt Disable Control 1 = Disable 0 = Enable
		APR_ EMRGENCY_ SHTDWN1 INT_DIS																	APR Emergency Shutdown Interrupt Disable Control 1 = Disable 0 = Enable
		CLIP_INT_ DIS																	Clip Interrupt Disable Control 1 = Disable 0 = Enable
		LOVDDDETB _INT_DIS																	Low Voltage Detection Interrupt Disable Control 1 = Disable 0 = Enable
		OVP_INT_ DIS																	Over Voltage Protection Interrupt Disable Control 1 = Disable 0 = Enable
		PWRUPEN_ INT_DIS																	Power Up Interrupt Disable Control 1 = Disable 0 = Enable
		Default	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0x007f

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
6	INT_CLR_ STATUS	INT_CLR_ STATUS																	Write Operation: Write bits [6:0] 1s to clear the corresponding Interrupt Status. Read Operation: REG6 [6:0] reads the interrupt status Bit6 = Watch Dog Timer Bit5 = DSP to I2C outbound data Valid Bit4 = Over current/temperature shutdown Bit3 = Clip Bit2 = Low Voltage Detection Bit1 = Over Voltage Protection Bit0 = Power Up
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read/Write
7	SAR_CTRL1	SAR_OUT_ INV																	SAR Channel output invert enable 1 = Enable 0 = Disable
		Reserved																	Reserved
		SAR_TRACK GAIN																	SAR Gain Tracking. Default setting = 001 000 = 1.0*VDDA 100 = 1.3*VDDA 001 = 1.0*VDDA 101 = 1.4*VDDA 010 = 1.1*VDDA 110 = 1.54*VDDA 011 = 1.2*VDDA 111 = 3.12*VDDA
		Reserved																	Reserved
		RES_SEL																	SAR Series Resistor, default set = 001 00 = 35 kOhms 001 = 70 kOhms 010 = 170 kOhms 011 = 360 kOhms 1xx = Short
		COMP_ SPEED																	Time Setting for Compare Cycle. The total conversion has 8 compare cycles. 00 = 500 nsec 01 = 1 µsec 10 = 2 µsec 11 = 4 µsec
		SAMPLE_ SPEED																	Sampling Phase Time 00 = 2 µsec 01 = 4 µsec 10 = 8 µsec 11 = 16 µsec
		SAR_ENA																	SAR Enable 1 = Enable 0 = Disable
		Default	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0x00b4
8	GPIO12_ CTRL																		reserved
																			reserved
																			reserved
																			reserved
		GPIO2OUT																	GPIO2 Pull Select 0 = Pull Down 1 = Pull Up
		GPIO2_PS																	GPIO2 input Pull Select 0 = Pull Down 1 = Pull Up
		GPIO2_DS																	GPIO2JD1 Drive Current Select 1 = High 0 = Low

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		GPIO2_PE_N																	GPIO2 Pin Pull enable 1 = Enable 0 = Disable
		GPIO2_OE																	GPIO2 programmable I/O mode selection 1 =Output 0 =Input
		GPIO1OUT																	GPIO1 pull selection 0=Pull down 1=Pull up
		GPIO1_PS																	GPIO1CSB Pull Select 0 = Pull Down 1 = Pull Up
		GPIO1_DS																	GPIO1CSB Current Drive Select 1 = High 0 = Low
		GPIO1_PE																	GPIO1CSB Pin Pull enable 1 = Enable 0 = Disable
		GPIO1_OE																	GPIO1CSB programmable I/O mode selection 1 =Output 0 =Input
		Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0x0102
9	GPIOOUT	GPIOOUTSEL																	GPIO1/GPIO2 Output Function Select (input default) 000 = GPIO1OUT / GPIO2OUT 001 = MCLK / SDB 010 = MCLKDET / OSC_CLK 011 = TALARM / MUTEB 100 = OVP / SHUTDWNDRVRR 101 = SHORTR / PWRDOWN1B_D 110 = PWRUPEN / PDOSCB 111 = SCLK_I / SD_I
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
A	IO_CTRL	IRQ_PL																	Default IRQ Logic 1 = Active High 0 = Active Low
		IRQ_PS																	IRQ Pin Pull Select 0 = Pull Down 1 = Pull Up
		IRQ_PE																	IRQ Pin Pull Enable 0 = Enable 1 = Disable
		IRQ_DS																	IRQ Current Drive Select 1 = High 0 = Low
		IRQ_OE_N																	IRQ Output Enable 1 = Enable 0 = Disable
		BCLK_DS																	BCLK IO Drive Strength 1 = Stronger 0 = Default
		LRC_DS																	LRC IO Drive Strength 1 = Stronger 0 = Default
		ADCDAC_DS																	ADCDAT IO Drive Strength 1 = Stronger 0 = Default
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
B	I2S_PCM_CTRL0	ALC_MODE																	ALC data communication on GPIO1 pin 1 = On 0 = Off
		ALC_SEND_ON_LOC																	1 = Device will send the ALC data in the first 8 cycles of BCLK when LRC is low, and will receive the ALC data during the second 8 cycles of BCLK. 0 = Device will receive the ALC data in the first 8 cycles of BCLK when LRC is low, and will send the ALC data during the second 8 cycles of BCLK.
																			Reserved
		DAC_SEL																	DAC Channel Source in TDM Mode 000 : from Slot 0 001 : from Slot 1 010 : from Slot 2 011 : from Slot 3 100 : from Slot 4 101 : from Slot 5 110 : from slot 6 111 : from Slot 7
		AEC_CH_SEL																	1 = Device will send AEC reference data through I2S left channel 0 = Device will send AEC reference data through I2S right channel
		AEC_SRC_SEL																	1 = Take the data before DAC digital filter as the AEC reference data 0 = Take the data from the DSP as the AEC reference data
		AEC_MODE																	1 = I2S will send out the AEC reference data 0 = I2S will send out the voltage and current data
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
C	TDM_CTRL	TDM																	TDM Enable 1 = Enable 0 = Disable
		PCM_OFFSET_MODE_CTRL																	PCM Offset Control in TDM 1 = Enable 0 = Disable
		PINGPONG_MODE																	PingPong Mode Selection. In PingPong mode, the ISENSE data and VSENSE data will not be transmitted out every cycle but every two cycles. 1 = Enable 0 = Disable
		ADC_I_ SEL																	ADC Current Channel Source in TDM Mode 100: from slot 1 101: from Slot 3 110: from Slot 5 111: from Slot 7 000 – 011: disable, no data transmission
		ADC_V_ SEL																	ADC Voltage Channel Source in TDM Mode 100: from Slot 0 101: from Slot 2 110: from Slot 4 111: from Slot 6 000 – 011: disable, no date transmission Note: xC[7:0]=24 for ADC output in non TMD mode
		Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0x0c00
D	I2S_PCM_CTRL1	Reserved																	Reserved
		Reserved																	Reserved

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		ADDAP0																	DAC Audio Data Input Option to route directly from ADC data stream 0 = No pass through, normal operation 1 = ADC output data stream routed to DAC input data path
		CMB8_0																	8-bit Word Enable 0 = Normal operation 1 = 8-bit operation
		Reserved																	Reserved
		BCP0																	Bit clock phase inversion option for BCLK 0 = Normal phase 1 = Input logic sense inverted
		LRP0																	PCMA and PCMB left/right word order control 0 = Right Justified/Left Justified/I2S/PCMA mode 1 = PCMB Mode Enable: MSB is valid on 1st rising edge of BCLK after rising edge of FS
		DACPHS0																	DAC audio data left-right ordering 0 = left DAC data in left phase of LRP 1 = left DAC data in right phase of LRP (left-right reversed)
		ADCPHS0																	ADC audio data left-right ordering 0 = left ADC data in left phase of LRP 1 = left ADC data in right phase of LRP (left-right reversed)
		WLEN0																	Port Word length (24-bits default) of audio data stream 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length 11 = 32-bit word length
		AIFMT0																	Port Audio interface data format (default setting is I2S) 00 = Right justified 01 = Left justified 10 = Standard I2S format 11 = PCMA or PCMB audio data format option
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0x000a
E	I2S_PCM_CTRL2	I2S_TRI																	I2S tri-state 0 = Normal mode 1 = Output high Z
		I2S_DRV																	I2S driving enable 0 = Normal mode 1 = Always out
		LRC_DIV																	LRC divide coefficient setting 00 = 1/256 01 = 1/128 10 = 1/64 11 = 1/32

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		PCM_TS_EN0																	0 = Only PCM_A_MODE or PCM_B_MODE (STEREO Only) can be used when PCM Mode is selected 1 = Time slot function enable for PCM mode
		TRI0																	Without TDM mode 0 = Drive the full Clock of LSB 1 = Tri-State the 2nd half of LSB
		PCM8BIT0																	0 = Use I2S_PCM_CTRL1.WLEN to select Word Length 1 = PCM Select 8-bit word length
		PCM_TS_SEL																	Reserved to 0
		ADCDAT0_PE																	ADCDAT IO Pull Enable 1 = Enable 0 = Disable
		ADCDAT0_PS																	ADCDAT IO Pull Up/Down Enable 1 = Pull Up 0 = Pull Down
		ADCDAT0_OE																	0 = ADCDAT out enable as an output buffer 1 = ADCDAT out enable; when no data out, ADCDAT pin becomes high Z
		MS0																	Master/Slave Mode Enable 0 = Slave Mode 1 = Master Mode
		BCLKDIV																	BCLK DIVIDE Setting from MCLK frequency 000 = 1 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		Default	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x8010
F	LEFT_TIME_SLOT	FS_ERR_CMP_SEL																	Triggers short frame sync signal if frame sync is less than 00 = 252 x MCLK 01 = 253 x MCLK 10 = 254 x MCLK 11 = 255 x MCLK
		DIS_FS_SHORT_DET																	Short Frame Sync detection logic Enable 0 = Enable 1 = Disable
		TSLOT_L0																	Left channel PCM time slot start value Or PCM TDM Offset Mode Slot start value
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
10	RIGHT_TIME_SLOT	TSLOT_R0																	Right channel PCM time slot start value Or unused for PCM TDM Offset Mode
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
12	HPF_CTRL	DAC_HPF_EN																	DAC High Pass Filter Enable 1 = Enable 0 = Disable
		DAC_HPF_APP																	DAC High Pass Filter Application Mode
		DAC_HPF_FCUT																	DAC High Pass Filter Cut Off Frequency 000 : 130Hz 001 : 155Hz 010 : 198Hz 011 : 248Hz 100 : 311Hz 101 : 398Hz 110 : 503Hz 111 : 614Hz
		ADC_HPF_EN																	ADC Left and Right Channel High Pass Filter Enable 1 = Enable 0 = Disable
		ADC_HPF_APP																	ADC Left and Right Channel High Pass Filter Application Mode

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		ADC_HPF_FCUT																	ADC Left and Right Channel High Pass Filter Cut Off Frequency 000 : 130Hz 001 : 155Hz 010 : 198Hz 011 : 248Hz 100 : 311Hz 101 : 398Hz 110 : 503Hz 111 : 614Hz
		ADC_HPF_SR																	Use this register to set the Sample Rate For the ADC High Pass Filter 000: 8 – 12k 001: 16 – 24k 010: 32 – 48k 011: 64 – 96k 100: 128 – 192k
		Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x0010
13	MUTE_CTRL	SOFT_MUTE																	Soft Mute Enable 1 = Gradually lower DAC volume to zero 0 = Gradually increase DAC volume to volume register setting
		AMUTE																	Auto Mute Enable Generate null output to analog circuitry when 1024 consecutive zeros are detected. De-assert as soon as first non-zero sample is detected
		SMUTE_CTRL																	0: Default 1: When soft mute is enabled, DAC limiter output is also muted to remove any dc offset produced by the audio processing block
		AMUTE_CTRL																	Auto Mute Control DAC Channel must have 0 values for 1024 samples before AMUTE turns on
		DAC_ZC_EN																	DAC Zero Crossing Enable
		Default	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0x00cf
14	ADC_VOL_CTRL	ADC_GAIN_V																	ADC V Channel Volume control. Expressed as a gain or attenuation in 0.125db steps, max is 24.125dB 0x00 = 0 dB 0x01 = 0.125 dB ▼ 0xc0 = + 24 dB 0xc1 = 24.125 dB ▼ 0xfe = 24.125 dB 0xff = Mute
		ADC_GAIN_I																	ADC I Channel Volume control. Expressed as a gain or attenuation in 0.125db steps, max is 24.125dB 0x00 = 0 dB 0x01 = 0.125 dB ▼ 0xc0 = +24 dB 0xc1 = +24.125 dB ▼ 0xfe = +24.125 dB 0xff = Mute
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
15	INT_COE	CICI_ADJ																	Interpolator coefficient To adjust the CICI filter gain
		Default	1	0	1	0	0	1	0	0	0	0	0	1	1	1	1	1	0xa41f
16	DEC_COE	CICD_ADJ																	Decimator coefficient To adjust the CICD filter gain
		Default	1	0	1	1	0	1	1	1	1	1	0	0	1	1	0	1	0xb7cd
17	Reserved	Reserved																	Reserved
		Reserved																	Reserved

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		Default	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0x3f00
18	CTRL2	TC_EN																	Temperature Compensation Enable 1 = Enable 0 = Disable
		SEL_DLY_L																	Option to add one delay sample to the Left Channel 1 = Add one sample delay to Left Channel 0 = No delay added to the Left Channel
		SEL_DLY_R																	Option to add one delay sample to the Right Channel 1 = Add one sample delay to Right Channel 0 = No delay added to the Right Channel
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
19	DSP_CORE_CTRL1	PRID																	Latched at reset into the low-order bits of the Processor ID special register for Tensilica DSP core
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1A	DSP_CORE_CTRL2	SEL_JTAG_PIN																	1 = MUX the JTAG interface to five pins 0 = JTAG interface all connected to 0
		SELDSP_DAC																	1 = The output DAC data is from the Tensilica DSP core output 0 = The output DAC data is from the Tensilica DSP core input
		RUNSTALL																	External signal from register bit to stall the Tensilica DSP core, high active 1 = Stall the processor 0 = Not Stall the processor
		STATVECTORSEL																	Selects between one of two stationary vector bases. 0 = Default 1 = Alternative
		Reserved																	Reserved
		BREAKIN																	External Debug Interrupt for the Tensilica DSP core
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1B	CLK_DOUBLER_O	TDC																	Clock Multiplier SAR Output for monitoring
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1C	Reserved	Reserved																	Reserved
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1D	GENERAL_STATUS0	BDM_DIV_SEL																	Output of the Auto Attenuate Control
		OSR100																	Indication of the system is in the OSR100(MIPS400 / MIPS500)
		MIPS500																	Indication of the system is in the MIPS500
																			Reserved
		GPIO2_IN																	GPIO Port 2 Input
		GPIO1_IN																	GPIO Port 1 Input
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1E	GENERAL_STATUS1	DEVID																	Indication what I2C device IP is using 0000 : I2C_DEVID1 0001 : I2C_DEVID2

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			0010 : I2C_DEVID3 0011 : I2C_DEVID4
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
1F	GENERAL_STATUS2																		Reserved
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
20	SAR_ADC_OUT_01	SAR_ADC_OUT1																	SAC ADC Channel 1 Output (Tj)
		SAR_ADC_OUT0																	SAC ADC Channel 0 Output (VDDD) (decimal reading from [7:0] x61 x35)/32767
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
21	SAR_ADC_OUT_23	SAR_ADC_OUT3																	SAC ADC Channel 3 Output (Aux)
		SAR_ADC_OUT2																	SAC ADC Channel 2 Output (Ta)
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
22	ALC_READ OUT1	FAST_DECREMENT																	ALC is in fast decrement
		PGA_GAIN																	ALC gain
																			Reserved
		CLIP																	System Clips
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
23	ALC_READ OUT2	PEAK_OUT																	ALC Peak Detector rectified peak detector output
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
24	ALC_READ OUT3	P2P_OUT																	ALC Peak Detector peak to peak calculation output
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
25	DSP_STATUS_0	PFAULTINFOVALID																	Strobe signal that is asserted for one cycle every time PFault Info signal changes its value
		PFATALERROR																	Sticky fatal error notification signal that is asserted when a fatal error condition occurs
		DOUBLEEXCETIONERROR																	Single cycle assertion for every time double exception faults occur
		PWAITMODE																	Indicate that the processor is in sleep mode
		IROM0LOAD																	Indicate that Load is occurring from instruction ROM
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
26	DSP_STATUS_1	PFAULTINFO																	Lowest 16 bit of the Fault information signal. Which mirrors the internal Fault Information Register in the Tensilica DSP core
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
27	DSP_STATUS_2	PFAULTINFO																	Highest 16 bit of the Fault information signal. Which mirrors the internal Fault Information Register in the Tensilica DSP core
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
28	ADC_RATE	I2S_MODE																	I2S Data Mode 1 = Normal I2S Audio Data mode, without SAR ADC data 0 = I2S Audio Interface contains both Audio data and SAR ADC data

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		UNSIGN_IV																	Choose the ISENSE VSENSE data signed or unsigned 1 = Unsigned 0 = Signed
		Reserved																	Reserved, always set to zero.
		Reserved																	Reserved, always set to zero.
		Reserved																	Reserved to Zero
		ADC_RATE																	ADC SINC Down selection 00 = Down 32 01 = Down 64 10 = Down 128 11 = Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0x0002
29	DAC_CTRL1	DISABLE_DEM																	0 = Normal 1 = Disable DEM control to RateConvert2 module
		DEM_DLY_N																	DAC DEM delay Enable 0 = Enable 1 = Disable
																			Reserved = 1 (default)
		CIC_GAIN_ADJ																	For fine tuning the DAC output
		DAC_RATE																	DAC oversample rate selection 000 = 64 001 = 256 010 = 128 100 = 32
		Default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0x0081
2A	DAC_CTRL2	DEM_DITHER																	Set probability of first order dynamic element matching dithering. Each level increments probability by 1/16 0000 = No dithering 0001 = 1/16 0010 = 1/8 0011 = 3/16 0100 = 1/4 0101 = 5/16 0110 = 3/8 0111 = 7/16 1000 = 1/2 1001 = 9/16 1010 = 5/8 1011 = 11/16 1100 = 3/4 1101 = 13/16 1110 = 7/8 1111 = 15/16
		SDMOD_DITHER																	Number of bits of dithering on SD modulator. Each level increments dithering by 1 bit 0000 = No dithering 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15
		DACPL																	DAC Output polarity 0 = Non-Inverted 1 = Inverted
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
2C	ALC_CTRL1	ALCMODE																	1 = Limiter Mode, 0 = Normal Mode
		ALC_ZC																	ALC Zero Cross Detection 0 = Disabled 1 = Enabled

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		Reserved																	Reserved to 1
		ALCPKSEL																	0 = Use rectified peak detector output for ALC gain updates. 1 = Use peak to peak calculation output for ALC gain updates.
		Reserved																	Reserved to 0
		SCLKEN																	Slow timer clock enable. Starts internal timer clock derived by dividing master clock 0 = Disable 1 = Enable
		ALCMAXGAIN																	Maximum ALC gain setting 000 = -7 dBFs 001 = -6 dBFs 010 = -5 dBFs 011 = -4 dBFs 100 = -3 dBFs 101 = -2 dBFs 110 = -1 dBFs 111 = 0 dBFs
		ALCMINGAIN																	Minimum ALC gain setting 000 = -3 dBFs 001 = -6dBFs 010 = -9 dBFs 011 = -12 dBFs 100 = -16 dBFs 101 – 111 : Reserved
		ALCGAIN_SEL_MODE																	ALC GAIN Selection mode enable. If enable this bit, the device will use the minimum ALC GAIN of the two devices in stereo application. If not, the device will always use its own ALC GAIN. 1 = Enable 0 = Disable
		Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0x2000
2D	ALC_CTRL2	ALCDCY																	ALC Decay Timer (0.1875 dB/ adjust step) 0000 = 500 µs/step 0001 = 1 ms/step 0010 = 2 ms/step 0011 = 4 ms/step 0100 = 8 ms/step 0101 = 16 ms/step 0110 = 32 ms/step 0111 = 64 ms/step 1000 = 128 ms/step 1001 = 256 ms/step 1010 =512 ms/step 1011 =1024ms/step 1100 – 1111 = Reserved
		ALCATK																	ALC Attack Timer (0.1875dB/ adjust step) 0000 = 2 µs/step 0001 = 4 µs/step 0010 = 8 µs/step 0011 = 16 µs/step 0100 = 32 µs/step 0101 = 64 µs/step 0110 = 128 µs/step 0111 = 256 µs/step 1000 = 512 µs/step 1001 = 1024µs/step 1010 =2048 µs/step 1011 =4196µs/step 1100 – 1111 = Reserved
		ALCHLD																	Hold time before ALC automated gain increase 0000 = 0.00 ms 0001 = 2.00 ms 0010 = 4.00 ms 0011 = 8.00 ms 0100 = 16.00 ms 0101 = 32.00 ms 0110 = 64.00 ms 0111 = 128.00 ms 1000 = 256.00 ms 1001 = 512.00 ms 1010 through 1111 = 1000.00 ms
		ALCLVL																	ALC target level 0000 = 0 dBFs 0001 = -1 dBFs 0010 = -2 dBFs 0011 = -3 dBFs 0100 = -4 dBFs 0101 = -5 dBFs 0110 = -6 dBFs 0111 = -7 dBFs 1000 = -8 dBFs 1001 = -9 dBFs

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			1010 = -10 dBFs 1011 = -11 dBFs 1100 = -12 dBFs 1101 = -13 dBFs 1110 = -14 dBFs 1111 = -15 dBFs
		Default	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0x8400
2E	ALC_CTRL3	ALC_EN																	0 = ALC/Limiter disabled (fixed gain) 1 = ALC/Limiter enabled
		LIM_MDE																	000 = Limiter mode with clip detection 001 = Low Battery Limiter mode with Clip Detection 010 = Limiter mode with pre-programmed limit level 011 = Low Battery Limiter mode with pre-programmed limit level 100 = Low Battery Limiter mode with pre-programmed VBAT ratio limit level
		VBAT_RATIO																	Set VBAT Limiter Ratio 00 = 3:1 01 = 6:1 10 = 9:1 11 = 12:1
		ALC_VBAT_THRESHOLD																	Low VBAT Limiter Mode Threshold 00000 = 16.25 V 01000 = 14.00 V 00001 = 16.00 V 01001 = 13.75 V 00010 = 15.75 V 01010 = 13.50 V 00011 = 15.50 V 01011 = 13.25 V 00100 = 15.25 V 01100 = 13.00 V 00101 = 15.00 V 01101 = 12.75 V 00110 = 14.50 V 01110 = 12.50 V 00111 = 14.25 V 01111 = 12.25 V 10000 = 12.00 V 11000 = 9.75 V 10001 = 11.75 V 11001 = 9.50 V 10010 = 11.25 V 11010 = 9.25 V 10011 = 11.00 V 11011 = 9.00 V 10100 = 10.75 V 11100 = 8.75 V 10101 = 10.50 V 11101 = 8.25 V 10110 = 10.25 V 11110 = 8.00 V 10111 = 10.00 V 11111 = 7.75 V
		Reserved																	Reserved to 0
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
2F	ALC_CTRL4	SEG_ALLON																	Segment Control bit, if set this bit 1, Then the output bits of the segment control will be set to 1.
		LPGAZC																	Channel input zero cross detection enable 0 = Gain changes to PGA register happen immediately (default) 1 = Gain changes to PGA happen pending zero crossing logic
		ALCCLIPSTEP																	Maximum Gain Adjustment step during any clipping event (0.25dB per step) 000 = (default) no adjustment 001 = 1 step 010 = 2 step 011 = 3 step 100 = 4 step 101 = 5 step 110 = 6 step 111 = 7 step
		VBAT_F_ANALOG																	1 = ALC uses the VBAT comparator based on register 0x6B [7:4]. 0 = ALC uses the VBAT comparator based on register 0x2E [9:5].
		SEG_COMP																	Choose the divide factor N for 4 comparator levels: 3/N x Full Scale, 6/N x Full Scale, 9/N x Full Scale, 12/N x Full Scale. 000: N= 64 001: N= 128 010: N= 256 011: N= 512 100: N= 1024 101: N= 2048 110: N= 4096 111: N= 8192

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		Reserved																	Reserved to 3F
		Default	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0x00BF
30	TEMP_ COMP_ CTRL	ACT1																	Coefficients used for the gain calculation in the Temperature Compensation module. Gaintc = ACT1[7:0]/TJ[7:0] + (1 - 2*ACT2[7])*ACT[6:0]/1024
		ACT2																	
		Default	0	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0x7df
31	UVLO_CTR L0	ENABLE_UV LOP																	UVLOP Gain Limiter Enable 1 = Enable 0 = Disable Note this function uses the VBAT comparator & threshold set in register x6B
		UVLOP_ATK																	UVLOP Gain Limiter Attack time setting 000: 2 µsec/step 001: 4 µsec/step 010: 8 µsec/step 011: 16 µsec/step 100: 32 µsec/step 101: 64 µsec/step 110: 128 µsec/step 111: 256 µsec/step
		UVLOP_HLD																	UVLOP Gain Limiter Hold time setting 000: 0 ms/step 001: 16 ms/step 010: 32 ms/step 011: 64 ms/step 100: 128 ms/step 101: 256 ms/step 110: 512 ms/step 111: 1024 ms/step
		UVLOP_RLS																	UVLOP Gain Limiter Release time setting 000: 0.5 ms/step 001: 2 ms/step 010: 8 ms/step 011: 32 ms/step 100: 128 ms/step 101: 256 ms/step 110: 512 ms/step 111: 1024 ms/step
		UVLOP_STEP																	UVLOP Gain Limiter Attack time step setting 00 : -0.5 dB/step 01 : -1 dB/step 10 : -1.5 dB/step 11 : -2 dB/step
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
32	UVLO_ CTRL1	UVLOP_ATTN																	UVLOP Minimum Limiter GAIN 00000 = 0 dBFs 00001 = -0.5 dBFs 00010 = -1 dBFs 00011 = -1.5 dBFs 00100 = -2 dBFs 00101 = -2.5 dBFs 00110 = -3 dBFs 00111 = -3.5 dBFs 01000 = -4 dBFs 01001 = -4.5 dBFs 01010 = -5 dBFs 01011 = -5.5 dBFs 01100 = -6 dBFs 01101 = -6.5 dBFs 01110 = -7 dBFs 01111 = -7.5 dBFs 10000 = -8 dBFs 00001 = -8.5 dBFs 10010 = -9 dBFs 00011 = -9.5 dBFs 10100 = -10 dBFs 00101 = -10.5 dBFs 10110 = -11 dBFs 00111 = -11.5 dBFs 11000 = -12 dBFs 01001 = -12.5 dBFs 11010 = -13 dBFs 01011 = -13.5 dBFs 11100 = -14 dBFs 01101 = -14.5 dBFs 11110 = -15 dBFs 01111 = -15.5 dBFs
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
33	LPF_CTRL	LPF_IN1_EN																	Low Pass Filter TJ channel Enable 1 = Enable 0 = Disable
		LPF_IN1_TC																	Low Pass Filter TJ channel Time Constant Setting (When CFG_REG7[6:5] = 2'b01 and CFG_REG7[3:2] = 2'b01) 1111 = 0.4 ms 1110 = 1ms 1101 = 2.1 ms 1100 = 4.5ms 1011 = 9.0 ms 1010 = 18.2ms 1001 = 36.6ms 1000 = 73.3ms 0111 = 146 ms 0110 – 0000: Reserved
		Reserved																	Reserved

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		Reserved																	Reserved
		LPC_QUICK_MODE																	Enable the LPF quick mode to make the time constant shorter 1 = Enable 0 = Disable
		Default	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0x7380
40	CLK_DET_CTRL	REG_APWRUPEN																	1 = the clock detection will require non_zero samples in order to enable to output power up signal.
		REG_CLKPWRUPN																	Clock Detection Module Enable 1 = Disable 0 = Enable
		REG_PWRUP_DFT																	When the Clock Detection Module is disabled, the default value for the PWRUPEN
		REG_SRATE																	Use this register to set the Sample Rate Range 000 = 8 – 12k 001 = 16 -24k 010 = 32 – 48k 011 = 64 – 96k 100 = 128 – 192k
		REG_ALT_SRATE																	Use this register to set the DAC/ADC Sample Rate of the DSP to 44.1kHz DAC and 11.025kHz ADC. 1 = DAC/ADC: 44.1kHz/11.025kHz 0 = DAC/ADC: 48kHz/12kHz If DAC/ADC is a different rate, will not matter what it is set to.
		REG_MINMAX																	0 = Choose the Divider Min 1 = Choose the Divider Max
		Default	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0xa801
41	Reserved																		Reserved
42	Reserved																		Reserved
43	Reserved																		Reserved
44	Reserved																		Reserved
45	Reserved																		Reserved
46	I2C_DEVICE_ID	I2C_DEVICE_ID																	I2C Device ID read in
		REG_SI_REV																	Indicates the Revised Silicon ID 0xFX – X is the Revised Silicon Number
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
49	Reserved	Reserved																	Reserved
		Reserved																	Reserved
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
4A	ANALOG_READ	LOVDDDETB																X	VBAT Under Voltage Lockout when ‘0’
		OVP															X		VBAT Over Voltage detection when ‘1’
		SHORT														X			Over Current detection when ‘1’
		TALARM													X				Over Temperature when ‘1’
		SHUTDOWN-DRIVER												X					Driver shutdown when ‘1’
		Driver2											X						Class-D driver 2 enabled when ‘1’
		Driver3										X							Class-D driver 3 enabled when ‘1’
		Driver4									X								Class-D driver 4 enabled when ‘1’
		Driver5								X									Class-D driver 5 enabled when ‘1’
		MCLKDET							X										MCLK detected when ‘1’
		PWRUPEN						X											Raw POWERUPEN signal
		Reserved					X												Reserved

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		AUTOATT0				X													Auto attenuator control bit 0
		AUTOATT1			X														Auto attenuator control bit 1
		AUTOATT2		X															Auto attenuator control bit 2
		Reserved																	
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**
55	MISC_CTRL	Reserved																	Reserved
		Reserved																	Reserved
		D2A_LOOP																	1: Use DAC Left Filter Input as ADC decimation filter output
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
60	BIAS_ADJ	MUTER																	Mute Isense PGA 1 = Enable0 = Disable
		Reserved																	Reserved
		VMID_SEL																	VMID tie-off selection options 00 = Open (Default and Recommended) 01 = 25k Ohm 10 = 125k Ohm 11 = 2.5k Ohm
		BIASADJ																	PGA Master bias current power options 00 = normal operation (default) 01 = 9% reduced bias current from default 10 = 17% reduced bias current from default 11 = 11% increased bias current from default
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
61	ANALOG_ CONTROL _1																		CURRENT SENSE AMPLIFIER enable 00 = CURRENT SENSE AMPLIFIER disabled 01 = CURRENT SENSE AMPLIFIER enable gated by POWERUP signal 10 = CURRENT SENSE AMPLIFIER disabled 11 = CURRENT SENSE AMPLIFIER enabled
																			ADC RESETBAR enable 00 = ADC RESETBAR disabled 01 = ADC RESETBAR enable gated by POWERUP signal 10 = ADC RESETBAR disabled 11 = ADC RESETBAR enabled
																			VOLTAGE SENSE AMPLIFIER enable 00 = VOLTAGE SENSE AMPLIFIER disabled 01 = VOLTAGE SENSE AMPLIFIER enable gated by POWERUP signal 10 = VOLTAGE SENSE AMPLIFIER disabled 11 = VOLTAGE SENSE AMPLIFIER enabled
																			ADC enable 00 = ADC disabled 01 = ADC enable gated by POWERUP signal 10 = ADC disabled 11 = ADC enabled
																			DAC Clock enable 00 = DAC Clock disabled 01 = DAC Clock enable gated by POWERUP signal 10 = DAC Clock disabled 11 = DAC Clock enabled

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			DAC enable 00 = DAC disabled 01 = DAC enable gated by POWERUP signal 10 = DAC disabled 11 = DAC enabled
																			Current BIAS reference enable 00 = BIAS reference disabled 01 = BIAS reference enable gated by POWERUP signal 10 = BIAS reference disabled 11 = BIAS reference enabled
																			VMID reference enable 00 = VMID reference disabled 01 = VMID reference enable gated by POWERUP signal 10 = VMID reference disabled 11 = VMID reference enabled
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
62	ANALOG_ CONTROL_ 2																		Reserved
																			CLASS-D enable 00 = CLASS-D disabled 01 = CLASS-D enable gated by POWERUP signal 10 = CLASS-D disabled 11 = CLASS-D enabled
																			VMID reference fast power up circuit disable 00 = VMID reference fast power up circuit enabled with VMID reference enable 01 = VMID reference fast power up circuit disabled with Class-D enable 10 = VMID reference fast power up circuit enabled with VMID reference enable 11 = VMID reference fast power up circuit disabled
																			Reserved = 0
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
63	ANALOG_ CONTROL_ 3																		PWM Modulation Selection 0 = BDM Modulation 1 = Ternary Modulation
																			Current Sense Amplifier Mute PWMP
																			Current Sense Amplifier Mute PWMN
																			Voltage Sense Amplifier Current Trim
																			Reserved
																			DAC Reference Voltage Decoupling Capacitors 00 = No Capacitors 01 = 1 Capacitor 10 = 2 Capacitors 11 = 3 Capacitors
																			DAC Reference fine adjust 00 = default 01 = -0.15 dB 10 = -0.24 dB 11 = -0.36 dB
																			Reserved
																			SAR ADC Reference Selection 0 = VREF (default) 1 = VDDA/2
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000, recommended 0x0030
64																			Reserved

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
	ANALOG_ CONTROL_ 4																		Auto-Attenuator Minimum Gain 0 = 12 dB 1 = 0 dB
																			Class-D P-Driver Short Circuit Threshold Adjustment 0000: Nominal 1000: -20% 0001: +33% 1100: -33% 0011: +100%
																			Class-D N-Driver Short Circuit Threshold Adjustment 0000: Nominal 1000: +33% 0001: -20% 1100: +100% 0011: -33%
																			Class-D P-Driver Slew Rate Adjustment (idle channel) 000: Nominal 100: Off, no edge 001: +25% 101: -75% 010: +50% 110: -50% 011: +75% 111: -25%
																			Class-D N-Driver Slew Rate Adjustment (idle channel) 000: Nominal 100: Off, no edge 001: +25% 101: -75% 010: +50% 110: -50% 011: +75% 111: -25%
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000, recommended 0x4007
65	ANALOG_ CONTROL_ 5																		Reserved
																			Bias Current Pre-Driver to NGATE Buffer 001-5uA 010-10uA ⋮ 111-35uA
																			Reserved
																			Reserved
																			Non-Overlapping-Time Control From NGate OFF to PGate ON 00 = 0 dly 10 = 2x dly 01 = 1x dly 11 = 3x dly
																			Non-Overlapping-Time Control From PGate OFF to NGate ON 00 = 0 dly 10 = 2x dly 01 = 1x dly 11 = 3x dly
																			Reserved
																			Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
66	ANALOG_ CONTROL_ 6																		Sense Resistor Adjust 000 = 200 ohm 100 = 343 ohm 001 = 218 ohm 101 = 400 ohm 010 = 240 ohm 110 = 171 ohm 011 = 300 ohm 111 = 150 ohm
																			Slew Rate Adjust: PGATE OFF 0,1,2 = faster 3 = slower
																			Slew Rate Adjust: PGATE ON 0,1,2 = faster 3 = slower
																			Slew Rate Adjust: NGATE ON 0,1,2 = faster 3 = slower
																			Slew Rate Adjust: NGATE OFF 0,1 = faster 2,3 = slower

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			Reserved
																			Bias Current Pre-Driver to PGATE Buffer 001-5uA 010-10uA ⋮ 111-35uA
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
68	ANALOG_ CONTROL_ 7																		Reserved
																			V-sense & I-sense ADC Reference Buffer gain adjust 00 = default 10 = -0.92dB 01 = -0.41 dB 11 = -1.57 dB
																			VREF Bandgap Reference Buffer voltage adjust 00 = 0.9V (default) 10 = 0.81V 01 = 0.85V 11 = 0.96V
																			Enable VREF Bandgap Reference Buffer 0 = VREF bandgap buffer off 1 = VREF bandgap buffer on
																			TJ signal to TA pin 0 = TA pin tied to current source 1 = TA pin tied to TJ signal
																			Bandgap Voltage to SAR ADC Input 0 = SAR ADC AUX input disconnected 1 = SAR ADC AUX input connected to bandgap voltage
																			MCLK Multiplier Range Control 0 = default range 1 = Half range
																			16x MCLK Enable 1 = 16x MCLK Multiplier enabled (requires 8xMCLK to be enabled & requires 0x68[3]=1) 0 = 16x MCLK Multiplier disabled
																			8x MCLK Enable 1 = 8x MCLK Multiplier enabled (requires 4xMCLK to be enabled) 0 = 8x MCLK Multiplier disabled
																			4x MCLK Enable 1 = 4x MCLK Multiplier enabled 0 = 4x MCLK Multiplier disabled
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000, recommended 0x640
69	CLIP_CTRL	CLIP																	Clip Function Enable 1 = Enable Clip detection 0 = Disable Clip detection
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
6B	ANALOG_ CONTROL_ 8																		Reserved
																			Reserved
																			UVLOP (regs 0x31 & 0x32) & Ilim VBAT Comparator Threshold 0000 = 10 Volt 1000 = 7.1 Volt 0001 = 9.6 Volt 1001 = 6.7 Volt 0010 = 9.3 Volt 1010 = 6.3 Volt 0011 = 8.9 Volt 1011 = 6.0 Volt 0100 = 8.5 Volt 1100 = 5.6 Volt 0101 = 8.2 Volt 1101 = 5.2 Volt 0110 = 7.8 Volt 1110 = 4.9 Volt 0111 = 7.4 Volt 1111 = 4.5 Volt
																			Reserved

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			Enable low VBAT Comparator for current and voltage limiter 0 = disabled 1 = enabled
																			Reserved
																			Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
71	ANALOG_ ADC_1	Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0x0011
72	ANALOG_ ADC_2	Reserved																	Reserved
		Reserved																	Reserved
		ADC_UPR																	Right (Isense) channel PGA bias current increase enable for driving the ADC at high sample rates 1 = Enable 0 = Disable
		Reserved																	Reserved
		BIAS1																	Change bias currents in ADC 00 = Nominal 01 = Double 10 = Half 11 = Quarter
		BIAS0																	
		VREFSEL1																	VREFSEL1: I-sense ADC Reference Selection 0 = ADC VREF buffer 1 = VDDA
		VREFSEL0																	VREFSEL0: V-sense ADC Reference Selection 0 = ADC VREF buffer 1 = VDDA
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0x0020
73	RDAC	Reserved																	Reserved
		Reserved																	Reserved
		Reserved																	Reserved

#	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DACVREFSEL																	DAC Reference Voltage Setting. Can be used for minor tuning of the output level. 00 voltage source directly from VDDA pin 01, 10,11 voltage is regulated by LDO 00 VDDA (unregulated) 01 VDDA x 1.5/1.8 V 10 default: VDDA x 1.6/1.8 V 11 VDDA x 1.7/1.8 V
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0x0008
76	PGA	Reserved																	Reserved
		STG2_SEL																	PGA in class A mode of operation enable instead of class AB (default) 1 = Enable 0 = Disable
		Reserved																	Reserved
		BYPS_IBCTR																	Bypass PGA current control enable 1 = Enable 0 = Disable
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
77	FEPGA	ACDC_CTRL																	DC State Control for Isense ACDC_CTRL[0] changes ground reference ACDC_CTRL[1] changes polarity 1 = Enable 0 = Disable
		Reserved																	Reserved
		Reserved																	Reserved
		IBCTR_ CODE																	Isense PGA: Supply Current Trim 000 maximum current ⋮ 111 minimum current
		CMLCK_ENB																	Isense PGA Common Mode Lock 0 = Enable 1 = Disable
		Reserved																	Reserved
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
7F	PGA_GAIN	PGA_GAIN																	Isense PGA Gain increments in 4 dB steps 0000 = 0 dB 0001 = 4 dB 0010 = 8 dB 0011 = 12 dB
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
80	BIQ0_COE_1	BIQ0_A1_L																	Program Band 1 BIQ0_A1 parameter Bit[15:0]
		Default	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0x0800
81	BIQ0_COE_2	BIQ0_A1_H																	Program Band 1 BIQ0_A1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
82	BIQ0_COE_3	BIQ0_A2_L																	Program Band 1 BIQ0_A2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
83	BIQ0_COE_4	BIQ0_A2_H																	Program Band 1 BIQ0_A2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
84	BIQ0_COE_5	BIQ0_B0_L																	Program Band 1 BIQ0_B0 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
85	BIQ0_COE_6	BIQ0_B0_H																	Program Band 1 BIQ0_B0 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
86	BIQ0_COE_7	BIQ0_B1_L																	Program Band 1 BIQ0_B1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
87	BIQ0_COE_8	BIQ0_B1_H																	Program Band 1 BIQ0_B1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
88	BIQ0_COE_9	BIQ0_B2_L																	Program Band 1 BIQ0_B2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
89	BIQ0_COE_10	BIQ0_B2_H																	Program Band 1 BIQ0_B2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
8A	BIQ1_COE_1	BIQ1_A1_L																	Program Band 2 BIQ1_A1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
8B	BIQ1_COE_2	BIQ1_A1_H																	Program Band 2 BIQ1_A1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
8C	BIQ1_COE_3	BIQ1_A2_L																	Program Band 2 BIQ1_A2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
8D	BIQ1_COE_4	BIQ1_A2_H																	Program Band 2 BIQ1_A2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
8E	BIQ1_COE_5	BIQ1_B0_L																	Program Band 2 BIQ1_B0 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
8F	BIQ1_COE_6	BIQ1_B0_H																	Program Band 2 BIQ1_B0 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
90	BIQ1_COE_7	BIQ1_B1_L																	Program Band 2 BIQ1_B1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
91	BIQ1_COE_8	BIQ1_B1_H																	Program Band 2 BIQ1_B1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
92	BIQ1_COE_9	BIQ1_B2_L																	Program Band 2 BIQ1_B2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
93	BIQ1_COE_10	BIQ1_B2_H																	Program Band 2 BIQ1_B2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
94	BIQ2_COE_1	BIQ2_A1_L																	Program Band 3 BIQ2_A1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
95	BIQ2_COE_2	BIQ2_A1_H																	Program Band 3 BIQ2_A1 parameter Bit[18:16]

#	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
96	BIQ2_COE_3	BIQ2_A2_L																	Program Band 3 BIQ2_A2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
97	BIQ2_COE_4	BIQ2_A2_H																	Program Band 3 BIQ2_A2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
98	BIQ2_COE_5	BIQ2_B0_L																	Program Band 3 BIQ2_B0 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
99	BIQ2_COE_6	BIQ2_B0_H																	Program Band 3 BIQ2_B0 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
9A	BIQ2_COE_7	BIQ2_B1_L																	Program Band 3 BIQ2_B1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
9B	BIQ2_COE_8	BIQ2_B1_H																	Program Band 3 BIQ2_B1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
9C	BIQ2_COE_9	BIQ2_B2_L																	Program Band 3 BIQ2_B2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
9D	BIQ2_COE_10	BIQ_ON																	BIQ Enable bit, active high Bit[15] : Band 3 Bit[14] : Band 2 Bit[13] : Band 1
		BIQ2_B2_H																	Program Band 3 BIQ2_B2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

6 SYSTEM DIAGRAM

6.1 Reference System Diagram

A basic system reference diagram is provided in **Figure 51**.

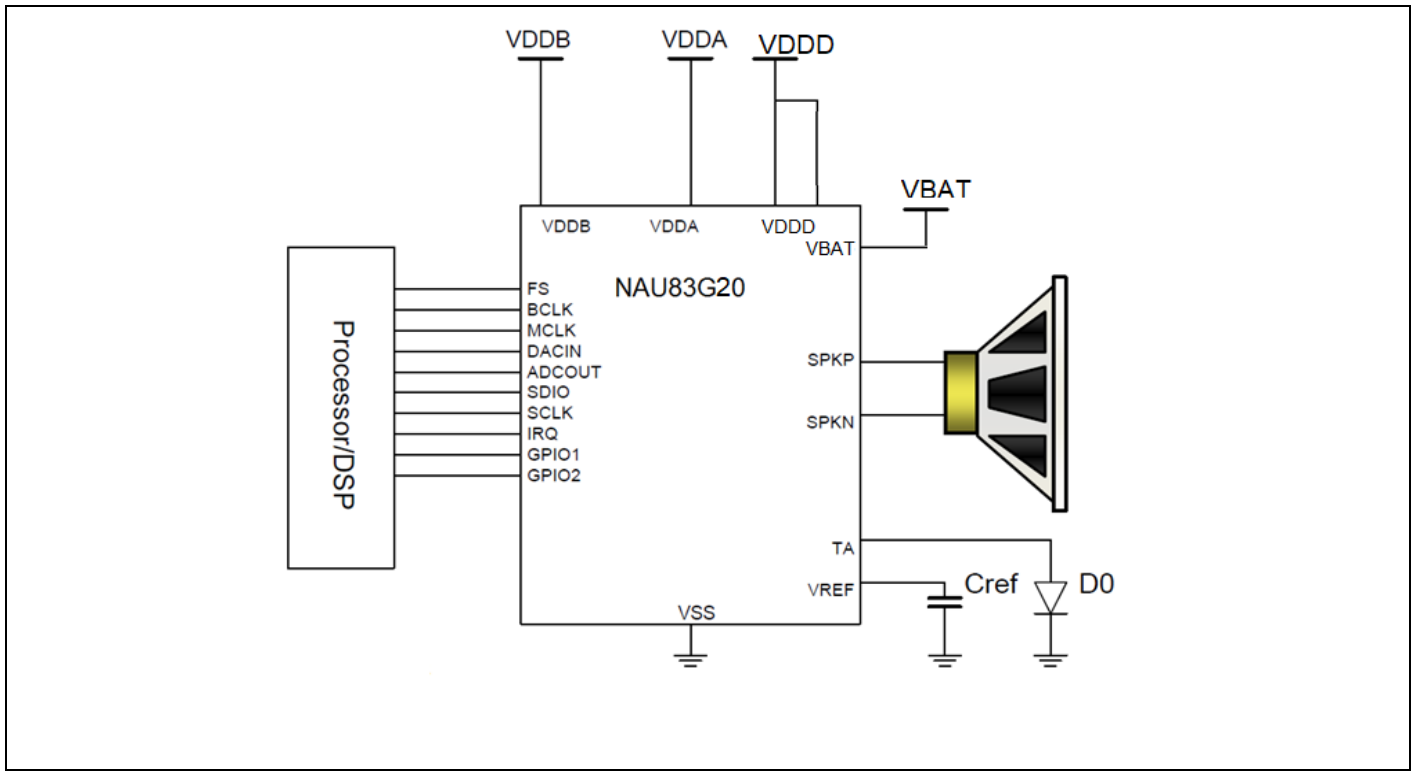


Figure 51 NAU83G20 Simplified System Diagram

7 Example of Register Setting

A register sequences settings are shown below which is based on MCLK is 12.288MHz, BCLK=3.072MHz, Fs=48KHz.

Register	*Value*	*Comment*
0000	0001	// Reset all registers
0000	0000	// Release reset
0002	0001	// Latch I2C address on GPIO's
0004	0700	// Block MCLK
001A	0010	// Stall DSP
000E	0000	// Default I2S setup
000C	0C24	// ADCOUT channels
0014	0162	// Set I-sense digital gain to +12.25dB
0076	4000	// Set I-sense PGA output stage Bias
0077	0780	// Set I-sense PGA Bias Current to minimum
007F	0030	// Set I-sense PGA to +12dB gain
0028	8001	// Set normal I2S with 64x ADC OSR
0029	0080	// Set normal 64x DAC OSR
0007	0095	// Enable SAR ADC with 4 µs sample time, 70kΩ and 0.5 µs compare cycle
002C	20E0	// Set ALC gain limits
002D	5350	// Set ALC settings
002E	C6E0	// Enable ALC & set threshold & mode
002F	00FF	// Set segment threshold
0040	0801	// Set target sample rate
0004	0707	// Enable DAC & ADC's; keeping MCLK blocked
0030	7d00	// Set Isense Temperature Coefficient
0033	bdc0	// Set Isense Temperature Coefficient low pas filter
0018	8000	// Set Temperature Coefficient EN
0073	0008	// Set DAC reference
0063	0030	// Set DAC reference capacitors
0064	0C1b	// Set slew rate
006B	0070	// Enable UVLOP comparator and set threshold
0031	0048	// Set UVLOP attack, release & hold time
0032	000F	// Set UVLOP minimum gain
0060	0000	// VMID resistor selection
0068	0640	// VREF Bandgap buffer ON, I/V Sense Ref Buffer Setting -1.5dB
0001	0000	// Soft Reset
0001	0000	// Soft Reset
0061	5555	// Enable Bias, DAC & ADC's with clock gating
0062	0014	// Enable Class-D & disable fast reference power up with clock gating
0003	08E0	// Set MCLK, ADC & DAC clock dividers
0068	064F	// VREF Bandgap buffer ON, I/V Sense Ref Buffer Setting -1.5dB
0004	0067	// DSP_CLK = (MCLK/2)*16 ; get MCLK from MCLK_PIN
0001	0000	// Soft Reset
0001	0000	// Soft Reset
000b	0000	// Enable AEC output on left I2S channel to replace Vsense data. Isense is still present
	****	***// need to implement a delay of at least 200ms before enabling DSP output***
001A	0020	// enable DSP output

8 Application Reference Circuit

Figure 52 provides an example application circuit diagram.

Table 25 provides a suggested Bill of Materials for the example reference circuit.

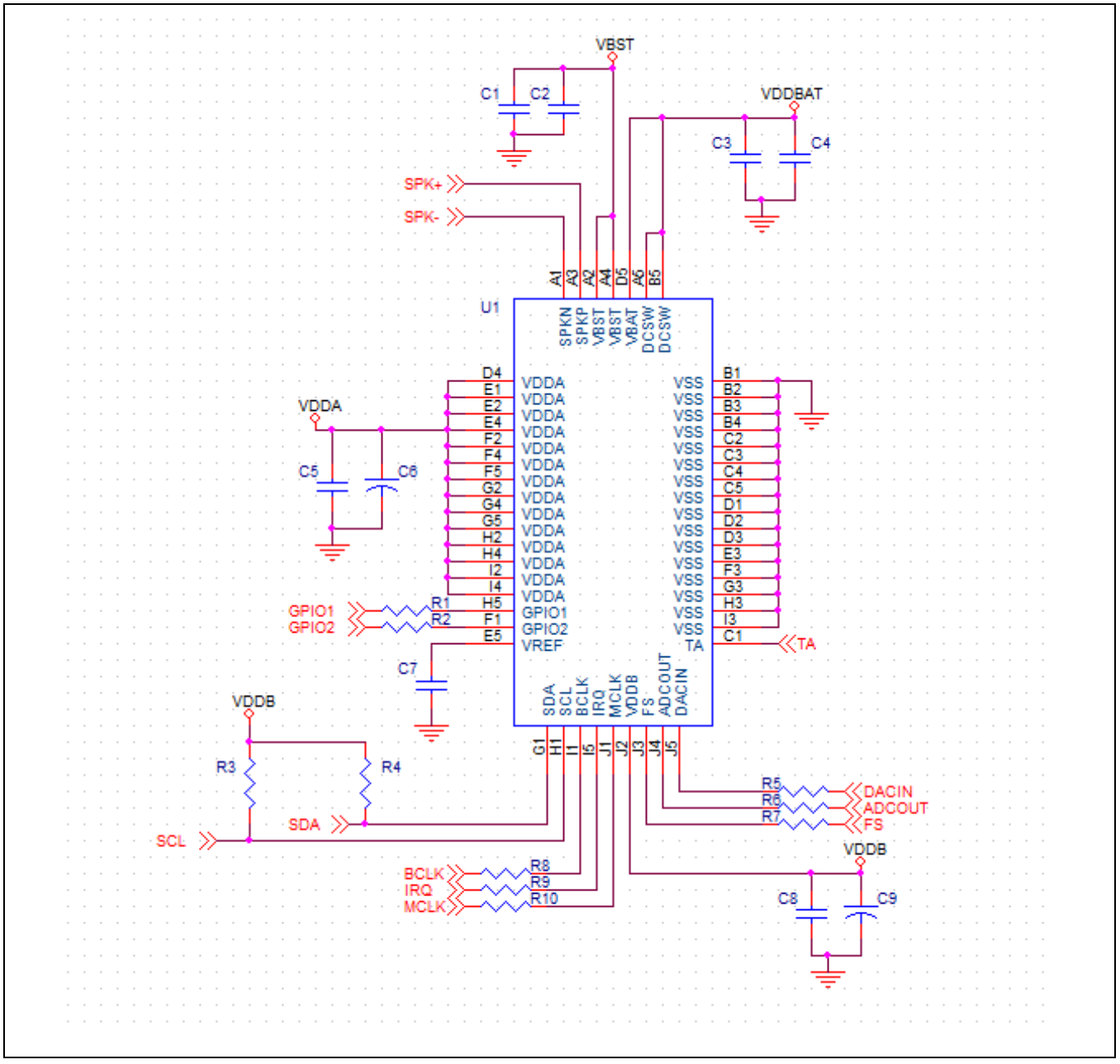


Figure 52 Application Reference Circuit Diagram

Table 25 NAU83G20 Application Reference Circuit Bill of Materials

Component	Description	Specification	Manufacturer	Quantity
U1	Smart Amplifier	NAU83G20	Nuvoton Technology	1
C1	Decoupling Capacitor, low ESL	22 uF+/-20%, X5R, 25 V		1
C2	Decoupling Capacitor	1 µF, 25V		1
C7	Bias Capacitor, low leakage	4.7 µF, 6.3 V		1
C5, C8, C3	Decoupling Capacitor	0.1 µF, 10V		3
C4, C6, C9	Decoupling Capacitor	4.7 µF, 6.3 V		3
R3, R4	I2C Pull-Up Resistor	4700 Ohm		2
R1, R2, R5, R6, R7, R8, R9, R10	Damping Resistor (optional for long inductive PCB traces)	200 Ohm		8

9 Package Specification

The NAU83G20 is a smart Mono Class-D Amplifier with DSP and I/V Sense is available in a small, 50-ball WLCSP package, using 0.5 mm pitch ball spacing, as shown in **Figure 53**.

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.567	0.625	0.683
STAND OFF		A1	0.22	---	0.28
WAFER THICKNESS		A2	0.325	0.35	0.375
FILM THICKNESS		A3	0.022	0.025	0.028
BODY SIZE	X	E	2.57		
	Y	D	5.28		
BALL/BUMP PITCH	X	SE	---		BSC
	Y	SD	---		BSC
EDGE BALL CENTER TO CENTER	X	E1	2		BSC
	Y	D1	4.5		BSC
PITCH		e	0.5		BSC
BALL DIAMETER (SIZE)			0.3		
BALL/BUMP WIDTH		b	0.28	---	0.34
BALL/BUMP COUNT		n	50		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.05		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		

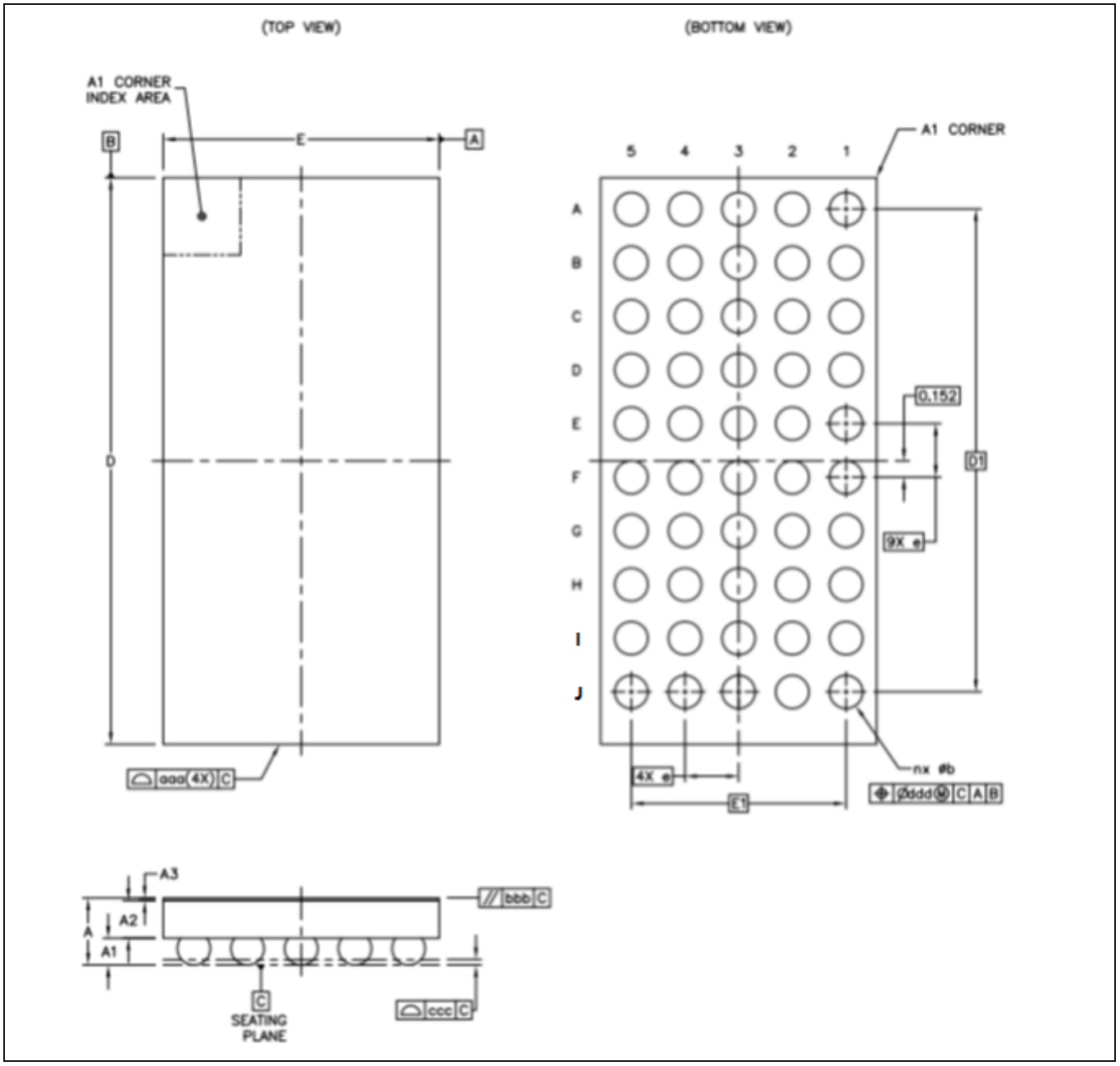


Figure 53 NAU83G20 Package Specification

10 ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU83G20VG	2.57mm x 5.28mm	WLCSP 50-Balls	Green

NAU83G20_ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

V = WLCSP-50

Feature:

G = Green Speaker Amplifier based on Klippel Control Sound (KCS)

11 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Mar 11, 2021	SAR ADC formula addition I2C address correction Reg0x20[7:0] formula correction
1.1	Apr 21, 2021	Reg0x6B delay line description removal
1.2	Jun 16, 2021	5.19.3-5.19.4 Device address change to 0x10
1.3	Jul 15, 2021	Adjust heading formats in section 5.20 for consistent bookmarks Remove excess spacing in register naming for better formatting in Control Register table.
1.4	Jul 20, 2021	Merge 3 separate tables into a single table 5
		Update OCP description
		Correct Figure 30 to show channels 3/5/7 instead of 1/3/5
		Register 5 description
		Register 8 GPIO1/2 description
		Clean up the table format for better clarity: • Separate the register bits into group of 4 • Minimize subtable break across pages • Registers 60-6B: arrange in order from MSB to LSB • Align register values
1.5	Aug 20, 2021	Remove Section 5.22.1 DSP Internal Ring Oscillator
		Set DSP_OSC_ENA and DSP_MCLK_SEL in Reg # 4 to Reserved
1.6	Apr 7, 2022	Adding NAU83G20 thermal information Correction: REG_CLKPWRUPN: 1=Disable 0=Enable Add Section 7 example of sequence setting Package dimention clearer diagram Change packing row number from J to I, K to J
1.7	May 26, 2022	Replaced dummy cycles with note to implement 60ms delay
1.8	Jul 22, 2022	Table 21 timing update Reg0xE[4] description
1.9	Sep 6, 2022	MCLK rate correction SPI removal Adding description and 0xb register
2.0	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description

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