NAU8318
DataSheet

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2 GENERAL DESCRIPTION

The NAU8318 is a mono high efficiency filter-free Class-D audio amplifier, which is capable of driving a 4Ω load with up to 3.2W output power. This device provides Enable control and I2S audio input with low standby current and fast start-up time.

The NAU8318 is ideal for portable applications, as it has advanced features like 82dB PSRR, 91% efficiency, ultra-low quiescent current and superior EMI performance. NAU8318 is available in a 14 ball Miniature WLCSP package and a 20-pin QFN package.

Key Features

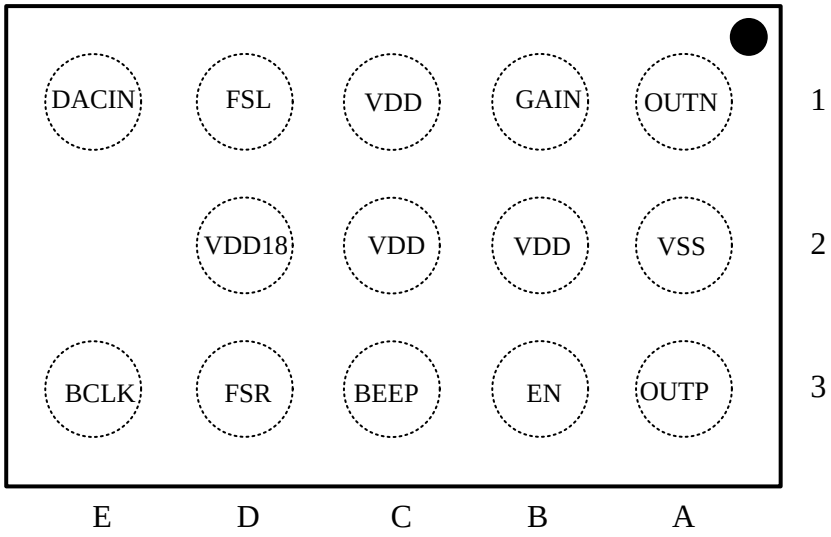
- Low VDD Quiescent Current
- Pin Selectable Features:
  - Gain Setting
  - I2S Left or Right Channel
  - PCM Timeslot Channels
  - Beep Generator
- Low Current Shutdown Mode
- Click-and Pop Suppression
- Sampling rate from 8K to 96 KHz
- Package: 14 ball WLCSP & 20-pin QFN
- Meets common portable Audio
- Package is Halogen-free, RoHS-compliant and TSCA-compliant
- Requirements:
  - 2.5V – 5.25V Operating Voltage
  - 1µWatt Shutdown Supply Power
  - 80dB PSRR @217Hz
  - Beat Tone Mitigation
  - 1.4V V_{IH}
  - Active Low Shutdown
  - 91% efficiency
  - +/- 1mV Offset Voltage
  - Low Output Noise: 9 μV_{RMS}
  - -94dBVrms pop noise
  - Self-Recovery Protection Mechanisms (OCP, UVLO, OTP, CTP)
  - True Filter Less Operation
- Powerful Mono Class-D Amplifier:
  - 3.2W (4Ω @ 5V, 10% THD+N)
  - 1.76W (4Ω @ 4.2V, 1% THD+N)
  - 1.8W (8Ω @ 5V, 10% THD+N)
  - 1W (8Ω @ 4.2V, 1% THD+N)

Applications

- Gaming Controllers
- Wireless (VR) Headset
- Smart Remote Controller
- Personal Media Players
- Ultrasonic speakers
- Chromebooks /Notebooks / Tablet PCs

3 PIN CONFIGURATIONS

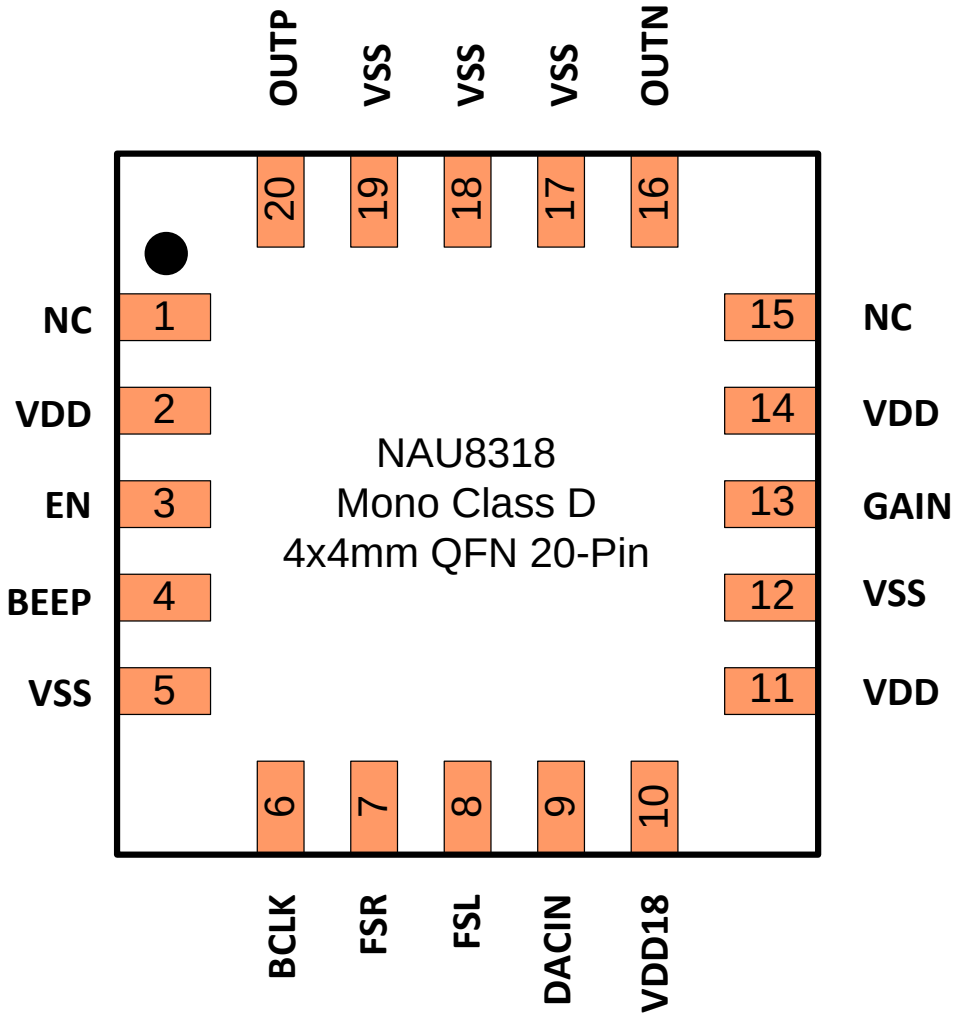
The NAU8318 **14 Ball WLCSP** package is shown in **Figure 1**.



Part Number	Dimension	Package	Package Material
NAU8318VG	1.18mm x 2.06mm	14-bump WLCSP (0.4 mm pitch)	Green

Figure 1 Pin Configuration of WLCSP14 NAU8318 (TOP VIEW)

The NAU8318 **20-pin QFN** package is shown in **Figure 1**.



QFN exposed thermal pad must be connected to VSS

Part Number	Dimension	Package	Package Material
NAU8318YG	4mm x 4mm	QFN-20	Green

Figure 2 Pin Configuration of QFN20 NAU8318

4 PIN DESCRIPTIONS

Pin descriptions for the NAU8318 are provided in **Table 1.**

Table 1 Pin Descriptions for the NAU8318

14 Ball WLCSP#	20-pin QFN* #	Name	Type	Description
E1	9	DACIN	Digital Input	I2S I/F DAC digital audio data
D1	8	FSL	Digital Input	I2S I/F Left Channel Frame clock
B1	13	GAIN	Analog IO	Gain Selection
A1	16	OUTN	Analog Output	Speaker negative output
B2	2	VDD	Supply	Power Supply
C1	11	VDD	Supply	Power Supply
C2	14	VDD	Supply	Power Supply
A2	5,12,17, 18,19	VSS	Supply	Ground
E3	6	BCLK	Digital Input	I2S I/F bit clock
D3	7	FSR	Digital Input	I2S I/F Right Channel Frame clock
B3	3	EN	Digital Input	Device Enable Input
A3	20	OUTP	Analog Output	Speaker positive output
C3	4	BEEP	Analog IO	BEEP Selection
D2	10	VDD18	Supply	1.8V Supply Voltage

*Note: For 20 pin QFN the NC pins can be tied to VSS for convenient PCB layout.

5 SYSTEM DIAGRAM

5.1 Reference System Diagram

A basic system reference diagram for stereo I2S is provided in **Figure 3**.

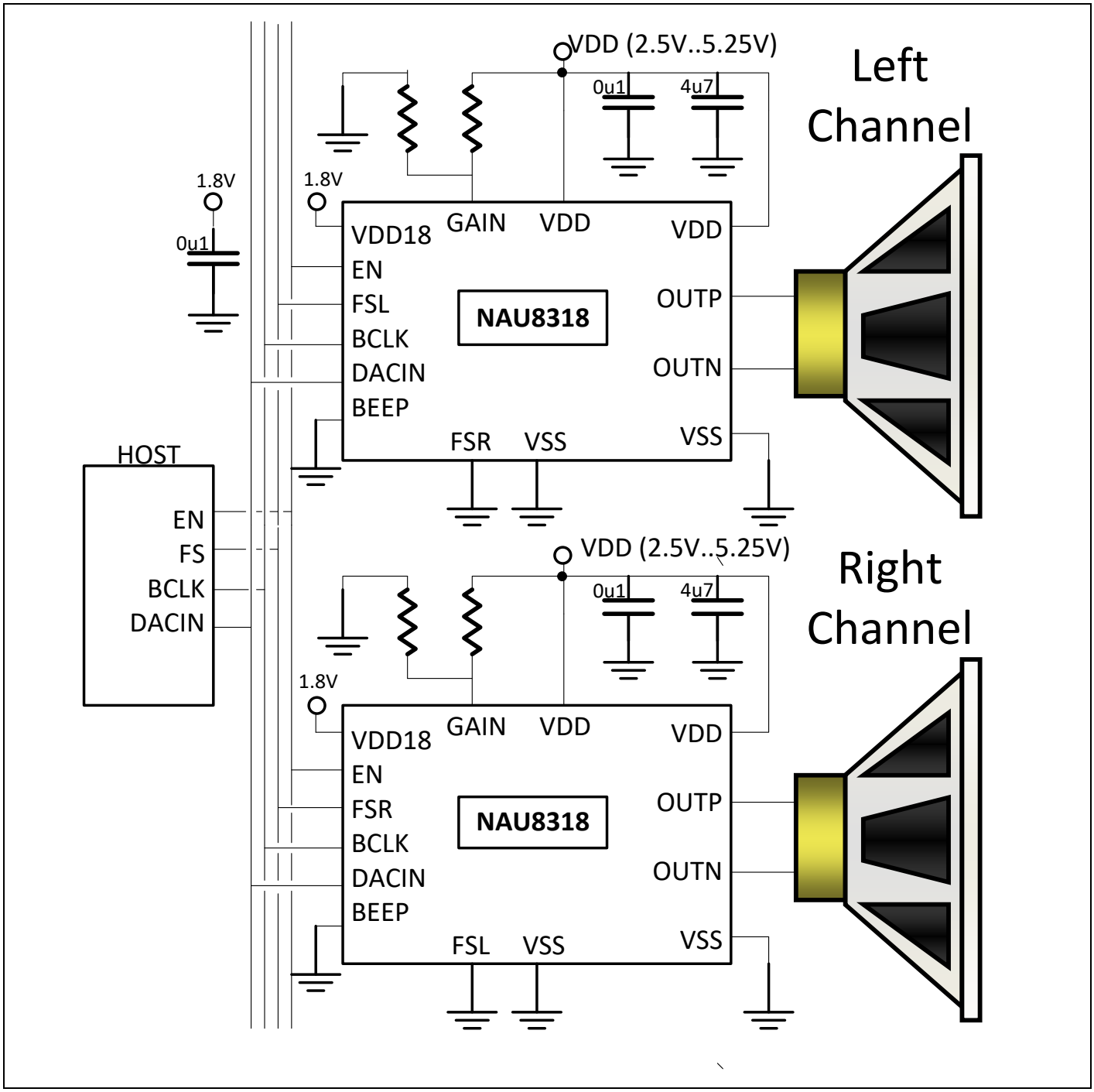


Figure 3 NAU8318 Simplified System Diagram

A basic system reference diagram for 2.1 I2S sound is provided below

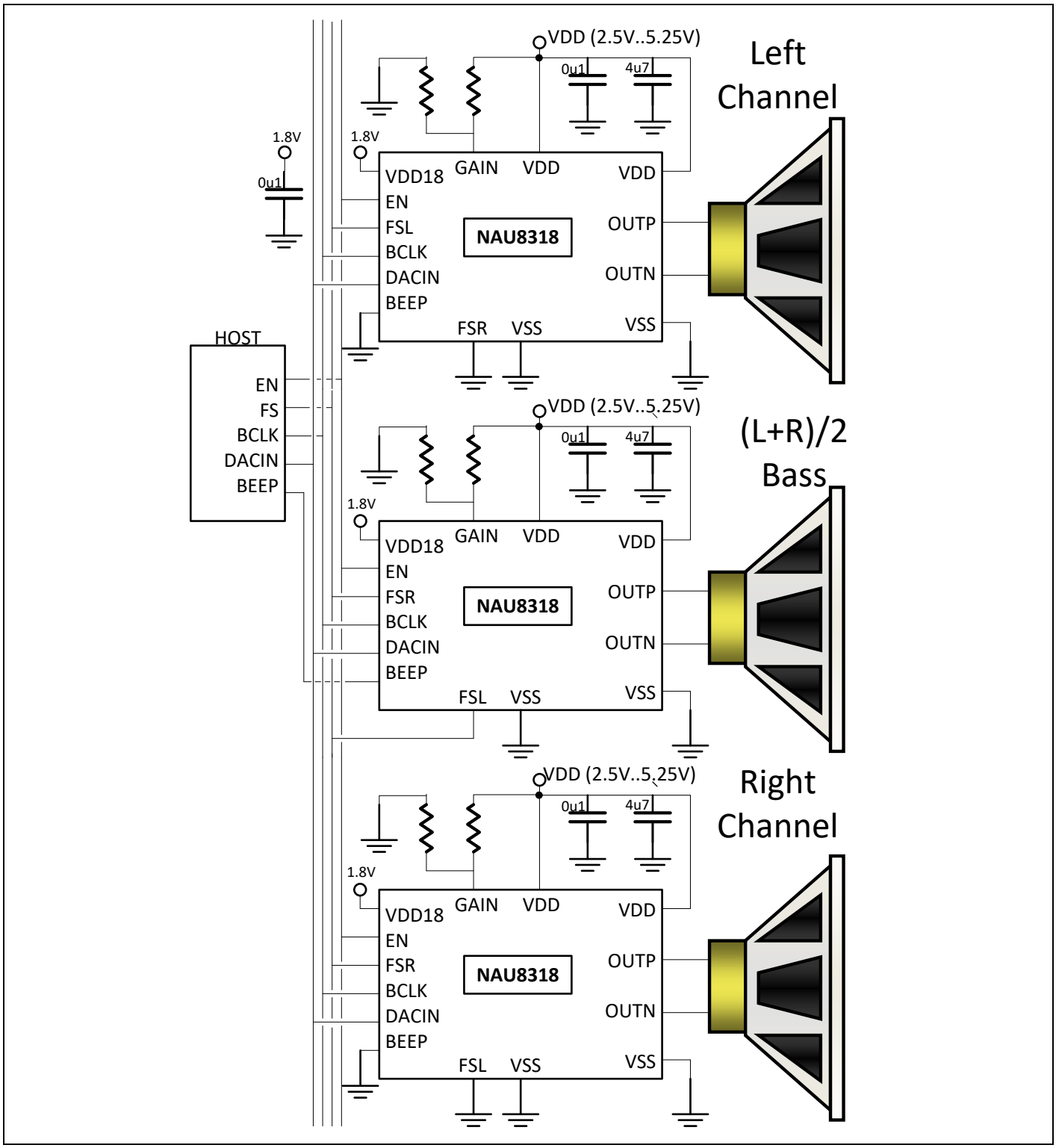


Figure 4 NAU8318 System Diagram for 2.1 sound

6 BLOCK DIAGRAM

A Block Diagram for the NAU8318 is provided in **Figure 5**.

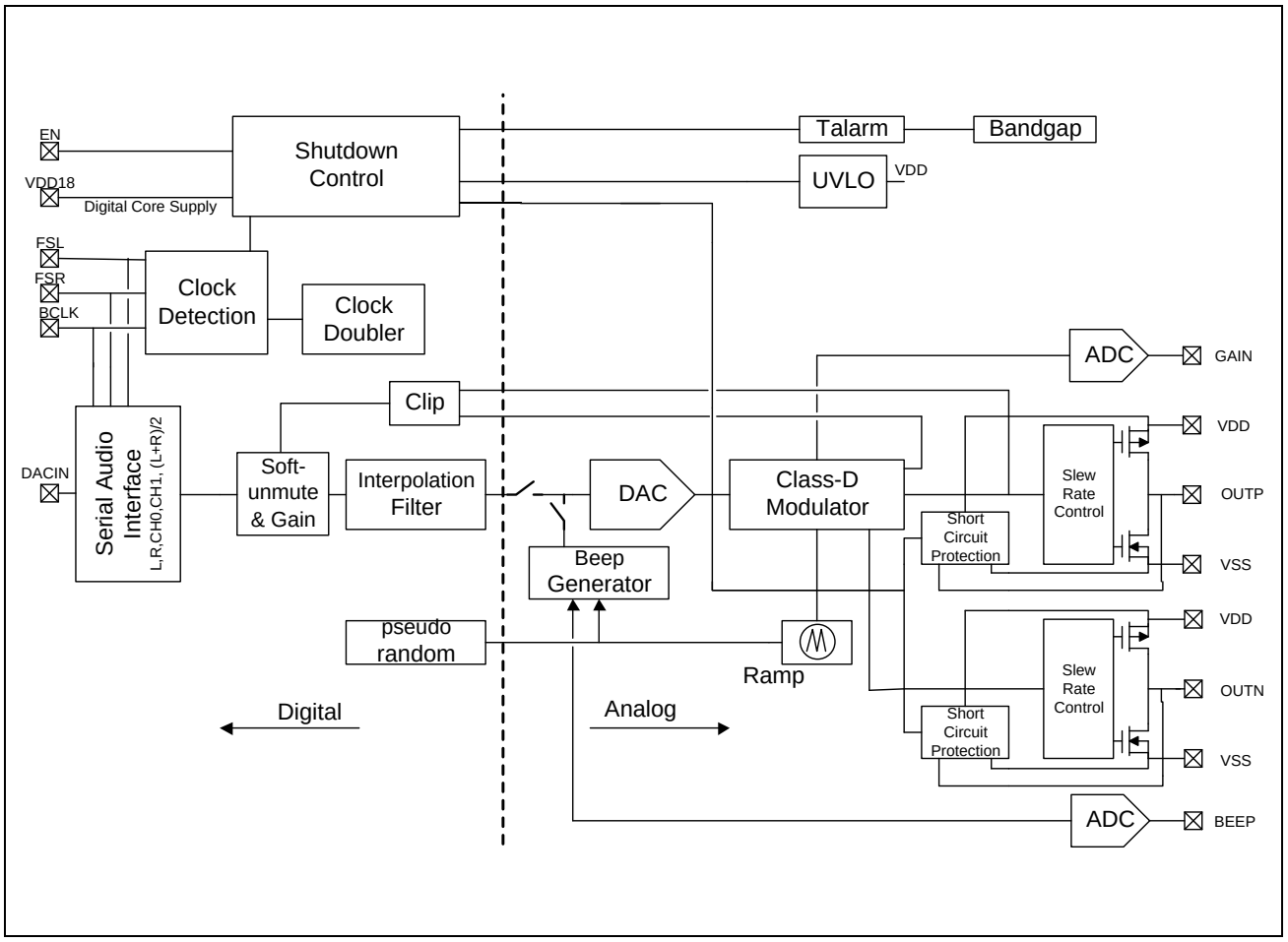


Figure 5 NAU8318 Block Diagram

7 Electrical Characteristics

The tables in this chapter provide the various electrical parameters for the NAU8318 and their values.

7.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
VDD Battery Supply Range	-0.3	6.0	V
VDD18 Digital Supply Voltage	-0.3	2.2	V
Voltage Input I/O Range	VSS - 0.3	VDD + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

7.2 Operating Conditions

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Battery Supply Range	VDD	2.50	4.2	5.25	V
Digital Supply Voltage	VDD18	1.71	1.8	1.89	V
Digital IO Range		1.8		VDD	
Ground	VSS		0		V
Industrial Operating Temperature		-40		+85	°C

7.3 Electrical Parameters

Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, gain=12dB, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units
ISD	Shutdown Supply Current	VDD, all clocks off, EN=0	0.04	16	µA
ISD18	Shutdown Supply Current	VDD18, all clocks off, EN=0	0.5	16	µA
ISB	Standby Mode Supply Current	VDD, clocks off, EN from 0 to VDD	0.16		µA
ISB18	Standby Mode Supply Current	VDD18, clocks off, EN from 0 to VDD	18		µA
IDD	Operating Mode Supply Current	VDD, idle Channel	1.85		mA
IDD18	Operating Mode Supply Current	VDD18, idle Channel	0.9		mA

Symbol	Parameter	Conditions	Typical	Limit	Units
		Class-D Channel			
P_O	Output Power	VDD=4.2V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **QFN-20**	0.98		W
		VDD=4.2V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **WLCSP14**	1.0		W
		VDD=5V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB, **QFN-20**	1.73		W
		VDD=5V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB, **WLCSP-14**	1.8		W
		VDD=4.2V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **QFN-20**	1.69		W
		VDD=4.2V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **WLCSP-14**	1.76		W
		VDD=5V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB, **QFN-20**	3.03		W
		VDD=5V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB, **WLCSP-14**	3.2		W
THD+N	Total Harmonic Distortion + Noise	R_L = 8 Ω + 33 µH, f=1kHz, P_O = 60m W, Gain=12dB	0.009		%
e_{OS}	Output Noise	A-Weighted, 20Hz-20kHz, no DAC input signal	9		µVrms
PSRR	Power Supply Rejection Ratio (Note 1)	DC, VDD = 3.2V – 4.2V, amplifier voltage GAIN = 6dB	82		dB
		f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 100mV_{P_P} amplifier voltage GAIN = 6dB	80	60	dB
		f_{RIPPLE} = 4kHz, V_{RIPPLE} = 100mV_{P_P} amplifier voltage GAIN = 6dB	77		dB
Fres	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, R_L = 8 Ω + 33 µH	+0.2/ -0.06		dB
V_{OS}	Output Offset Voltage	Idle Channel, Gain= 6dB	±1	±5	mV

Symbol	Parameter	Conditions	Typical	Limit	Units
Kpop	Pop and Click Noise	A-weighted, Idle DAC input, toggling clocks on/off, Gain= 6dB	0.026		mVrms
		A-weighted, Idle DAC input, toggling EN pin with clocks running, Gain= 6dB	0.019		mVrms
Fsw	Switching Frequency	Average (Note2)	450	600	kHz
Fbeep	BEEP Frequency	Average	440	+/-25%	Hz
Class-D					
Neff	Power Efficiency	Output Power = 1.4W, VDD = 4.2 V	91		%

***Note 1** : PSRR = 20 x LOG10(GAIN x ΔVDD/Δ(SPKP-SPKN)) dB, using -100dBFs activation signal*

***Note 2** : Random cycle to cycle oscillator jitter of up to about +/-5% will result in variable cycle to cycle PWM period results. This random oscillator jitter reduces EMI at fixed out of band frequencies.*

7.4 Digital Input Parameters

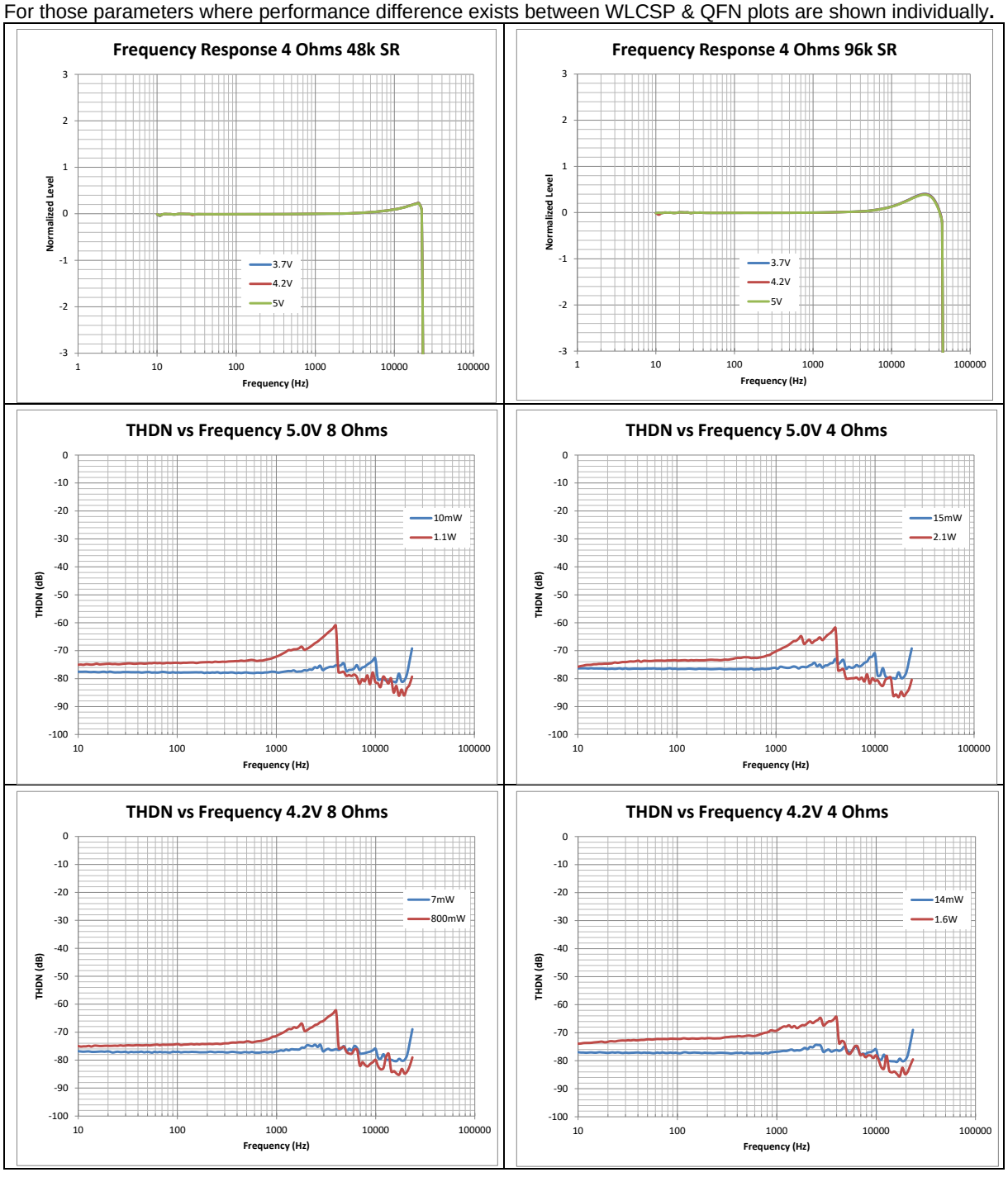
Digital Inputs FS, BCLK, DACIN & EN.

Parameter	Symbol	Comments/Conditions	Min	Max	Units
Input LOW level	V_{IL}	VDD = 2.5V – 5.25V		0.4	V
Input HIGH level	V_{IH}	VDD = 2.5V – 5.25V	1.3*		V
Input Leakage Current	I_{IL}	VDD = 2.5V – 5.25V	-0.001	+0.001	mA

Note: I2S signals can be driven from external 1.8V GPIO's

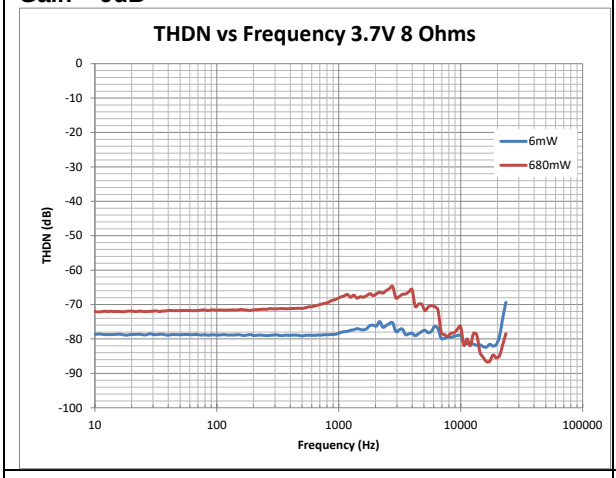
7.5 Typical Operating Plots

Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified. Note that both 4 Ohm & 8 Ohm loads include 33 µH inductance in series. For those parameters where performance difference exists between WLCSP & QFN plots are shown individually.

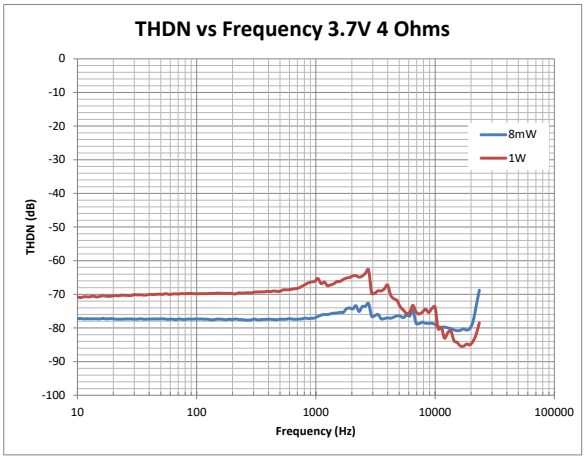


Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified**.** Note that both 4 Ohm & 8 Ohm loads include 33 µH inductance in series. For those parameters where performance difference exists between WLCSP & QFN plots are shown individually.

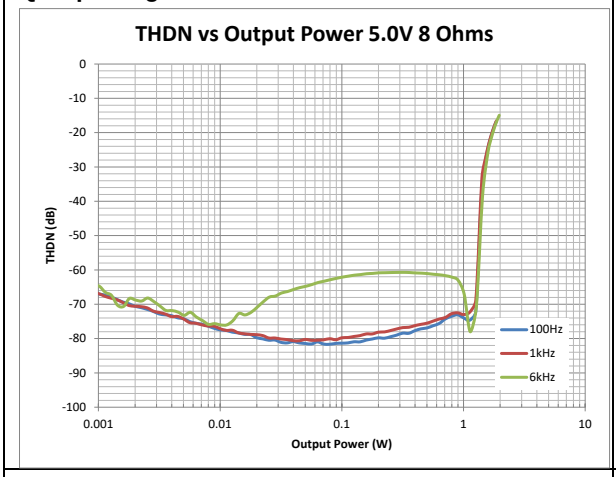
Gain = 9dB



Gain=9dB



QFN package



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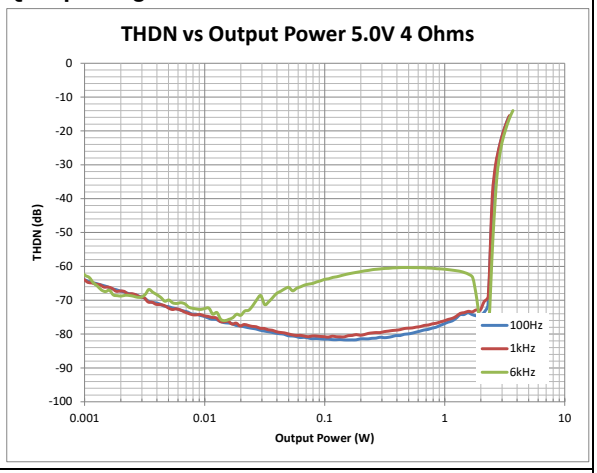
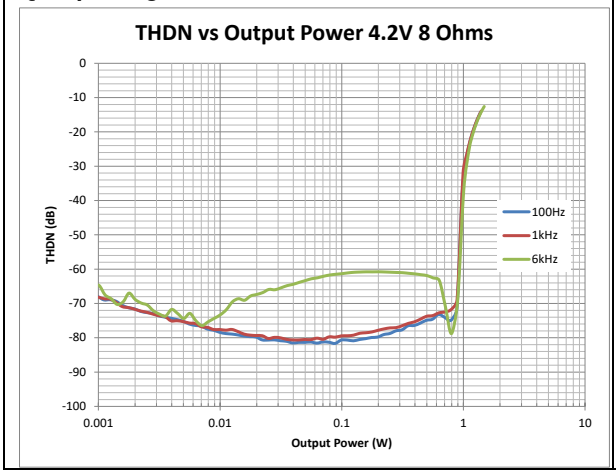
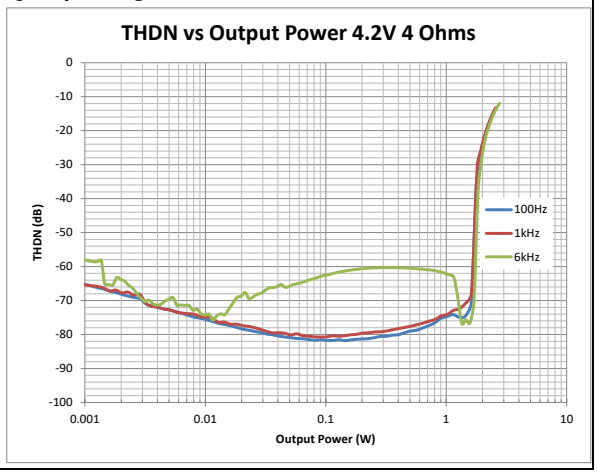


QFN package

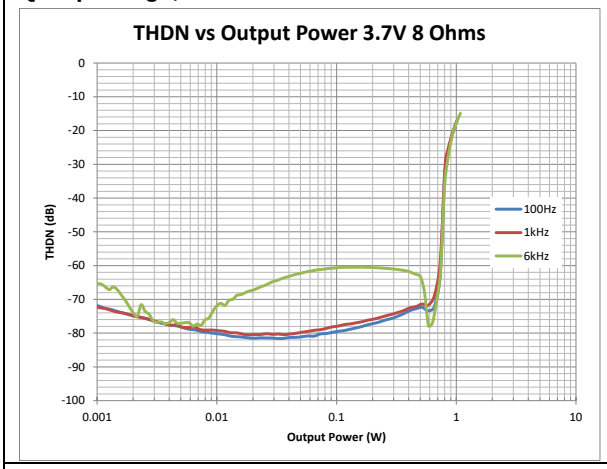


QFN package

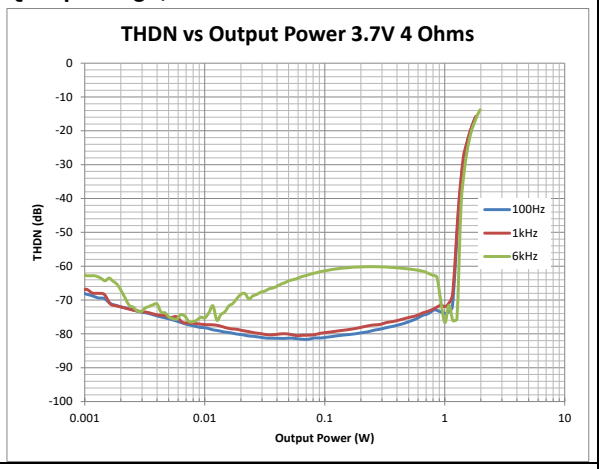


Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified**.** Note that both 4 Ohm & 8 Ohm loads include 33 µH inductance in series. For those parameters where performance difference exists between WLCSP & QFN plots are shown individually

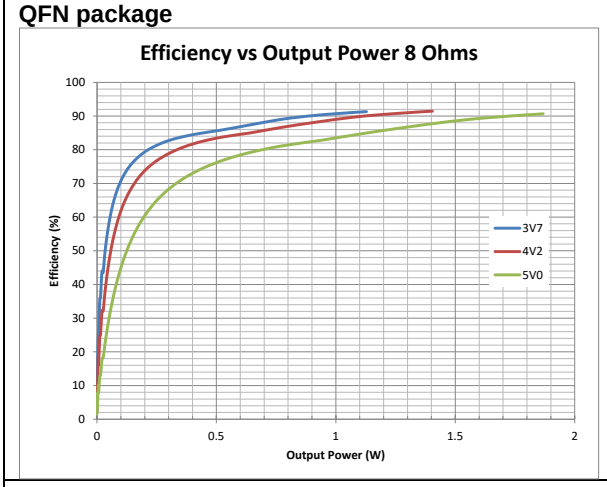
QFN package, Gain=9dB



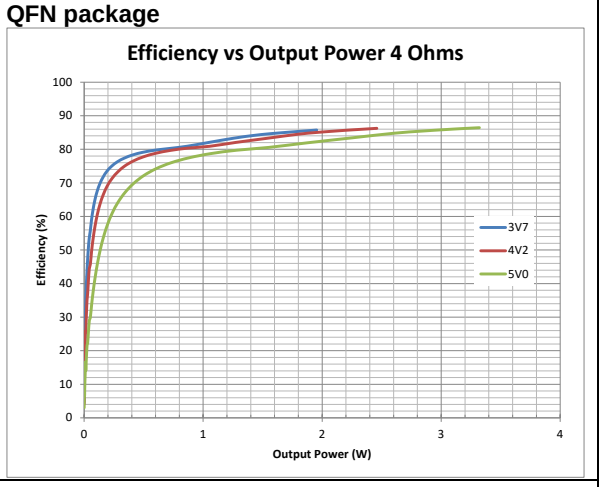
QFN package, Gain=9dB



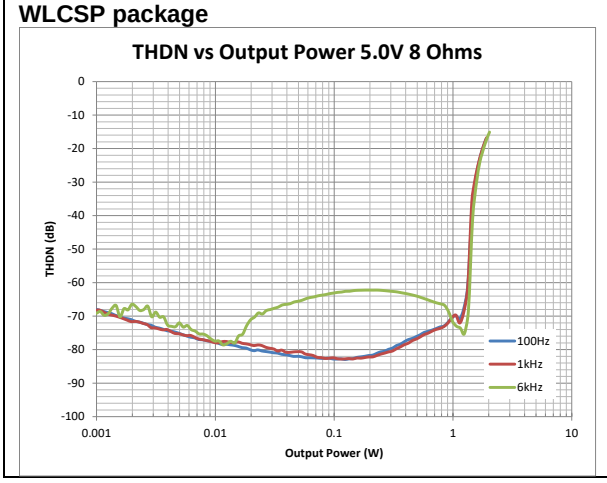
QFN package



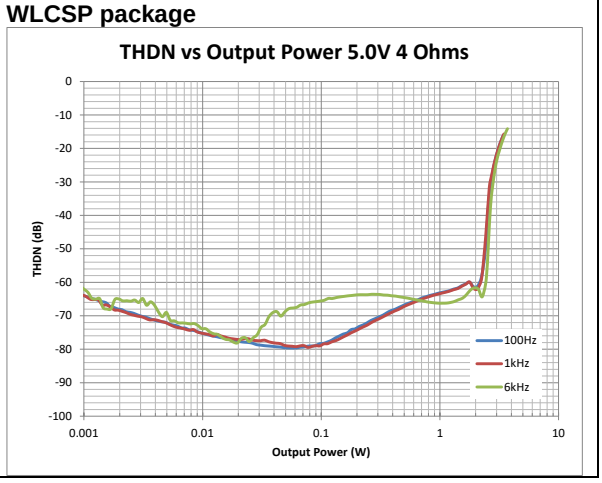
QFN package



WLCSP package

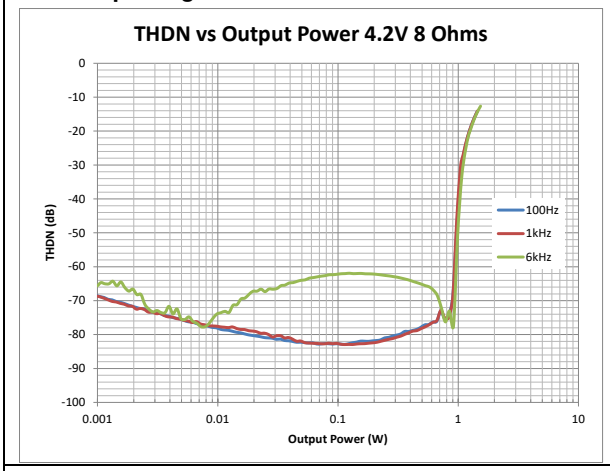


WLCSP package

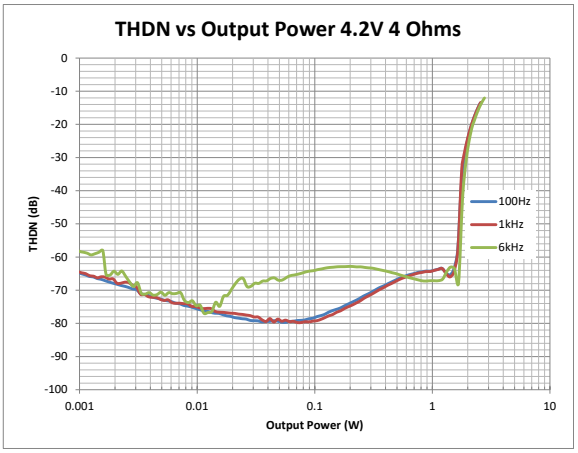


Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified**.** Note that both 4 Ohm & 8 Ohm loads include 33 µH inductance in series. For those parameters where performance difference exists between WLCSP & QFN plots are shown individually.

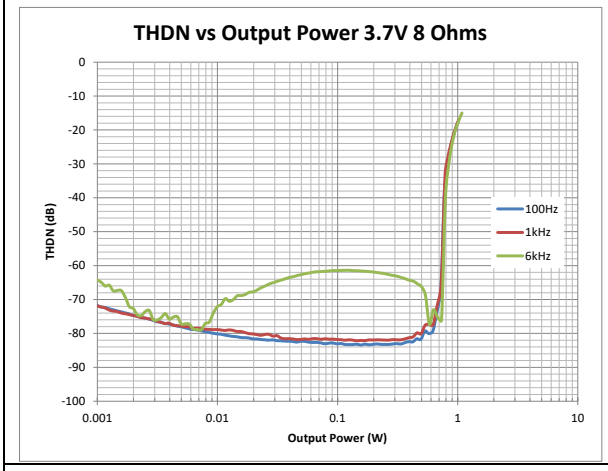
WLCSP package



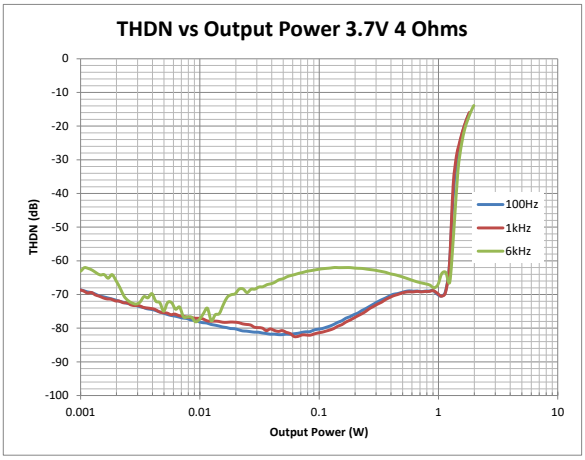
WLCSP package



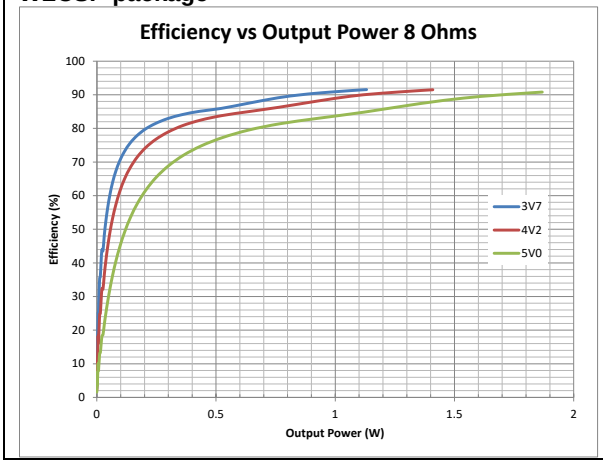
WLCSP package, Gain = 9dB



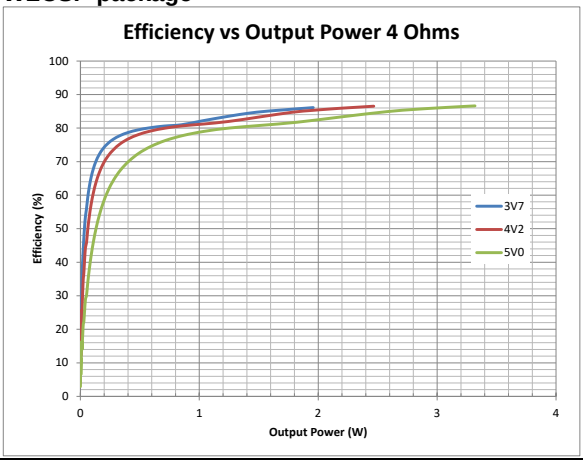
WLCSP package, Gain = 9dB



WLCSP package



WLCSP package



8 FUNCTIONAL DESCRIPTION

This chapter provides detailed descriptions of the major functions of the NAU8318 Amplifier.

8.1 Inputs

The NAU8318 provides digital inputs to acquire and process audio signals with high fidelity and flexibility. The audio input path is from an I2S/PCM Interface, using the FSL, FSR, BCLK & DACIN pins.

The device is enabled by setting the EN pin high and is disabled by setting EN to 0V. The EN, FSL, FSR, BCLK & DACIN pins all have a low input threshold voltage to allow for operation from a host with low IO supply voltage.

The GAIN input pin is a special input pin, which essentially is an ADC input. The ADC tied to this pin has 5 decision levels and can therefore select 5 modes of operation each.

The GAIN input pin can be configured as shown in the table below. The GAIN set represents the signal voltage gain of the differential DAC outputs to the differential modulator outputs or speaker outputs. The differential DAC full scale reference is 1.75Vpk.

Table 2 GAIN Configurations for the NAU8318

Gain Mode #	Interface Mode #	GAIN (dB) MODE	-6dBFs Output (Vpk)	GAIN Pin Configuration
1	2,3,4	9	2.455	GAIN pin tied to VSS
2	10 - 14	12	3.435	GAIN pin tied to VSS
3	2 - 9	3	1.240	GAIN pin tied to VSS through 100 kOhm +/- 5% resistor
4	2 - 9	12	3.435	GAIN pin tied to VDD
5	2 – 9	Max. 12 CLIP ALC	3.435 (no clipping)	GAIN pin tied to VDD through 100 kOhm +/- 5% resistor
6	2 - 9	6	1.750	GAIN pin floating

The GAIN input ADC converts the input levels set by the external pin configuration and internal voltage dividers into a digital representation that sets the internal GAIN mode. There are a total of 6 modes having different gains as shown above. Gain mode 5 also enables the CLIP detection ALC, which then allows the gain to be reduced automatically as the supply voltage decreases. Gain Mode #1 & #2 use the same GAIN pin configuration, but the gain setting is determined by the Interface Mode (see interface mode table). When using time slots 4 through 7 in PCM timeslot mode, the GAIN pin has to be tied to VSS and the GAIN is fixed to 12dB. When using time slots 0 through 3 in PCM timeslot mode all gain settings except for 9dB are available. In the I2S interface modes all gain modes are available.

The BEEP input pin is another special input pin which essentially is also an ADC input. The ADC tied to this pin has 5 decision levels and can therefore select 5 modes of operation including disabled and 4 specific levels of the BEEP generator output square wave.

The BEEP input pin can be configured as shown in the table below. In order for the BEEP generator to be enabled, the EN pin needs to be set high. The BEEP Mode set represents the BEEP signal voltage gain of the differential DAC outputs to the differential modulator outputs or speaker outputs. The differential DAC full scale reference is 1.75Vpk. Depending on the GAIN setting of 3,6,9 & 12 dB corresponding to 1.41x, 2x, 2.82x & 4x respectively, the peak output level can be calculated using the table below.

Table 3 Beep Configurations for the NAU8318

Beep Mode #	BEEP Pin Configuration (EN=1)	BEEP Peak Output Level (Vpk)
1	BEEP pin tied to VSS	disabled
2	BEEP pin tied to VSS through 100 kOhm +/- 5% resistor	0.656 x GAIN
3	BEEP pin tied to VDD18	0.547 x GAIN
4	BEEP pin tied to VDD18 through 100 kOhm +/- 5% resistor	0.438 x GAIN
5	BEEP pin floating	0.328 x GAIN

The BEEP input ADC converts the input levels set by the external pin configuration and internal voltage dividers into a digital representation that sets the internal BEEP mode. There are a total of 5 modes having different output levels as shown above. Beep mode 1 disables the BEEP.

For instance, if an Open Drain output is used, the BEEP pin configuration is switched between Mode 1 (disabled) & Mode 5. If the GAIN is set to 12dB, then the output level will be 1.313Vpk, resulting in a 0.22 Watt square wave output power into an 8 Ohm speaker and 0.43 Watt square wave output power in a 4 Ohm speaker. Note that for a square wave the peak and rms levels are identical.

The BEEP pin selections can be controlled through a tri-state GPIO by the host controller. The following diagrams show how this is accomplished. When BEEP is pulled low the Beeper is disabled for all configurations. To enable it using a GPIO with complete software control, the BEEP pin is either forced high, floating or tied to an resistor to VDD18 or VSS by setting the controller GPIO either high or to tri-state. For applications with GPIO's allowing only Open Drain software on/off control, the BEEP modes can be configured using the external resistor population options.

IMPORTANT NOTE: For Open Drain BEEP Mode #3 additional supply current is consumed when EN=VDD18 and BEEP=VSS. For this Mode of approximately 180uA of additional current is consumed by the pull up resistor.

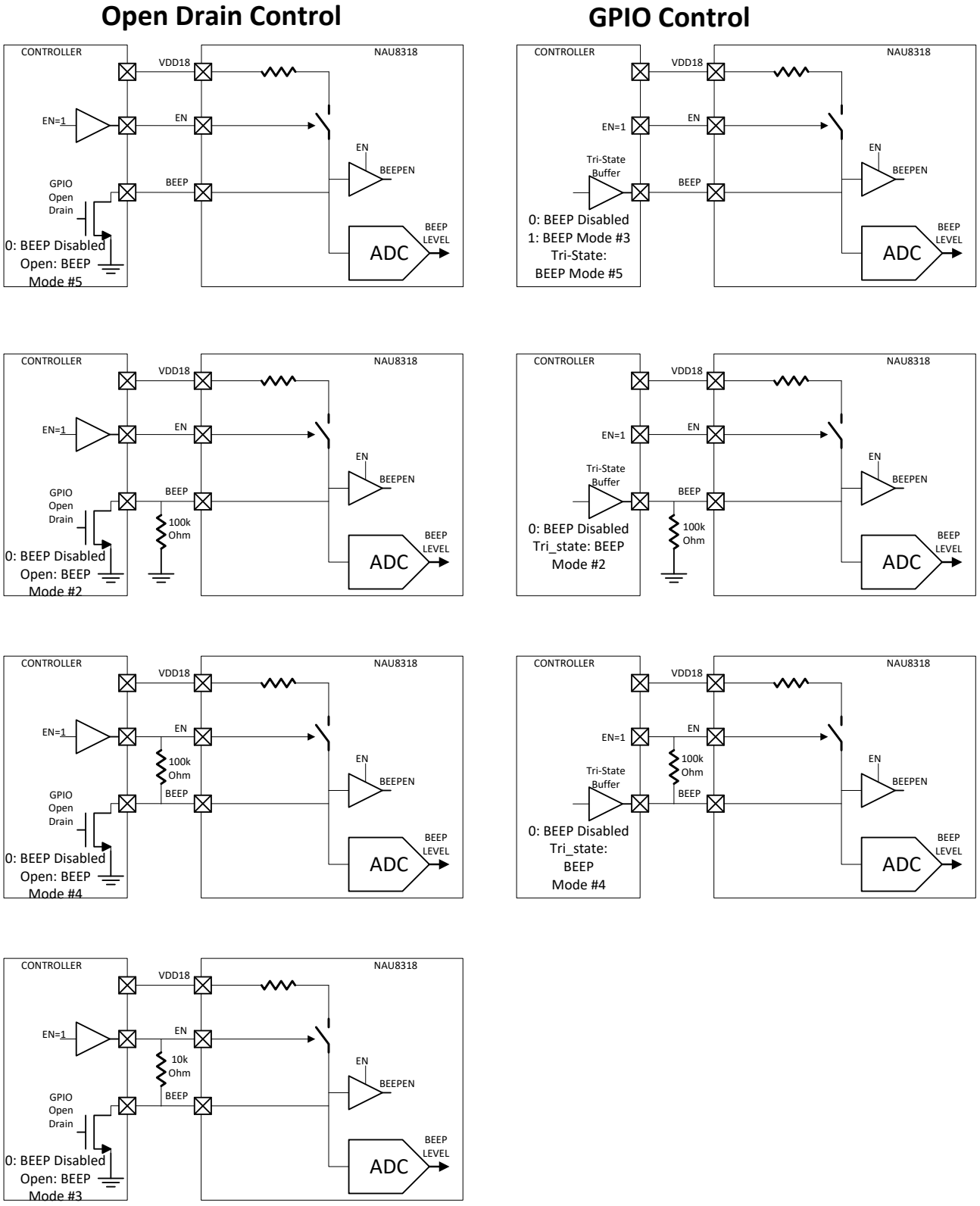


Figure 6 BEEP Pin Configurations & Settings

The figure below shows the system level timing used to enable the beeper from power up. Note that Tdb1 can be as low as 0 seconds.Tdb2 is used to make sure the output returns to 0 before disabling the NAU8318 drivers at the end of the beep.

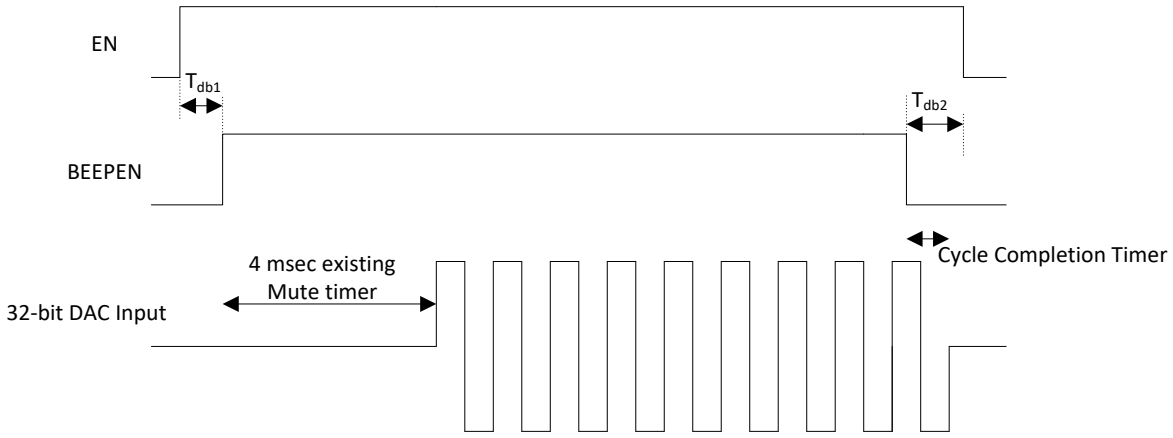


Figure 7 BEEP Timing upon power up

The figure below shows the system level timing used to enable the beeper during operation. Tdb2 is used again to make sure the output returns to 0 before disabling the NAU8318 drivers at the end of the beep.

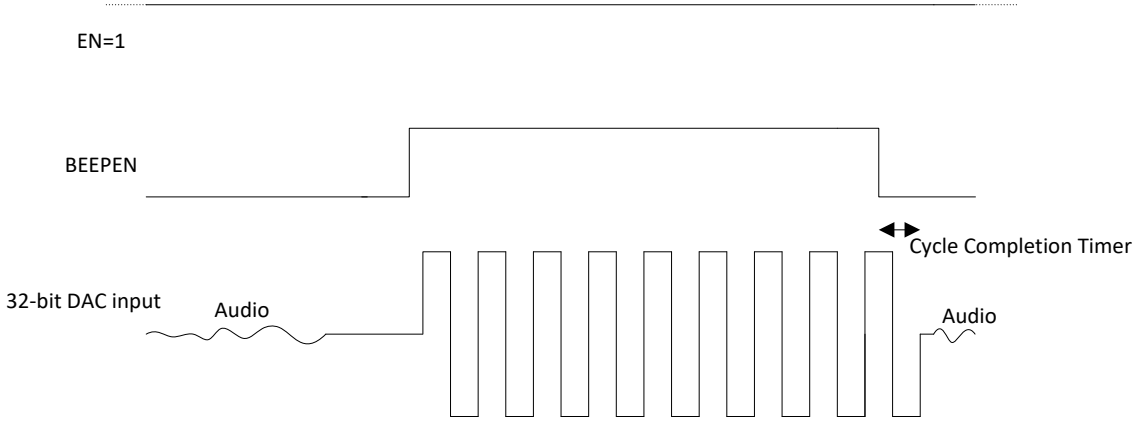


Figure 8 BEEP Timing during operation

The FSR & FSL input pins are used to set the I2S and PCM interface modes. The table below shows the modes supported.

Table 4 Audio Interface Configurations for the NAU8318

Interface Mode #	Gain Mode #	Interface MODE	FSL Pin Configuration	FSR Pin Configuration
1	NA	Power Down or Standby	tied to VDD or VSS	tied to VDD or VSS
2	NA	Left Channel I2S	Toggling with valid BCLK/FSL ratio and FSL is high for more than 2 BCLK rising edges	tied to VDD or VSS
3	NA	Right Channel I2S	tied to VDD or VSS	Toggling with valid BCLK/FSR ratio and FSR is high for more than 2 BCLK rising edges
4	NA	I2S (L+R)/2	Toggling with valid BCLK/FSL ratio and FSL is high for more than 2 BCLK rising edges. FSL & FSR signals are the same.	Toggling with valid BCLK/FSR ratio and FSR is high for more than 2 BCLK rising edges. FSL & FSR signals are the same.
5	3-6	16 or 32 bit PCM Timeslot 0	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges	tied to VSS
6	3-6	16 or 32 bit PCM Timeslot 1	tied to VSS	Toggling with valid BCLK/FSL ratio and FSR is high for less than 2 BCLK rising edges
7	3-6	16 or 32 bit PCM Timeslot 2	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges	tied to VDD
8	3-6	16 or 32 bit PCM Timeslot 3	tied to VDD	Toggling with valid BCLK/FSL ratio and FSR is high for less than 2 BCLK rising edges
9	3-6	16 or 32 bit PCM (Timeslot0+Timeslot1)/2	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges. FSL & FSR signals are the same.	Toggling with valid BCLK/FSL ratio and FSR is high for less than 2 BCLK rising edges. FSL & FSR signals are the same.
10	2	16 or 32 bit PCM Timeslot 4	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges	tied to VSS
11	2	16 or 32 bit PCM Timeslot 5	tied to VSS	Toggling with valid BCLK/FSL ratio and FSR is high for less than 2 BCLK rising edges
12	2	16 or 32 bit PCM Timeslot 6	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges	tied to VDD

Interface Mode #	Gain Mode #	Interface MODE	FSL Pin Configuration	FSR Pin Configuration
13	2	16 or 32 bit PCM Timeslot 7	tied to VDD	Toggling with valid BCLK/FSL ratio and FSR is high for less than 2 BCLK rising edges
14	2	16 or 32 bit PCM (Timeslot4+Timeslot5)/2	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges. FSL & FSR signals are the same.	Toggling with valid BCLK/FSL ratio and FSR is high for less than 2 BCLK rising edges. FSL & FSR signals are the same.

I2S data is 24-bit by default. For the PCM Timeslot interface modes the host can sent 16 bit or 32 bit data. Therefore, for the PCM Timeslot Interface Mode the BCLK frequency is either Fbclk = Ffs x 32 x 8 = 256 x Ffs or Fbclk = Ffs x 16 x 8 = 128 x Ffs.

8.2 Outputs

The NAU8318 Mono Class-D PWM Amplifier has a gain range from 3dB to 12dB, and is powered by a separate power supply VDD, which can go up to 5V. This amplifier is capable of delivering up to 3.2W into a 4Ω load with a 5V supply.

8.3 Digital Interfaces

Audio data is passed to the device through a serial data interface compatible with industry standard I2S and PCM devices, using the FSL, FSR, BCLK & DACIN pins. The NAU8318 has no serial interface for control input. Operating modes are defined by the external pin configurations.

8.4 Power Supply

This NAU8318 has been designed to operate reliably under a wide range of power supply conditions and Power-On/Power-Off sequences. However, the Electro Static Detection (ESD) protection diodes between the supplies and the IO pins impact the application. Please refer to the absolute maximum ratings and operating conditions to determine the safe operating range.

8.5 Power-On-and-Off Reset

The NAU8318 includes a Power-On-and-Off Reset circuit on-chip. The circuit resets the internal logic control at VDD supply power-up and this reset function is automatically generated internally when power supply is too low for reliable operation. Typical reset thresholds are **1.9** V for VDD during a power-on ramp, and **1.65** V for VDD during a power-down ramp. It should be noted that these values are much lower than the required voltage for normal operation of the chip. In addition VDD18 resets the internal logic. Typical reset thresholds are **1.25** V for VDD18 during a power-on ramp, and **0.93** V for VDD18 during a power-down ramp.

The reset is held ON while the power level for VDD is below the threshold. Once the power level rises above the threshold, the reset is released. Once the reset is released, the device will respond to control from external inputs.

An additional internal RC filter-based circuit is added which helps the circuit to respond for fast ramp rates (~3 µsec) and to generate the desired reset period width (~3 µsec at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50 nsec.

In addition setting the enable pin ‘EN’ low will reset the internal logic.

8.6 Power Up & Down Sequence

A diagram of the typical power up sequence is shown in the figure below. At first, the power supply is ramped up. Note that the VDD18 & VDD supplies can be powered up independently. The VDD supply is powered up before the logic IO signals are applied.

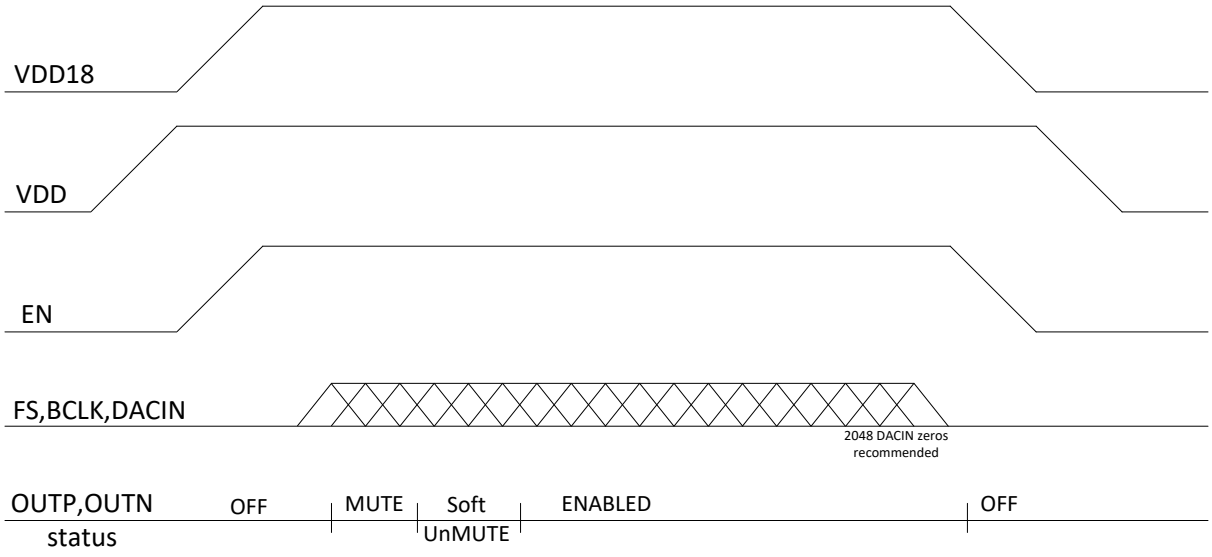


Figure 9 NAU8318 Power Up & Down Sequence

Once the supply is powered up, the enable pin ‘EN’ can be set high in order to set the device in standby state. Note that the ‘EN’ pin can also ramp up the same time as the supply voltage. During the standby state the outputs OUTN & OUTP are still off. After enabling VDD & EN ,the BCLK detection circuit is activated. External clocks and data can be applied right away if needed. Once the FS & BCLK are applied the clock detection module will validate the BCLK/FS ratio and set the internal clock dividers. When a valid BCLK/FS ratio is detected and the clock dividers are set, a 2.7 millisecond mute

period is enabled during which all circuits are powered up and the DAC digital volume control is in the muted state. The mute period is followed by a soft-unmute, which gradually increases the DAC digital volume to full scale. After this event the signal path is fully active and the outputs are fully enabled. At the end of playback it is recommended to add 2048 zero samples to the DACIN input for a pop-less shutdown. When either one or both of the FS & BCLK clocks is stopped the clock detection circuit will power down the device. The detection time depends on the clock frequency used, but is approximately 50usec when BCLK is stopped. Once detected, the output drivers will shut down.

8.7 Clocking and Sample Rates

The internal clocks for the NAU8318 are derived from the external BCLK clock source. This master system clock can set directly by the BCLK input or it can be generated from a clock multiplier using the BCLK as a reference.

8.7.1 Clock Control and Detection

The NAU8318 includes a Clock Detection circuit that is used to enable and disable the audio paths. The actual power up/down is gated by the clock detection circuit. The block diagram of the clock detection circuit is shown in **Figure 10**.

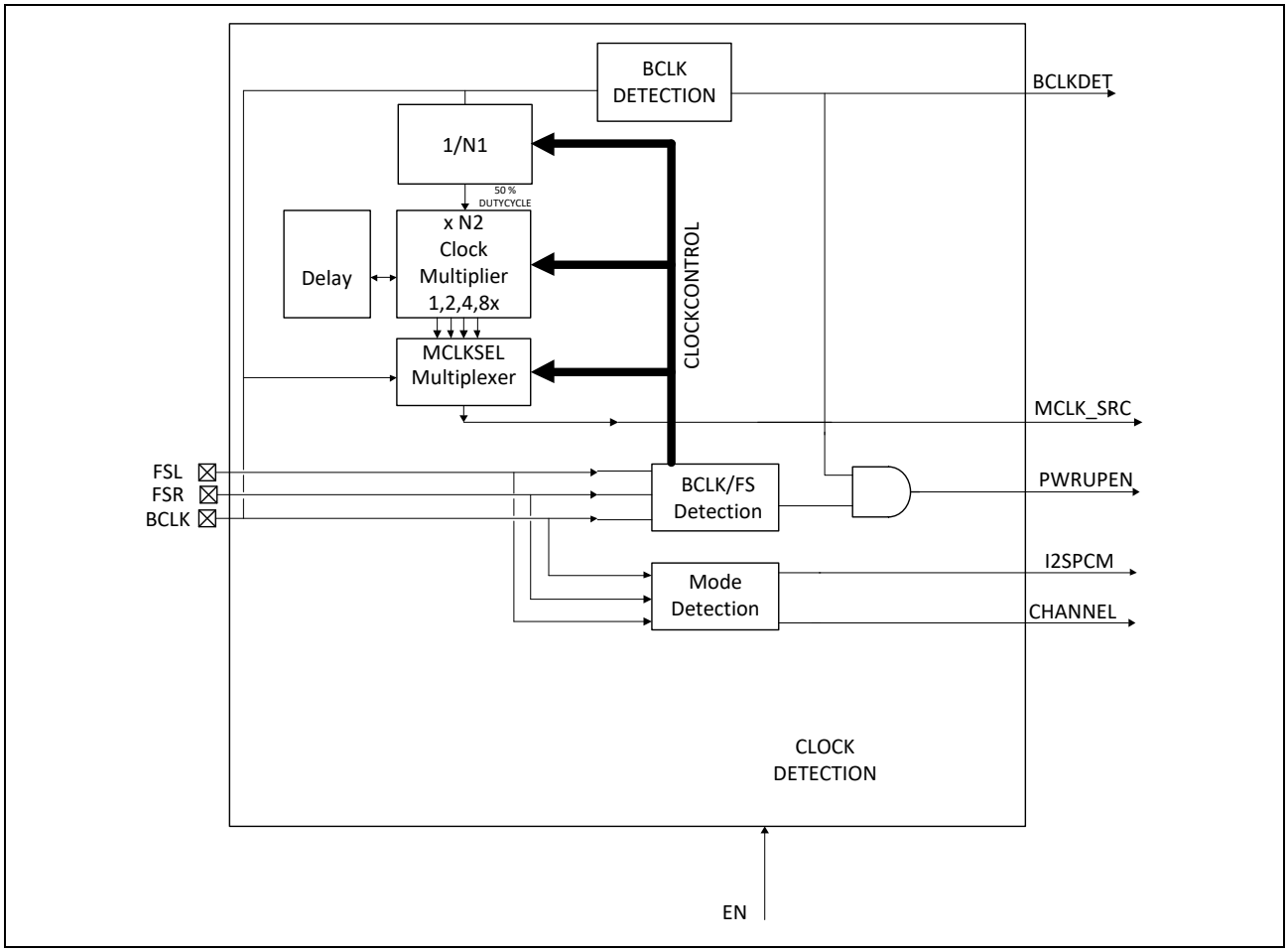


Figure 10 NAU8318 Clock Detection Circuit

Clock Detection by the NAU8318 uses the BCLK FSL, FSR and EN to control the internal PWRUPEN signal and set the clock divider ratios.

8.7.2 Automatic Power Control and Mute.

Clock detection and automatic power control in the NAU8318 is enabled by meeting two conditions, depending on the configuration. If all conditions are met, the PWRUPEN signal will be asserted to 1. If any of the conditions are not met, the PWRUPEN signal is set to 0.

The conditions for generating the PWRUPEN signal are:

1) The NAU8318 has custom logic clock detection circuits that detect if BCLK is present. Upon BCLK detection, the detector output BCLKDET goes to 1. When the BCLK disappears, BCLKDET goes back to 0. Up to 1 µsec is required to detect BCLK and the BCLK release time is about 50 µsec.
2) The clock detection logic also needs to detect the ratio BCLK /FS of 32, 50, 64, 100, 128, 200, 256, 400, 500.

The PWRUPEN signal is capable of controlling all the analog power consuming blocks.

A Mode Detection circuit also determines one of the I2S/PCM operating mode and channel (as shown in Table 3) once a valid BCLK/FS ratio is detected.

When PWRUPEN goes high an internal sequence is triggered to bring up analog functions. This includes an analog MUTE to allow stabilization of internal analog blocks, followed by a soft unmute of the DAC. The analog MUTE time is 2.7ms. The soft unmute then ramps the gain 512 MCLK_SRC periods per gain step. For the 512 setting, the soft unmute takes 256 * 512 * Tmclk_src seconds to reach 0dB (10ms for 12.288MHz MCLK_SRC). This ensures pop free startup of the amplifier. An example of this startup is shown in figure below triggering on the start of BCLK and showing the filtered OUTP signal.

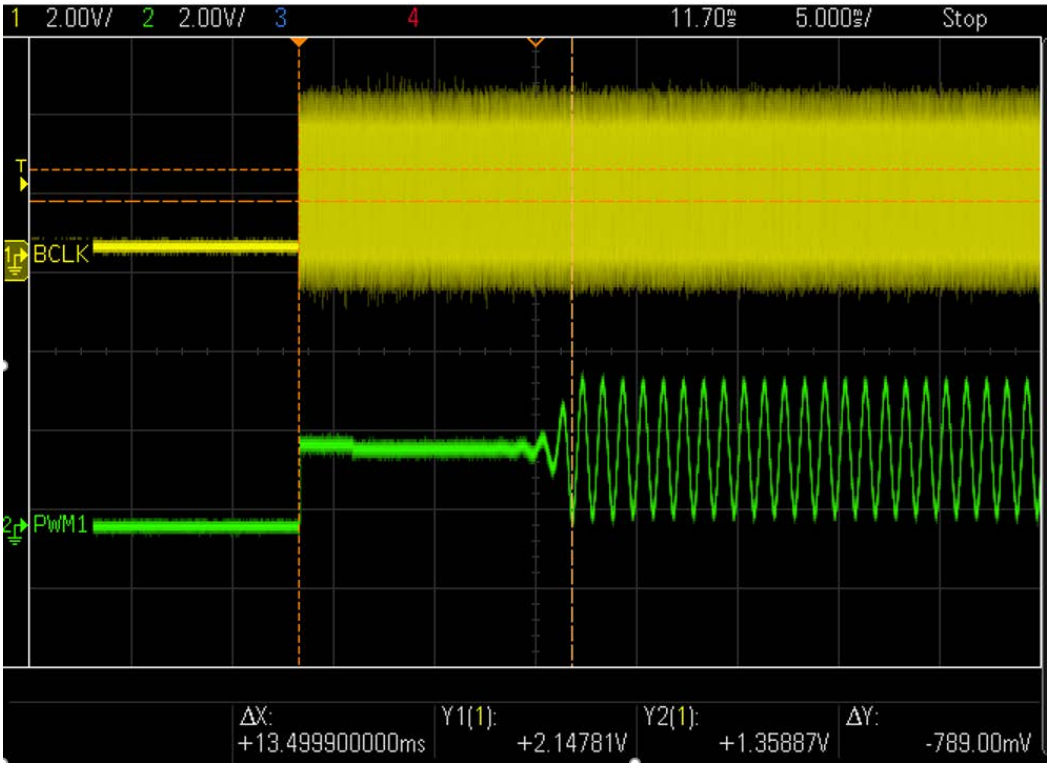


Figure 11 PWRUPEN startup sequence.

Before reaching the DAC the incoming PCM signal is processed by a digital signal path. To ensure complete flushing and transient free audio of this path it is recommended that 2048 zero samples are sent to the device before stopping clocks. The DAC soft unmute function is also beneficial for eliminating any audio transients from audio path

8.7.3 Input Clock Rates

The range of the input clocks is shown in **Table 5**.

Table 5 Range of Input Clocks

Signal	Min	Max
Frame Synch (FS) (kHz)	8	96
Bit Clock BCLK (MHz)	0.256	38.400

8.7.4 Sample and Over Sampling Rates

Possible BCLK/FS ratios are shown in **Table 6** and **Table 7**. Table 4 shows the relation between the BCLK/FS ratio and the internal OSR and MCLK_SRC/FS ratio. The divider and multiplier N1 & N2 are set accordingly by the clock detection logic. Table 7 shows the possible FS & BCLK ranges for each BCLK/FS ratio.

Table 6 BCLK/FS ratios and Over Sampling Rates

BCLK/FS ratio	Lower Decision Threshold	Upper Decision Threshold	MCLK_SRC/BCLK	MCLK_SRC/FS	OSR	DAC_CLK/BCLK
32	31	33	8	256	64	2
50	49	51	8	400	100	2
64	63	65	4	256	64	1
100	99	101	4	400	100	1
128	127	129	2	256	64	0.5
200	199	201	2	400	100	0.5
256	255	257	1	256	64	0.25
400	399	401	1	400	100	0.25
500	499	501	1	500	100	0.2

For PCM Time Slot Mode, the only possible BCLK/FS ratios are 128 or 256.

Table 7 Ranges of Sampling Frequencies and BCLK Rates

	Fs (Hz)							
BCLK/FS	8000	16000	24000	32000	44100	48000	88200	96000
ratio								
	BCLK(Hz)							
32	256000	512000	768000	1024000	1411200	1536000	2822400	3072000
50	400000	800000	1200000	1600000	2205000	2400000	4410000	4800000
64	512000	1024000	1536000	2048000	2822400	3072000	5644800	6144000
100	800000	1600000	2400000	3200000	4410000	4800000	8820000	9600000
128	1024000	2048000	3072000	4096000	5644800	6144000	11289600	12288000
200	1600000	3200000	4800000	6400000	8820000	9600000	17640000	19200000
256	2048000	4096000	6144000	8192000	11289600	12288000	22579200	24576000
400	3200000	6400000	9600000	12800000	17640000	19200000	35280000	38400000
500	4000000	8000000	12000000	16000000	22050000	24000000	NA	NA

For BCLK/FS ratios of 32 & 50 a low jitter BCLK source with accurate duty cycle must be used.

8.8 Automatic Level Control

The digital Automatic Level Control (ALC) function supports the DAC digital audio path of the NAU8318. It can be enabled as by setting the GAIN pin to 12dB gain with ALC. This function can be used to manage the gain to optimize the signal level at the output of the Class-D Amplifier by automatically amplifying input signals that are too small or automatically decreasing the amplitude signals that are too loud. The ALC is designed such that it adjusts the output level in order to prevent clipping. This may be use-full in battery operated applications, where the battery supply voltage decreases as the battery discharges. At lower supply voltages the outputs will more likely clip at higher output levels. In such case, the ALC would decrease the output level just below the clipping level and maintain high quality sound as well as decreasing the peak power drain from the battery.

The Figure below illustrates the relationship of the ALC to other major functions of the NAU8318.

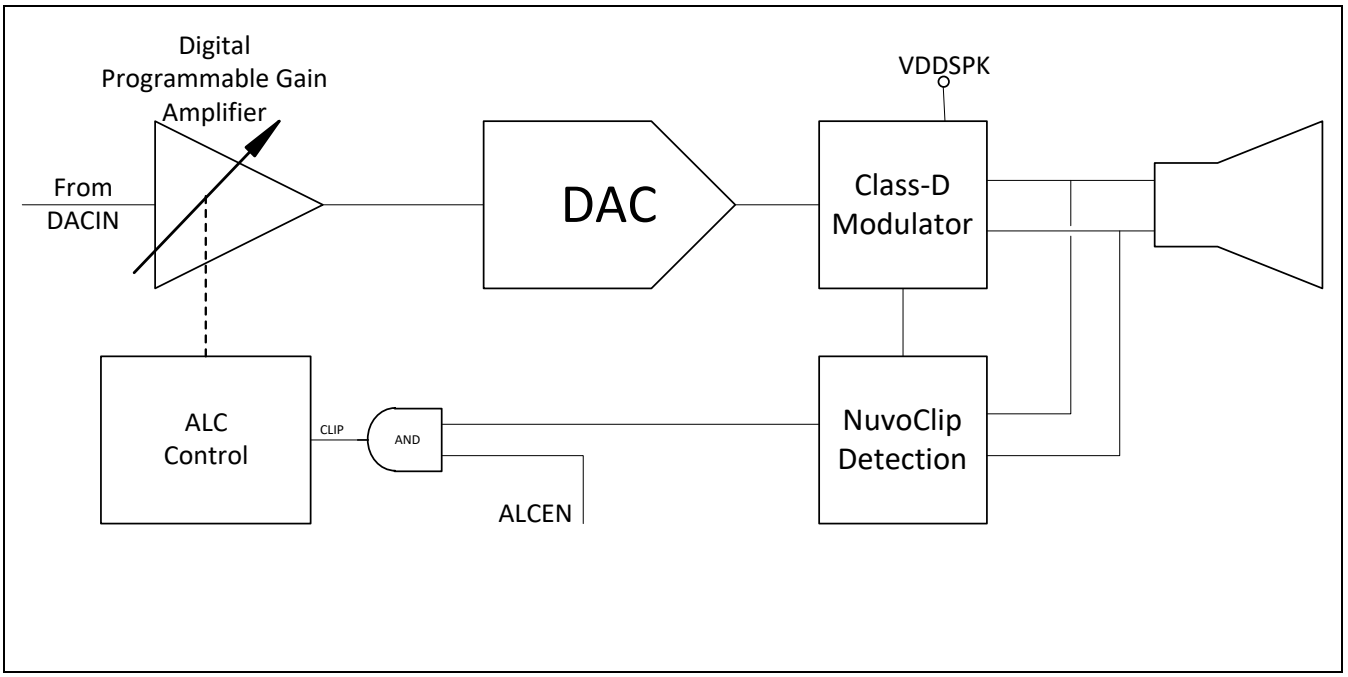


Figure 12 ALC Control Loop Block Diagram

8.8.1 ALC Operation

A clip detection signal is provided by the clip detection circuit as soon as the input signal is clipping at its peak levels. The ALC block then ramps down the gain at the pre-programmed ALC Attack Time rate. This continues until the clipping detection no longer detects a clipping signal or until the maximum gain decrement per clipping event is reached. When the clipping is no longer occurring, the ALC gain is held for the hold time. The ALC gain is then ramped up to the target following the pre-programmed ALC Release Time rate

8.8.2 ALC Parameter Definitions

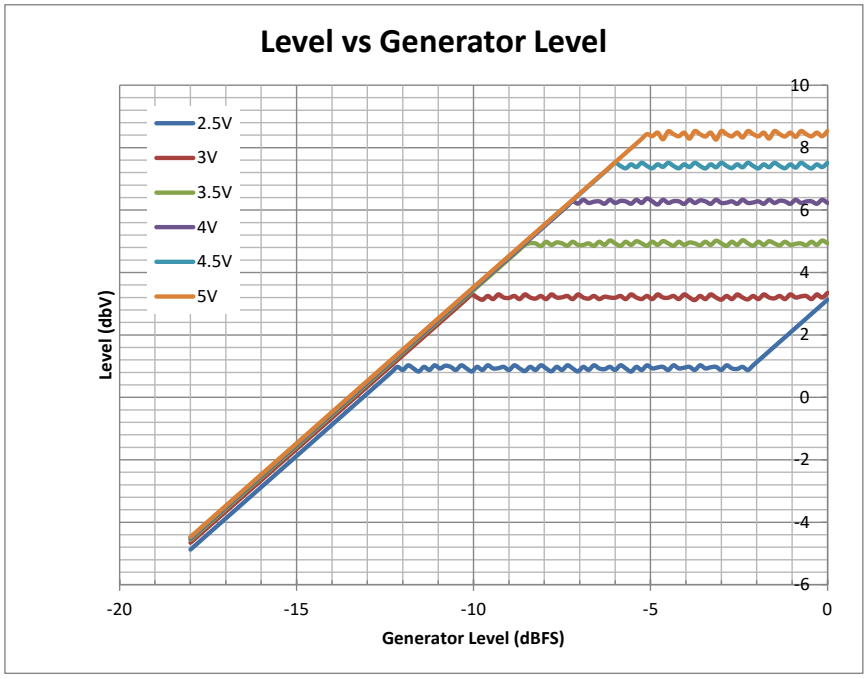
ALC Minimum Gain (ALCMIN): This sets the minimum allowed gain during all modes of ALC operation. This is useful to keep the ALC operating range close to the desired range for a given application scenario.

ALC Attack Time (ALCATK): Attack time refers to how quickly a system responds to a clipping event. Typically, attack time is much faster than decay time.

ALC Decay Time (ALCDCY): Decay time refers to how quickly a system responds after the hold time. Typically, decay time is much slower than attack time. When no more clipping events occur, the gain will increase at a rate determined by this parameter.

ALC Hold Time (ALCHLD): Hold time refers to the duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU8318, the hold time value is the duration from the last clipping event before there is an actual gain increase during the decay time.

CLIP_GAINADJUST sets the maximum gain decrease per clipping event. During a clipping even the gain decreases by 0.250dB (1-1/64) per attack time step until the clipping event no longer occurs or the maximum gain reduction limit set in CLIP_GAINADJUST has been reached or the ALC Minimum Gain is reached.



ALC Response at Various Supply Levels

8.9 Device Protection

The NAU8318 includes the following types of device protection:

- Over Current Protection (OCP)
- Under Voltage Lock Out (UVLO)
- Over Temperature Protection (OTP)
- Clock Termination Protection (CTP)

Over Current Protection is provided in the NAU8318. If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 14µs, the output drivers will be disabled for 67ms. The output drivers will then be re-enabled and checked for a short circuit again. If the short circuit is still present for another 14µs, the cycle will repeat until the short circuit has been fixed. The short circuit threshold is set at 2.1A with a full scale input signal and the threshold is reduced for lower input signals.

Under Voltage Lock Out (UVLO) provides Supply Under Voltage Protection in the NAU8318 If the VDD drops under 2.1V, the output drivers are disabled, however, the NAU8318 control circuitry will still operate. This is useful to help avoid the battery supply voltage dropping before the host processor can safely shutdown the devices on the system. If the VDD drops below 1.61V, the internal power-on-reset will activate and put the class-D driver in power down state.

Over Temperature Protection (OTP) is provided in the event of thermal overload. When the device internal junction temperature reaches 143°C, the NAU8318 will disable the output drivers. Once the device cools down to a safe operating temperature (123°C) for at least 100us, the output drivers will be re-enabled.

Clock Termination Protection (CTP) is provided in the NAU8318. If the FS and/or BCLK clock stops running, the NAU8318 automatically shuts down the Class-D driver and therefore prevents DC voltages to remain at the outputs.

8.10 Power-up and Power-Down Control

When the supply voltage ramps up, the internal power on reset circuit is triggered. At this time, all internal circuits will be set to the power-down state. The device can be enabled by setting EN to VDD and starting the clocks. Upon starting the clocks, the device will go through an internal power-up sequence in order to minimize ‘pops’ on the speaker output. While Audio will be audible within 10msec, the complete power-up sequence requires about 12.66 msec at 48kHz. The device will typically power down in about 22 µsec, when the clocks are stopped.

NOTE: It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize ‘pops’ when the clocks are stopped.

8.11 Bypass Capacitors

Bypass capacitors are required to remove the AC ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 2 x 4.7 µF and 0.1 µF are sufficient to achieve good performance.

8.12 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. It is better to use low-resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

8.12.1 PCB Layout Notes

The Class-D Amplifier is a high power switching circuits that can cause Electro Magnetic Interference (EMI) when poorly connected. Therefore, care must be taken to design the PCB eliminate Electro Magnetic Interference (EMI), reduce IR drops, and maximize heat dissipation.

The following notes are provided to assist product design and enhance product performance:

- Use a VSS plane, preferably on both sides, to shield clocks and reduce EMI
- Maximize the copper to the VSS pins and have solid connections to the plane
- Planes on VDD are optional
- The VDD connection needs to be a solid piece of copper
- Use thick copper options on the supply layers if cost permits
- Keep the speaker connections short and thick. Do not use VIAs
- Use a small speaker connector like a wire terminal block (Phoenix Contact)
- For better heat dissipation, use VIAs to conduct heat to the other side of the PCB
- Do not use VIA's to connect OUTP & OUTN. Use a direct top layer copper connection to the pins. Thick copper is preferred.
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane
- The digital IO lines can be shielded between power planes

8.13 Filters

The NAU8318 is designed for use without any filter on the output line. However, the NAU8318 may be used with or without various types of filters, depending on the needs of the application.

8.13.1 Class D without Filters

The NAU8318 is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filter-less design is suitable for portable applications where the speaker is very close to the amplifier. In other words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. **Figure 13** illustrates this simple configuration.

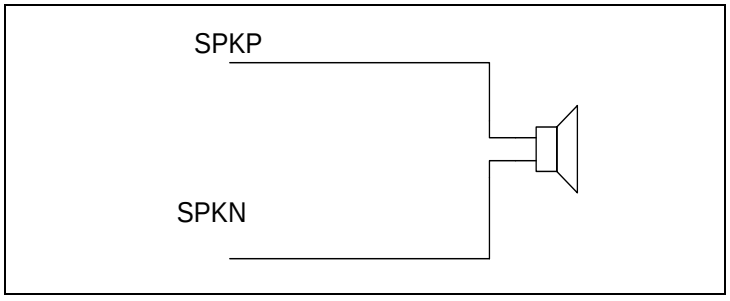


Figure 13 NAU8318 Speaker Connections without Filter

8.13.2 Class D with Filters

In some applications, shorter trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, long traces will cause EMI issues. Several types of filter circuits are available to reduce the EMI effects. These are Ferrite Bead Filters, LC filters, Low-Pass LCR Filters, and High-Pass Filters.

Ferrite Bead Filters are used to reduce high-frequency emissions. The characteristic of a Ferrite Bead Filter is such that it offers higher impedance at high frequencies. For better EMI performance, select a Ferrite Bead Filter which offers the highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. The typical circuit diagram using a Ferrite Bead Filter for each output to the speaker is shown **Figure 14**.

NOTE: Usually, the ferrite beads have low impedance in the audio range, so they will act as pass-through filters in the audio frequency range.

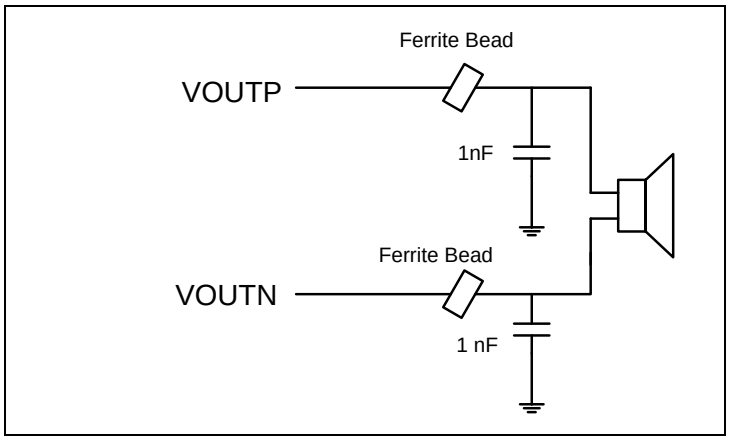


Figure 14 NAU8318 Speaker Connections with Ferrite Bead Filters

LC Filters are used to suppress low-frequency emissions. The diagram in **Figure 15** shows the NAU8318 outputs connected to the speaker with an LC Filter circuit. R_L is the resistance of the speaker coil.

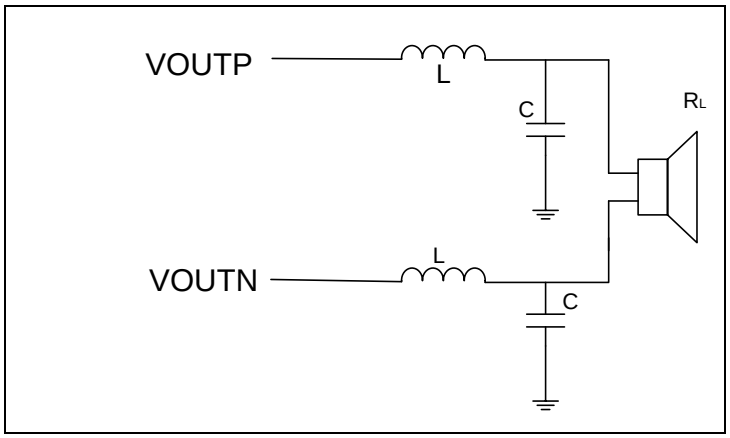


Figure 15 NAU8318 Speaker Connections with LC Filters

Low-Pass LCR Filters may also be useful in some applications where long traces or wires to the speakers are used. **Figure 16** shows the speaker connections using standard Low-Pass LCR Filters.

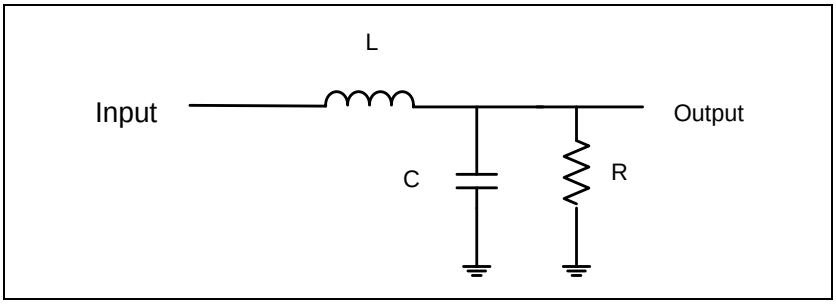


Figure 16 NAU8318 Speaker Connections with Low-Pass Filters

The following equations apply for critically damped ($\zeta = 0.707$) standard Low-Pass LCR Filters:

$$2\pi fc = \frac{1}{\sqrt{(LC)}} \qquad fc \text{ is the cut-off frequency}$$

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

NOTE: The L and C values for differential configuration can be calculated by duplicating the single-ended configuration values and substituting RL = 2R.

NOTE: The ferrite beads and inductors used in the external filters may exhibit non-linear behavior that can attribute to a degradation in THDN performance parameters.

9 Control

The NAU8318 Audio Interface is set to default I2S and PCM time slot modes as described in the FSL & FSR operating mode table. Other modes may be feasible through metal mask option changes upon special request.

9.1 Digital Audio Interface

The NAU8318 is an I2S or PCM Timeslot slave device. In I2S Slave Mode, an external controller supplies BCLK (bit clock) and the frame synchronization or FS signal. Data is latched on the rising edge of BCLK.

The NAU8318 reads 24 bit I2S data on DACIN. For the BCLK/FS rate of 32, only the 16 MSB bits are read.

9.1.1 I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Left Channel data is received; when FS is HIGH, Right Channel data is received. This can be seen in **Figure 17.**

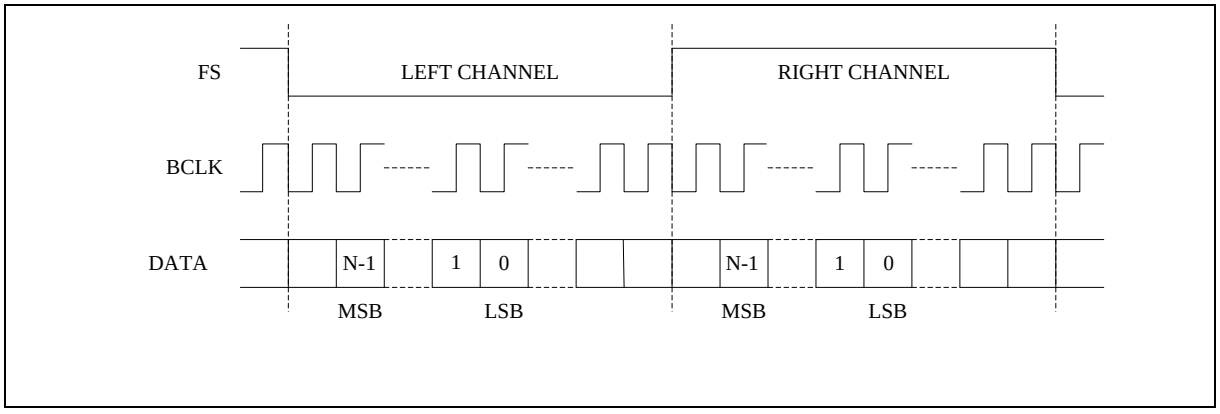


Figure 17 I2S Audio Data

9.1.2 PCM Time Slot Audio Data

PCM Time Slot Mode is used to share Audio data on the same interface. This can be useful when multiple NAU8318 chips or other devices share the same audio bus. NAU8318 supports 8 channels or time slots with 16 or 32 bits each. Therefore, the BCLK/FS ratio has to be set to either 128 or 256 to allow for detection of the channel length.

Normally, the DAC data is clocked immediately after the Frame Sync (FS); however, in PCM Time Slot Mode, the audio data can be delayed to a specific channel or time slot. These channels or time slots can be seen in **Figure 18**.

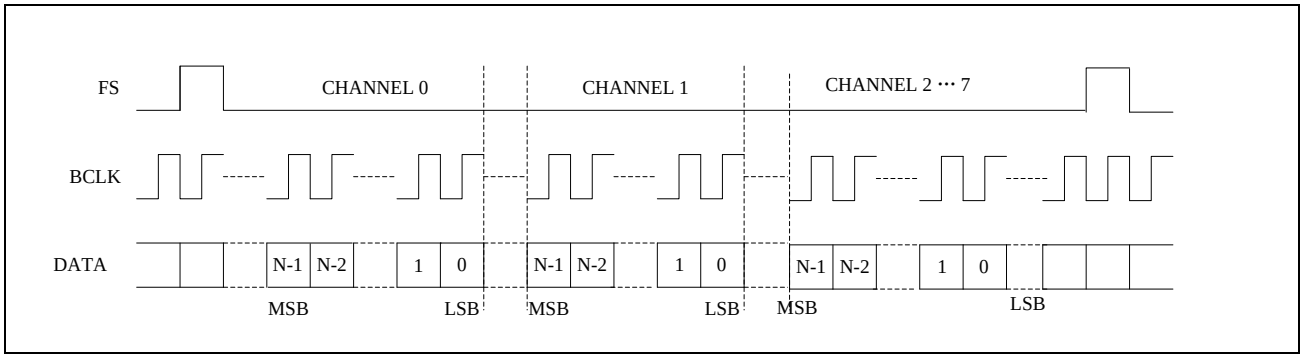


Figure 18 PCM Time Slot Audio Data

9.2 Digital Audio Interface Timing Diagrams

9.2.1 I2S Audio Interface

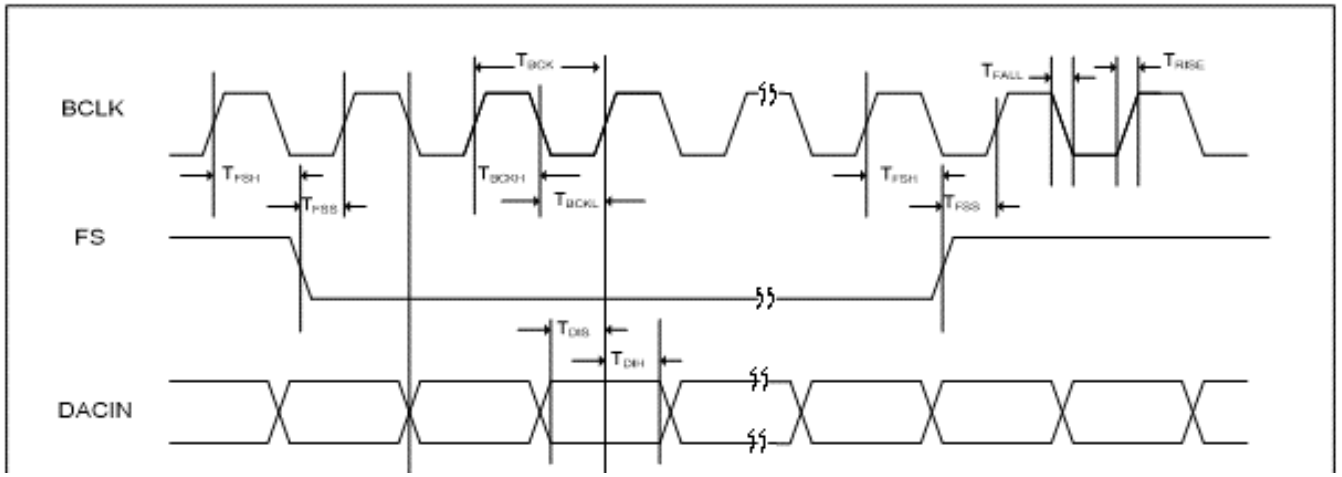


Figure 19 I2S Audio Interface

9.2.2 PCM Audio

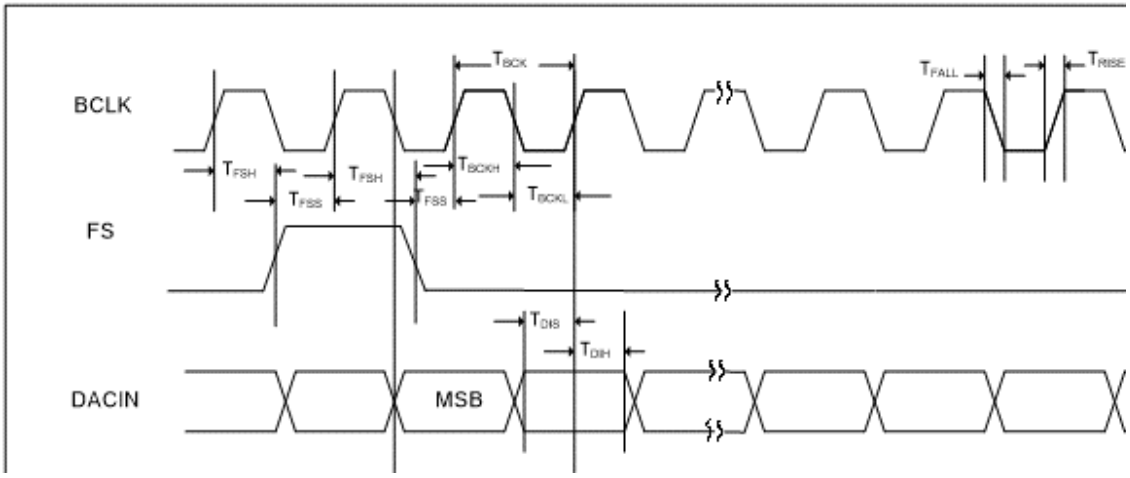


Figure 20 PCM Audio Interface

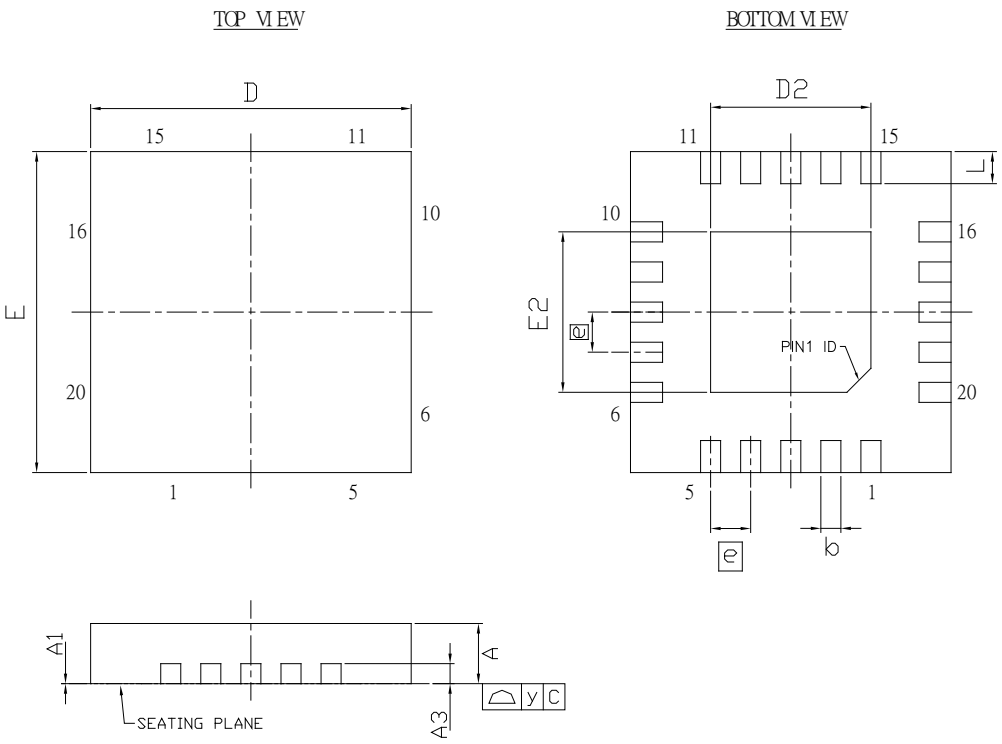
Table 8 Digital Audio Interface Timing Parameter

VDD 2.5 - 5.25V

Description	Symbol	Min	Typ	Max	Unit
BCLK Cycle Time	T_{BCK}	26	---	---	ns
BCLK High Pulse Width	T_{BCKH}	12	---	---	ns
BCLK Low Pulse Width	T_{BCKL}	12	---	---	ns
Fs to BCLK Rising Edge Setup Time	T_{FSS}	20	---	---	ns
BCLK Rising Edge to Fs Hold Time	T_{FSH}	10	---	---	ns
Rise Time for All Audio Interface Signals	T_{RISE}	---	---	20	ns
Fall Time for All Audio Interface Signals	T_{FALL}	---	---	20	ns
BCLK Rising Edge to DACIN Hold Time	T_{DIH}	10	---	---	ns

10 Package Specification

The NAU8318 Mono Class-D Amplifier is available in a small, 20 pin QFN package, using 0.5 mm pitch, as shown below.



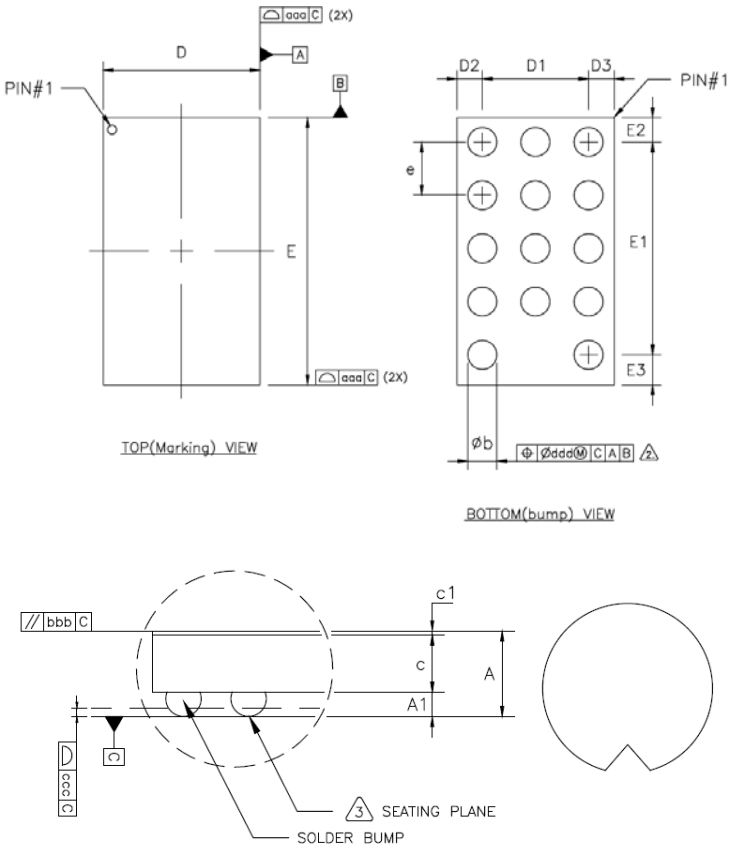
Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note:D2,E2 by die size difference .

NAU8318 20 pin QFN Package Specification

The NAU8318 Mono Class-D Amplifier is also available in a small, 14 Ball WLCSP package, using 0.4 mm pitch, as shown below.



Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.4829	0.5260	0.5691	0.0190	0.0207	0.0224
A1	0.1359	0.1510	0.1661	0.0054	0.0059	0.0065
c1	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
c	0.3250	0.3500	0.3750	0.0128	0.0138	0.0148
D	1.1500	1.1800	1.2100	0.0453	0.0465	0.0476
E	1.9800	2.0100	2.0400	0.0780	0.0791	0.0803
b	0.1845	0.2170	0.2496	0.0073	0.0085	0.0098
D1	---	0.8000	---	---	0.0315	---
D2	---	0.1900	---	---	0.0075	---
D3	---	0.1900	---	---	0.0075	---
E1	---	1.6000	---	---	0.0630	---
E2	---	0.1850	---	---	0.0073	---
E3	---	0.2250	---	---	0.0089	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.0300	---	---	0.0012	---
bbb	---	0.0600	---	---	0.0024	---
ccc	---	0.0500	---	---	0.0020	---
ddd	---	0.0150	---	---	0.0006	---

NAU8318 14 Ball WLCSP Package Specification

11 ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU8318YG	4mm x 4mm	QFN-20	Green
NAU8318VG	2.06mm x 1.18mm	WLCSP-14	Green

NAU8318 _ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-20

V = WLCSP-14

12 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	May 25, 2022	Initial Release
1.1	May 27, 2022	Update Shutdown Power, clarify BEEP level calculation, add PSRR test condition & update results, update ISB18 standby current, update efficiency charts, update timing parameters, formatting updates
1.2	Jul 24, 2022	Update WLCSP14 ordering number to NAU8318VG
1.3	Aug 1, 2022	Formatting updates and formal release
1.4	Sep 7, 2022	Update WLCSP14 package information
1.5	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description

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