

2048-BIT BIPOLAR RAM (256 × 8)**8X350 (T.S.)**

www.DataSheet4U.com

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X300 based system. Internal circuitry is provided for direct use in 8X300 applications. When used with the 8X300, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-state outputs.

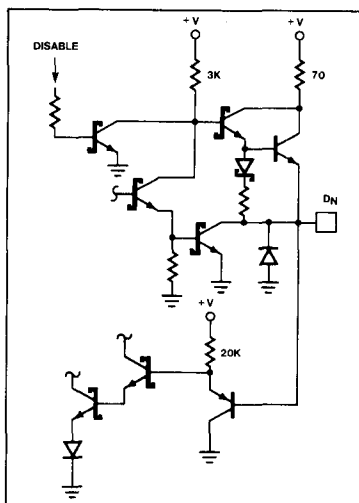
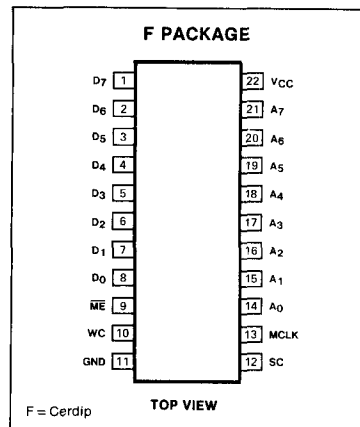
The 8X350 is available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N8X350-F, and for the military temperature range (-55°C to +125°C) specify S8X350-F.

FEATURES

- On-chip address latches
- 3-state outputs
- Schottky clamped TTL
- Internal control logic for 8X300 system
- Directly interfaces with the 8X300 bipolar microprocessor with no external logic
- May be used on left or right bank

APPLICATIONS

- 8X300 or 8X305 working storage

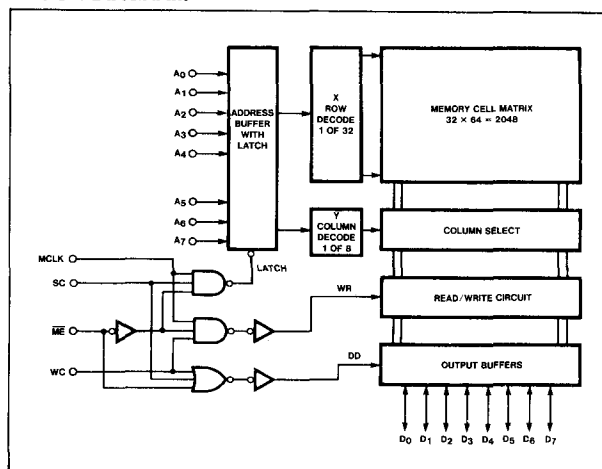
TYPICAL I/O STRUCTURE**PIN CONFIGURATION****ABSOLUTE MAXIMUM RATINGS**

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V _{OH}	High	+5.5	
V _O	Off-state	+5.5	
	Temperature range		°C
T _A	Operating		
	Commercial	0 to +75	
	Military	-55 to +125	
T _{STG}	Storage	-65 to +150	

TRUTH TABLE

Note X = Don't care

MODE	ME	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address					
Disable data out	1	X	X	X	High Z data out
Input new address	0	1	0	1	Address High Z
Hold address					
Disable data out	0	1	0	0	High Z data out
Hold address					
Write data	0	0	1	1	Data in
Hold address					
Disable data out	0	0	1	0	High Z data out
Hold address					
Read data	0	0	0	X	Data out
Undefined state ¹²	0	1	1	1	—
Hold address ¹²					
Disable data out	0	1	1	0	High Z data out

BLOCK DIAGRAM

2048-BIT BIPOLAR RAM (256 × 8)

8X350 (T.S.)

www.DataSheet4U.com

DC ELECTRICAL CHARACTERISTICS² N8X350: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S8X350: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	N8X350			S8X350			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low ¹ High ¹ Clamp ^{1,3}	V _{CC} = Min V _{CC} = Max V _{CC} = Min, I _{IN} = -12mA			.85 -1.2 2.0			V
V _{OL} V _{OH}	Output voltage Low ^{1,4} High ^{1,5}	V _{CC} = Min I _{OL} = 9.8mA I _{OH} = -2mA			0.5 2.4 .5			V
I _{IL} I _{IH}	Input current Low High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 25 -150 50			μA
I _O (OFF) I _{OS}	Output current High Z state Short circuit ^{3,6}	ME = High, V _{OUT} = 5.5 V ME = High, V _{OUT} = 0.5 V SC = WC, ME = Low, V _{OUT} = 0V, Stored High			40 -100 -20 -70 -15 -85			μA μA mA
I _{CC}	V _{CC} supply current ⁷	V _{CC} = Max			185 200			mA
C _{IN} C _{OUT}	Capacitance Input Output	ME = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V			5 8 5 8			pF

AC ELECTRICAL CHARACTERISTICS^{2,9} N8X350: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 S8X350: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TO	FROM	N8X350			S8X350			UNIT
			Min	Typ	Max	Min	Typ	Max	
T _{E1} T _{E2}	Enable time Output Output	SC- ME-	35 35			40 40			ns
T _{D1} T _{D2}	Disable time Output Output	SC+ ME+	35 35			40 40			ns
T _W	Pulse width Master clock ⁸		40			50			ns
T _{SA} T _{HA} T _{SD} T _{HD} T _{S3} T _{H3} T _{S1} T _{H2} T _{S2} T _{H1} T _{H4}	Setup and hold time Setup time Hold time Setup time Hold time Setup time Hold time Setup time Hold time Setup time Hold time Setup time Hold time	MCLK- Address MCLK- Data in MCLK- ME- ME+ MCLK- ME- ME- MCLK- SC-, WC- MCLK- MCLK-	30 5 35 5 40 5 30 5 0 5 5			40 10 45 10 50 5 40 5 5 5 5			ns

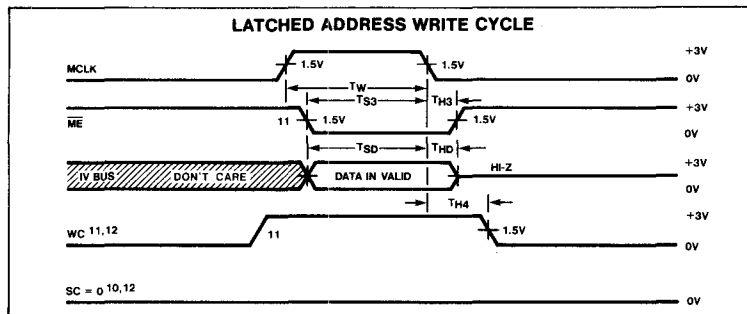
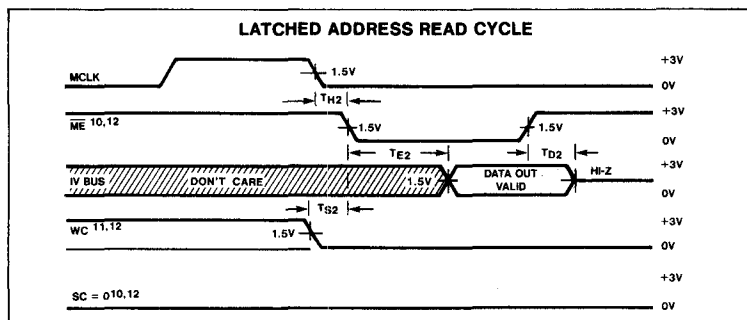
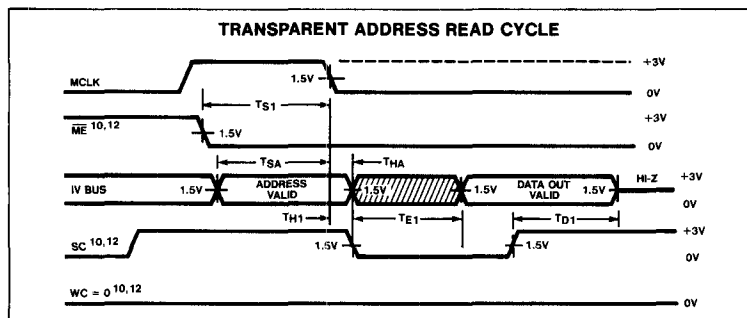
Notes on following page.

2048-BIT BIPOLAR RAM (256 × 8)

8X350 (T.S.)

www.DataSheet4U.com

TIMING DIAGRAMS



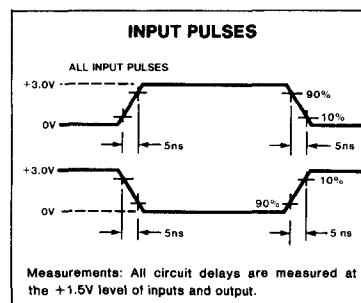
NOTES

- All voltage values are with respect to network ground terminal.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
Typical thermal resistance values of the package at maximum temperature are:
 θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
 θ_{JA} junction to ambient - still air - 90°C/watt
 θ_{JA} junction to case - 20°C/watt
- Test each pin one at a time.
- Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with a logic high stored.
- Duration of the short circuit should not exceed 1 second.
- I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V and the output open.
- Minimum required to guarantee a Write into the slowest bit.
- Applied to the 8X300 based system with the data and address pins tied to the IV Bus.
- SC + ME = 1 to avoid bus conflict.
- WC + ME = 1 to avoid bus conflict.
- The SC and WC outputs from the 8X300 are never at 1 simultaneously.

TIMING DEFINITIONS

- TS1** Required delay between beginning of Master Enable low and falling edge of Master Clock.
- TSA** Required delay between beginning of valid address and falling edge of Master Clock.
- THA** Required delay between falling edge of Master Clock and end of valid Address.
- TH1** Required delay between falling edge of Master Clock and when Select Command becomes low.
- TE1** Delay between beginning of Select Command low and beginning of valid data output on the IV Bus.
- TD1** Delay between when select Command becomes high and end of valid data output on the IV Bus.
- TH2** Required delay between falling edge of Master Clock and when Master Enable becomes low.
- TE2** Delay between when Master Enable becomes low and beginning of valid data output on the IV Bus.
- TD2** Delay between when Master Enable becomes high and end of valid data output on the IV Bus.
- TS2** Required delay between when Select Command or Write Command becomes low and when Master Enable becomes low.
- TW** Minimum width of the Master Clock pulse.
- TS3** Required delay between when Master Enable becomes low and falling edge of Master Clock.
- TH3** Required delay between falling edge of Master Clock and when Master Enable becomes high.
- TS4** Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
- THD** Required delay between falling edge of Master Clock and end of valid data input on the IV Bus.
- TH4** Required delay between falling edge of Master Clock and when Write Command becomes low.

VOLTAGE WAVEFORM

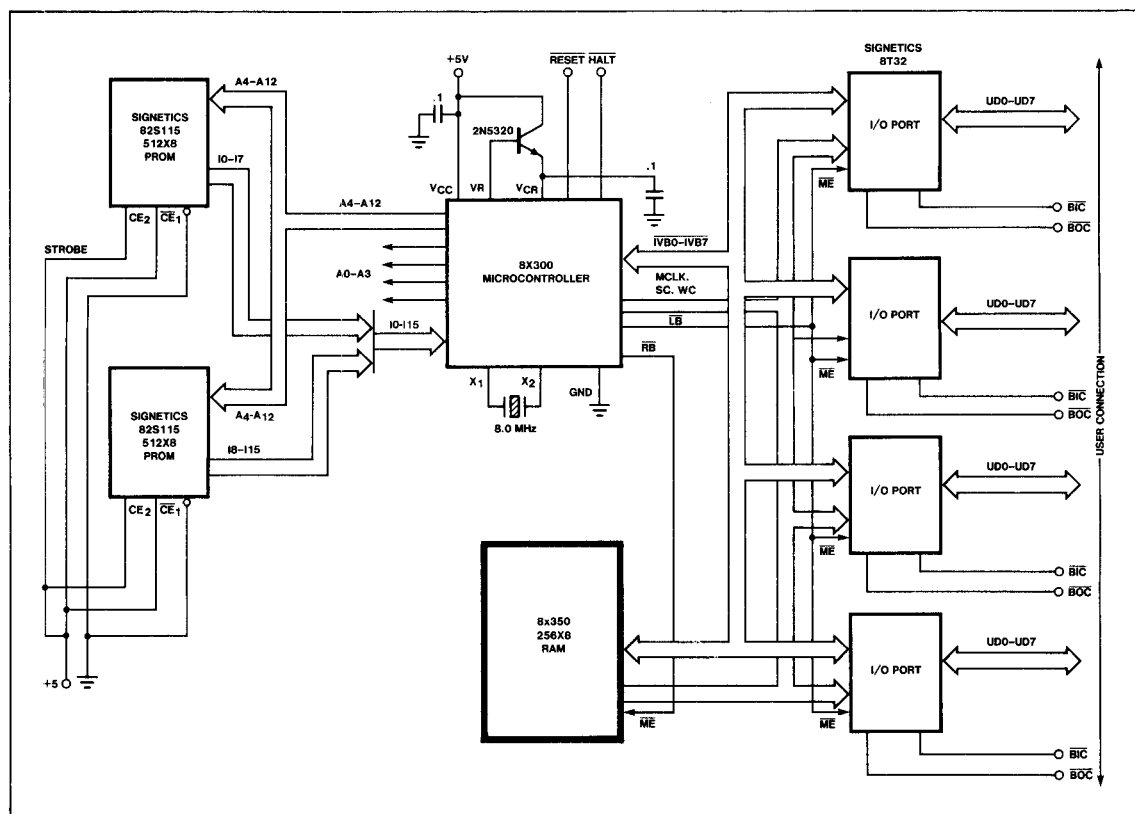


2048-BIT BIPOLAR RAM (256 × 8)

8X350 (T.S.)

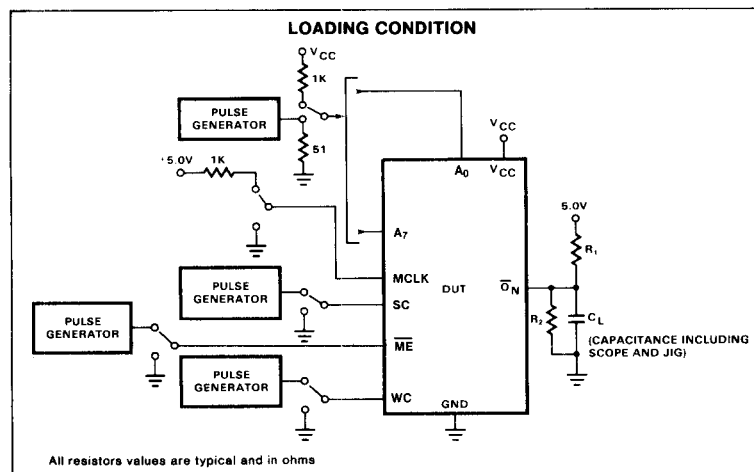
www.DataSheet4U.com

TYPICAL 8X350 APPLICATION



5

TEST LOAD CIRCUIT



Signetics

5-15

www.DataSheet4U.com