DESCRIPTION

This family of low power 1024x1 Rams with a typical access time of 30ns, are ideal for cache buffer applications and for systems requiring very high speed main memory.

These products require a single +5V power supply and feature very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

All devices are available in the commercial temperature range (0°C to +75°C), and military temperature range (-55°C to +125°C).

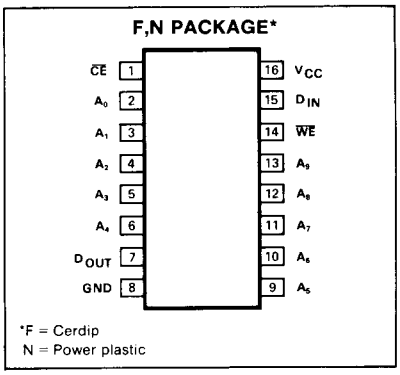
FEATURES

- **Address access time: 45ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 0.2mW/bit typ**
- **Input loading: -250μA max**
- **On-chip address decoding**
- **Output options:**
  - **82LS10, 93L415: Open collector**
  - **82LS11, 93L425: Tri-state**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION



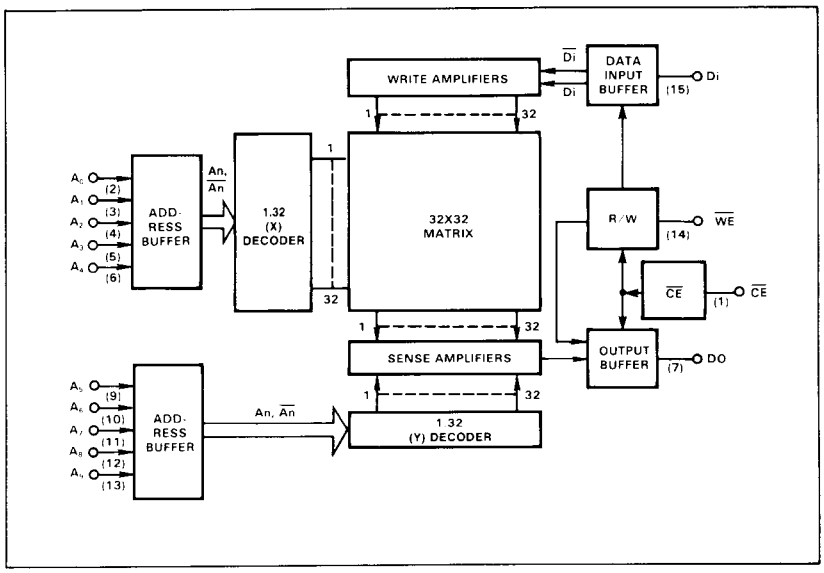
*F = Cerdip
N = Power plastic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82LS10/93L415	82LS11/93L425
Read	0	1	X	Stored data	Stored data
Write low	0	0	0	1	High-Z
Write high	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER[1]	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High 82LS10/93L415	+5.5	
V_O	Off-state 82LS11/93L425	+5.5	
	Temperature range		°C
T_A	Operating		
	N Grade	0 to +75	
	S Grade	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[9]

N Grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S Grade: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82LS10/11 N93L415/425			S82LS10/11 S93L415/425			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.1			2.1			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 16mA		0.35	0.45		0.35	0.50	
V_{OH}	High (Tri-state)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-250		-10	-250	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (Open collector)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (Tri-state)[6]	V_{OUT} = 5.5V		1	60		1	100	μA
		V_{OUT} = 0.45V		-1	-60		-1	-100	
I_{OS}	Short circuit (Tri-state)[7]	V_{OUT} = 0V	-20		-100	-20		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max, $0 < T_A < 25°C$, $T_A \ge 25°C$, $T_A \le 0°C$			65			75	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		7			4		
C_{OUT}	Output	V_{OUT} = 2.0V							

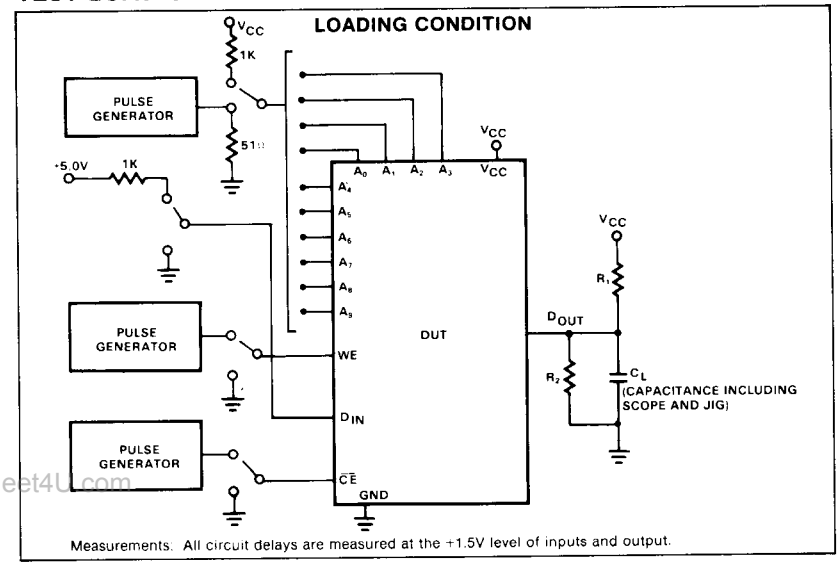
AC ELECTRICAL CHARACTERISTICS[9]

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N Grade: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S Grade: $-55°C \leq T_A + 125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER	TO	FROM	N82LS10 N82LS11			S82LS10 S82LS11			N93L415 N93L425			S93L415 S93L425			
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time															ns
T_{AA} Address	Output	Address		30	45		30	70		30	60			70	
T_{CE} Chip enable	Output	Chip enable		15	30		15	45			40			45	
T_{CD} Disable time	Output	Chip enable		15	30		15	45			40			50	ns
T_{WD} Response time	Output	Write enable		20	30		20	45			45			45	ns
T_{WR} Write recovery time				20	30		20	45			45			55	ns
Setup and hold time															ns
T_{WSA} Setup time	Write enable	Address	5	0		10	0		5	0		10			
T_{WHA} Hold time			5	0		10	0		5	0		10			
T_{WSD} Setup time	Write enable	Data in	40	30		55	35		50			60			
T_{WHD} Hold time			5	0		5	0		5			10			
T_{WSC} Setup time	Write enable	CE	5			5			5			10			
T_{WHC} Hold time			5	0		5	0		5			10			
Pulse width															ns
T_{WP} Write enable[10]			35	25		50	25		45			50			

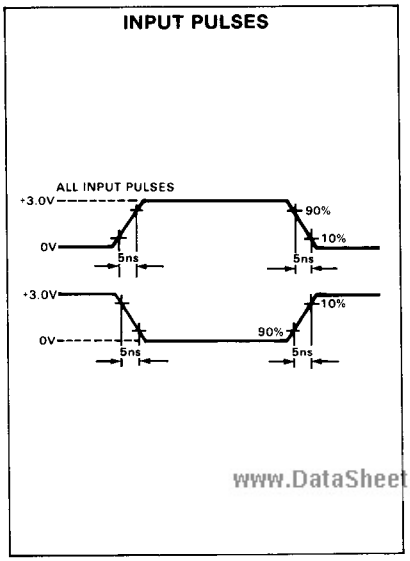
NOTES
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} junction to ambient at 400fpm air flow-50° C/watt
   θ_{JA} junction to ambient-still air-90° C/watt
   θ_{JA} junction to case-20° C/watt
10. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUIT

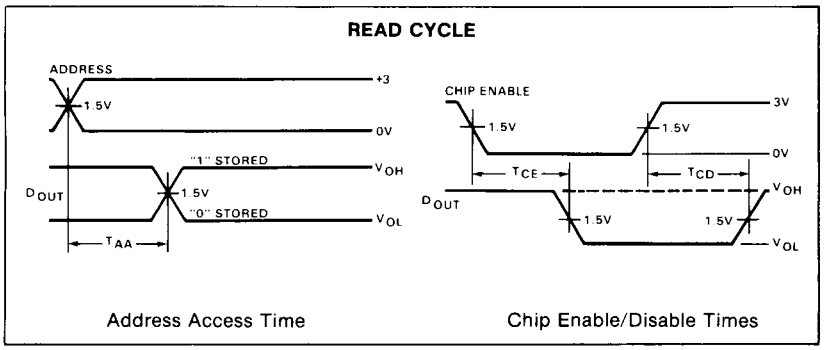


Measurements. All circuit delays are measured at the +1.5V level of inputs and output.

VOLTAGE WAVEFORM

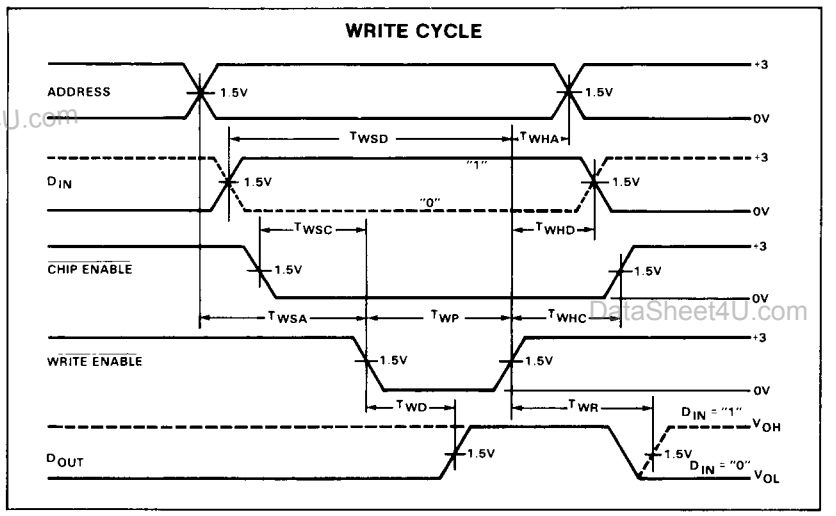


TIMING DIAGRAMS



Address Access Time

Chip Enable/Disable Times



MEMORY TIMING DEFINITIONS

T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid—not as shown.)
T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output is in off state.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.