N57L5125

Product Preview
32-tap Digital Potentiometers (POTs) with 2-wire Interface

Description

N57L5125 linear-taper digital POTs perform the same function as a mechanical potentiometer or a variable resistor. This device consists of a fixed resistor and a wiper contact with 32-tap points that are digitally controlled through a 2-wire up/down serial interface.

The N57L5125 is configured as a potentiometer. Three resistance values are available: 10 kΩ, 50 kΩ and 100 kΩ. All devices are available in a space-saving 6-pin SOT–23 package.

Features

- 0.3 µA Ultra-low Standby Current
- Single-supply Operation: 2.7 V to 5.5 V
- Glitchless Switching between Resistor Taps
- Power-on Reset to Midscale
- 2-wire Up/Down Serial Interface
- Resistance Values: 10 kΩ, 50 kΩ and 100 kΩ
- Low Wiper Resistance: 80 Ω
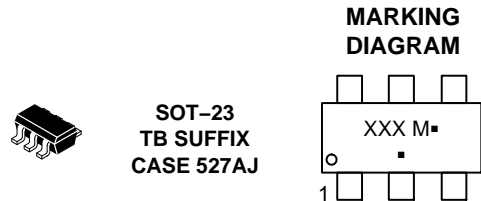- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- LCD Screen Adjustment
- Volume Control
- Mechanical Potentiometer Replacement
- Gain Adjustment
- Line Impedance Matching

ON Semiconductor®

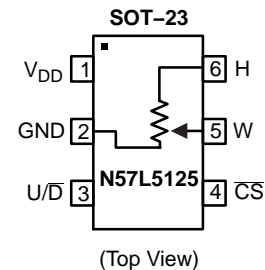### MARKING DIAGRAM

SOT–23
TB SUFFIX
CASE 527AJ

XXX M■

1

XXX = Specific Device Code
M = Date Code
■ = Pb–Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS

SOT–23

V_DD 1		6 H
GND 2		5 W
U/D̄ 3	N57L5125	4 C̄S̄

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

N57L5125
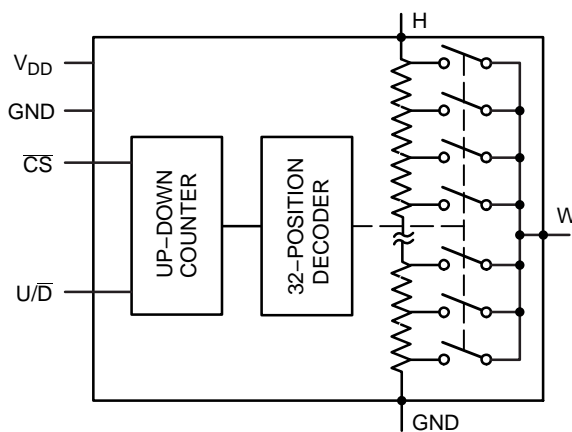
Figure 1. Functional Diagram

Table 1. PIN DESCRIPTIONS

Pin Num-ber	Pin Name	Description
1	V_{DD}	Power Supply
2	GND	Ground
3	U/$\overline{D}$	Up/$\overline{Down}$ Control Input. With $\overline{CS}$ low, a low-to-high transition increments or decrements the wiper position.
4	$\overline{CS}$	Chip Select Input. A high-to-low $\overline{CS}$ transition determines the mode: increment if U/$\overline{D}$ is high, or decrement if U/$\overline{D}$ is low.
5	W	Wiper Terminal of Resistor
6	H	High Terminal of Resistor

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{DD} to GND	−0.3 to +6	V
All Other Pins to GND	−0.3 to (V_{DD} + 0.3)	V
Input and Output Latch–Up Immunity	±200	mA
Maximum Continuous Current into H, L and W 100 kΩ 50 kΩ 10 kΩ	 ±0.6 ±1.3 ±1.3	mA
Continuous Power Dissipation (T_A = +70°C) 6-pin SC–70 (Note 1)	 245	mW
Operating Temperature Range	−40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature Range	−65 to +150	°C
Soldering Temperature (soldering, 10 sec)	+300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Derate 3.1 mW/°C above T_A = +70°C

Table 3. ELECTRICAL CHARACTERISTICS
(V_{DD} = 2.7 V to 5.5 V, V_H = V_{DD}, V_L = 0, T_A = −40°C to +85°C. Typical values are at V_{DD} = 2.7 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC PERFORMANCE						
Resolution			32			Taps
End-to-End Resistance (−00)			80	100	120	kΩ
End-to-End Resistance (−50)			40	50	60	
End-to-End Resistance (−10)			8	10	12	
End-to-End Resistance Tempco	TC_R			30	300	ppm/°C
Ratiometric Resistance Tempco				5		ppm/°C
Integral Nonlinearity	INL				±0.5	LSB
Differential Nonlinearity	DNL				±0.5	LSB
Full-Scale Error				±0.1		LSB
Zero-Scale Error					1	LSB
Wiper Resistance	R_W			80	200	Ω
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
TIMING CHARACTERISTICS (Figures 5, 6)						
U/$\overline{D}$ Mode to $\overline{CS}$ Setup	t_{CU}		25			ns
$\overline{CS}$ to U/$\overline{D}$ Step Setup	t_{CI}		50			ns
$\overline{CS}$ to U/$\overline{D}$ Step Hold	t_{IC}		25			ns
U/$\overline{D}$ Step Low Period	t_{IL}		25			ns
U/$\overline{D}$ Step High Period	t_{IH}		25			ns
Up/$\overline{Down}$ Toggle Rate (Note 2)	f_{TOGGLE}			1		MHz
Output Settling Time (Note 3)	t_{SETTLE}	100 kΩ variable resistor configuration, C_L = 10 pF		1		μs
		100 kΩ potentiometer configuration, C_L = 10 pF		0.25		
POWER SUPPLY						
Supply Voltage	V_{DD}		2.7		5.5	V
Active Supply Current (Note 4)	I_{DD}				35	μA
Standby Supply Current (Note 5)	I_{SB}	V_{DD} = +5 V		0.3	1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Up/Down Toggle Rate: f_{TOGGLE} = 1 / t_{SETTLE}
3. Typical settling times are dependent on end-to-end resistance.
4. Supply current measureed while changing wiper tap, f_{TOGGLE} = 500 kHz.
5. Supply current measureed while wiper position is fixed.

N57L5125

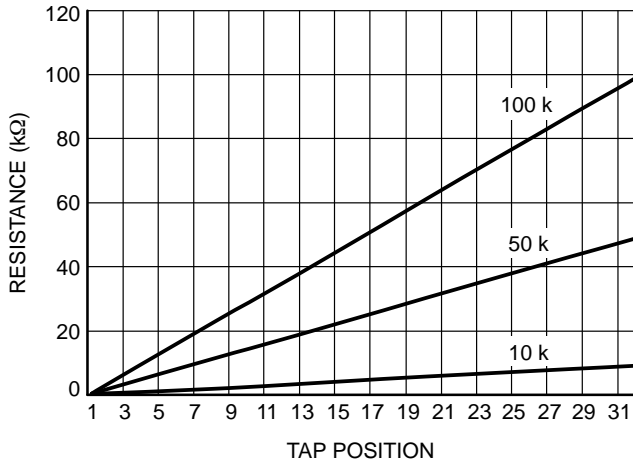## TYPICAL OPERATING CHARACTERISTICS

(T$_A$ = 25°C, unless otherwise noted.)

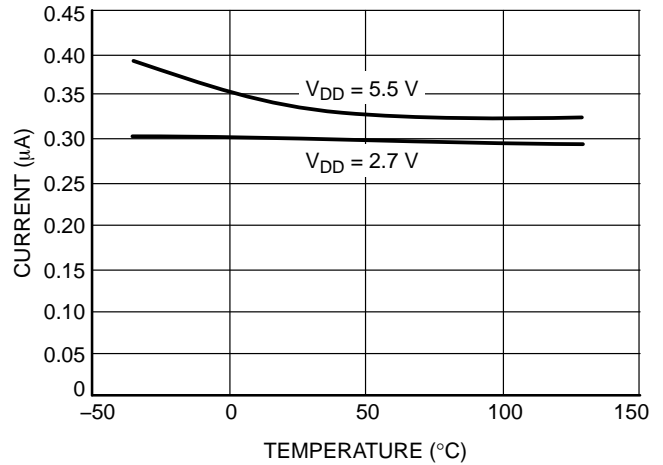**Figure 2. W-to-GND Resistance vs. Tap Position**
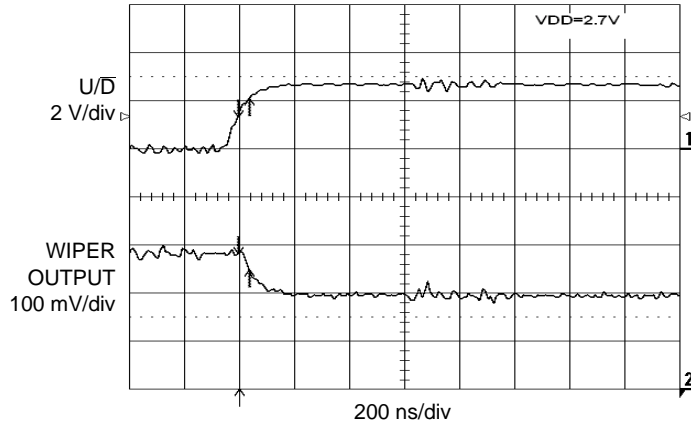

Figure 3. Supply Current vs. Temperature

Figure 4. Tap-to-Tap Switching Transient

FUNCTIONAL DESCRIPTION

The N57L5125 consists of a fixed resistor and a wiper contact with 32–tap points that are digitally controlled through a 2-wire up/down serial interface. Three end-to-end resistance values are available: 10 kΩ, 50 kΩ and 100 kΩ.

The N57L5125 is designed to operate as a potentiometer. In this configuration, the low terminal of the resistor array is connected to ground (pin 2).

Digital Interface Operation

The devices have two modes of operation when the serial interface is active: increment and decrement mode. The serial interface is only active when $\overline{CS}$ is low.

The $\overline{CS}$ and U/$\overline{D}$ inputs control the position of the wiper along the resistor array. When $\overline{CS}$ transitions from high to low, the part will go into increment mode if U/$\overline{D}$ input is high, and into decrement mode when U/$\overline{D}$ input is low. Once

the mode is set, the device will remain in that mode until $\overline{CS}$ goes high again. A low-to-high transition at the U/$\overline{D}$ pin will increment or decrement the wiper position depending on the current mode (Figures 5 and 6).

When the $\overline{CS}$ input transitions to high (serial interface inactive), the value of the counter is stored and the wiper position is maintained.

Note that when the wiper reaches the maximum (or minimum) tap position, the wiper will not wrap around to the minimum (or maximum) position.

Power-On Reset

All parts in this family feature power-on reset (POR) circuitry that sets the wiper position to midscale at power-up. By default, the chip is in the increment mode.

Note: "W" is not a digital signal. It represents wiper transitions.
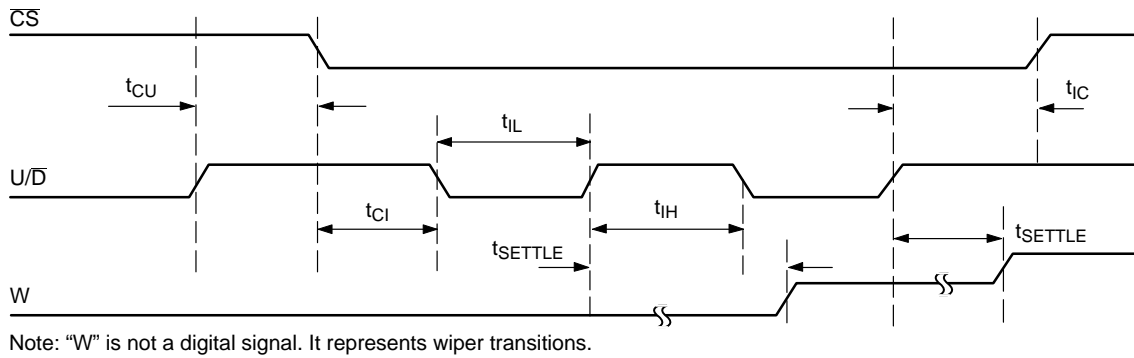
Figure 5. Serial Interface Timing Diagram, Increment Mode

Note: "W" is not a digital signal. It represents wiper transitions.
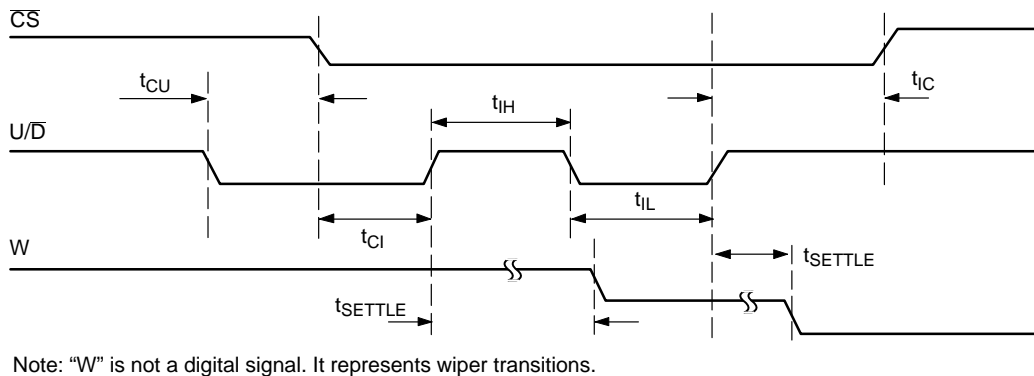
Figure 6. Serial Interface Timing Diagram, Decrement Mode

N57L5125

APPLICATIONS INFORMATION

The devices are intended for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control, where voltage biasing adjusts the display contrast.

Alternative Positive LCD Bias Control

An op amp can be used to provide buffering and gain on the output of the N57L5125. This can be done by connecting the wiper output to the positive input of a noninverting op amp as shown in Figure 7.
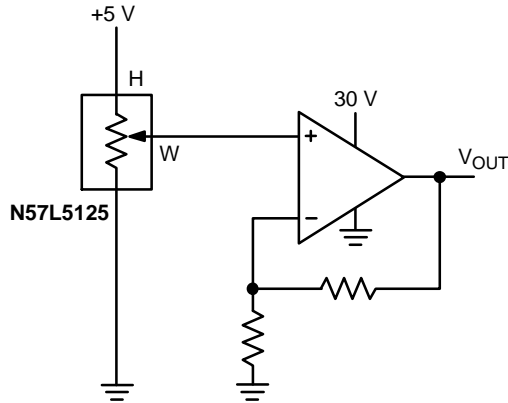
Adjustable Gain

Figure 8 shows how to use a potentiometer to digitally adjust the gain of a noninverting op amp configuration, by connecting the devices in series with a resistor to ground. The devices have a low 5 ppm/°C ratiometric tempco that allows for a very stable adjustable gain configuration over temperature.

Figure 7. Positive LCD Bias Control
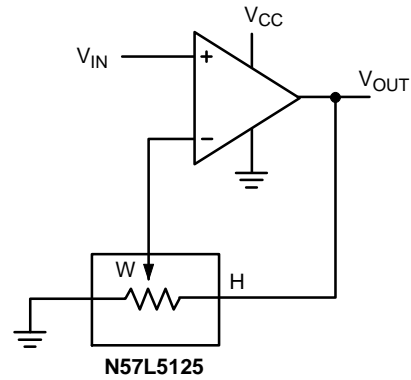
Figure 8. Adjustable Gain Circuit

N57L5125

Table 4. ORDERING INFORMATION

Device	Orderable Part Number	Resistor [kΩ]	Pin Package	Shipping†
N57L5125	N57L5125TBD10TG	10	SOT23–6	3000 / Tape & Reel
	N57L5125TBD50TG (Note 7)	50	SOT23–6	3000 / Tape & Reel
	N57L5125TBD00TG (Note 7)	100	SOT23–6	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.
7. Contact factory for availability.
8. All packages are RoHS-compliant (Pb-Free, Halogen-Free).
9. The standard finish is NiPdAu.
10. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

N57L5125

PACKAGE DIMENSIONS

SOT–23, 6 Lead
CASE 527AJ
ISSUE B

TOP VIEW

SIDE VIEW

DETAIL A

END VIEW
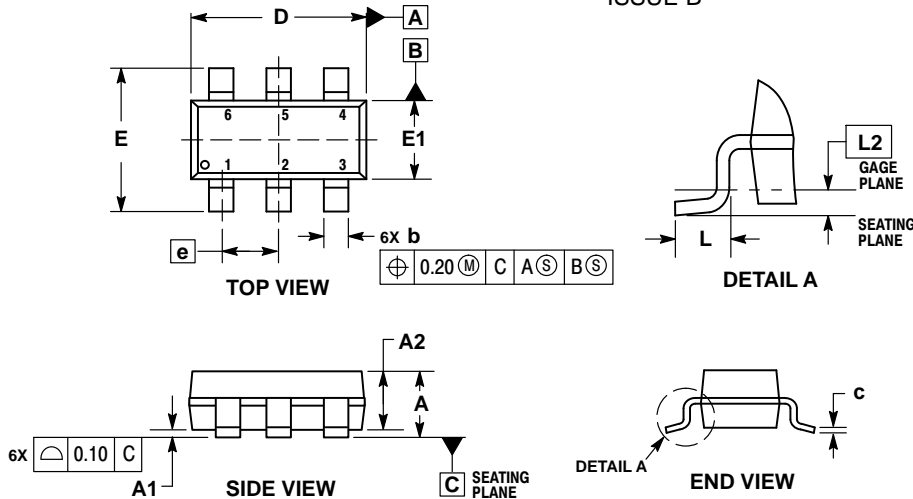
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

DIM	MILLIMETERS	
	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

3.30

6X 0.85

6X 0.56

0.95 PITCH
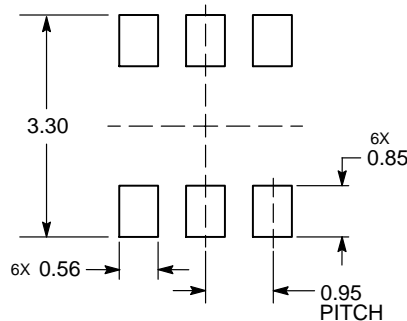
DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.