Agilent Technologies InfiniiVision MSO N5434A FPGA Dynamic Probe for Altera

Data Sheet

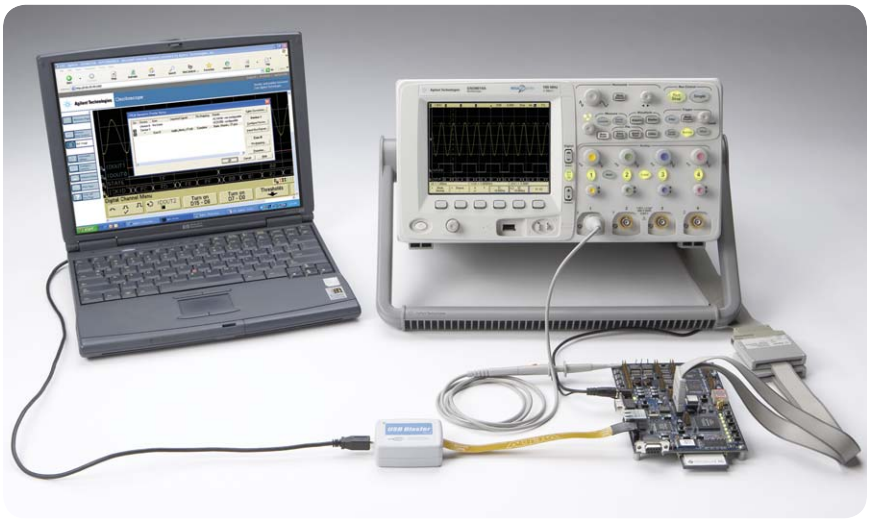


Figure 1. FPGA dynamic probe for Altera used in conjunction with an InfiniiVision 6000 or 7000 Series MSO provides an effective solution for simple through complex debugging of systems incorporating Altera FPGAs.

The challenge

You rely on the insight a MSO (mixed-signal oscilloscope) provides to understand the behavior of your FPGA in the context of the surrounding system. Design engineers typically take advantage of the programmability of the FPGA to route internal nodes to a small number of physical pins for debugging. While this approach is very useful, it has significant limitations.

- Since pins on the FPGA are typically an expensive resource, there are a relatively small number available for debug. This limits internal visibility (i.e. one pin is required for each internal signal to be probed).
- When you need to access different internal signals, you must change your design to route these signals to the available pins. This can be time consuming and can affect the timing of your FPGA design.
- Finally, the process required to map the signal names from your FPGA design to the MSO digital channel labels is manual and tedious.

  When new signals are routed out, you need to manually update these signal names on the MSO, which takes additional time and is a potential source of confusing errors.

Debug your FPGAs faster and more effectively with a MSO

FPGA dynamic probe lets you:

View internal activity – With the digital channels on your MSO, you are normally limited to measuring signals at the periphery of the FPGA. With the FPGA dynamic probe, you can now access signals internal to the FPGA. You can measure up to 256 internal signals for each external pin dedicated to debug, unlocking visibility into your design that you never had before.

Make multiple measurements in seconds – Moving probe points internal to an FPGA used to be time consuming. Now, in less than a second, you can easily measure different sets of internal signals without design changes. FPGA timing stays constant when you select new sets of internal signals for probing.

Leverage the work you did in your design environment – The FPGA dynamic probe maps internal signal names from your FPGA design tool to your Agilent MSO. Eliminate unintentional mistakes and save hours of time with this automatic setup of signal and bus names on your MSO.

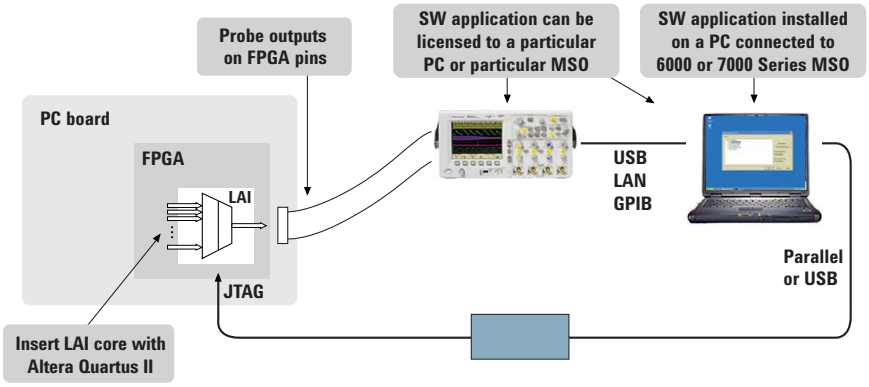


Figure 2. The FPGA dynamic probe requires Altera's Quartus II design software with its LAI (logic analyzer interface) and Altera programming hardware setup. The Quartus II (ver. 6.0 or higher) LAI allows you to create and insert a debug core that interacts with the FPGA dynamic probe application on your MSO. The FPGA dynamic probe controls which group of internal signals to measure via the Altera programming hardware connected to the JTAG port of the FPGA.

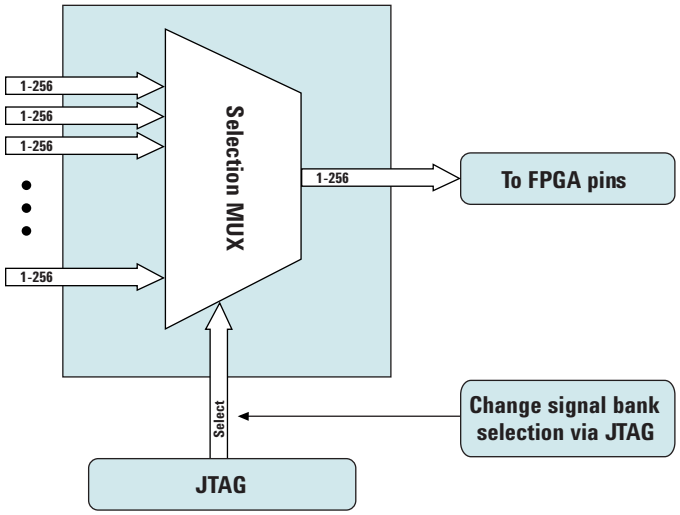
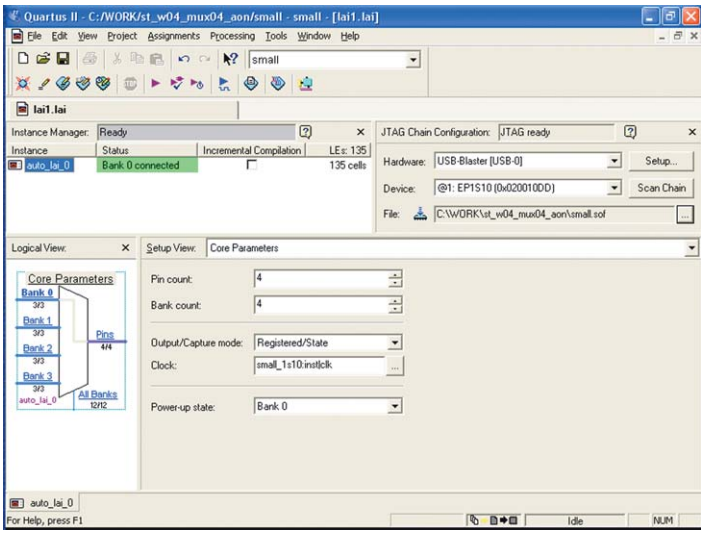


Figure 3. Access up to 256 internal signals for each debug pin. Signal banks all have identical width (1 to 256 signals wide) determined by the number of device pins you devote for debug. Each pin provides sequential access to one signal from every input bank. MSO6000 series can acquire up to 16 signals using digital channels.

A quick tour of the application

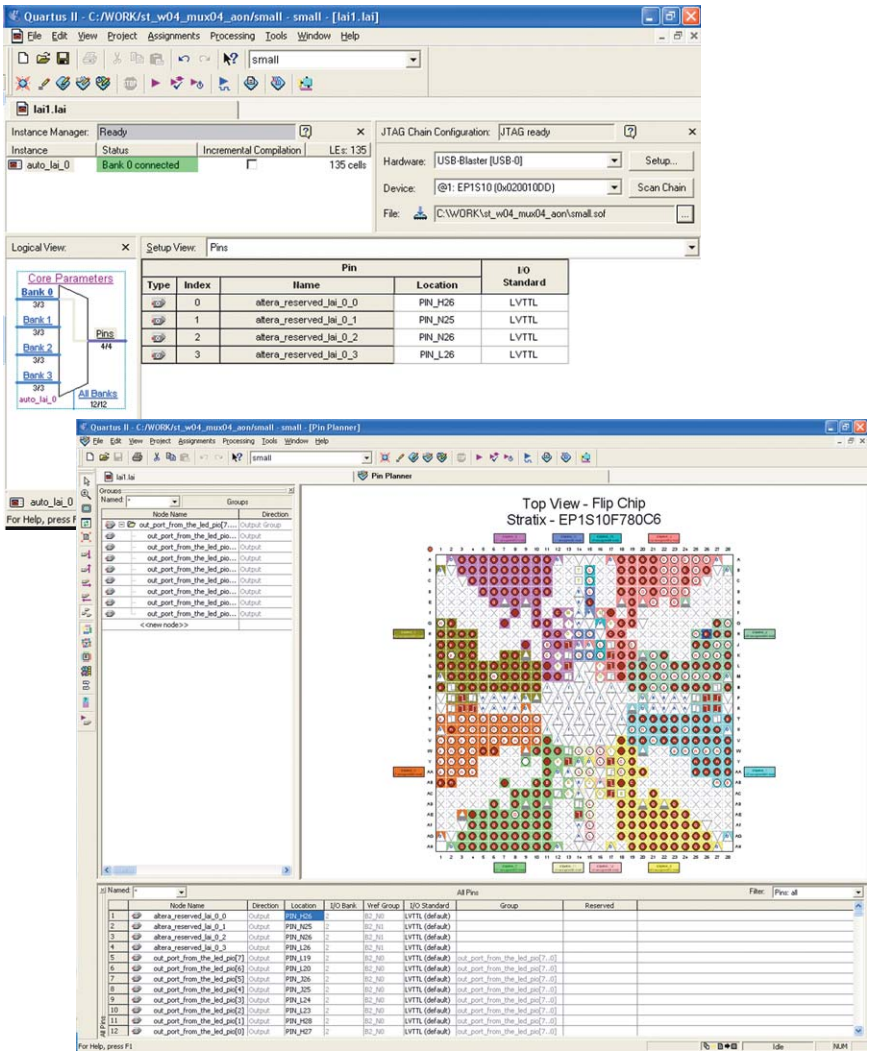
Design step 1: Configure the logic analyzer interface file and core parameters

You need to create a Altera LAI file with MSO in Quartus II. This file defines the interface that builds a connection between the internal FPGA signals and the MSO digital channels. You can then configure the core parameters, which include number of pins, number of signal banks, the type of measurement (state or timing), clock and the power-up state.



Design step 2: Map the Altera LAI core outputs to available I/O pins

Use Pin Planner in Quartus II to assign physical pin locations for the LAI.

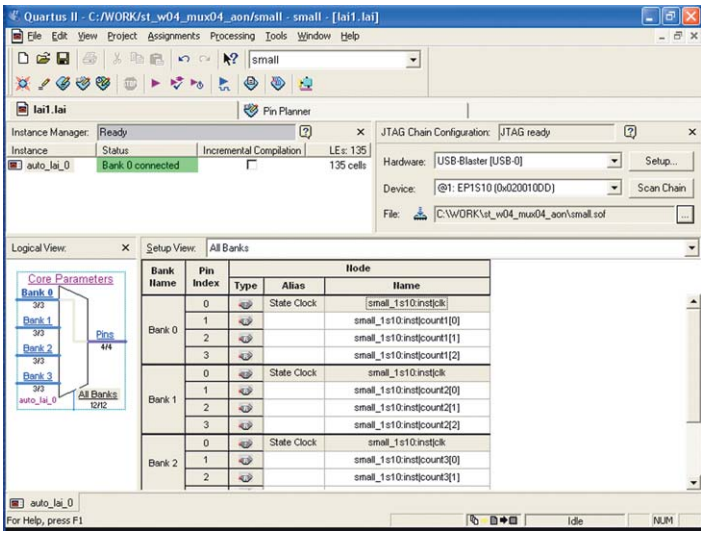


A quick tour of the application (continued)

Design step 3: Assign LAI bank parameters

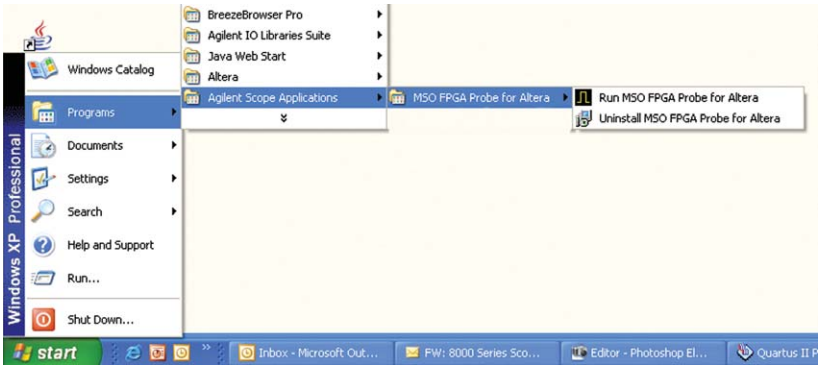
Assign internal signals to each bank in the LAI after you have specified the number of banks to use in the core parameters. Find the signals you want to acquire with the Node Finder and assign them to the banks.

With the LAI core fully configured and instantiated into your FPGA design, you're ready to compile your design to create the device programming file (.sof). Then, to make measurements you'll move to the Agilent MSO with FPGA dynamic probe software.



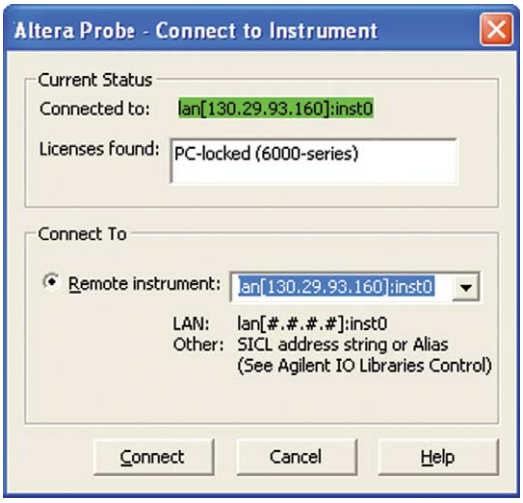
Activate FPGA dynamic probe for Altera

The FPGA dynamic probe application allows you to control the LAI and set up the MSO for the desired measurements. This application runs on a PC.



Connect your MSO to your PC

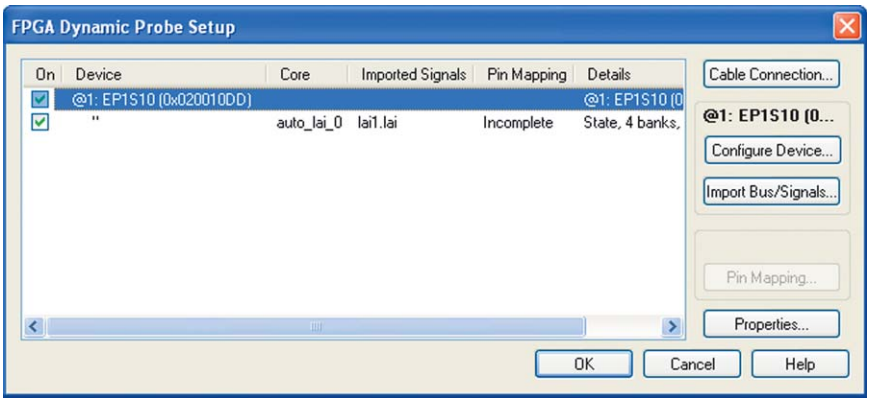
From FPGA dynamic probe application software, specify the communication link between your PC and MSO.



A quick tour of the application (continued)

Measurement setup step 1: Establish a connection between the MSO and the LAI

The FPGA dynamic probe application establishes a connection between the MSO and the FPGA via a JTAG cable. It also determines what devices are on the JTAG scan chain and lets you pick the one with which you wish to communicate.

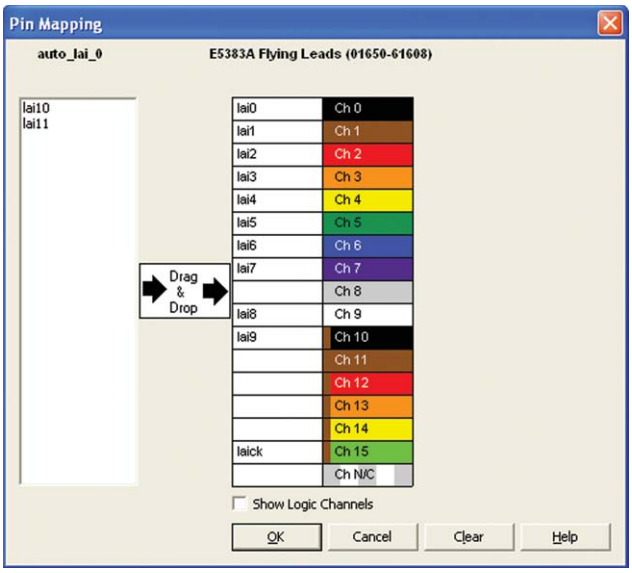


Measurement setup step 2: Configure the device and import signal names

If needed, you can configure the device with the SRAM object file (.sof) that includes the logic analyzer interface file. The FPGA dynamic probe application reads a .lai file produced by Quartus II. The names of signals you measure will now automatically appear in the label names on your Agilent MSO.

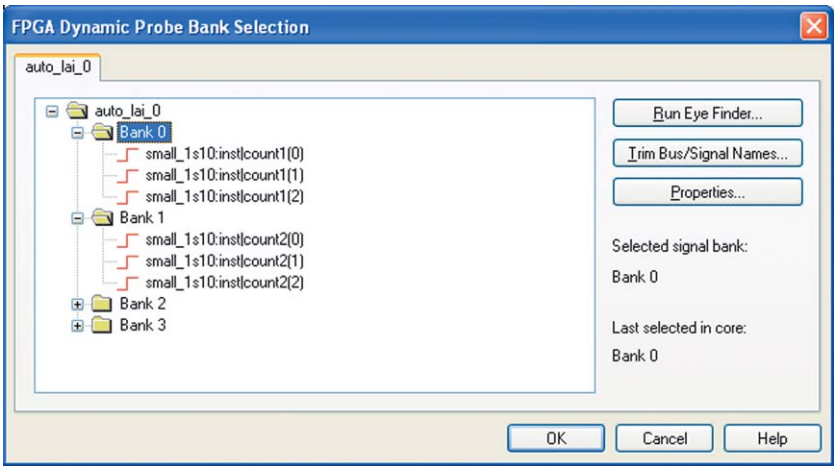
Measurement setup step 3: Map FPGA pins

Select your probe type and easily provide the information needed for the MSO to automatically track names of signals routed through the LAI file.



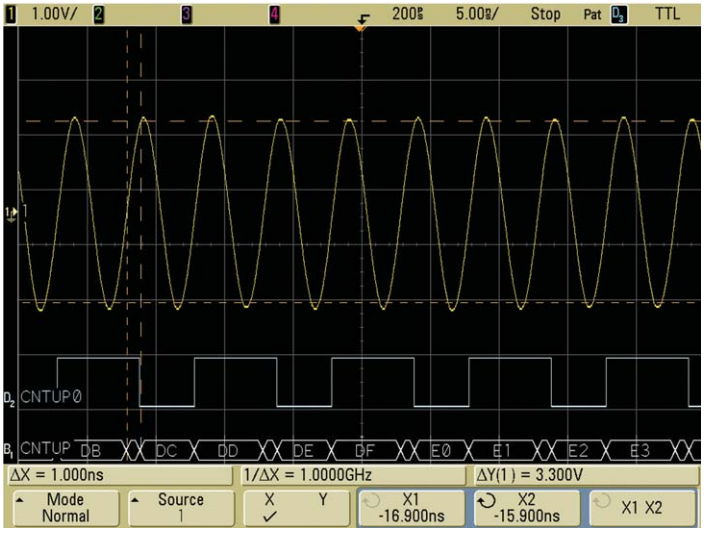
A quick tour of the application (continued)

Setup complete: Make measurements
Quickly change which signal bank is routed to the MSO. A single mouse click tells the LAI core to switch to the newly specified signal bank without any impact to the timing of your design. To make measurements throughout your FPGA, change signal banks as often as needed. With each new selection of a signal bank, FPGA Dynamic Probe updates new signal names from your design to the MSO. User-definable signal bank names make it straight forward to select a part of your design to measure.



Triggering on valid states
MSOs incorporate logic state triggering for triggering on specific states. Set up a valid state trigger by specifying the appropriate LAI clock edge and the desired bus/signal pattern. Because the LAI core outputs both the clock signal and bus values, triggering on the combination ensures your state trigger is valid—even though the digital channels are sampling asynchronously. Track valid states by measuring the bus value on each falling clock edge for the image shown.

Correlate internal FPGA activity with external measurements
View internal FPGA activity and time-correlate internal FPGA measurements with external analog and digital events in the surrounding system. FPGA Dynamic Probe unlocks the power of the MSO for system-level debug with FPGAs.



Agilent N5434A specifications and characteristics

Supported logic analyzers	
Standalone oscilloscopes	InfiniiVision 6000 and 7000 Series MSOs
MSO Digital Channels	16
Bus groupings	Up to 2, each with 6 character labels
Triggering capabilities	Determined by MSO, all have state triggering
Supported Altera FPGA families	All families that the Altera LAI core supports, including Stratix IV, Stratix III, Stratix II, Stratix, Cyclone III, Cyclone II, Cyclone, Arrix II and Arria
Supported Altera cables (required)	Altera USB Blaster or ByteBlaster
Supported probing mechanisms	Soft touch (34-channel and 17-channel), Mictor, Samtec, Flying lead, 6000 and 7000 Series MSOs come standard with a 40 pin probe cable and flying leads. Cables and probing for Mictor, soft touch, or Samtec probing must be purchased separately.

Altera LAI characteristics	
Number of output signals	User definable: 1 to 256 signals in 1 signal increments
Signal banks	User definable: 1 to 256 banks
Modes	State (synchronous) or timing (asynchronous) mode

Compatible software	
Altera Quartus II 6.0 or greater	Agilent InfiniiVision 6000 and 7000 Series software version 4.0 or greater

Additional information available via the Internet: **www.agilent.com/find/6000-altera** and **www.agilent.com/find/7000-altera**.

Ordering information

Ordering options for the Agilent N5434A FPGA dynamic probe for Altera	
Option 001	• Entitlement certificate for perpetual node-locked license locked to oscilloscope (most common)
Option 002	• Entitlement certificate for PC locked license

Related literature

Publication title	Publication type	Publication number
Frequently Asked Questions N5433A and N5434A Agilent MSO FPGA Dynamic Probe for Altera	Data Sheet	5989-5957EN
Agilent Technologies 6000 Series Oscilloscopes	Data Sheet	5989-2000EN
Agilent Technologies InfiniiVision 7000 Series Oscilloscopes	Data Sheet	5989-7736EN

Product Web site

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