Agilent
N4850A DigRF v3 Acquisition Probe
N4860A DigRF v3 Stimulus Probe

Data Sheet

Evaluate and integrate your DigRF v3 components more easily

DigRF v3 Challenges

The DigRF v3 standard presents new challenges for mobile wireless development, integration and validation teams as the communications link between the BB-ICs and the RF-ICs evolve from analog to digital. Digital IQ data and control information are transferred between the BB-IC and the RF-IC over the DigRF v3 interface. Engineers traditionally use spectrum analyzers to evaluate the analog interface between the BB-IC and the RF-IC, but now they need new tools because spectrum analyzers are incapable of measuring the DigRF v3 digital serial interface.

RF-IC development teams must verify operation of the RF-IC before the start of the handset integration phase. Spectrum analyzers and signal sources are no longer sufficient for characterizing the new generation of RF-ICs that comply to the DigRF v3 standard. To validate RF-IC operation, engineering teams need DigRF v3 digital serial stimulus and analysis tools that operate in concert with the traditional RF tools.

The challenges for BB-IC validation teams mirrors that of the RF-IC teams, as the signal sources and spectrum analyzers must be replaced by DigRF v3 digital serial stimulus and analysis tools to validate BB-IC functionality.

Meeting the DigRF v3 Challenges

The Agilent Technologies N4850A acquisition probe and the N4860A stimulus probe operate in conjunction with Agilent 16800 and 16900 Series serial logic analyzers to provide the digital serial stimulus and acquisition capabilities required to independently evaluate an RF-IC or BB-IC with a DigRF v3 interface or integrate your mobile wireless designs.

Figure 1. N4850A DigRF v3 acquistion probe

Figure 2. N4860A DigRF v3 stimulus probe

Introduction to DigRF v3

The DigRF v3 standard was designed to enable interoperability between RF-ICs and BB-ICs from different suppliers. Additional benefits include reduced cost, higher bandwidth and extended battery life.

The physical layer of the DigRF v3 interface consists of six signals (see Figure 3) with independent transmit and receive paths. Additional signals are specified for diversity mode. The DigRF v3 specification allows for 1.8 V LVDS, 1.2 V LVDS or SLVDS electrical interface voltages. The DigRF v3 interface transitions between high speed, low power and sleep modes dynamically.

The DigRF v3 standard specifies data packets and control packets. Embedded in the data packets is the digital IQ representation of the RF signal. Control packets contain the configuration and status information necessary to keep the BB-IC and RF-IC operating in synchronization.

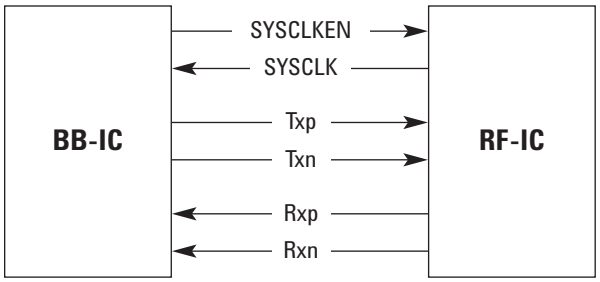
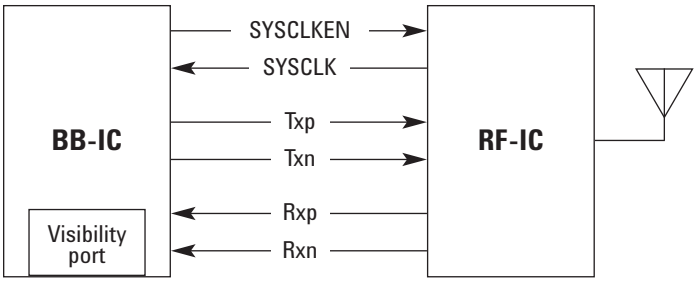


Figure 3. DigRF v3 physical interconnect scheme

Test Scenarios

RF-IC development teams, BB-IC development teams and integration teams each have unique test and measurement requirements as they validate their products, as shown in Figures 4a-4c.

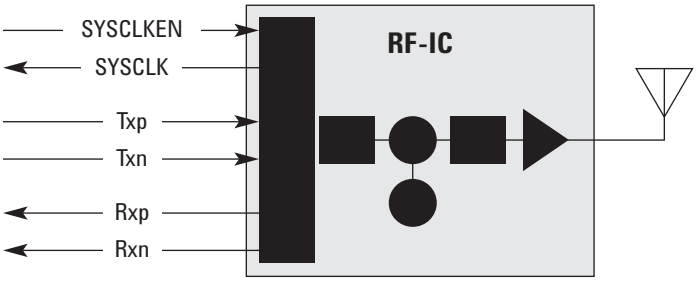
Integration measurement needs



- Acquire Tx and Rx transactions
- Decode/view control packets
- Extract digital IQ (Rx and Tx) for vector signal analysis
- Monitor BB-IC internal operations

Figure 4a. The integration team's measurement needs

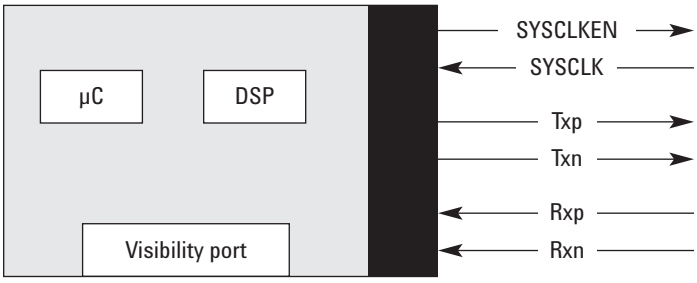
RF-IC evaluation measurement needs



- Generate and drive control packets
- Generate and drive digital IQ (Tx)
- Acquire digital IQ (Rx) for vector signal analysis

Figure 4b. Measurement needs for evaluating the RF-IC

BB-IC evaluation measurement needs



- Decode and view control packets (Tx)
- Extract digital IQ (Tx) for vector signal analysis
- Generate and drive digital IQ (Rx)
- Monitor BB-IC internal operations

Figure 4c. Measurement needs for evaluating the BB-IC

BB-IC/RF-IC Integration

Figure 5 shows the equipment required to integrate the RF-IC with the BB-IC. A signal generator and spectrum analyzer provide stimulus/response capabilities in the RF domain. Traffic on the DigRF v3 link between the RF-IC and BB-IC is monitored by the N4850A acquisition probe. Control packets are viewed in the logic analyzer's packet viewer, and IQ data packets are analyzed using the Agilent 89601A vector signal analysis package. The logic analyzer monitors the BB-IC visibility port to help you gain insight into µC and DSP and correlate these internal operations with traffic on the DigRF v3 interface.

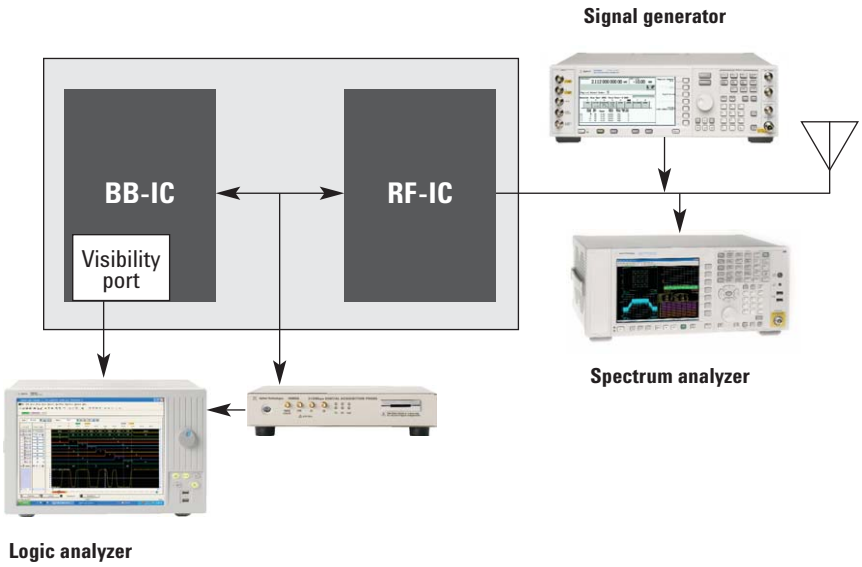


Figure 5. Test and measurement configuration for RF-IC BB-IC integration

Visibility into the internal operation of the BB-IC can be achieved by monitoring the visibility port, which is designed into the BB-IC. Typically, you can track operation of the microcontroller and DSP through the visibility port. This allows you to analyze control flow, track internal processing of digital IQ and correlate BB-IC internal operations to DigRF v3 traffic.

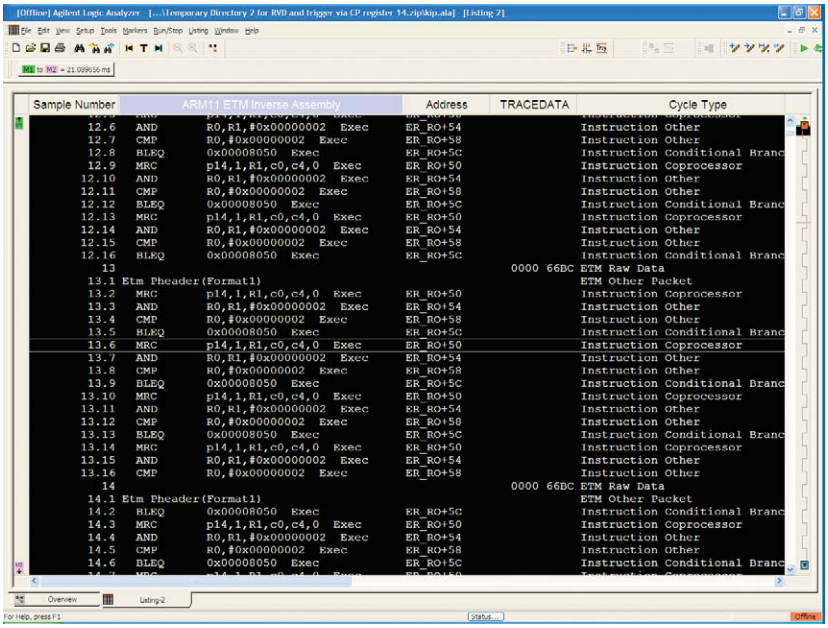


Figure 6. Decoder view of BB-IC internal operation

The N4850A acquisition probe captures transactions on the Tx and Rx paths of the DigRF v3 interface independently. Control packets are decoded and displayed on the logic analyzer's packet viewer as illustrated in Figure 7. These capabilities enable you to track the status and control flow of the system under test to identify defects and tune performance parameters.

There is a two-step process for analyzing the digital IQ data packets that are acquired by the N4850A acquisition probe. Using the signal extractor tool, the headers and padding are removed, leaving the digital IQ representation of the RF signal. The IQ data then can be analyzed by the vector signal analysis package to evaluate EMV, sidebands and other critical RF parameters. This capability enables systems integrators to characterize RF-IC behavior and adjust DSP algorithms or the RF-IC configuration to optimize performance.

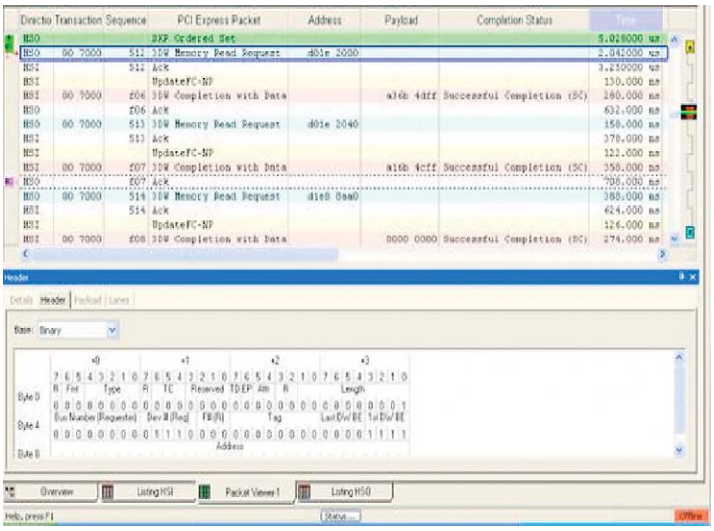


Figure 7. Packet view of DigRF v3 control traffic

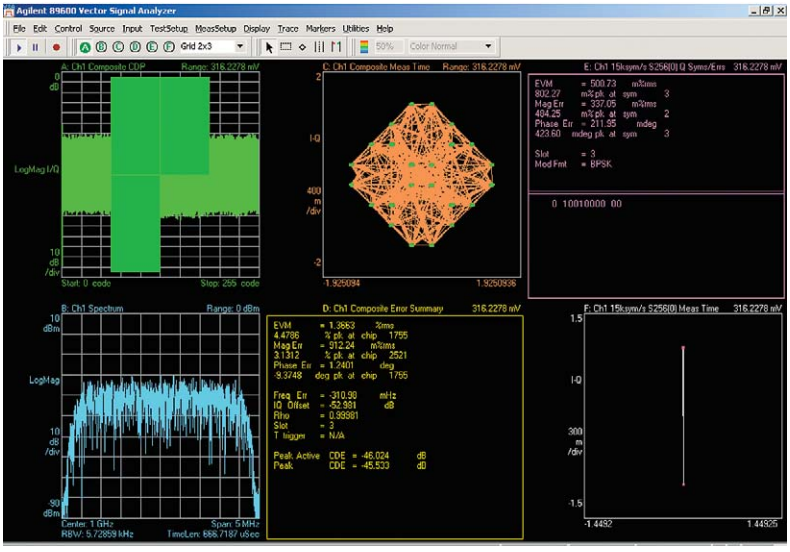


Figure 8. Vector signal analysis of DigRF v3 digital IQ

RF-IC Evaluation

Figure 9 shows a test and measurement configuration that will enable RF-IC designers to verify operation of their components with the DigRF v3 interface. Stimulus and analysis of the RF interface is provided by a signal generator and a spectrum analyzer. Serial digital acquisition and stimulus for the DigRF v3 interface are provided by the N4850A and N4860A operating under control of an Agilent 16800 or 16900 Series logic analyzer. With the ability to monitor and control the RF-IC through the DigRF v3 interface, validation engineers can evaluate transmitter and receiver behavior.

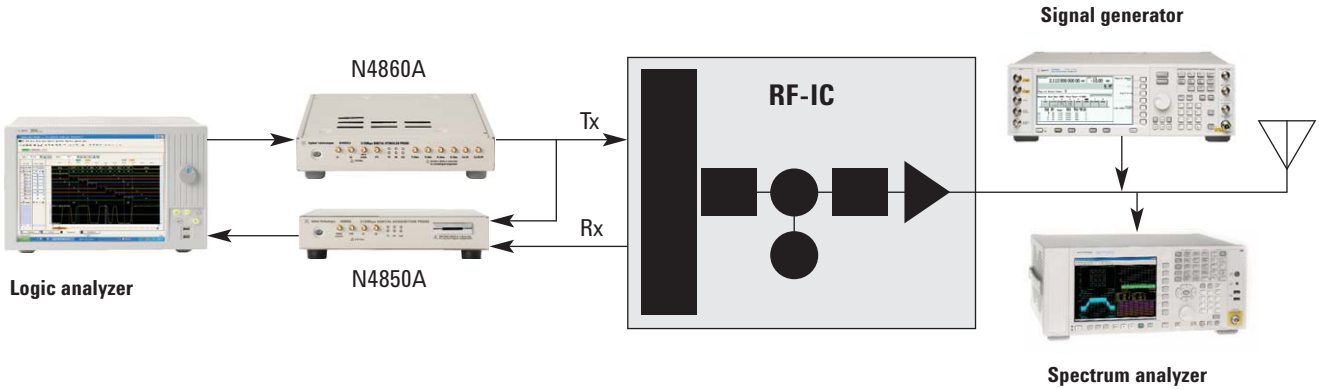


Figure 9. Test equipment configuration to verify RF-IC operation

The logic analyzer enables you to specify the desired RF-IC configuration. The specified configuration is embedded into DigRF v3 control packets. The N4860A stimulus probe outputs DigRF v3-compliant control packets that configure the RF-IC.

Digital IQ data can be loaded into the logic analyzer from a variety of sources, including Signal Studio and Advanced Design System (ADS). The logic analyzer embeds the IQ data in DigRF v3-compliant packets. The data packets are transferred to the RF-IC with the proper timing by the stimulus probe. The RF-IC processes the digital IQ data and generates an RF signal, which is characterized using a spectrum analyzer. Control packets, as specified by the user, can be inserted into the data packet flow while looping through the waveform. With this feature, you can make RF-IC configuration adjustments – like the gain setting of the RF amplifiers – interactively.

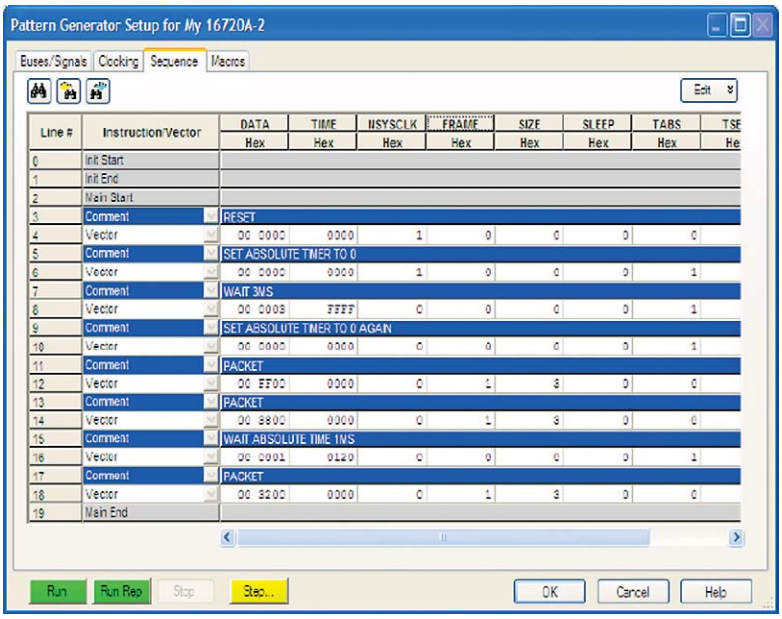


Figure 10. Conversion of control bit into DigRF v3 packets

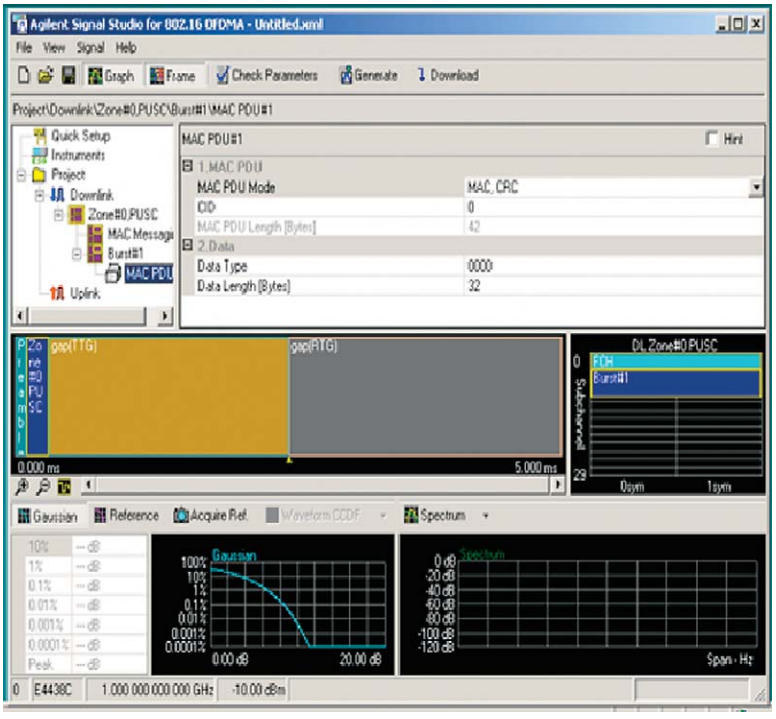


Figure 11. Generation of digital IQ representation of RF signal

Using the logic analyzer and stimulus probe, the RF-IC can be configured to receive an RF signal. The RF signal source generates the RF waveform of interest. The RF-IC processes the waveform and generates a DigRF v3 serial bit stream with the resulting digital IQ data. The acquisition probe captures the DigRF v3 data packets generated by the RF-IC and extracts the digital IQ data for analysis using the vector signal analysis package.

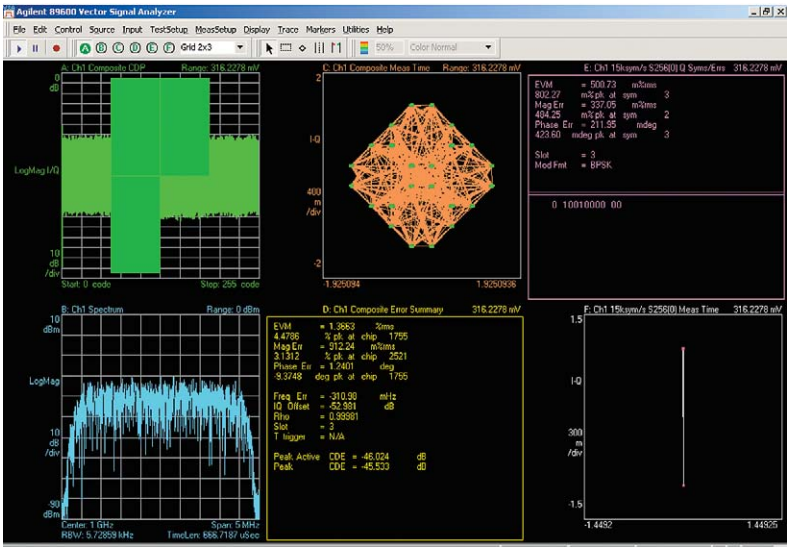


Figure 12. Vector signal analysis of digital IQ on the logic analyzer

BB-IC Evaluation

Figure 13 shows the test and measurement configuration that will enable BB-IC designers to verify operation of their components with the DigRF v3 interface. Visibility into the internal operation of the BB-IC is acquired by the logic analyzer through the BB-IC visibility port. The acquisition probe enables the logic analyzer to monitor traffic on the DigRF v3 Tx path as generated by the BB-IC. The stimulus probe can be configured to generate control and digital IQ data packets for the BB-IC over the DigRF v3 Rx path. Validation engineers can use these capabilities to evaluate many of the critical blocks within the BB-IC.

Visibility into the internal operation of the BB-IC can be achieved by monitoring the visibility port, which is designed into the BB-IC. Typically, you can track microcontroller and DSP operation through the visibility port. In this manner, control flow can be analyzed and internal processing of digital IQ can be tracked.

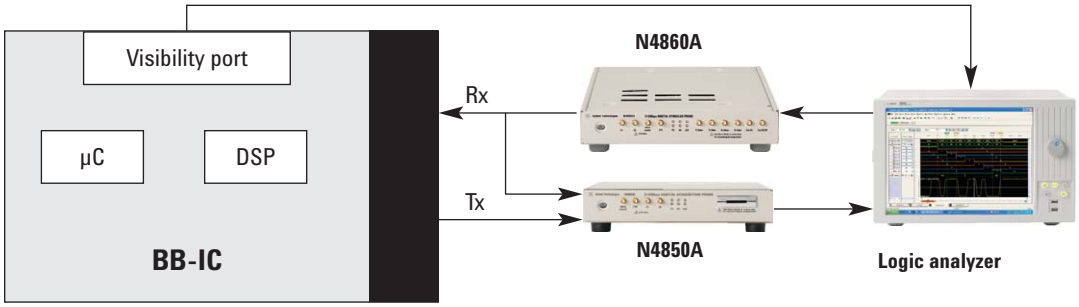


Figure 13. Test equipment configuration needed to verify BB-IC operation

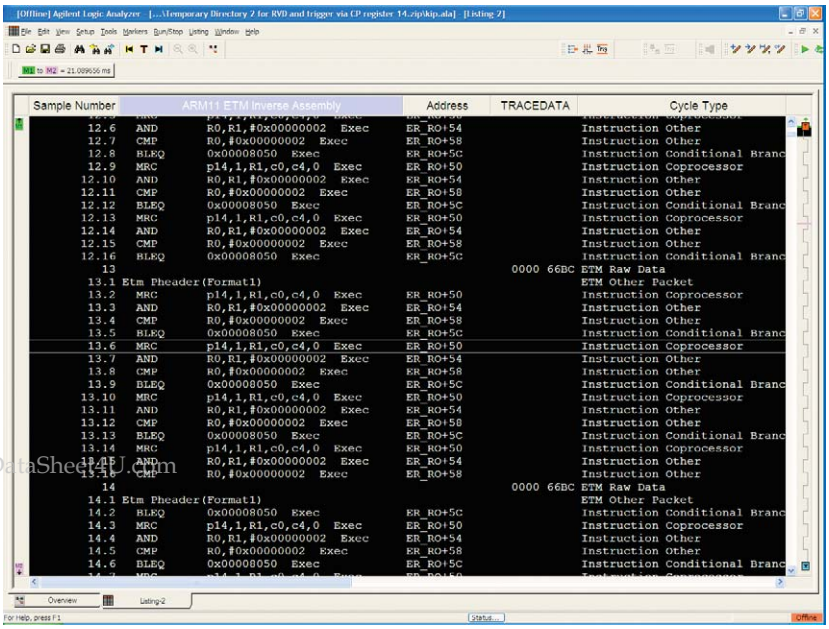


Figure 14. Decoder view of BB-IC internal operation

The N4850A acquisition probe captures the Tx traffic generated by the BB-IC. The control packets are identified by the logic analyzer, decoded and displayed on the logic analyzer using the packet viewer. Debug and validation of the configuration and control functions of the BB-IC/RF-IC interface are accelerated by using these capabilities.

The N4850A acquisition probe captures the Tx traffic generated by the BB-IC. The data packets are identified and the digital IQ data is extracted from these packets using the signal extractor tool. The digital IQ data is analyzed by the 89601A vector signal analysis tools running on the logic analyzer. These capabilities enable BB-IC validation team to validate that the digital IQ was properly converted to DigRF v3 format. In addition, the DSP algorithms that generated the IQ can be evaluated.

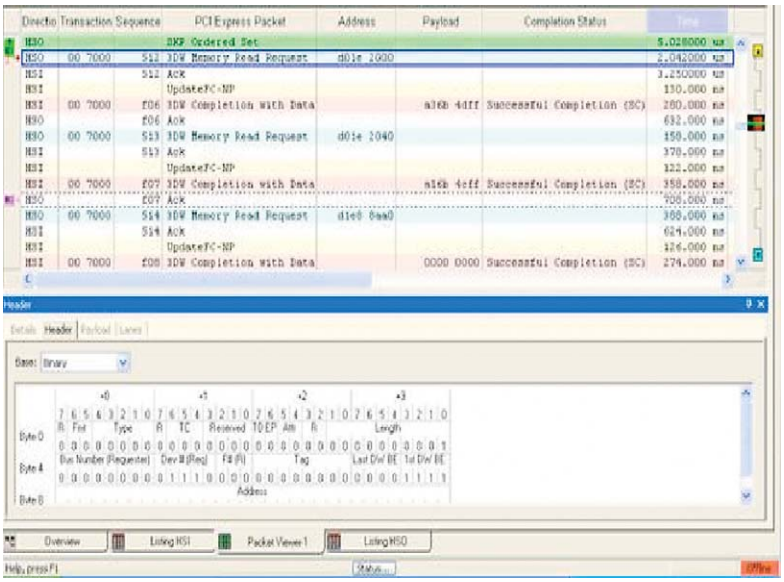


Figure 15. Protocol decode view of DigRF v3 control traffic

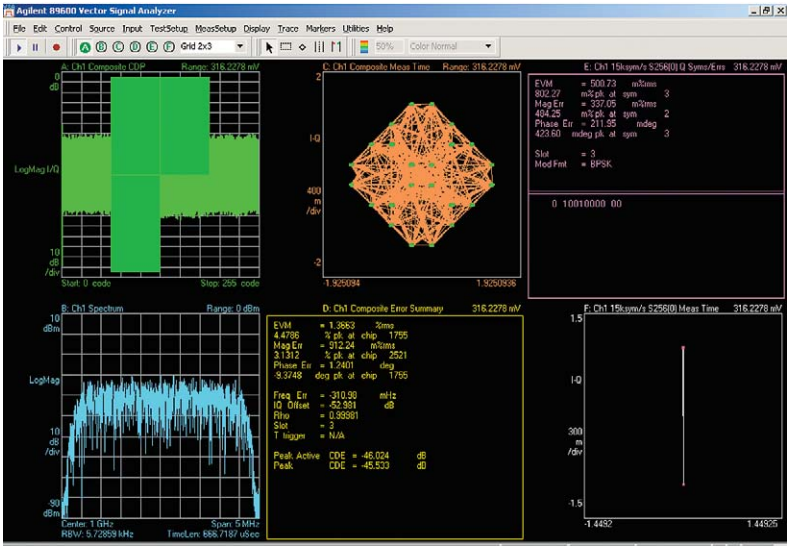


Figure 16. Vector signal analysis of DigRF v3 digital IQ

Digital IQ data and control signals are formatted into DigRF v3-compliant packets on the logic analyzer. The N4860A stimulates the BB-IC with the specified data and control packets. In this manner, BB-IC validation teams can analyze how the BB-IC handles the breadth of status and control responses that an RF-IC could generate and how the BB-IC handles various digital IQ streams.

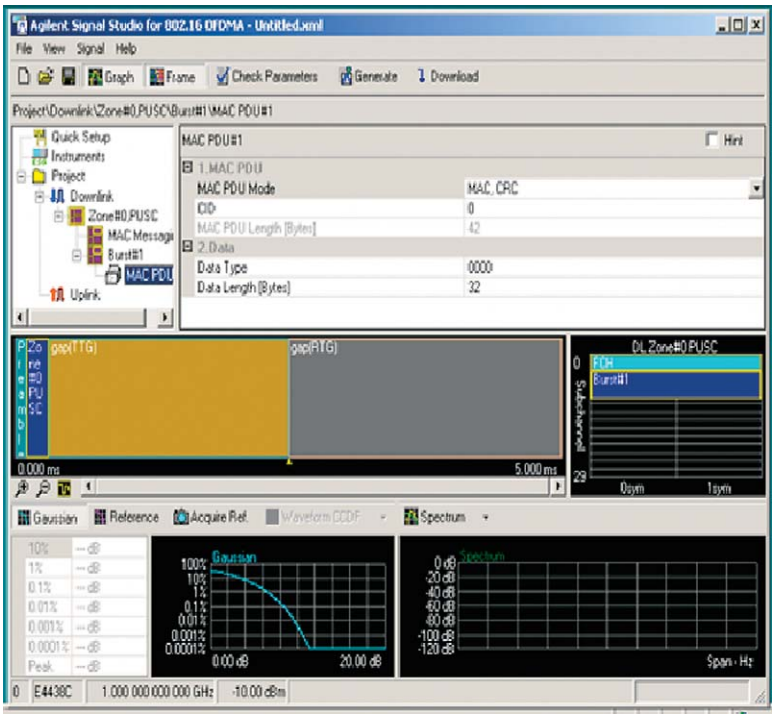


Figure 17. Generation of digital IQ representation of RF signals using Signal Studio

Characteristics for N4850A DigRF v3 Digital Acquisition Probe

Features	Benefits
Supports state analysis of DigRF v3 standard; 2.5G and 3GPP air standards – e.g. GSM, EDGE, CDMA, CDMA-2K, W-CDMA	Validate and troubleshoot handsets and mobile wireless devices incorporating DigRF v3 across a wide variety of over-air standards
Maximum acquisition speed: 312 Mbps	Run at any DigRF v3-compliant operating mode (sleep, low, medium, high speed) with performance headroom
Supports Voltage Level compliant with standard	Acquire traffic, no matter which DigRF v3-compliant voltage level you are using.
SysClk speed support: 19.2 MHz, 26.0 MHz, 38.4 MHz	Acquire traffic, no matter which DigRF v3-compliant speed you are using
Tracks changes in speed modes	Verify mode change algorithms real time with a single acquisition
Acquire 17 differential channels	Simultaneously monitor a Tx/Rx bidirectional bus, even with Tx and Rx running at different bus modes
Converts serial bus stream to parallel format	Parallel format enables you to trigger on protocol-specific packets, specific bits within a packet (for example, control bits within a packet), and protocol violations – getting you to the root cause of a problem quicker. In addition, combine the parallel format with a logic analyzer that has deep acquisition memory to capture even more system activity, in both directions, for analysis and debug.
DigRF v3 protocol decoder and packet viewer	Quickly analyze and debug DigRF v3 digital control and raw IQ data in an intuitive format. The packet viewer lets you operate at the packet level or view detailed information for each individual packet.
LEDs: Two each for Tx, Rx, and CLK Tx: Speed and synchronization status Rx: Speed and synchronization status CLK: SysClk is enabled, disabled	Quickly identify the status of your system by just looking at the probe. DigRF v3 error detection includes: Tx/Rx • Detected data speed does not match requested speed • Unable to locate stable data; excessive jitter impacts data eye closure • Too little time between SysClk toggling to data toggling (time definition is user defined) Clock • Clock stopped in the middle of a frame • SysClk toggling when SysClkEN is false • Start-of-frame sync not found even though data is toggling
Select the specific Tx/Rx signals, control, and data information to be captured by the logic analyzer	Focus only on the data you want to see

Characteristics for N4850A DigRF v3 Digital Acquisition Probe (continued)

Features	Benefits
Extract and transfer digital IQ generated from your over-air data to 89600 VSA software	Rapidly work through scenarios that let you identify RF signal problems quickly and fine tune your DSP algorithm
Connection port to N4860A digital stimulus probe	Perform comprehensive stimulus and acquisition testing
Identifies invalid sync words so you can trigger on them with an external device, like an oscilloscope	Quickly identify faults in order to perform functional and parametric analysis around the fault condition
Supports up to 2048 bits for user-defined payload	The tools provide support for your custom data packets
Stack or rack multiple N4850A acquisition or N4860A stimulus probes	The small probe minimizes the footprint of test equipment next to the device under test
Configuration files	Saves time and simplifies measurement setup
Probe the device under test with a variety of differential probes: E5381A flying leads, E5387A or 5495A soft touch connectorless probes, or the E5379A Samtec probe	The high-bandwidth E5381A differential flying leads provide the highest signal-quality measurement. In addition, probing flexibility allows you to use soft touch or Samtec probes.
Correlate DigRF v3 activity with microcontroller and DSP operation	A correlated system view enables you to rapidly isolate defects and verify system operation

Characteristics for N4860A 312-Mbps Digital Stimulus Probe

Features	Benefits
Pattern generator loop macros	Provide continuous DigRF v3 stimulus to replace a missing DigRF v3-based BB-IC or RF-IC
Maximum stimulus speed: 312 Mbps	Run at any DigRF v3-compliant operating mode (sleep, low power or high speed) with performance headroom
Stimulus Voltage Level compliant with standard	Generate DigRF v3 traffic, no matter which DigRF v3-compliant voltage level you are using
SysClk speed support: 26.0 MHz	Generate DigRF v3 traffic, no matter which DigRF v3-compliant speed you are using.
Connect to target via SMA connectors	Provide stimulus to compensate for a missing BB-IC or RF-IC
Modify critical control settings while looping (e.g. adjust RF-IC amplifier gain)	See how your device or system responds without stopping the stimulus probe to change control settings
Create digital control and data stimulus in a simple ASCII format using Signal Studio, Advanced Design System (ADS), a captured logic analyzer trace, or a custom programming package	Use your tool of choice to generate your stimulus data
Convert raw IQ ASCII data and user-defined control information to DigRF v3-compliant data and control packets	Automation saves time and eliminate errors
User specification of order and timing of control and data packets.	Evaluate the DUT under a variety of control configurations, data patterns, and timing sequences. NOTE: Stimulus order and timing of control and data packets is determined when the N4860A is set up. Order and timing of data and control packets is NOT altered in response to the "Clear To Send" when stimulating the RF-IC.

N4850A and N4860A Physical Characteristics

Dimensions

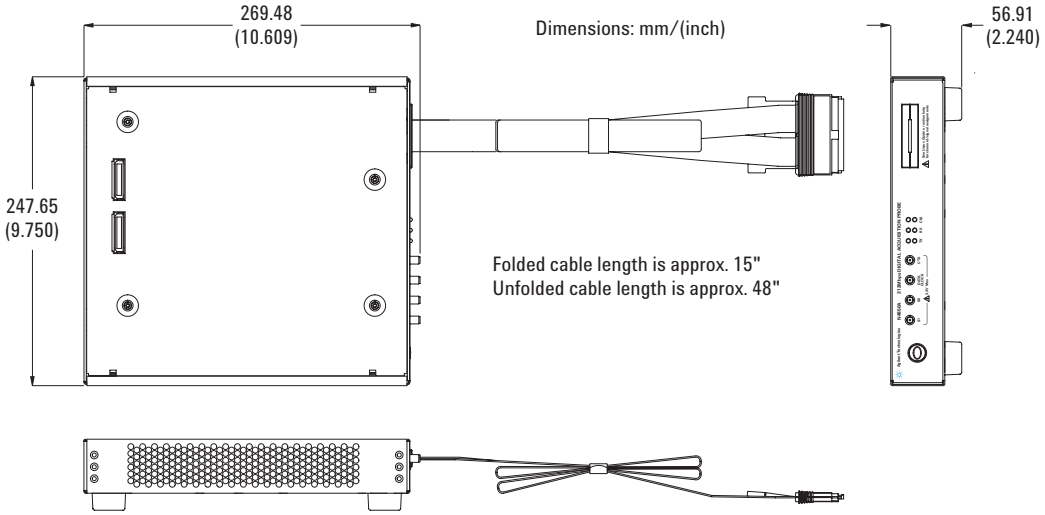


Figure 18. N4850A exterior dimensions

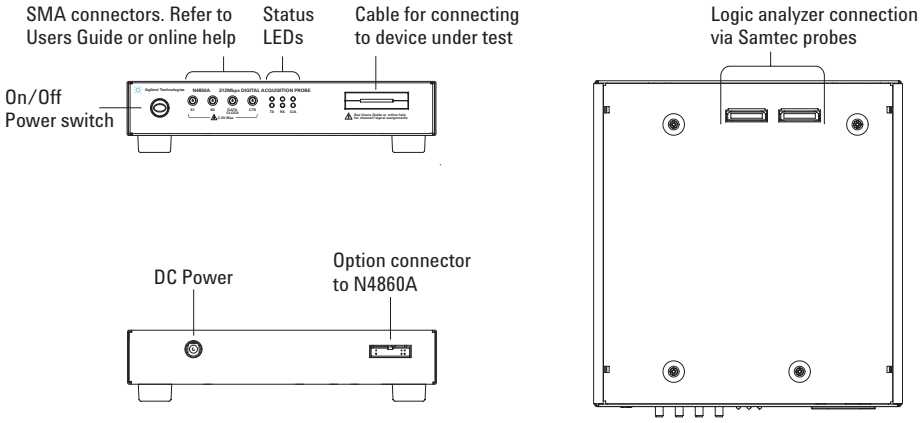


Figure 19. N4850A front panel, rear panel, and top view

N4850A and N4860A Physical Characteristics (continued)

Dimensions

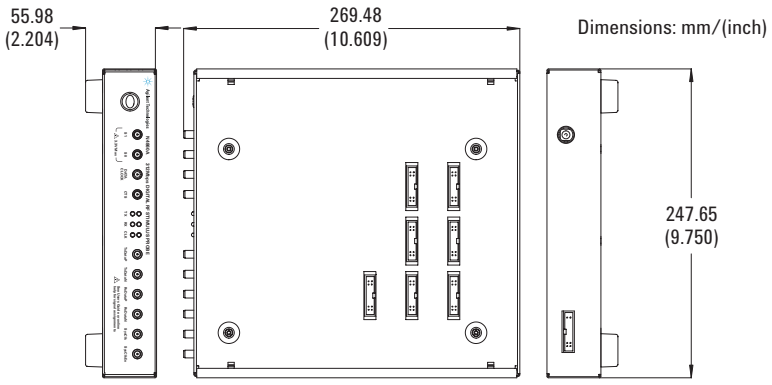


Figure 20. N4860A exterior dimensions

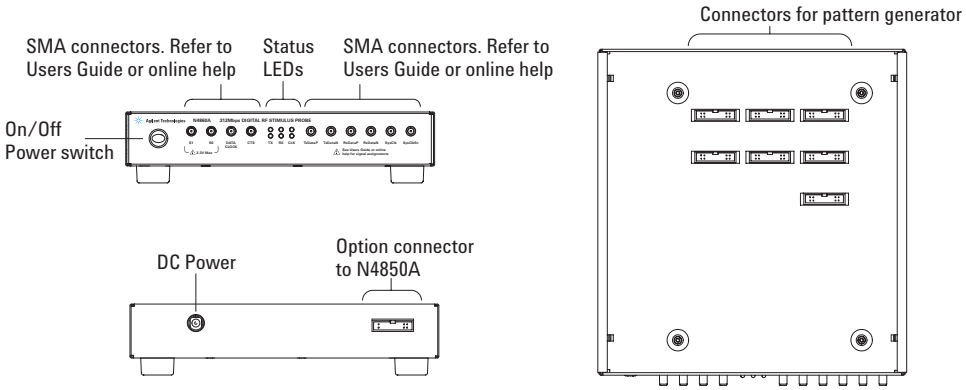


Figure 21. N4860A front panel, rear panel, and top view

Power

12 V and 5 A (60 W) max

Weight

Max net	2.0 kg (4.4 lbs)
Max shipping	4.5 kg (10.0 lbs)

Instrument operating environment

Temperature	0 °C to 55 °C (32 °F to 131 °F)
Altitude	To 3000 m (10,000 ft)
Humidity	8 to 80% relative humidity at 40 °C (104 °F)

Ordering Information

When you configure your DigRF v3 measurement system,consider the following:

1. **Ability to provide DigRF v3 stimulus:** For comprehensive stimulus and response testing of your DigRF v3 device or system, select a logic analyzer with digital pattern generation capability (16822A, 16823A, or a 16900 modular logic analysis system with a 16720A pattern generator module).

2. **Flexibility to grow as your measurement needs evolve:** A modular 16900 Series logic analyzer addresses your measurement needs today and allows you to grow as your needs evolve.

3. **Modification of the logic analyzer's DigRF v3 protocol decoder:** The DigRF v3 standard provides the flexibility to customize your control structure and data packets for your specific application. With the B4641A protocol development kit, you can modify the logic analyer's DigRF v3 protocol decoder to track your custom solution.

Target design and test equipment requirements for DigRF v3 digital acquisition and stimulus measurements

In addition to compatible measurement equipment, the device under test (DUT) requires the following to ensure proper acquisition and stimulus of the DUT.

DUT requirements for the N4850A acquisition probe:

- Access to SysClk to determine when data is valid on the serial bus

- Probing connection for the acquisition probe, preferably at the receiver. Please refer to the N4850A User Guide and the Agilent N4850A Design Guide (N4850-97002) for information on designing a connection with good signal integrity.

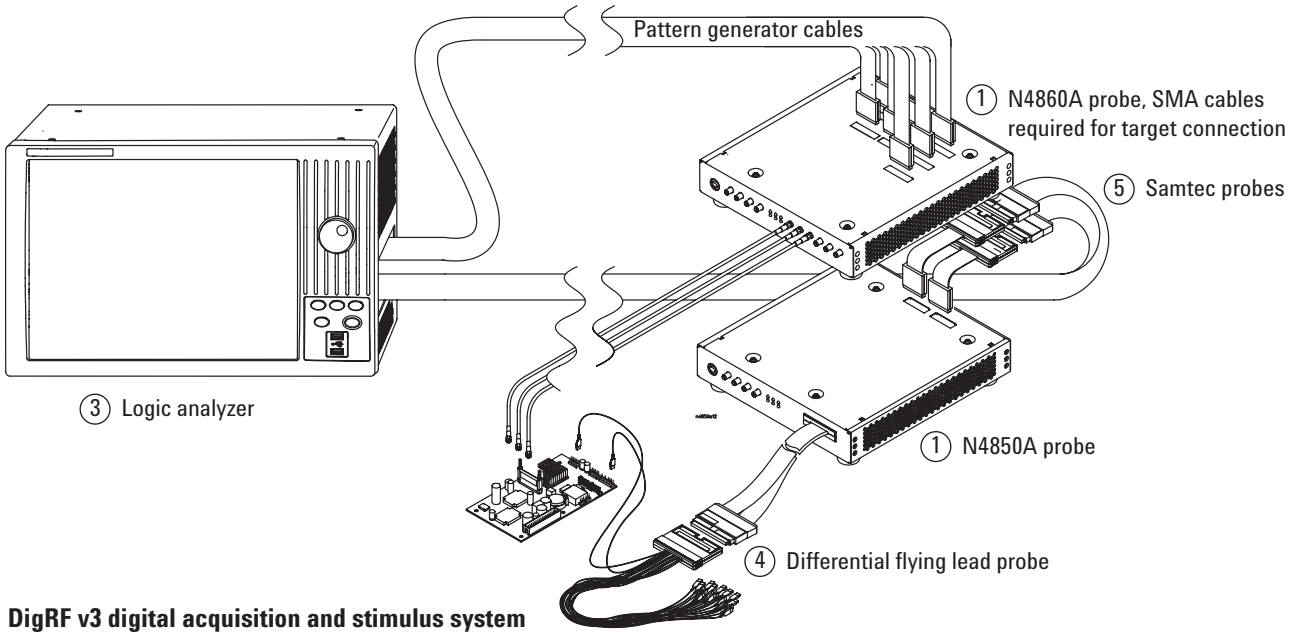
DUT requirements for use with N4860A stimulus probe:

- SMA (m-m) connectors on the target. The number of SMA connectors depends on your test scenario: BB-IC turn on, RF-IC validation, or system integration

- Place a 50-ohm termination resistor between the positive and negative differential pair

Ordering Information (continued)

To configure a complete DigRF v3 digital acquisition and stimulus system, you will need to order or have the following items:



DigRF v3 digital acquisition and stimulus system

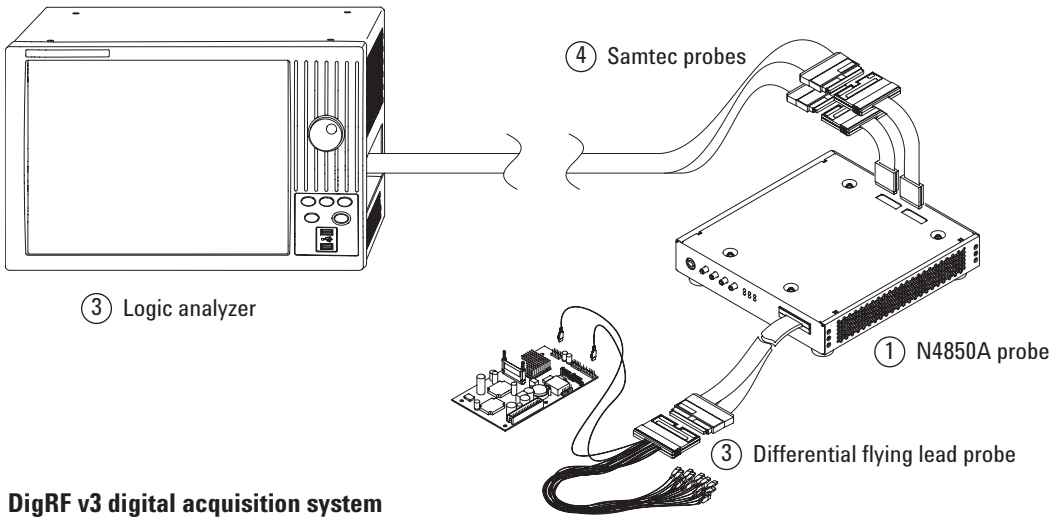
			Probes between the N4850A and the...	
1. DigRF v3 probes[1] (One each per Tx/Rx pair)	**2. Method to create IQ data**	**3. Logic analyzer with 48-channel pattern generator[2]**	**4. Device under test (One of the following for each N4850A)**	**5. Logic analyzer (Two Samtec probes per N4850A – one for Tx and one for Rx. Select probe that is compatible with your logic analyzer)**
N4860A 312 Mbps digital stimulus probe • N4860A-040: Set of four 40 inch SMA cables N4850A 312 Mbps digital acquisition probe • -010 for node-locked license • -020 for floating (server) license	• Signal Studio • ADS • Convert captured logic analyzer trace to stimulus • Custom programmatic generation	16800 Series portables • 16822A – 68 ch • 16823A – 102 ch 16900 Series modular mainframe with at least one each of the following: • 16900 Series module(s) • 16720A pattern generator module	• E5381A differential flying lead probe • E5405A differential pro series soft touch probe • E5387A differential soft touch probe • E5379A differential Samtec probe	• E5385A for logic analyzers with a 40-pin cable connection (16822A, 16823A, 16910/11A) • E5378A for logic analyzers with a 90-pin cable connection (1695X modules)

1 N4860A digital stimulus probe requires an N4850A digital acquisition probe to operate

2 Compatible with 16800 or 16900 Series logic analyzers with 68 channels or more. Diversity mode requires use of a 16900 modular system with one 68-channel (or more) logic analyzer module for each Tx/Rx pair.

Ordering Information (continued)

To configure a complete DigRF v3 digital acquisition system, you will need to order or have the following items:



DigRF v3 digital acquisition system

		Probes between the N4850A and the...	
1. DigRF v3 probes (One per Tx/Rx pair)	**2. Logic analyzer[1]**	**3. Device under test (One of the following for each N4850A)**	**4. Logic analyzer (Two Samtec probes per N4850A – one for Tx and one for Rx. Select probe that is compatible with your logic analyzer)**
N4850A 312-Mbps digital acquisition probe • -010 for node-locked license • -020 for floating (server) license	16800 Series portables • 16802A – 68 ch • 16803A – 102 ch • 16804A – 136 ch • 16806A – 204 ch • 16822A – 68 ch • 16823A – 102 ch 16900 Series modular mainframe with at least one 16900 Series module	• E5381A differential flying lead probe • E5405A differential pro series soft touch probe • E5387A differential soft touch probe • E5379A differential Samtec probe	• E5385A Samtec probe for logic analyzers with a 40-pin cable connection (16800 Series, 16910/11A) • E5378A Samtec probe for logic analyzers with a 90-pin cable connection (1695X modules)

1 Compatible with 16800 or 16900 Series logic analyzers with 68 channels or more

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LXI

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LXI is the LAN-based successor to GPIB, providing faster, more efficient connectivity. Agilent is a founding member of the LXI consortium.

Remove all doubt

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Related literature

Publication title	Publication type	Publication number
Agilent 16800 Series Portable Logic Analyzers	Data sheet	5989-5063EN
Agilent 16900 Series Logic Analysis Mainframes	Data sheet	5989-0421EN
Probing Solutions for Agilent Technologies Logic Analyzers	Catalog	5968-4632E

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