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32Mb Ultra-Low Power Asynchronous CMOS PSRAM

2M x 16 bit

Overview

The N32T1630C1E is an integrated memory device containing a 32 Mbit Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 2,097,152 words by 16 bits. It is designed to be identical in operation and interface to standard 6T SRAMS. The device is designed for low standby and operating current and includes a power-down feature to automatically enter standby mode. Also included are several other power saving modes: a deep sleep mode where data is not retained in the array and partial array refresh mode where data is retained in a portion of the array. Both these modes reduce standby current drain. The device can operate over a very wide temperature range of -25°C to +85°C.

Features

- **Dual voltage for Optimum Performance:**
  Vccq - 2.7V to 3.3V
  Vcc - 2.7V to 3.3V
- **Fast Cycle Times**
  T_{ACC} < 60 nS
  T_{ACC} < 70 nS
- **Very low standby current**
  I_{SB} < 120µA
- **Very low operating current**
  Icc < 25mA
- **Dual rail operation**
  V_{CCQ} and V_{SSQ} for separate I/O power rail
- **Compact Space Saving BGA Package**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply	Speed	Standby Current (I_{SB}), Max	Operating Current (Icc), Max
N32T1630C1EZ	48-BGA	-25°C to +85°C	2.7V - 3.3V(V_{CC})	60ns 70ns	120 µA	3 mA @ 1MHz

Figure 1: Pin Configuration

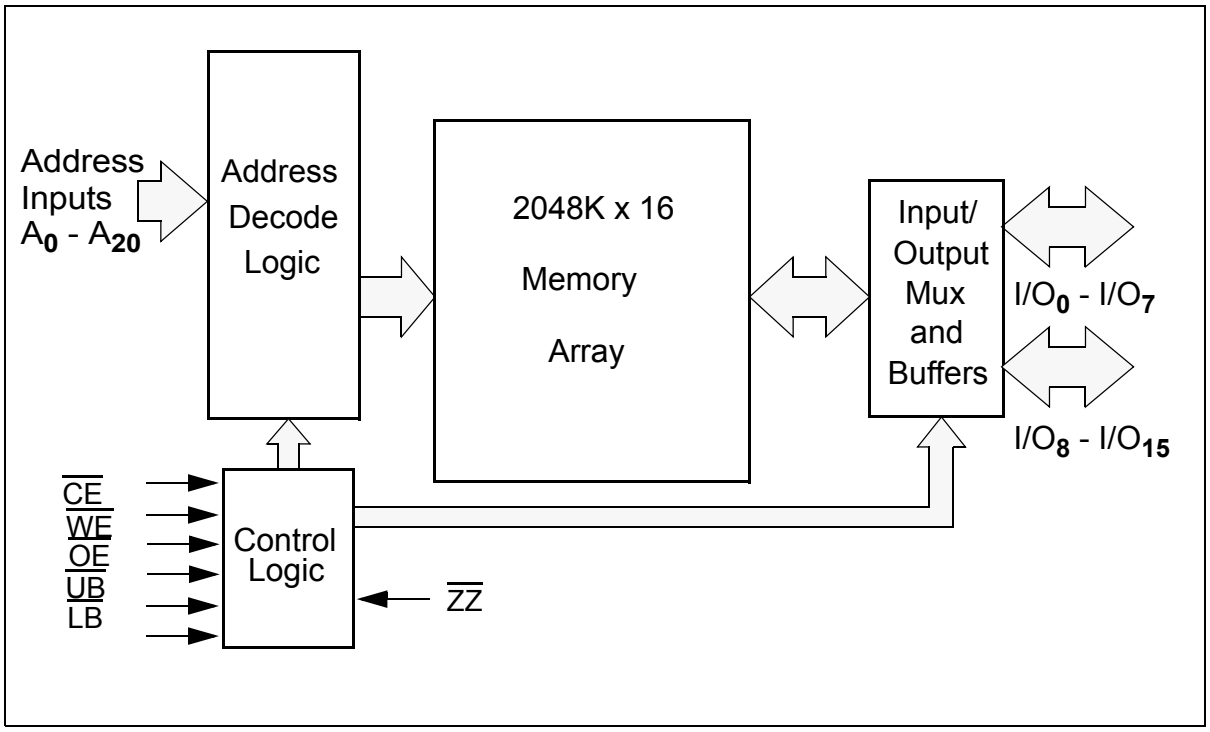
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	$\overline{ZZ}$
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SSQ}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CCQ}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{20}

48 Pin BGA (top)
6 x 8 mm

Table 1: Pin Descriptions

Pin Name	Pin Function
A_0-A_{20}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
$\overline{ZZ}$	Deep Sleep Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
V_{CCQ}	Power I/O only
V_{SSQ}	Ground I/O only

Functional Block Diagram



Functional Description

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$/$\overline{LB}$	$\overline{ZZ}$	I/O[1]	MODE	POWER
H	X	X	X	H	High Z	Standby[2]	Standby
X	X	X	H	H	High Z	Standby[2]	Standby
L	L	X[3]	L[1]	H	Data In	Write[3]	Active
L	H	L	L[1]	H	Data Out	Read	Active
L	H	H	L[1]	H	High Z	Output Disabled	Active
H	X	X	X	L	High Z	Low Power Modes	Low Power

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - IO_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown. If both $\overline{UB}$ and $\overline{LB}$ are in the deselect mode (high), the chip is in a standby mode regardless of the state of $\overline{CE}$.

2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.2 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.2 to 3.6	V
Power Dissipation	P_D	1	W
Storage Temperature	T_{STG}	–65 to 125	°C
Operating Temperature	T_A	-25 to +85	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Comments	Min.	Typ[1]	Max.	Unit
Supply Voltage	V_{CC}		2.7	3.0	3.3	V
Supply Voltage for I/O	V_{CCQ}		2.7	3.0	3.3	V
Input High Voltage	V_{IH}		$0.8V_{CCQ}$		V_{CC}+0.2	V
Input Low Voltage	V_{IL}		–0.2		$0.2V_{CCQ}$	V
Output High Voltage	V_{OH}	I_{OH} = -0.5mA	$0.8V_{CCQ}$			V
Output Low Voltage	V_{OL}	I_{OL} = 0.5mA			$0.2V_{CCQ}$	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	-1		1	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled	-1		1	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=V_{CC}MAX, V_{IN}=V_{IH} / V_{IL} Chip Enabled, I_{OUT} = 0			3	mA
Read/Write Operating Supply Current @ Min Cycle Time[2]	I_{CC2}	V_{CC}=V_{CC}MAX, V_{IN}=V_{IH} / V_{IL} Chip Enabled, I_{OUT} = 0			25	mA
Standby Current	I_{SB}	Chip deselected, $\overline{CE}$>VCC-0.2, $\overline{ZZ}$>VCC-0.2 and VIN = 0 or VCC			120	µA

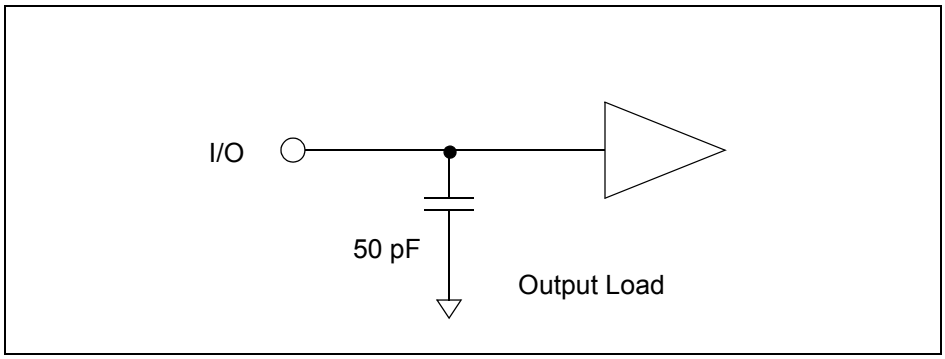
1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9\ V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5\ V_{CC}$
Operating Temperature	-25 °C to +85 °C

Output Load Circuit



Power Up Sequence

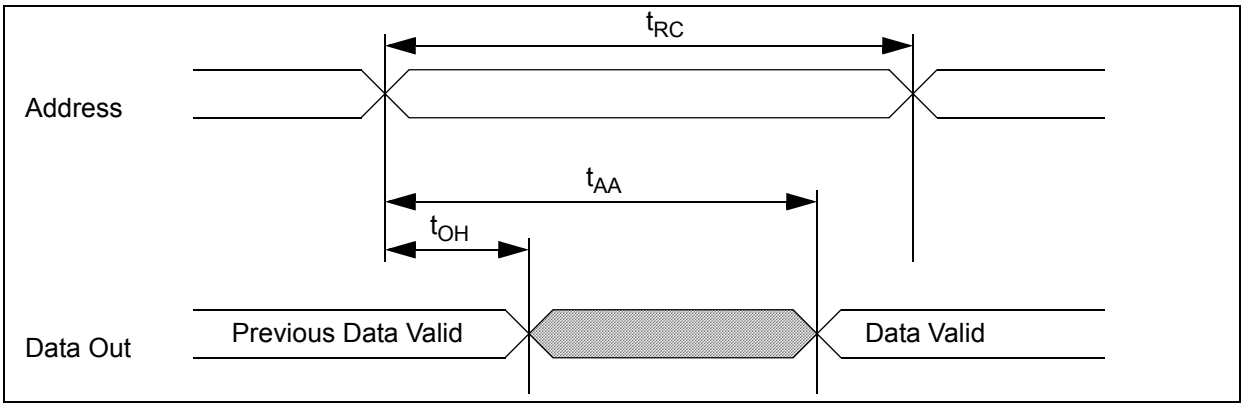
After applying power, maintain a stable power supply for a minimum of 200us after $\overline{CE}$ > VIH.

Timings

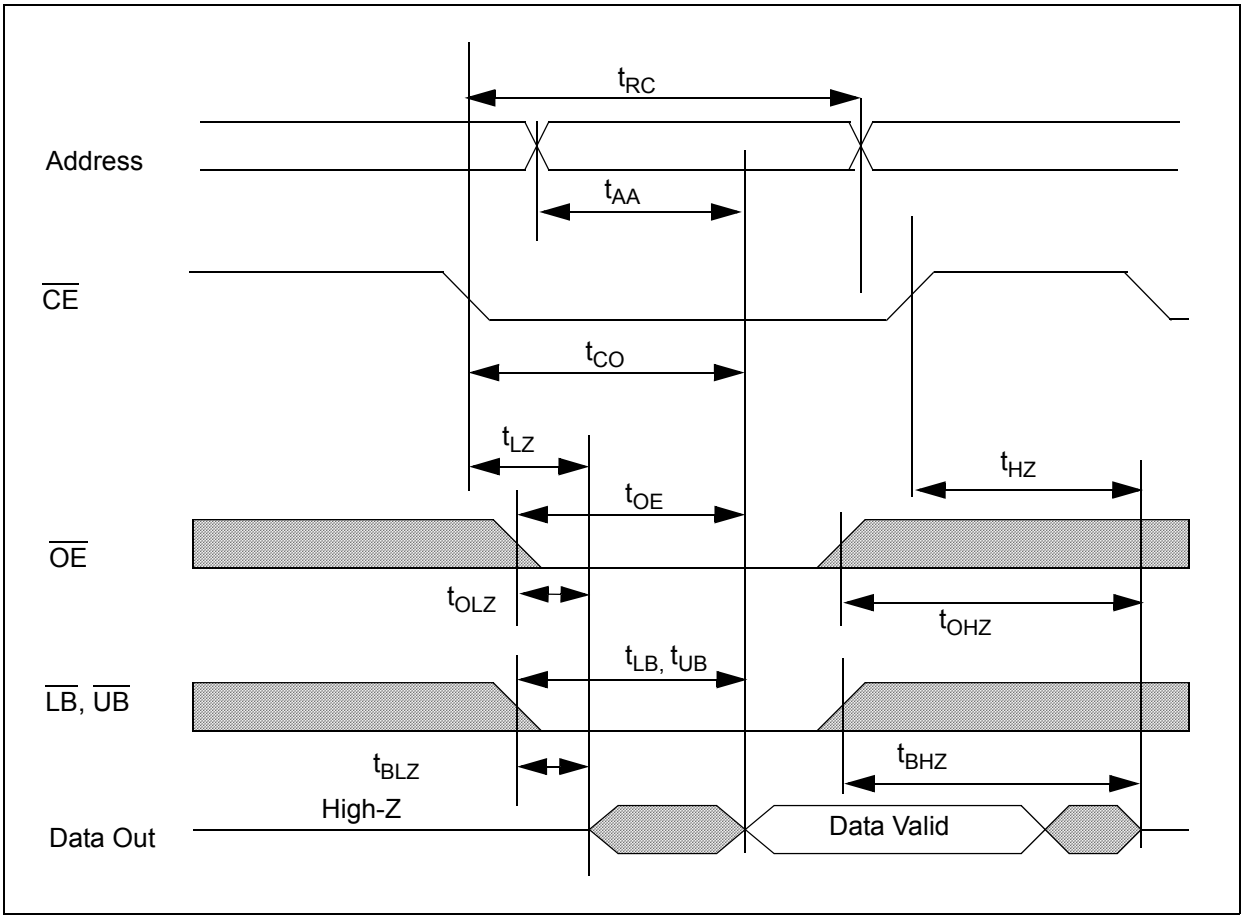
Item	Symbol	-60		-70		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	60	20000	70	20000	ns
Address Access Time	t_{AA}		60		70	ns
Page Mode Read Cycle Time	t_{PC}	25	20000	25	20000	ns
Page Mode Access Time	t_{PA}		25		25	ns
Chip Enable to Valid Output	t_{CO}		60		70	ns
Output Enable to Valid Output	t_{OE}		25		25	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		60		70	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{BZ}	10		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	5	0	5	ns
Output Disable to High-Z Output	t_{OHZ}	0	5	0	5	ns
Byte Select Disable to High-Z Output	t_{BHZ}	0	5	0	5	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Write Cycle Time	t_{WC}	60	20000	70	20000	ns
Page Mode Write Cycle Time	t_{PWC}	25	20000	25	20000	ns
Chip Enable to End of Write	t_{CW}	50		60		ns
Address Valid to End of Write	t_{AW}	50		60		ns
Byte Select to End of Write	t_{BW}	50		60		ns
Write Pulse Width	t_{WP}	50		50		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		5		5	ns
Address Setup Time	t_{AS}	0		0		ns
Data to Write Time Overlap	t_{DW}	20		20		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns
Maximum Page Mode Cycle	t_{PGMAX}		20000		20000	ns
Chip Enable High Pulse Width	t_{CP}	10		10		ns

Do not access device with invalid cycle time (shorter than tRC, tWC) for a continous period > 20us.

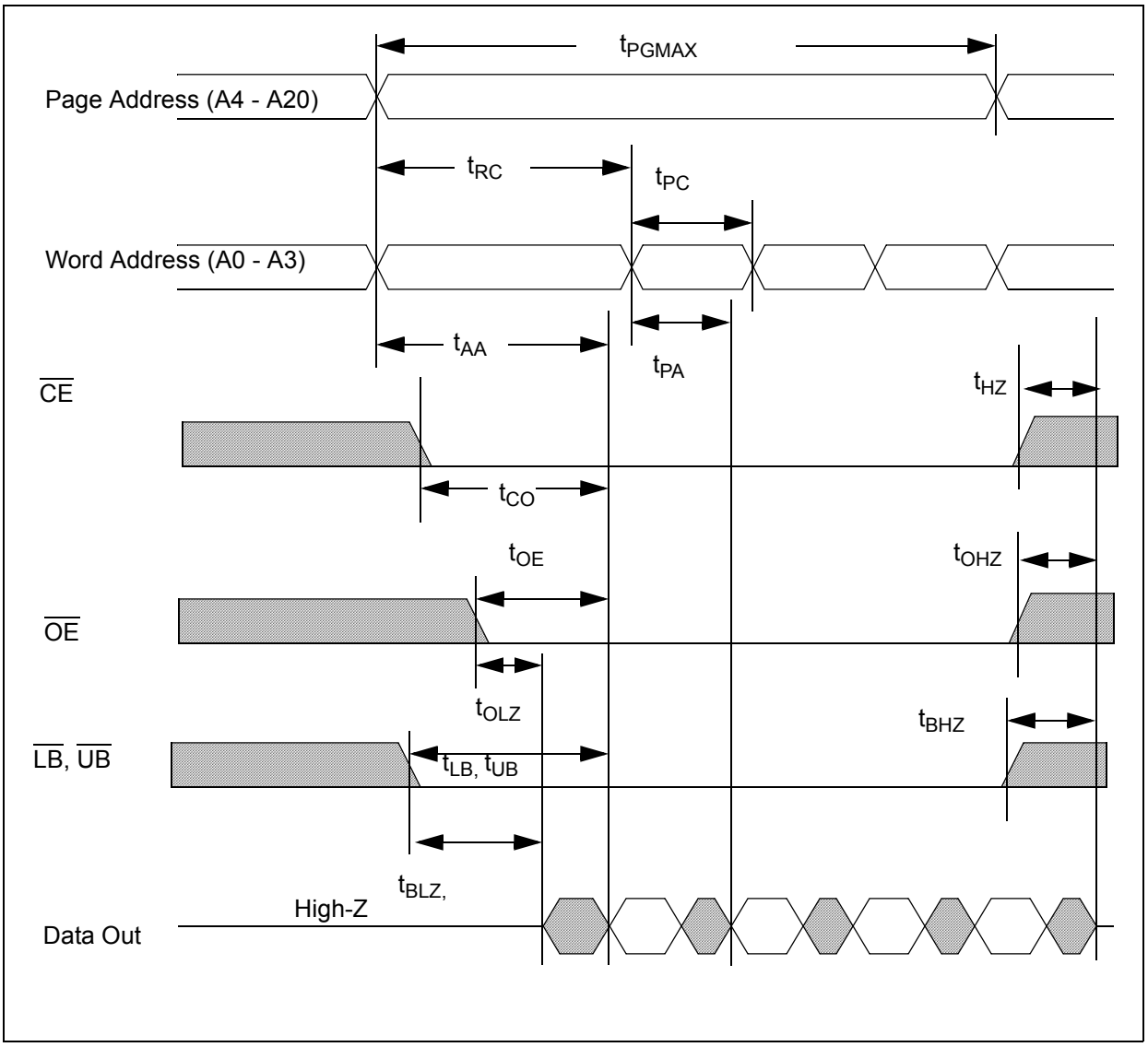
Timing of Read Cycle ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = $\overline{ZZ}$ = V_{IH})



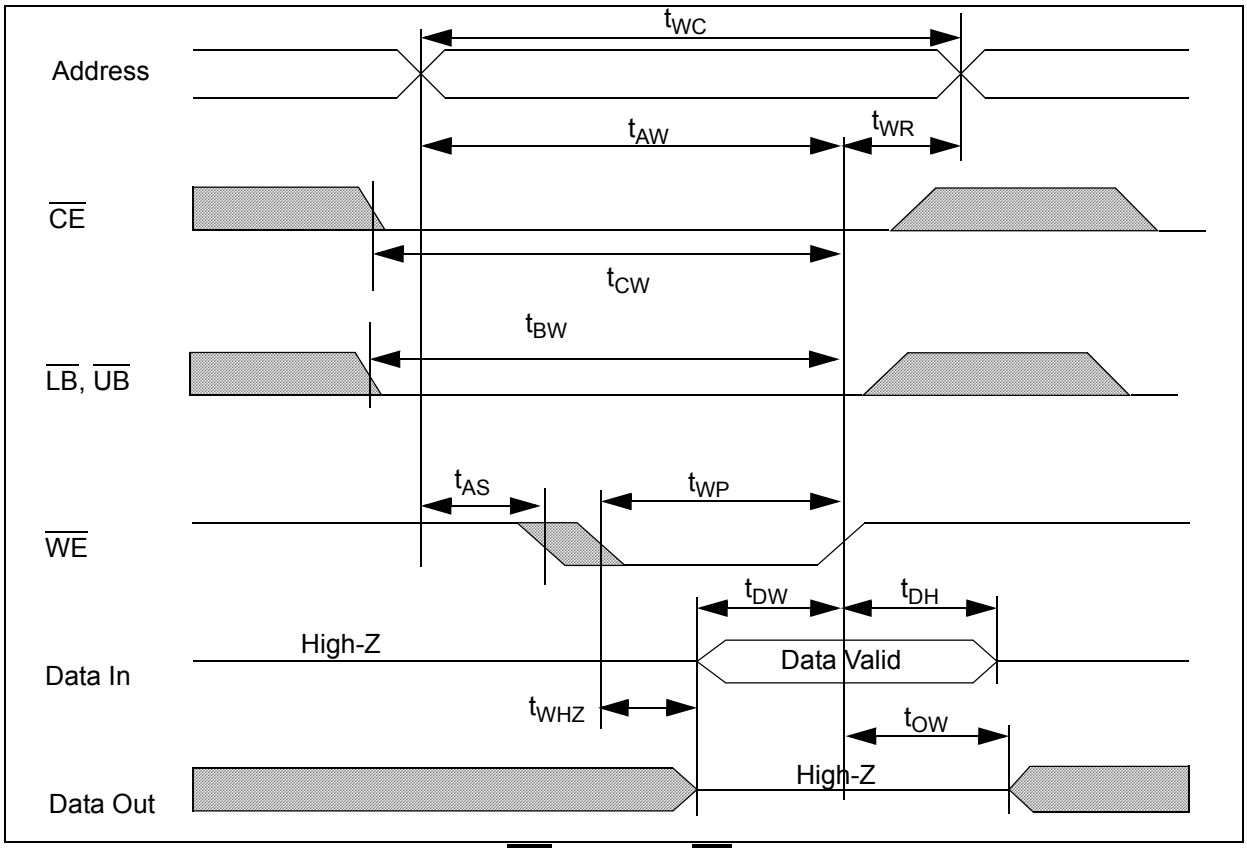
Timing Waveform of Read Cycle ($\overline{WE}$ = $\overline{ZZ}$ = V_{IH})



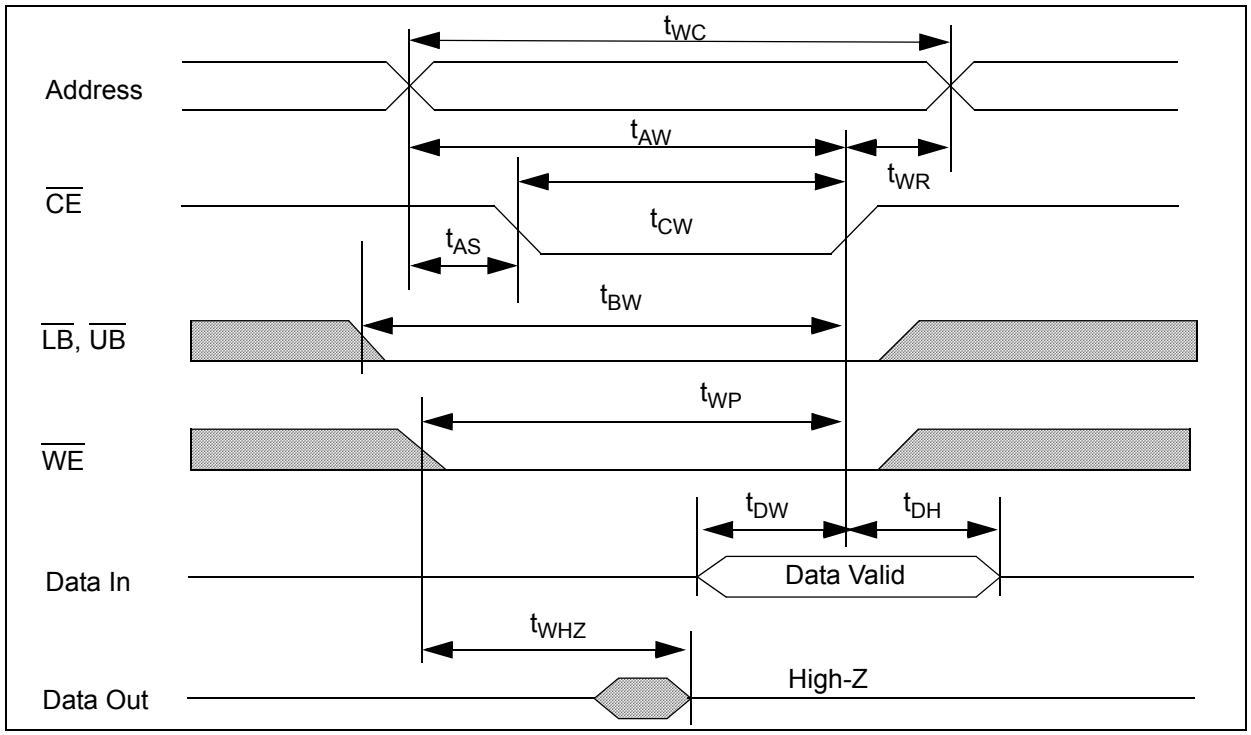
Timing Waveform of Page Mode Read Cycle ($\overline{WE}$ = $\overline{ZZ}$ = V_{IH})



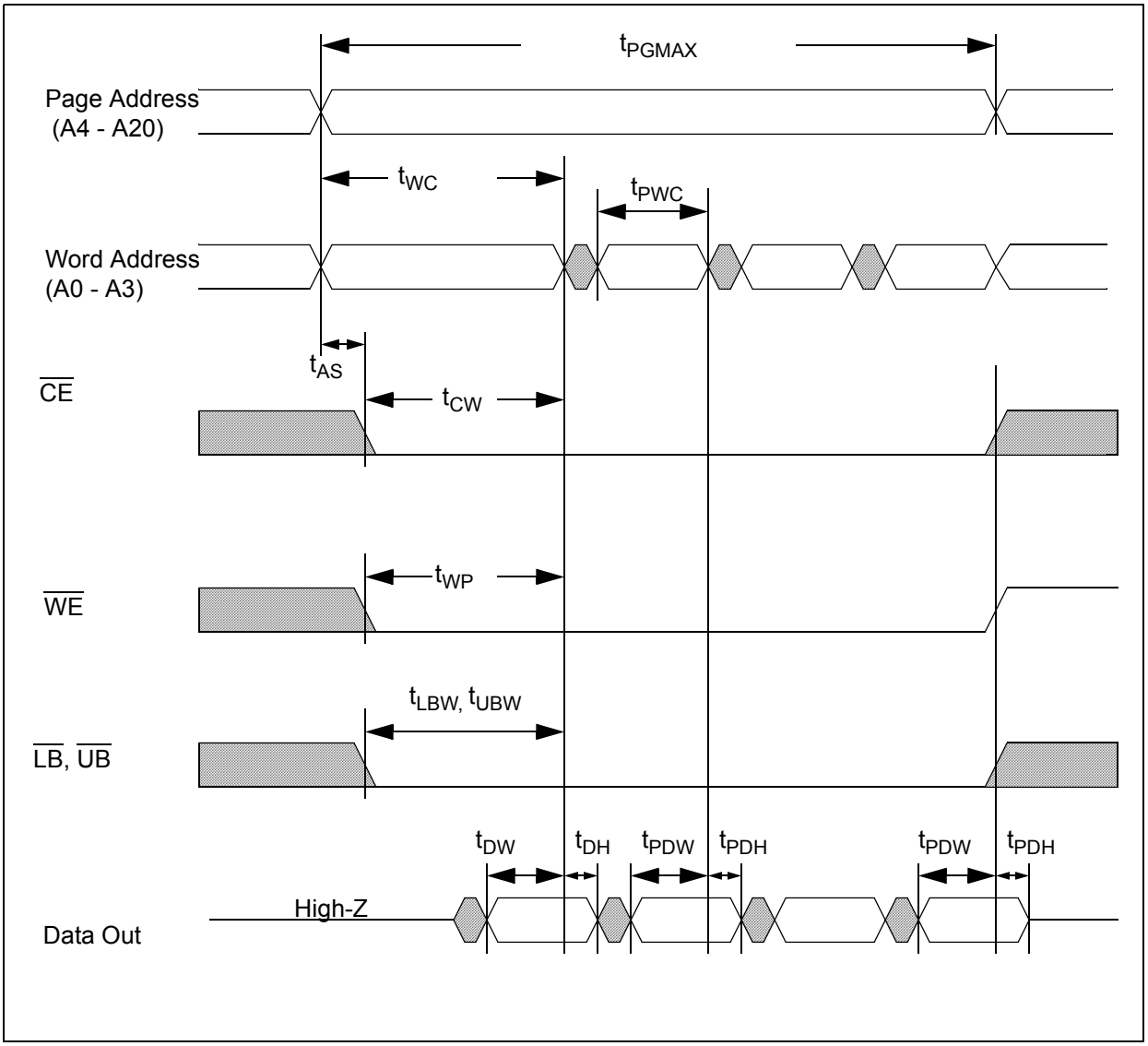
Timing Waveform of Write Cycle ($\overline{WE}$ control, $\overline{ZZ}$ = V_{IH})



Timing Waveform of Write Cycle ($\overline{CE}$ Control, $\overline{ZZ}$ = V_{IH})



Timing Waveform of Page Mode Write Cycle ($\overline{ZZ}$ = V_{IH})



Power Savings Modes

The three low power modes are:

- **Reduced Memory Size**
- **Partial Array Refresh**
- **Deep Sleep Mode**

The operation of the power saving modes is controlled by setting the Variable Address Register (VAR). This VAR is shown in the following “Variable Address Register” figure and is used to enable/disable the various low power modes. The VAR is set by using the timings defined in the figure titled “Variable Address Register (VAR) Update Timings”. The register must be set in less then 1us after $\overline{ZZ}$ is enabled low.

1) Reduced Memory Size (RMS)

In this mode of operation, the 32Mb PSRAM can be operated as a 8Mb or 16Mb device. The mode and array size are determined by the settings in the VA register. The VA register is set according to the following timings and the bit settings in the table “Address Patterns for RMS”. The RMS mode is enabled at the time of ZZ transitioning high and the mode remains active until the register is updated. To return to the full 32Mb address space, the VA register must be reset using the previously defined procedures. While operating in the RMS mode, the unselected portion of the array may not be used.

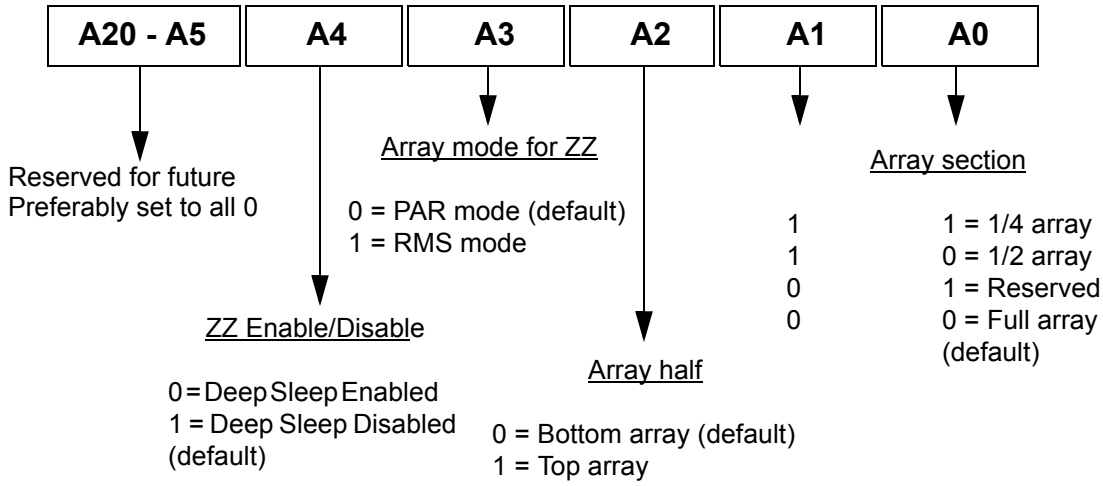
2) Partial Array Refresh (PAR)

In this mode of operation, the internal refresh operation can be restricted to a 8Mb or 16Mb portion of the array. The mode and array partition to be refreshed are determined by the settings in the VA register. The VA register is set according to the following timings and the bit settings in the table “Address Patterns for PAR”. In this mode, when $\overline{ZZ}$ is active low, only the portion of the array that is set in the register is refreshed. The operating mode is only available during standby time ($\overline{ZZ}$ low) and once $\overline{ZZ}$ is returned high, the device resumes full array refresh. All future PAR cycles will use the contents of the VA register that has been previously set. To change the address space of the PAR mode, the VA register must be reset using the previously defined procedures.

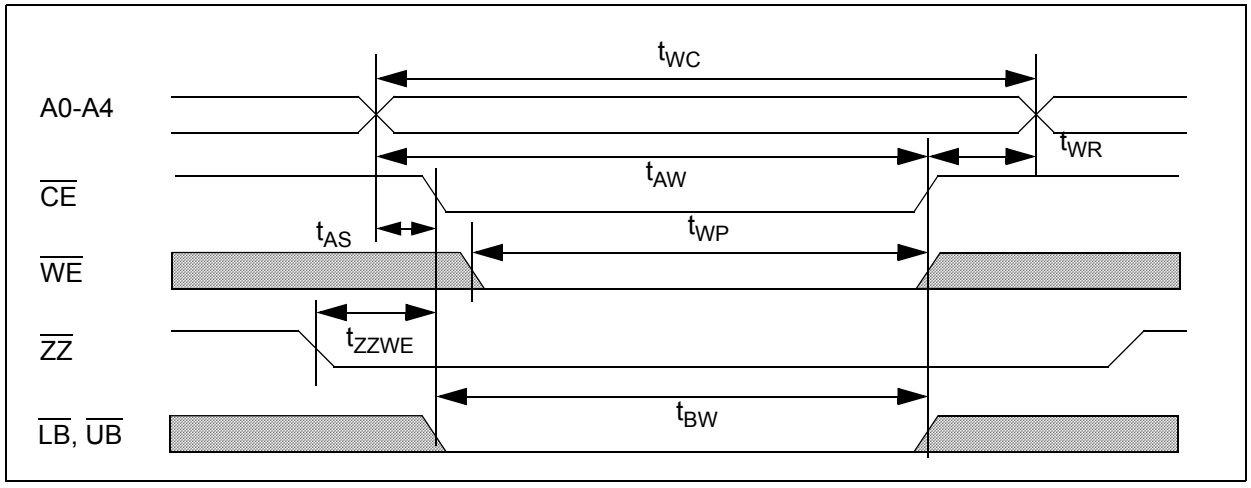
3) Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing $\overline{ZZ}$ low with the A4 register programmed to “Deep Sleep Enabled”. The device will remain in this mode as long as $\overline{ZZ}$ remains low and when ZZ is driven high, all register settings will return to default states.

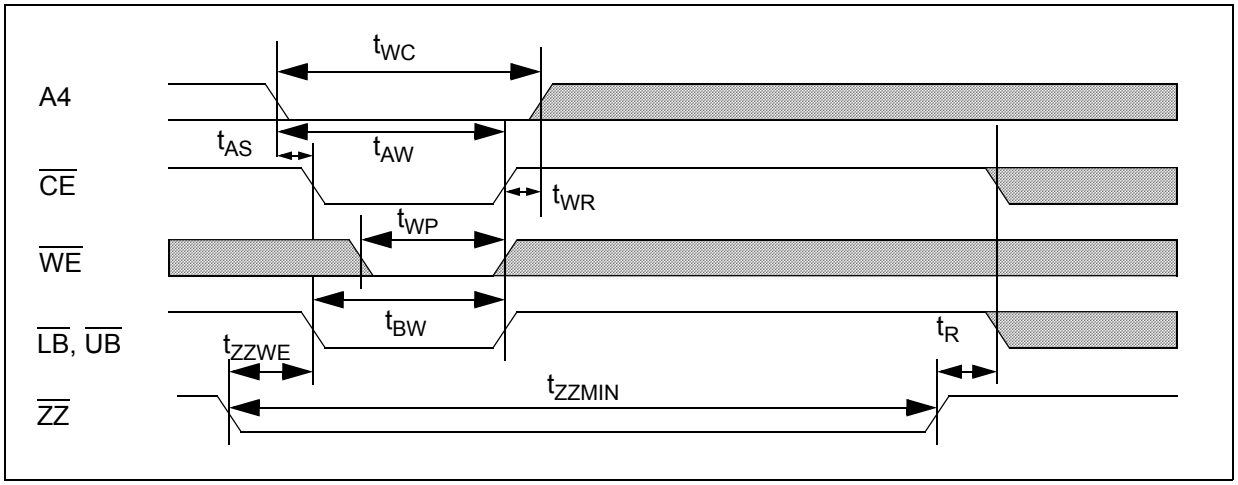
Variable Address Register



Variable Address Register (VAR) Update Timings



Deep Sleep Mode - Entry/Exit Timings



VAR Update and Deep Sleep Timings

Item	Symbol	Min	Max	Unit
$\overline{ZZ}$ low to $\overline{WE}$ low	t_{ZZWE}		1	us
Deep Sleep Mode	t_{ZZMIN}	10		us
Deep Sleep Recovery	t_R	200		us

Address Patterns for PAR (A3 = 0, A4 = 1)

A2	A1	A0	Active Section	Address space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
x	0	0	Full die	000000h - 1FFFFFh	2Mb x 16	32Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

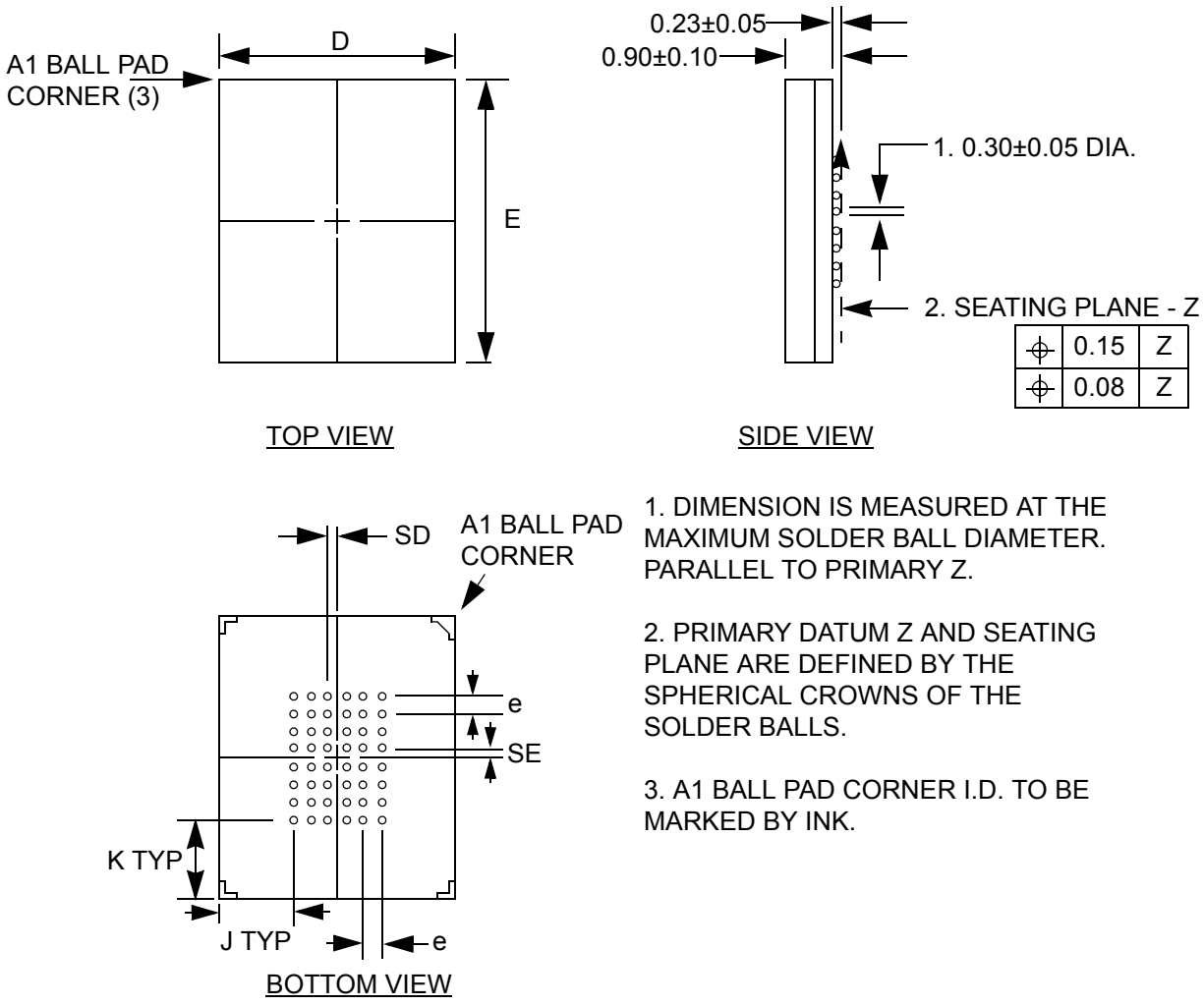
Address Patterns for RMS (A3 = 1, A4 = 1)

A2	A1	A0	Active Section	Address space	Size	Density
0	1	1	One-quarter of die	000000h - 07FFFFh	512Kb x 16	8Mb
0	1	0	One-half of die	000000h - 0FFFFFh	1Mb x 16	16Mb
1	1	1	One-quarter of die	180000h - 1FFFFFh	512Kb x 16	8Mb
1	1	0	One-half of die	100000h - 1FFFFFh	1Mb x 16	16Mb

Low Power ICC Characteristics

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85^oC$	1/4 Array		75	uA
			1/2 Array		90	
RMS Mode Standby Current	I_{RMSSB}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85^oC$	4Mb Device		75	uA
			8Mb Device		90	
Deep Sleep Current	I_{ZZ}	$V_{IN} = V_{CC}$ or 0V, Chip in $\overline{ZZ}$ mode, $t_A = 85^oC$			10	uA

Figure 2: Ball Grid Array Package



1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

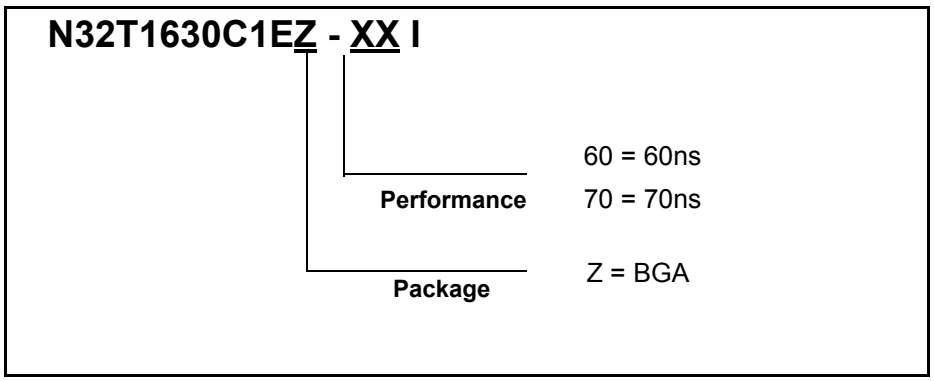
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Table 2: Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information



Revision History

Revision	Date	Change Description
A	Feb 2004	Initial Advance Release Package Datasheet
B	Mar 2004	Multiple Changes. Change ISB to 120uA. Added tCP timing parameter.
C	December 2004	Changed load circuit to 50pF and clarified low power mode with CE# high